Dynamic Evaluation of High Speed, High Resolution D/A Converters

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CSD/Telephonics

Practically speaking, the all-digital receiver will never exist. Yet, as digitally uncharted waters dwindle, many traditionally analog functions are being replaced by their digital counterparts — augmenting the performance of the remaining analog components and thus the overall system. One interface device that merges these two technologies is the high speed, high resolution digital-to-analog converter (DAC or D/A Converter). Two potential applications of DACs are shown in Figure 1. While DAC applications are not limited to receiver design, virtually all high speed/high resolution applications require careful evaluation of potential candidates to assure that the appropriate device is selected. Although most manufacturers provide a comprehensive set of characterization data, the device will often not be specified under the specific conditions called for in an application.

To alleviate this uncertainty, the D/A dynamic evaluation techniques outlined in this article were developed. Through a trio of tests: single tone, two tone, and noise power ratio (NPR), the performance of a potential D/A can be comprehensively analyzed. While this article will focus on RF applications, these tests are applicable to the dynamic characterization of most any DAC.

The Test Set Up

As depicted in Figure 2, the DAC under evaluation receives digital inputs that are generated as follows: A TTL clock of the required sampling frequency, f_s, drives a counter chain which generates addresses for the high speed memory (EPROM or RAM). Contained in the memory is the look-up table of codes that generate the appropriate test tone or tones. The sampling frequency will often dictate the memory type that is employed. EPROMs can provide a convenient storage medium, however, they typically exhibit slower access times than RAMs. One drawback to using RAMs however, is the continual need for the download hardware.

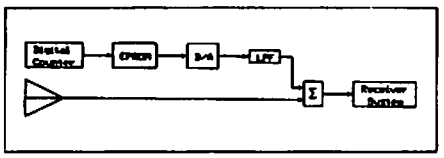

Figure 1a. A built-in test tone injection application for a high speed, high resolution DAC.

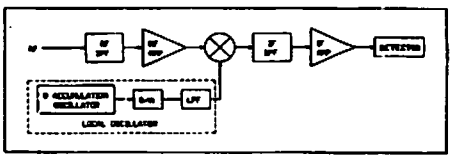

Figure 1b. A superheterodyne receiver with digitally generated local oscillator.

Wave generation software is used to create and download the look up table data to the memory devices. The software also loads in a reset command that will clear the counter chain, once the final data point is read. This allows the counter to continuously run from 0 to some maximum value, N-1. Data output from the memory is latched to minimize erroneous transitional data, and then presented to the D/A converter. This look-up table generation technique is preferred over other approaches by virtue of its ease of implementation and multi-tone generation capability.

The analog output of the DAC is presented to the spectrum analyzer where the frequency spectrum is monitored. Due to the high image frequencies contained in the D/A output, it is sometimes necessary to limit the bandwidth with a low pass filter depending on the test equipment limitations.

Each test of the trio is useful for examining various D/A performance parameters. For example, harmonic distortion (HD) and signal to quantization noise performance are readily accomplished with the single tone test. Since the resulting spectrum is relatively uncluttered, as compared to the other tests, the single tone analysis is also useful for characterizing other DAC parameters, such as power supply rejection and gain accuracy.

Harmonic distortion is characterized by products that occur at integer multiples of the fundamental frequency. Often, the second and third products of a DAC are most prominent.

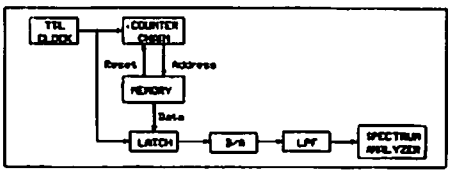

Figure 2. DAC test set up.

The two tone test is useful for examining intermodulation products, a nonlinearity characterized by distortion products that occur at sums and differences of integer multiples of the two primary frequencies. Typically, the dominant IM products are among the second order components located at f_2-f_1 and $f_1 + f_2$, and the third order components located at $2f_1 - f_2$ and $2f_2 - f_1$. Although this test can also be used for signal to noise ratio evaluation, it is limited to less than full scale testing due to saturation problems that would arise if the instantaneous amplitude of the combined signals exceeded the full scale limit. For example, if two equal amplitude tones are considered, the level of each must be at least 6.02 dB below the D/A full scale level to avoid saturation.

The NPR test, considered the most stringent of the three, is used to evaluate a converter's ability to replicate wide band signals such as those encountered in spread spectrum communication. This test entails generating a comb of uniformly spaced frequencies over a range dictated by the application. The comb is then characterized by a narrow notch that is usually located in the *center of* the frequency range.

Inside the notch, below the lower frequency limit, and above the upper frequency limit would appear the culmi-

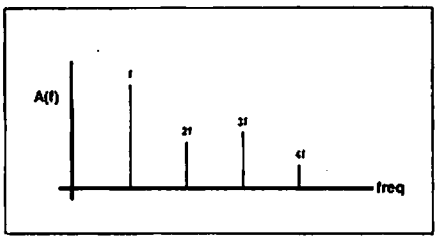

Figure 3. Harmonic distortion.

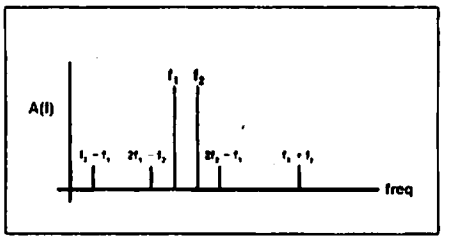

Figure 4. Intermodulation products.

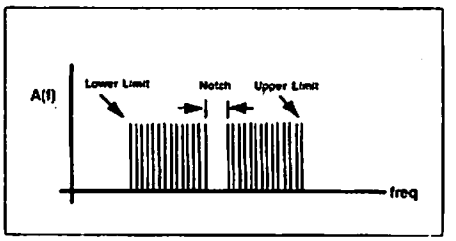

Figure 5. NPR signal.

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nation of the nonlinear products generated by the converter. Often, the discrete products of these nonlinearities are so numerous that a wide band noise appearance is created — which is particularly noticeable in the notch. This test can be especially useful since manufacturers rarely evaluate the NPR performance of their devices.

The wave generation software mentioned earlier, also contains a fast fourier transform (FFT) algorithm that allows the look-up table data to be viewed in the frequency domain prior to downloading. This useful reference illustrates the performance of an ideal DAC of the desired resolution. Use of the FFT algorithm however, restricts the number

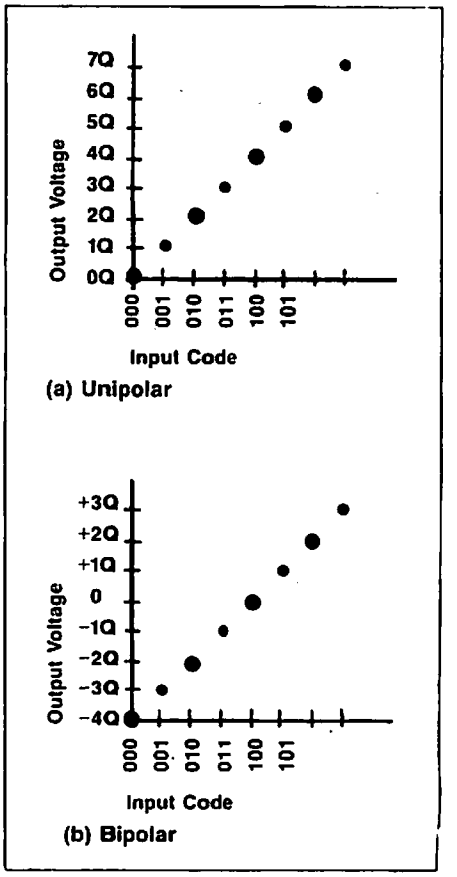

Figure 6. Ideal 3 Bit DAC transfer function.

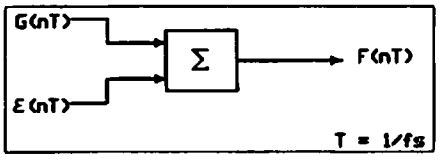

Figure 7. Ideal DAC quantization error representation.

of data points to powers of 2, which can yield a cumbersome resolution frequency (discussed in a following section) depending on the sampling rate.

A Focus on D/A Dynamic Errors

The transfer function of an ideal DAC is characterized by a linear relationship, where the analog output is proportional to the digital input code. For example, the transfer function of an ideal 3 bit DAC is shown in Figure 6.

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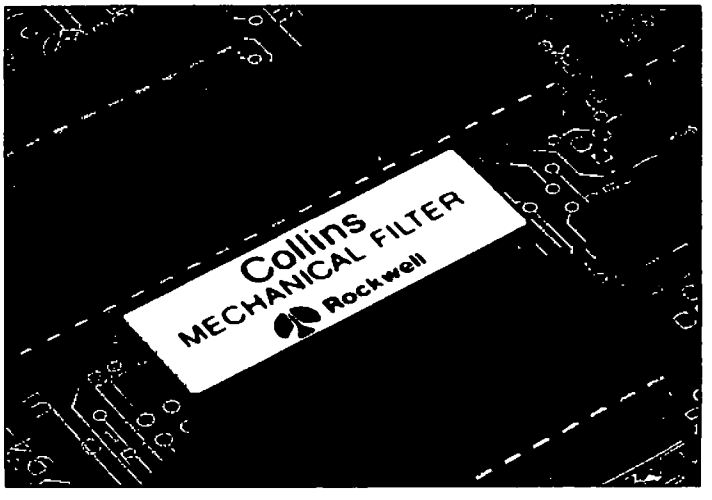

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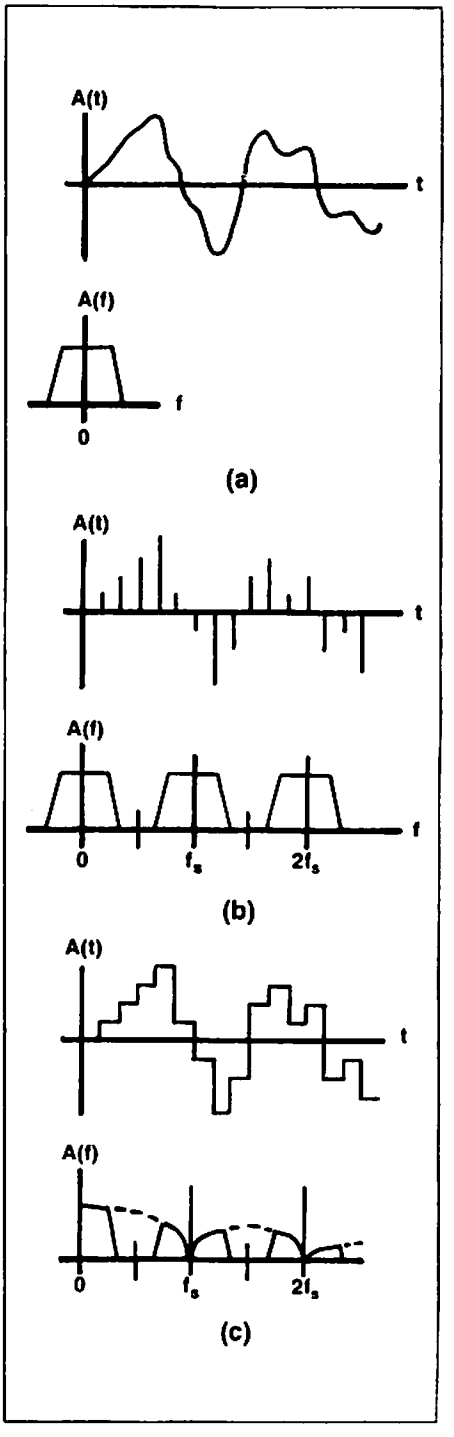

Figure 8. Time and frequency domain of a sampled signal a) original waveform, b) sampled representation, c) staircased representation.

Q refers to the weight or value that corresponds to 1 least significant bit (LSB).

$$Q = \frac{V_{FS}}{2^{N_c}} \quad (1)$$

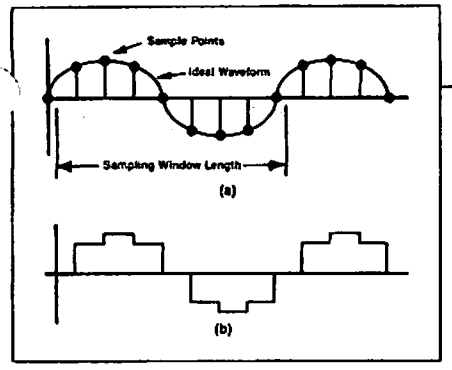

Figure 9. A limited number of DAC codes are exercised when the fundamental is a non-prime multiple of the resolution frequency a) sampled data points of the ideal waveform, b) DAC staircased output.

DAC Characteristic	Impact on AC Performance
Monotonicity	Code Dependent Spurs
Differential Non Linearity	Increased Quantization Noise
Integral Non Linearity	IM and HD Distortion
Glitch Impulse	Spurious
Digital Feed-through	Spurious
Power Supply Rejection	Spurious
Settling Time	Spurious, also dictates maximum f_s
Slew Rate	IM and HD Distortion
Gain	Amplitude error
Offset	Usually none, if AC Coupled

Table 1. DAC characteristics and their impact on AC performance.

Where:

V_{FS} = Full scale peak-to-peak voltage
N_b = Number of bits

Due to this finite resolution, even the ideal DAC would exhibit a fundamental quantization error of ± Q/2. Higher DAC resolution (i.e. more bits) yields a smaller quantization error, allowing greater fidelity in the reconstruction of a desired signal. Calculating the theoretical DAC noise produced by this quantization error, begins by modeling the DAC output, F(nT) as the sum of the exact sequence of sampled values G(nT) corrupted by an error component, ε(nT), which shifts the exact value to the nearest quantization level.

The maximum sine wave mean square value that can be generated before clipping is:

$$P_{Max} = \left[\frac{Q(2^{N_b-1})}{\sqrt{2}}\right]^2 = 2^{2N_b-3}Q^2 \qquad (2)$$

Based on the assumption that ε is a uniformly distributed and uncorrelated random variable over the range of $-Q/2 \leq \varepsilon \leq +Q/2$, its variance "power" is given by:

$$P_\varepsilon = \frac{\left[\frac{Q}{2} - \left(\frac{-Q}{2}\right)\right]^2}{12} = \frac{Q^2}{12} \qquad (3)$$

The sought after DAC dynamic range (maximum sine level to quantization noise over the Nyquist bandwidth) is calculated by simply taking the ratio of the two powers:

$$DR = 10\ Log_{10}\left[\frac{2^{2N_b-3}Q^2}{\frac{Q^2}{12}}\right] \qquad (4)$$

$$= 6.02\ N_b + 1.76$$

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Resolution Bandwidth	Dynamic Range
100 kHz	96.3 dB
30 kHz	101.5 dB
10 kHz	106.3 dB

Table 2. Theoretical dynamic range of a 12 bit DAC converting at 34 MHz, at three typical spectrum analyzer resolution bandwidths.

Since the quantization noise is uniformly distributed over the Nyquist bandwidth, determination of the dynamic range in a smaller bandwidth, f_{bw}, is simply:

$$DR = 6.02\ N_b + 1.76 + 10\ \text{Log}_{10}\left[\frac{f_s}{2f_{bw}}\right] \quad (5)$$

Ideally, reconstruction of an analog signal from its samples would be represented in the frequency domain as the convolution of the original analog signal spectrum and a train of impulse functions. The resulting spectrum, as depicted in Figure 8b, would consist of the original signal spectrum plus its images centered at integer multiples of the ampling frequency, f_s.

Since an impulse function would place unrealistic slew rate demands on a real world DAC, its output is instead characterized by a "staircase" function as depicted in Figure 8c. Although the resulting frequency spectrum of the staircased waveform also contains the original spectrum and images, the envelope is attenuated by a sine x/x roll off:

$$\text{Atten} = 20\ \text{Log}_{10}\left[\frac{\sin\left(\frac{\pi f}{f_s}\right)}{\frac{\pi f}{f_s}}\right] \quad (6)$$

where f = Output frequency
f_s = DAC sampling rate

Typically in DAC applications, only the spectrum from DC to the Nyquist Frequency ($f_s/2$) would be of interest, thus the higher frequency images are filtered with an LPF. The sine x/x roll-off however, will attenuate a signal at the Nyquist limit by 3.92 dB as compared to frequencies at the low end of the spectrum. Demanding applications would digitally correct this problem by placing an inverse sine x/x filter before the DAC.

In addition to the fundamental considerations of quantization noise and sine x/x roll-off, DACs also exhibit other characteristics which must be carefully considered in high speed applications. Some of these characteristics and their associated impact on AC performance are listed in Table 1.

Monotonicity indicates whether or not the analog output will consistently increase with increasing input code. Only when the signal passes through the non-monotonic portion of the transfer function, will it be tainted. Depending on where this discontinuity exists the resulting spurs may be signal level (code) dependent. As an example, if a non-monotonic point existed at BFO (Hex code of a 12 bit converter), smaller signals that did not exercise this code are unaffected, while larger signals that pass through this point will be corrupted. Fortunately, monotonicity is virtually always guaranteed by DAC manufacturers over the applicable temperature range, and is not usually a consideration.

Differential non-linearity, usually expressed in LSB weights, refers to the incremental accuracy of the DAC transfer function. Since this parameter dictates an increase in spread of quantization error, the resulting noise floor increase is readily predictable. Integral non-linearity pertains to the overall deviation of the DAC transfer function. Often characterized as a "bowing" deviation, this type of error will create distortion products in the DAC output. Glitch impulse, sometimes referred to as glitch energy, is a measure of the

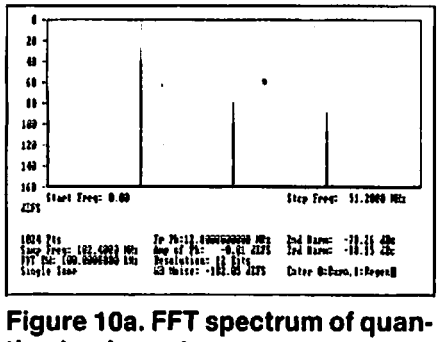

Figure 10a. FFT spectrum of quantized noise-extreme case.

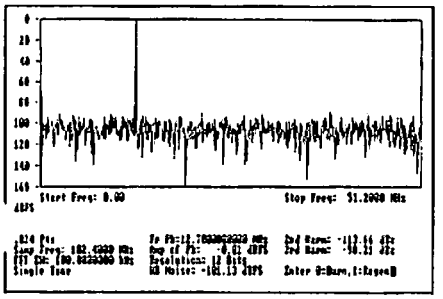

Figure 10b. FFT spectrum of quantized noise-even distribution.

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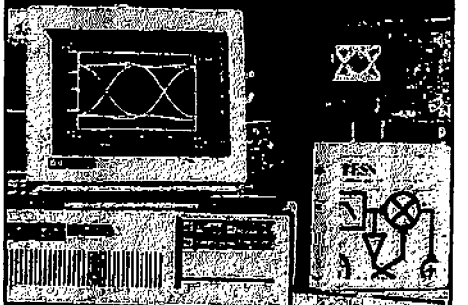

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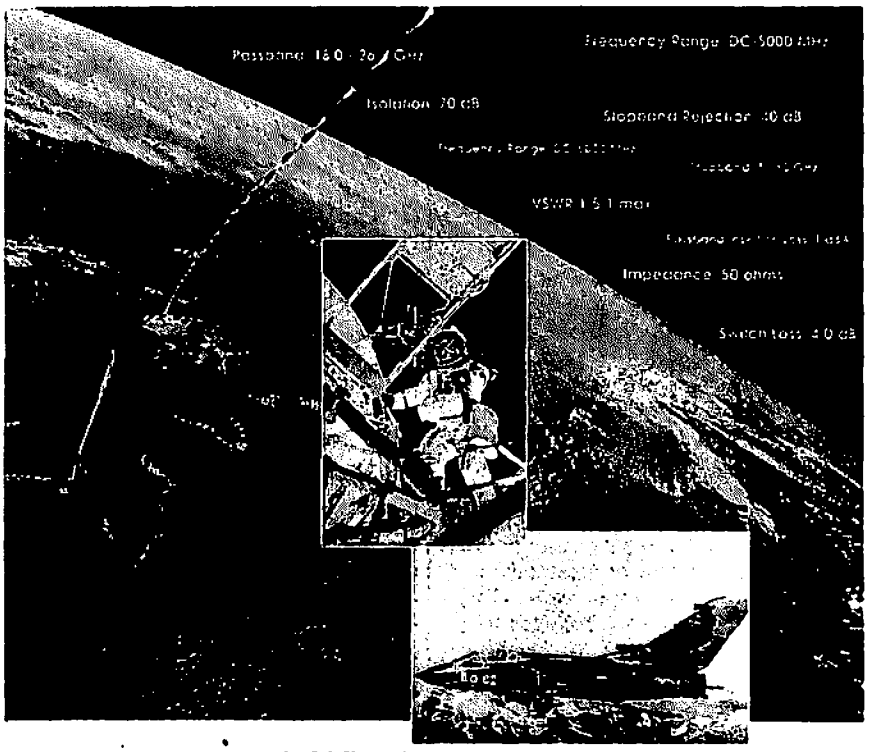
glitch area that is created by switching transients between updates. Although it is sometimes possible to de-skew the most significant bits (MSBs) to reduce the glitch impulse area, the efficacy of this technique is very limited, usually to about a 40 or 50 percent reduction. If needed, a much more effective method in reducing glitch area is to employ a sample and hold amplifier (SHA) at the DAC output. The SHA would maintain the proper analog level while the DAC is transitioning to the next value, buffering the output from the glitch activity. The DAC-02315 and DGL-02316 manufactured by Data Device Corporation is a good example of a DAC/SHA pair which is specifically intended for this purpose.

Digital feed-through pertains to the isolation that exists between the digital signals and the analog output. This feed-through is most problematic in high speed applications where high slew rate logic often carries higher frequency ripple components. Since this parameter is very dependent on circuit layout and implementation, it is often unspecified by manufacturers. Latching the digital data will limit coupling of extraneous noise riding on the logic signals, but will do nothing to prevent logic edge coupling. Maximizing the distance between the digital and analog circuitry will minimize capacitive coupling, while minimizing loop areas of both the analog and digital circuitry will minimize inductive coupling. Unfortunately, even the most carefully executed layout will not reduce the stray coupling capacitance that exists between the chip boundaries of the DAC, which is typically on the order of 0.2 pF. Manufacturers usually limit this capacitance by placing the digital signal pins as far away as practical from the analog pins. One method of reducing the effect of this coupling capacitance is to incorporate a Faraday shield around the DAC package — thi' will be discussed in more detail in the test results section.

Power supply rejection ratio (PSRR), frequently specified only at DC, is expressed in terms of percent of full scale change for a DC percent change in power supply voltage. Although this is helpful for determining amplitude variation over a given supply voltage range, this DC specification will provide little information about high frequency rejection. In high speed applications, judicious use of the proper bypass capacitors and filter inductors will complement the PSRR to maintain the proper noise immunity. Providing a capacitor pair consisting of a 0.001 – 0.1 uF ceramic and ~5 uF tantalum on each supply pin helps stabilize the voltage over a wide frequency range. The capacitors can be augmented by series inductors to further cleanse the supply lines.

Settling time of a DAC is traditionally defined as the time from the digital input transition to the time the DAC output has settled to within a certain error band, usually ± 1/2 LSB. A portion of this delay may be attributed to a fixed "pipeline" delay due to latch and switch propagation times, during which the analog output is unchanged. Therefore, in AC applications DAC settling time may be redefined in terms of the output alone: i.e., as the time the output leaves a ±1/2 LSB error band to the time the output



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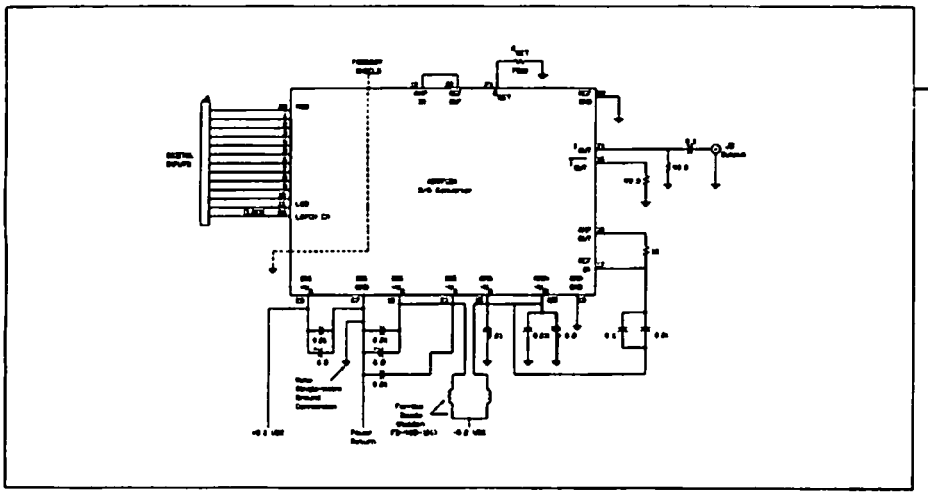

Figure 11. AD9713A test schematic.

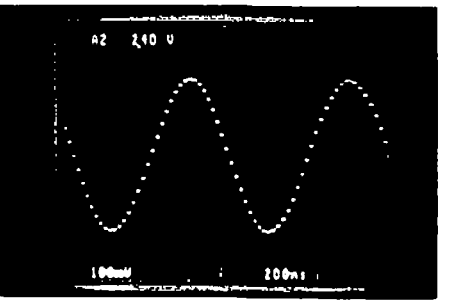

Figure 12a. Single tone test, time domain.

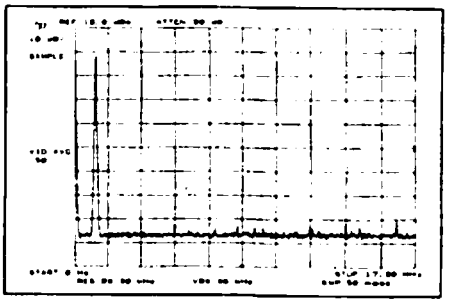

Figure 12b. Single tone test, frequency domain.

settles to within a ±1/2 LSB band. Ideally, a DAC should be chosen with a settling time that is much shorter than the sampling period.

The remaining DAC parameters: slew rate, gain and offset are relatively straightforward. DAC slew rate limitations are similar to that of other analog components, where the maximum output frequency is limited to:

$$f_{max} = \frac{SR}{2\pi Vp} \qquad (7)$$

where V_p = Maximum peak voltage level
SR = Slew rate (V/S)

Gain error, often expressed as a percent of the full scale (FS) output, relates to the amplitude accuracy of the DAC output. For example a 0.1 percent of FS gain error would dictate an amplitude error of less than 0.01 dB. Small gain errors are common, and are therefore not of significant concern in AC applications. Offset, which is also expressed as a percent of full scale output pertains to the resulting output level that would appear at the DAC output when it is instructed to output 0 volts. The offset is usually not significant, and is easily removed with AC coupling.

Test Considerations

Before discussing actual D/A test results, a few items should be addressed concerning the test parameters. The sampling window that contains the digital waveform must embody an integral number of cycles. Failure to assure this will result in discontinuities when the transition from the end of the data period to the start of the new one occurs.

The frequency resolution is simply:

$$f_{res} = \frac{f_s}{N} \qquad (8)$$

where: f_s = sampling frequency
N = Length of the sampling window (number of points)

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Avoiding the discontinuity requires that the fundamental frequency be an integer multiple (m) of the resolution frequency:

$$f_i = m\, f_{res} = m\, \frac{f_s}{N} \qquad (9)$$

Other considerations should also be heeded. To maximize the number of DAC codes exercised, the sampling window length, N, should be as long as practical while the integer multiple, m, chosen in the above equation should be odd and prime. The problems associated with choosing a small sampling window or a non-prime multiple can be visualized by examining the following example: consider a sampling frequency of f_s = 102.4 MHz that generates a tone at f_i = 12.8 MHz. Regardless of how large the sampling length is, under these conditions there will always exist exactly 8 samples per cycle which would utilize a very limited number of DAC codes.

When viewed in the frequency domain, the quantization errors of the tone are concentrated at the harmonics of the fundamental as depicted in Figure 10a. This anomaly yields misleading results concerning the true HD performance of the DAC — a problem that is easily solved by allowing the largest length (N) that is practical and by selecting the fundamental to be an odd and prime multiple on the resolution frequency. This would slightly offset subsequent cycles, maximizing the number of codes exercised —"spreading" the quantization error. Referring back to the example, by reselecting the fundamental to be 12.7 MHz (which is an odd and prime multiple of the resolution frequency of 0.1 MHz) the resulting frequency domain plot, Figure 10b, depicts an evenly distributed quantization noise floor.

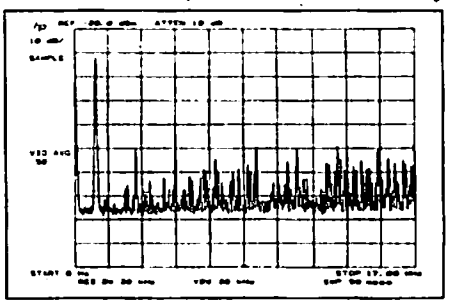

Figure 13a. -30 dB full scale test-without Faraday shield.

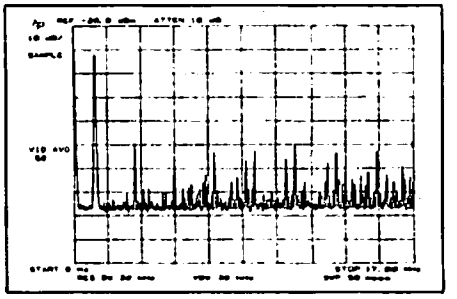

Figure 13b. -30dB full scale test-with Faraday shield.

An interesting consideration that arises during DAC evaluation is the performance limitations of the test equipment. Recall that the theoretical DAC dynamic range (defined as the full scale sine amplitude to the quantization noise floor ratio) is:

$$DR = 6.02\, N_b + 1.76 + 10\ \mathrm{Log}\left(\frac{f_s}{2f_{bw}}\right) \qquad (10)$$

where: N_b = converter resolution (num-

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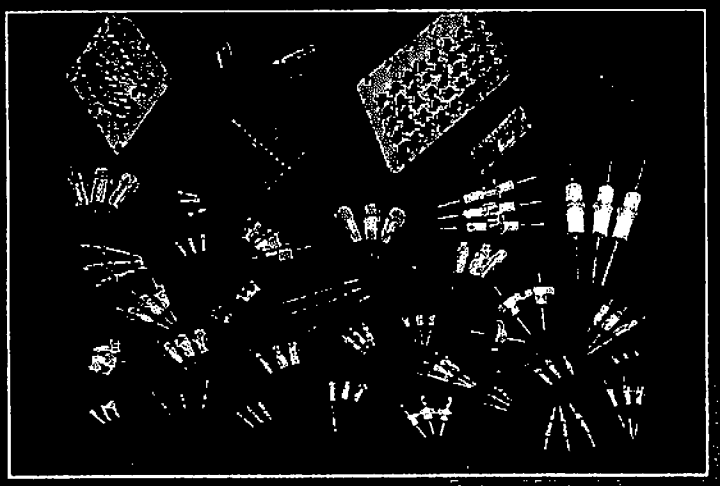

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ber of Bits)
f_s = Sampling frequency
f_{bw} = Measurement bandwidth

Considering, for example, a 12 bit DAC converting at 34 MHz, the resulting theoretical dynamic ranges for some typical spectrum analyzer bandwidths are listed in Table 2.

Measuring instantaneous dynamic ranges of greater than 80 or 90 dB generally place formidable demands on a spectrum analyzer. Therefore, some tests encountered in the evaluation of a quality high speed, high resolution DAC, will be limited by the test equipment. Fortunately, techniques frequently exist to circumvent this problem — as will be discussed in the following section.

Test Results

The AD9713A by Analog Devices was characterized at 34 MHz with the test trio to determine its suitability in various applications. The schematic of the DAC test circuit is shown in Figure 11. The unipolar current source DAC output is specified for a full scale level of 20.65 mA, with a set resistor of 7.5 kohms. Placing the 50 ohm resistor at the output creates a 50 ohm Thevenin 1.033 unipolar voltage source. This dictates an available power of −1.8 dBm into an AC coupled 50 ohm load. Applications requiring higher level outputs can be accommodated with a high speed transconductance amplifier, such as the AD9617.

The Faraday shield was constructed with 3 mil copper tape wrapped around the length of the IC package and connected to the board ground plane. Except where noted in the single tone case, the Faraday shield was used in all the following tests.

DAC characterization for a 1.01270 MHz local oscillator is accomplished with the single tone test. The time domain and frequency domain results are shown in Figures 12a and 12b respectively. Note that in the time domain, the duration of the switching transients between updates are substantially shorter than the update period. The staircased appearance is easily smoothed with an LPF. In examining the frequency domain, it is important to note that the observed noise floor is that of the spectrum analyzer which masks the quantization noise and all but the most ornery of DAC spurs. Being consistent with the data sheet specification, these spurs and HD products are observed to be at least 68 dBm down from the full scale carrier. Note also that with the peak amplitude of −1.8 dBm, the theoretical quantization noise floor in the resolution bandwidth of 30 kHz will be 101.5 dB below the peak at −103.3 dBm, well below the analyzer's noise floor. Reducing the analyzer's internal attenuator from 30 to 20 dB will improve its effective noise figure, but will create misleading harmonic products as the front end of the spectrum analyzer will add distortion to the signal.

Digitally reducing the signal to −30 dBFS (below full scale) reduces the instantaneous dynamic range requirement of the spectrum analyzer, allowing for a more comprehensive observation of the DAC performance, as depicted in Figures 13a and 13b. However, depending on the application the digital level reduction may not be a valid test since the DAC spurious content will likely be signal level dependent. In such a case, it would be more meaningful to attenuate the fundamental in the analog domain with a notch filter, to reduce the analyzer instantaneous dynamic range requirement. However, careful implementation of the filter is required to assure that it does not generate distortion products that would create misleading test results.

The numerous spurs are caused by both capacitive coupling of the digital data to the analog circuitry and DAC nonlinearities. Although careful layout can limit the coupling problem, it can do little for the coupling that exists within the DAC itself, as discussed in a previous section. Use of the Faraday Shield can attenuate the effect of the coupling capacitance (as illustrated in a comparison of the Figures 13a and 13b), though its efficacy is limited since its proximity to the die is constrained by the package. Nevertheless, most of the spurs and harmonics are attenuated, some by as much as 8 dB. Ignoring the discrete spurs, Figure 13 reveals a noise floor of −96 dBm which again is limited by spectrum analyzer performance.

Although many manufacturers do specify harmonic distortion, the single tone HD test is useful in situations where data sheet test conditions do not parallel the specific application. Additional uses for this test include: verifying the DAC circuit configuration and characterization of other DAC parameters such as power supply rejection.

Frequently unspecified by a manufacturer, intermodulation distortion (IMD) is another important DAC parameter which is useful for example, in evaluating a

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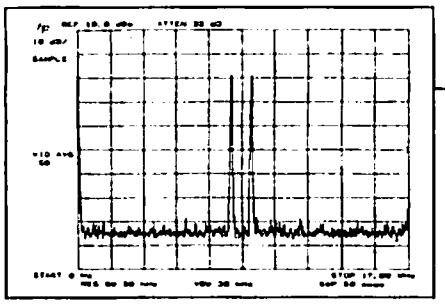

Figure 14. Two tone DAC performance.

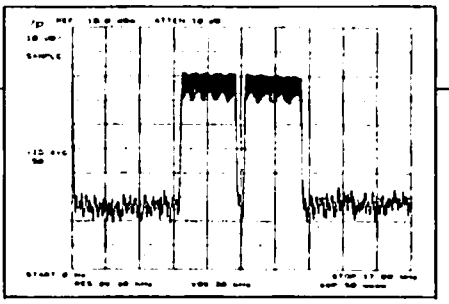

Figure15a. NPR DAC performance DC to 17 MHz.

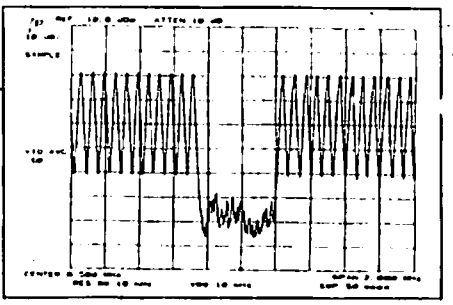

Figure 15b. NPR DAC performance, focus on notch.

DAC intended to inject a built-in-test (BIT) signal consisting of two tones. Figure 14 illustrates the DAC performance in generating a two tone signal at approximately 7.952 and 8.981 MHz. To avoid saturation, the amplitude of each signal is at −8 dBm, slightly less than half the full scale amplitude of −1.8 dBm.

Note that the largest of the IM components is the second order product at 16.933 MHz which is at −64 dBm (56 dBc).

The final and most stringent test of the trio is the noise power ratio, which is especially useful in DAC characterization in wide band applications. In the following example, the NPR test was used to characterize potential DACs for use in the IF output generation of a ground based satellite receiving system. Since the IF consisted of a PN modulated 6 MHz bandwidth carrier centered at 8.5 MHz, the NPR test was developed using a comb of frequencies ranging from approximately 5.5 to 11.5 MHz with a void from approximately 8.25 to 8.75 MHz. The discrete frequencies were spaced at four times the resolution frequency of 16.6 kHz, providing about 82 components. Randomizing the phases of each signal is necessary to minimize the peak-to-RMS voltage ratio, thus maximizing the number of DAC codes exercised.

Actual NPR performance of the AD9713A is depicted in Figure 15. Note the noise floor of −85 dBm depicted in Figure 15a, falls far short of the theoretical level of −103 dBm. In actuality the noise floor is a culmination of the numerous HD and IMD products of each of the frequency components that make up the NPR test, as anticipated previously. The 2 MHz frequency span of Figure 15b details the notch spectrum. Note that the individual frequency components, spaced at 66.4 kHz, are easily resolved in this figure. Although the DAC performance is impressive, under these conditions it will only yield an instantaneous dynamic range equivalent to that of an ideal 9 Bit converter. Depending on the application requirements, this may not be a significant limitation since as the NPR signal is digitally attenuated, the noise floor decreases.

It is interesting to note the slight decline in signal amplitude at the higher NPR frequencies. This is not due to the frequency response of the physical part, but is rather a consequence of the sine x/x attenuation discussed earlier.

Summary

Most manufacturers do an excellent job specifying DAC performance. Unfortunately, data sheet specifications often reflect operation under conditions unlike those called for in a specific application — or worse a desired parameter such as IM performance, may not be specified at all. Dynamic evaluation with the single tone, two tone and NPR tests will help define DAC uncertainties, providing an efficient means to characterize and evaluate DACs for a wide variety of applications. *RF*

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2. Alen Oppenheim, *Digital Signal Processing*, Prentice-Hall, 1975.

About the Author

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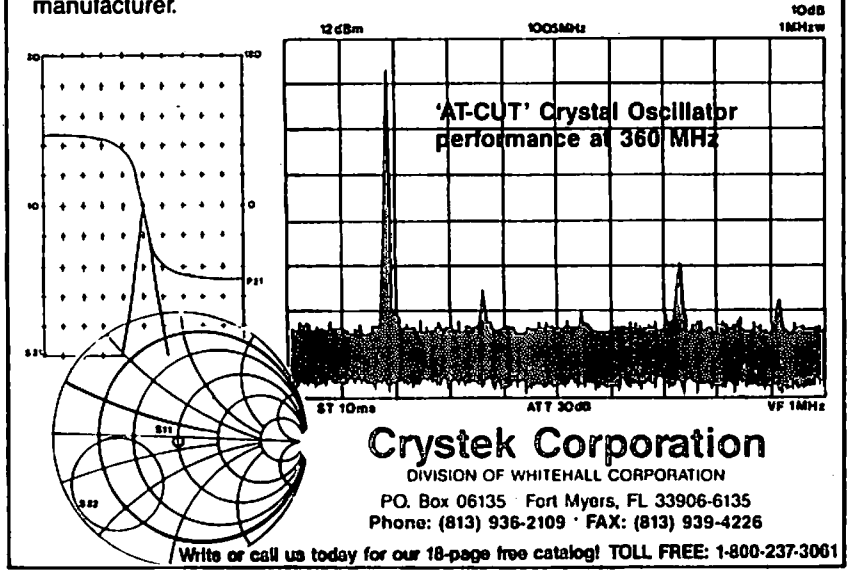

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