FPGA LEVEL IN-HARDWARE VERIFICATION FOR DO-254 COMPLIANCE

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Abstract

RTCA/DO-254, "Design Assurance Guidance for Airborne Electronic Hardware" [1] is currently enforced by the FAA via the Advisory Circular (AC) 20-152 [2] as a means of compliance and guidance for the design assurance of complex electronic hardware such as FPGAs, PLDs and ASICs in airborne systems.

RTCA/DO-254 Section 6 (Verification Process) defines a set of verification objectives and methods that present several new challenges to design and verification engineers of airborne electronic hardware.

This paper points out the most significant challenges that can be encountered during the hardware verification process of FPGA designs under DO-254 guidelines. More importantly, this paper proposes a verification methodology that replays RTL simulation during hardware testing at full speed utilizing the same simulation testbench as test vectors.

Introduction

The main purpose of DO-254 Verification Process (section 6.2 of DO-254 specification) is not merely to verify the functionality of the design but also to obtain assurance that the hardware implementation meets the requirements defined in the early stages of DO-254 targeted project. DO-254 certification relies on the information which is gathered from the project conception, planning, design creation and implementation through the testing stages. Essentially, the requirements verified during RTL simulation must be verified again during hardware verification.

An FPGA implementation is usually verified through RTL simulation. In most cases, this simulation is performed after the design requirements have been identified. RTL and timing simulation are accompanied by code coverage analysis tool that ensures 100% coverage of all possible input signal combinations within the applied tests. While simulation results can be easily visualized, analyzed, compared and requirements traceability easily

maintained, the design behavior in hardware cannot be easily traced to simulation. As a result, a great amount of time and engineering effort is required to check all of the requirements during hardware verification.

Hardware Verification Challenges

Traditionally, hardware verification is performed at the board level. The board contains the FPGA under test as its primary component with the most complex functions and controls, and possibly even the main IP (Intellectual Property) of the board. The FPGA is also interconnected with other components on the board, and with the lack of test headers on the FPGA pins visibility and controllability at the FPGA pin level is limited. There are times that the board even contains multiple FPGAs, and verification at the board level without first stabilizing each FPGA individually can lead to many problems and longer project delays. A simplified example of a board under test is shown in Figure 1.
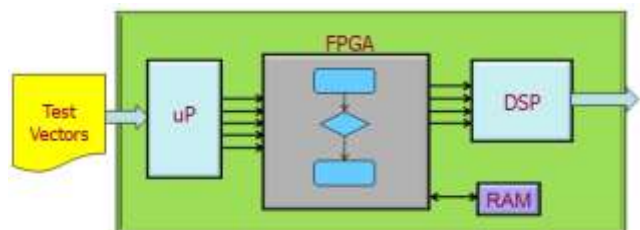

Figure 1. Board Under Test (Board Level View)

There are several significant challenges that come up when verifying FPGA level requirements at the board level, and they include the following:

- The traceability of testing results which involves re-mapping and comparing the hardware outputs to its corresponding RTL simulation results, and tracing them to the design requirements is a considerable challenge in DO-254 certification. Since most of the traditional DO-254 testing methods do not allow driving the hardware with all combinations of stimulus defined by

code coverage for RTL simulation, not all requirements can be traced and additional analysis is usually required.

- Creation of test vectors to verify requirements is a manual effort that could take 3-6 months for Levels A/B designs. For RTL simulation, testbenches are created to verify specific requirements, and the challenge is determining a way to reuse them to shorten the time spent during hardware testing.

- The FPGA design implementation process may introduce errors in functionality or timing of the design under test (DUT). Sometimes, even an update of the synthesis tool may result in such errors. Since the target device cannot contain any additional debug modules (e.g. probes used by JTAG debug tools), it is not easy to analyze and debug the problems.

- Visibility and controllability at the FPGA pin level is limited. The FPGA under test is interconnected with other components in the board. Additionally, the board might not have enough test headers on the FPGA pins or logic analyzers are not able to capture all required data,

- Multiple testing environments are needed to verify different sets of test cases. This also involves manual bypasses of wires and cables that is prone to human errors. Documenting this process is also a challenge.

- Automation of the verification process is critical and can significantly reduce the project completion time and the overall project cost. Typically, multiple test cases must be developed, executed and analyzed to verify design requirements and any design change or fix. This process, if handled manually, could take months to complete.

Verifying FPGA level requirements is imperative, but performing this process at the board level is quite challenging and at times not feasible. The methodology proposed in this paper provides a feasible solution to verify FPGA level requirements such that test vectors and test cases from RTL simulation can easily be reused and repeated during hardware verification.

FPGA Level In-Hardware Verification

The proposed methodology is based on a bit-accurate in-hardware verification platform that is able to verify and trace the same FPGA level requirements from RTL to the target device at full speed.

The solution's name is DO-254/CTS™ (Compliance Tool Set), a certifiable at-speed FPGA level in-hardware verification environment for Levels A/B complex designs, and is dedicated to address the stringent guidelines of DO-254 Section 6 Verification Process. DO-254/CTS consists of a fully customized hardware and software package designed to replay RTL simulation during in-hardware verification reusing the testbench as test vectors. It provides a single and automated environment to test all FPGA level requirements with full visibility and controllability at the FPGA pin level [3]. The components of DO-254/CTS and their primary tasks are:

1. **Custom Daughter Board**
   - Customized to target FPGA and DUT
   - Contains target FPGA and DUT
   - Isolates FPGA for functional test
2. **COTS Mother Board**
   - Sends test vectors into daughter board and captures the results from daughter board
   - 1-environment to test all FPGA level requirements
   - PCIe interface to PC
   - 2GB DDRII (Expandable)
3. **Compliance Software Package**
   - Test Vectors Generation – automatic generation of test vectors from simulation testbenches
   - Controls in-hardware verification
   - Samples FPGA I/Os and writes to waveform file

Automatic Test Vectors Generation

For RTL simulation, testbenches are created to contain test vectors that verify the requirements. Reusing the same data will save tremendous time required for creation of the test vectors for in-hardware verification. The generation of test vectors

based on the testbenches can be accomplished by adding a special simulator plug-in which enables storing the sequences of stimulators and events during RTL simulation. Additionally, the plug-in automatically generates test vectors from many different testbenches. The key benefits derived from using RTL simulation data for in-hardware verification include:

- All testbenches have been written
- Testbenches contain the requirements
- Requirements have been verified
- Code coverage has been reported

The flow of test vectors generation is displayed in Figure 2 below. The process generates two sets of vectors: **Golden Vector**s and **Input Vectors**. The Golden Vectors are the RTL simulation results which will be the reference for results comparison. The Input Vectors are the test vectors generated based on the testbench which will be used for in-hardware verification.
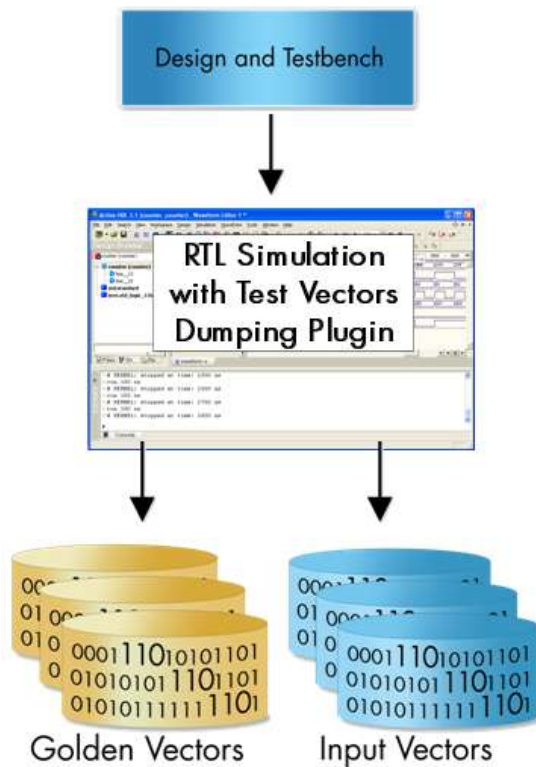

Figure 2. Test Vectors Generation Process

The Test Vectors Generation Process offers several advantages:

- Time savings on test vectors development – automated process, no need to write new tests; a script- driven process generates vectors for all applicable testbenches.

- The RTL golden vectors provided by RTL simulation are treated as a reference for comparison with in-hardware verification results.

- Test vectors for in-hardware verification – if recorded in a waveform format, are used for additional review and analysis before and after in-hardware verification.

In-Hardware Verification Process

Since the problem of test vectors creation has been resolved by automated test vectors generation, the next tasks now are to:

- Use the test vectors for at-speed in-hardware verification

- Document the results

- Trace the results to RTL simulations, ensure the RTL simulation and in-hardware verification results match

- Shorten the time spent on these activities.

Figure 3 shows the in-hardware verification process. The Input Vectors are uploaded from the workstation to mother board via PCIe interface. The Input Vectors are then processed and stored in a 2GB DDRII on-board memory (expandable) of the mother board. Once all of the vectors are stored, then real clocks will be released to start the at-speed in-hardware verification of the FPGA under test in the daughter board. The testing process is automated by a specialized application capable of reading and applying the Input Vectors file during in-hardware verification. This application controls the verification process by feeding the Input Vectors to FPGA pins at full speed using real clocks.

The results obtained during in-hardware verification are sampled at full speed, and recorded in a waveform file called Output Vectors. Another specialized application automatically compares the in-hardware verification results (Output Vectors) with the RTL simulation results (Golden Vectors). Further investigation of any discrepancies can easily be done by using the waveform comparison feature of the RTL simulator.
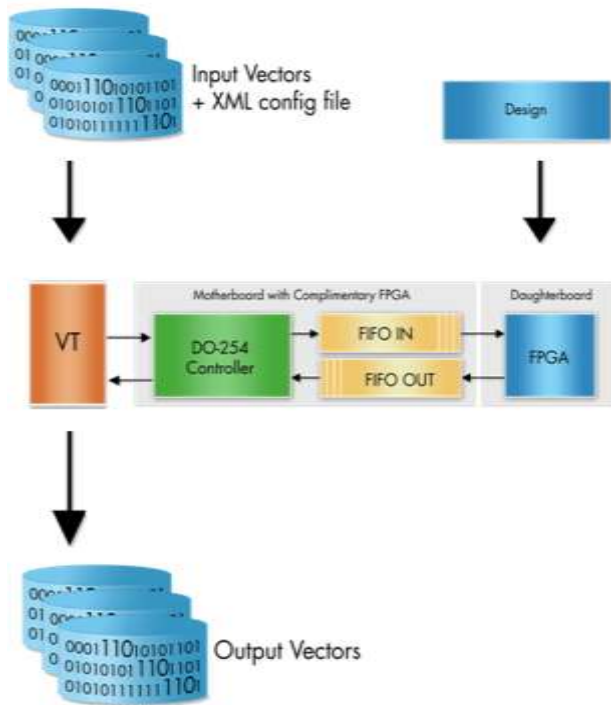
Figure 3. In-Hardware Verification Process

Key characteristics of at-speed in-hardware verification:

- RTL simulation testbenches have established code coverage
- Input Vectors derived from RTL testbenches have known test coverage
- Input Vectors drive target device at-speed, which produces Output Vectors
- Golden Vectors in a waveform format allow fast analysis and documenting results
- Golden Vectors allow traceability of in-hardware verification outputs back to the RTL simulation results.
- Provides a script-driven verification environment for any test scenarios.

At-Speed Testing

Running the target FPGA and DUT at the required operational speed (at-speed or full speed) is necessary to obtain compliance. This is actually one of the primary safety critical requirements to assure the device performs its intended functions.

DO-254/CTS implements a simulation-like approach utilizing real clocks running at full speed unlike hardware accelerators that run on testbench clocks that are limited to the simulator's speed. If the required simulation time is 500 ms then in-hardware verification will complete within this period.

Furthermore, because of the at-speed testing capability, DO-254/CTS can help to detect errors such as:

- Errors caused by Synthesis and P&R tools
- SSO (Simultaneous Switching Output) problems that can lead to signal integrity problems which refers to switching many signals/pins at the same time
- Differences between simulation models and netlists
- Clocking and resetting errors
- Some general limitations/requirements of the FPGA that are not visible during simulation (e.g. clock connected to regular I/O instead of clock pin)

FPGA Level Verification vs. Board Level Verification

The FAA Advisory Circular (AC) 20-152 explicitly applies DO-254 to complex programmable devices like FPGAs. This means FPGA level verification is significant and paramount for compliance. Testing the FPGA in isolation before board level testing assures the device is bug-free and stable.

DO-254/CTS supplements final board level testing. Once all the FPGA level requirements have been verified using DO-254/CTS they do not have to be verified again at the board level. Only high level requirements such as environmental, interfaces and board level functions need to be verified at the board level.

Test cases created for RTL simulation can be leveraged and reused for hardware verification. This ensures that hardware verification results can be easily traced and mapped to RTL simulation results fulfilling section 6.2 Verification Process guidelines and objectives.

FPGA level verification by testing the device in isolation provides several advantages:

- Assurance that the device is functionally verified and stable.

- The same number of tests can be run on the target device as in the simulator; 100% or desired level of code coverage can be easily assured and automatically implemented.

- Since the test vectors are generated automatically, there is no need to develop additional tests for hardware testing.

- Full design verification in target device can be made before a system/board test. Credits can be obtained from the verification performed using DO-254/CTS.

- Automated and single testing environment for all FPGA level requirements.

- In-hardware testing results are automatically recorded in a waveform format for better visibility, easier analysis and more reliable documentation.

Conclusion

FPGA level verification with full visibility and controllability at the pin level is ideally preferred, but this method is not feasible with the traditional hardware testing methods. The amount of work that is needed to verify and preserve the same FPGA level requirements in the target FPGA at full speed is tremendously challenging. With DO-254/CTS, FPGA level verification is now feasible and fully supports the verification objectives and methods of DO-254. The FPGA device is assured to function and behave as to what the RTL implementation intended.

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References

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[3] DO-254/CTS (Compliance Tool Set), Aldec's At-Speed In-Hardware Verification Methodology, 2007, http://www.aldec.com/do254