A Flexible Volterra-Based Adaptive Digital Pre-Distortion Solution for Wideband RF Power Amplifier Linearization

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Abstract: **This paper presents an efficient and flexible hardware implementation of a Volterra-based digital pre-distortion linearizer to provide efficiency enhancements for high power RF power amplifiers. The adaptive digital pre-distortion solution presented here extends the linear range of power amplifiers, and in combination with crest factor reduction, enables RF power amplifiers to be driven harder and more efficiently while meeting transmit spectral efficiency and modulation accuracy requirements. The pre-distorter presented is part of TI's GC5322 transmit solution, which incorporates digital up-conversion, crest factor reduction and digital pre-distortion in a multi-million gate ASSP in 0.13u CMOS technology. This modulation agnostic processor supports signal bandwidths up to 30MHz. It can reduce PARs for 3G signals by as much as 6dB and for OFDM signals by as much as 4dB while meeting ACPR and EVM specs. It can correct for up to 11th order non-linearities and PA memory effects up to 200ns. It typically provides greater than 20dB ACPR improvement and over 4x increase in power efficiency for a variety of power amplifier topologies, resulting in as much as 60% reduction in the static power consumption for typical base-stations. This flexible Volterra based pre-distorter can be optimized for a variety of RF architectures, modulation standards and signal bandwidths.**

Index terms—**Crest Factor Reduction, Adaptive Digital Pre-Distortion, Power Amplifier Linearization.**

I. INTRODUCTION

Non-constant envelope modulation schemes like those used in 3G and other emerging air interface standards are spectrally more efficient, but have high peak to average signal ratios, necessitating a higher Power Amplifier (PA) back-off. This decreases the PA efficiency, and increases the cooling and operational costs of the base-stations. Lower efficiency RF PA's typically account for up to 30% of the overall base station system cost and have a considerable environmental footprint. Increasing push towards 'green' technologies combined with rising energy costs and increasing spectral efficiency and signal bandwidth requirements of current and evolving wireless standards make power amplifier linearity a crucial design issue in next generation base stations. A variety of power amplifier linearization techniques like RF feed-forward, RF feedback, RF/IF pre-distortion and post-distortion have been proposed and implemented over the years. Of these, adaptive digital pre-distortion (DPD) schemes have proven to be the most efficient and cost effective compared to traditional analog/RF linearization techniques. Increasing DSP/ASSP computational capacities make digital pre-distortion an ever more attractive option.

The GC5322 transmit solution presented here combines digital up-conversion (DUC), crest factor reduction (CFR) and digital-pre-distortion (DPD) in a highly integrated ASSP (Application Specific Signal Processor), with real-time adaptation control provided by software residing in a TI C67x DSP. It can be optimized for a variety of RF architectures and supports multiple air interface standards including CDMA2000, W-CDMA, TD-SCDMA, MC-GSM, WiMax and LTE. The flexible pre-distorter can be used efficiently with a variety of power amplifier topologies like typical class A/B or Doherty, and is designed to support communication systems with signal bandwidths up to 30MHz. This paper is focused pre-dominantly on the hardware implementation of the digital pre-distortion solution.

This paper is organized into 6 sections. Section 2 presents a brief overview of current digital pre-distortion and power amplifier modeling schemes described in the literature. Section 3 presents details of the pre-distortion scheme implemented in the GC5322. In section 4, the DSP based software adaptation techniques are discussed in brief. Results from the lab are presented in section 5. And finally, section 6 concludes the paper.

II. OVERVIEW OF DIGITAL PRE-DISTORTION TECHNIQUES

Third-generation (3G) code-division multiple-access (CDMA)-based systems and multi-carrier systems such as orthogonal frequency division multiplexing (OFDM) exhibit signals with high peak-to-average ratios (PARs), also known as crest factors. The non-constant envelope-modulation techniques such as quadrature amplitude modulation (QAM) employed in such systems have very stringent Error Vector Magnitude (EVM) requirements. This requires a highly linear PA amplitude and phase response. High power amplifiers typically have a limited linear range of operation. PA non-linearities cause inter-modulation distortion in the transmitted signal, leading to spectral splatter and reduction in adjacent channel power ratio (ACPR). A simple solution to this problem is to back off the PA inputs so that the signal lies completely within the linear operating region of the PA. PA power efficiency decreases considerably at lower input power levels, making this a highly sub-optimal solution. Moreover, advanced, more efficient topologies like Doherty PA's have considerable non-linearities even at backed-off power levels resulting in poor EVM and ACPR performance.

Efficiencies of traditional class AB power amplifiers widely in use today when operated under a back-off condition range from 5-10%. But with crest factor reduction and adaptive digital pre-distortion techniques, the efficiencies can be improved by 3-5x. Newer PA topologies like Doherty's, or class AB with

dynamic envelop tracking in combination with digital pre-distortion and newer GaN or GaAs power transistors can achieve efficiencies approaching 50%.

Current DPD implementations mostly use memory-less linearization techniques where the pre-distortion is an instantaneous non-linearity which compensates for the instantaneous non linear behavior of the power amplifier. Memory-less power amplifiers can be characterized by their amplitude and phase transfer characteristics, commonly referred to as AM-to-AM (or gain compression) and AM-to-PM characteristics. A generalized look up table can be used for the pre-distorter gain/phase correction for such a memory-less power amplifier. Figure 1 shows the gain compression and AM-PM characteristics for a typical Doherty PA.

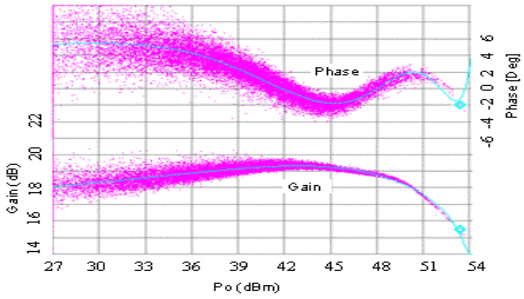


Figure 1: Gain compression and AM-PM characteristics for a typical Doherty PA

The gain and phase characteristics of the PAs change with temperature, voltage and component ageing, requiring an adaptive control of the look-up tables for efficient linearization.

For communication systems where the power amplifier has to support higher RF modulation bandwidths, this memory-less model proves to be highly inadequate since it is only amplitude dependent, not frequency dependent. High power RF amplifiers that need to support large signal bandwidths exhibit significant memory effects due to the long time constants of components in the DC biasing networks and rapid thermal effects of the active devices. This causes the PA characteristics to change as a function of past input levels, and necessitates use of a pre-distortion architecture that can alleviate these memory effects.

Any efficient linearization scheme requires a highly accurate model for the pre-distorter, and for the power amplifier if it uses a direct learning adaptation architecture. A variety of techniques have been proposed in the literature for modeling non-linear systems with memory, with none being a universal solution. This makes model selection highly challenging and dependent on the application. An efficient PA model needs to be able to model the different types of non-linearities and memory effects seen in high power amplifiers with reasonable accuracy.

One of the most general models for time-invariant non-linear systems with memory is the Volterra series. It consists of a sum of multidimensional convolutions, which in discrete time causal form can be written as:

$$Y(n) = Y1(n) + Y2(n) + Y3(n) + Y4(n) + Y5(n) + \ldots + v(n) \quad (1)$$

Where,

$$Y1(n) = \sum^{i=0:M1} h1(i).x(n-i)$$

$$Y2(n) = \sum^{i1=0:M2} \sum^{i2=0:M2} h2(i1,i2).x(n-i1).x(n-i2)$$

$$Y3(n) = \sum^{i1=0:M3} \sum^{i2=0:M3} \sum^{i3=0:M3} h3(i1,i2,i3).x(n-i1).x(n-i2).x(n-i3)$$

$$Y4(n) = \sum^{i1=0:M4} \sum^{i2=0:M4} \sum^{i3=0:M4} \sum^{i4=0:M4} h4(i1,i2,i3,i4).x(n-i1).x(n-i2).x(n-i3).x(n-i4)$$

$$Y5(n) = \sum^{i1=0:M5} \sum^{i2=0:M5} \sum^{i3=0:M5} \sum^{i4=0:M5} \sum^{i5=0:M5} h5(i1,i2,i3,i4,i5).x(n-i1).x(n-i2).x(n-i3).x(n-i4).x(n-i5)$$

Here the multi-dimensional matrices h1, h2, … hn are the n^{th} order Volterra coefficients which model the non-linearity, and Mn is the finite length memory of the non-linearity. With the memory depths (up to 1us) and non-linearity orders (up to 11^{th} order) to be considered for RF power amplifiers, the above model becomes computationally intractable. Simplification schemes must be employed to yield a practical pre-distorter product. These simplifications can be placed into 2 basic approaches:

1] Algorithmic approaches – The generic Volterra model in (1) has a number of attractive arithmetic properties that can be exploited to come up with efficient implementations.

2] Model reduction approaches – Although a totally generic Volterra (or some other generic model) is desired, it is known that RF power amplifier models typically have a lot of Volterra terms that are insignificant for practical implementation. These terms may be dropped without measurable degradation of the linearization performance.

A variety of different simplified pre-distortion systems, all using variations of the generalized model in (1), have been proposed in current literature. A few of them are listed here:

A] Truncated Volterra Systems [3, 5]

Direct-form, parallel-cascade, V-vector algebra based and a few other realizations of truncated Volterra systems have been proposed in the literature. These algorithmic reduction approaches are very efficient at linearization, but are computationally complex and often intractable due to the large number of parameters to be estimated, making them unattractive for real-time implementations.

B] Wiener Systems [6, 7]

A significant simplification of the Volterra model, the Wiener model consists of a linear filter followed by a memory-less non-linearity. A look-up table can be used to model the non-linearity, and an FIR filter to model the linear filter. Its effectiveness in modeling most RF power amplifiers is very limited. The estimation of the model parameters is reasonably complicated, making it unattractive for real-time adaptation.

C] Hammerstein Systems [6, 7]

Again, a reduction of the Volterra model, the Hammerstein model consists of a memory-less non-linearity followed by a linear filter. It is a simple memory nonlinear model, and it is easier to compute its model parameters than for a Wiener model. This model too is of limited effectiveness for modeling all types of RF power amplifiers.

D] Wiener-Hammerstein Systems [6, 7]

Cascading a linear filter, a memory-less non-linearity and another linear filter form a Weiner-Hammerstein model. This model is more general than a Weiner or a Hammerstein model, and covers a lot more

terms from the Volterra series enabling better modeling of the non-linearity.

E] Memory polynomial Systems [2, 4]

Constraining the Volterra series in (1) so that everything except the diagonal terms in the kernels are zero, i.e. hn(i1,i2,i3…) != 0 only when i1=i2=i3…, we get a memory polynomial model:

$$\mathbf{Y(n) = \sum^{k=0:K} \sum^{i=0:M} h_k(i).x(n-i)|x(n-i)|^k}$$

Where M is the memory length and K is the non-linearity order. This model (and its variations) has been shown to be very effective at linearizing wideband power amplifiers, and have reasonable hardware and software computational requirements.

Various combinations of the above models have also been suggested in the literature, each with its own pros and cons. A commercially viable pre-distorter needs to be adept at tackling a wide variety of non-linear behaviors, and might require different modeling schemes for different applications.

For most of these models, the pre-distorter coefficients are adapted with an indirect learning architecture using least squares identification.

III. GC5322 PRE-DISTORTION TECHNIQUE

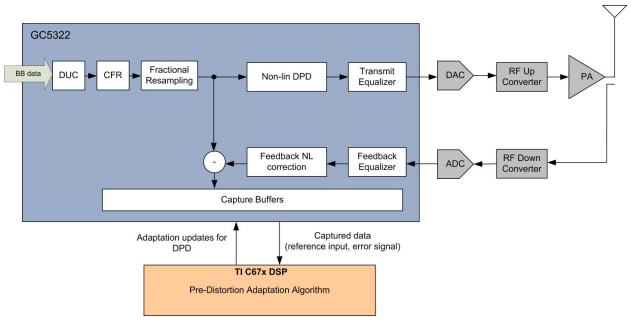


Figure 2: DPD System Diagram

In the GC5322 pre-distorter implementation a combination of algorithmic and model reduction approaches are utilized for a tractable realization. The number of terms in (1) can be significantly reduced by eliminating redundancies associated with various index permutations. And the Volterra coefficients can be assumed to be symmetric without any loss of generality. Furthermore, the real input signal to the power amplifier x(n) can be expressed in terms of its complex baseband representation $x(n) = Re\{e^{jw0n}X(n)\}$, where $w0=2\pi f0$, and f0 is the center frequency of the band of interest.

Since for band-limited systems we are only interested in frequency components close to the carrier frequency f0, writing the Volterra series in terms of complex baseband signals will help in significantly reducing the number of terms we have to consider and guides the choice of model architecture. For example, the even order inter-modulation terms will lie far away from the frequency band of interest, allowing us to further drop half the terms in (1). The model is rotationally invariant, which allows for further simplifications. This means that a phase shift on the input of the PA produces exactly the same phase shift on the output. The implication is that (1) can then be reduced to terms involving products of the signal and powers of its magnitude squared. Moreover it is known that the PA is causal, and it is assumed that the linear portion of the PA is minimum phase (or sufficiently so). This further restricts the Volterra terms.

In PA implementations, the processing is performed in stages. By exploiting this, the model can be simplified (in the number of terms required for a given application) into cascade sections with each matched to the needs of compensating the distortions induced by the particular PA stage.

The digital pre-distorter implemented in the GC5322 is split into these 3 major blocks:

1. Linear Equalizer

Restricting the Volterra series in (1) to only the linear terms with memory M1, we get the model for the linear equalizer block:

$$\mathbf{Y1(n) = \sum^{i=0:M1} h1(i).x(n-i)} \qquad \mathbf{(2)}$$

A (M1-1) taps long complex transmit equalizer can account for linear distortions in the RF transmit path and the power amplifier. It can be considered as the linear time-invariant half of a Hammerstein model. This equalizer primarily compensates for filtering in series with the amplifier, such as matching networks, duplexers, and IF filtering. The equalizer implemented in the GC5322 provides a correction time span from 100 to 200ns depending on the clock rates chosen. This places a maximum amplitude and group delay constraint on the analog design. A 2ns peak-peak group delay and a 1dB peak to peak amplitude ripple specification for the analog portion of the transmitter design was deemed to be a reasonable compromise between the analog and digital complexities.

The hardware implementation of (2) provides a complex FIR filter on both the real and imaginary data streams. This allows for independent equalization of the real and imaginary signal paths, and can compensate for I/Q gain/phase/delay mismatch.

2. Non-Linear DPD

Non-linear memory effects in PA's can range from a couple of ns to as much as 1us depending on the PA design and signal BW. This combined with the high orders of non-linearity (form 5th order for class AB PA's all the way to 11th order for Doherty PA's) to be compensated for makes selection of suitable non-linear pre-distorter architectures a daunting task.

Simplifying the Volterra series in (1) by restricting it to only the non-linear diagonal terms with memory M2, and dropping even terms as mentioned above, we get a model for the non-linear pre-distorter block:

$$\mathbf{Y(n) = \sum^{i=0:M2} h3(i,i,i).x(n-i).|x(n-i)|^2 + \sum^{i=0:M2} h5(i,i,i,i,i).x(n-i).|x(n-i)|^4 + \sum^{i=0:M2} h7(i,i,i,i,i,i,i).x(n-i).|x(n-i)|^6}$$

+ other higher order terms depending on the polynomial modeling accuracy requirements of the adaptation algorithm. **(3)**

This pre-distorter block can account for the bulk of the PA non-linearity. If memory in this block is ignored, it

can be considered as the memory less non-linearity portion of a Hammerstein model. With memory included, it can be used as a memory-polynomial based pre-distorter. Rearranging terms, we get:

$$Y(n) = \sum^{i=0:M2} \{ h3(i,i,i).|x(n-i)|^2 + h5(i,i,i,i,i).[|x(n-i)|^2]^2 + h7(i,i,i,i,i,i,i).[|x(n-i)|^2]^3 + \text{higher order terms}\}.x(n-i)$$

$$= \sum^{i=0:M2} LUT(|x(n-i)|^2).x(n-i)$$

This re-arrangement of terms has reduced the equation to an FIR form, and enables us to implement the polynomial in $|x(n-i)|^2$ in a hardware efficient look-up table (LUT) form. The order of the polynomial is limited by the modeling accuracy tolerance of the adaptation algorithm.

For some types of RF power amplifiers there are additional memory effects that are dependent on the signal envelope history. These could be due to thermal and power supply transients that act nearly as a multiplicative gain that is a function of the power history. Considering terms from the Volterra series in (1) that involve cross products between the signal and its exponentiated envelope (and excluding terms already covered by equation 3), we get:

$$\begin{aligned} Y(n) = & \sum^{i=0:M3} h3(i,i,0).|x(n-i)|^2.x(n-i) + \\ & \sum^{i=0:M3} h5(i,i,0,0,0).|x(n-i)|^2.|x(n)|^2.x(n) + \\ & \sum^{i=0:M3} h5(i,i,i,i,0).|x(n-i)|^4.x(n) + \\ & \sum^{i=0:M3, i\neq j} \sum^{j=0:M3} h5(i,i,j,j,0).|x(n-i)|^2.|x(n-j)|^2.x(n) + \\ & \sum^{i=0:M3} h7(i,i,0,0,0,0,0).|x(n-i)|^2.|x(n)|^4.x(n) + \\ & \sum^{i=0:M3} h7(i,i,i,i,0,0,0).|x(n-i)|^4.|x(n)|^2.x(n) + \\ & \sum^{i=0:M3} h7(i,i,i,i,i,i,0).|x(n-i)|^6.x(n) + \\ & \sum^{i=0:M3, i\neq j} \sum^{j=0:M3} h7(i,i,j,j,0,0,0).|x(n-i)|^2.|x(n-j)|^2.|x(n)|^2.x(n) + \\ & \sum^{i=0:M3, i\neq j} \sum^{j=0:M3} h7(i,i,i,i,j,j,0).|x(n-i)|^4.|x(n-j)|^2.x(n) \\ & + \text{higher order terms} \end{aligned} \quad (4)$$

We see that most terms in this desired memory model involve single dimensional convolutions of the signal envelopes $|x(n)|^2$,$|x(n-i)|^4$ and $|x(n-i)|^6$ and can be very well implemented using FIR filters.

The non-linear DPD implementation in the GC5322 provides a programmable memory depth between 10-60ns depending on the clock rates chosen, and typically uses a polynomial order in the range of 3 to 15 (depending on the amplifier type) to model the non-linearity. Interpolating look-up tables are used in the GC5322 pre-distorter to model complex polynomials of a high order enabling a large dynamic range.

3. Feedback Non-Linear Compensator and Smart Capture Buffers

Referring to figure 2, the feedback signal from the power amplifier is used to compute the instantaneous error, which along with the reference transmit signal can be captured in a pair of on-chip memories. These captured signals can be read back by the DSP processor which implements the adaptation algorithms for the pre-distorter blocks. Different signal metrics (like average signal levels, or peak content), are monitored and can trigger a capture when an optimum data set is collected. This programmable data monitoring technique helps the adaptation algorithms to converge faster and prevents it from diverging in the absence of suitable transmit data. An 8-tap complex linear equalizer and a non-linear compensator consisting of a complex multiplier and a look up table help compensate for distortions in the RF/analog feedback signal chain.

A high power 150W Doherty PA with significant memory effects for a 20MHz high PAR OFDMA based system might require all of the above pre-distorter blocks presented here to achieve optimum linearization. Whereas a smaller 5W class-AB PA for a 5MHz low PAR application might do just well with only one of the LUTs in the non-linear DPD block active, and without any adaptive compensation to keep costs low. The pre-distorter implemented in the GC5322 is intended to be flexible enough to work with a vast variety of power amplifier models, and comprehensive enough to account for a majority of the power amplifier non-linear effects while still keeping complexity low to enable real time adaptation.

IV. Pre-distortion Adaptation Algorithm

A direct learning architecture has been used in the pre-distortion adaptation algorithm implemented on a TI C67x DSP. A model of the pre-distorter is maintained in software, and its parameters optimized to minimize the error signal captured in the hardware. The adaptation algorithm periodically reads back the captured signals from the hardware capture buffers, and uses them to train the pre-distorter model. The optimized pre-distorter parameters are then regularly updated back to the hardware. Square root Kalman filter based minimization algorithms are used to adapt the pre-distorter model parameters so as to minimize the parameter RMS error. The frequency of updates required to the DPD parameters depend on the PA topology and its operating conditions. More details on these adaptation algorithms will be presented in a future paper.

V. Lab Results

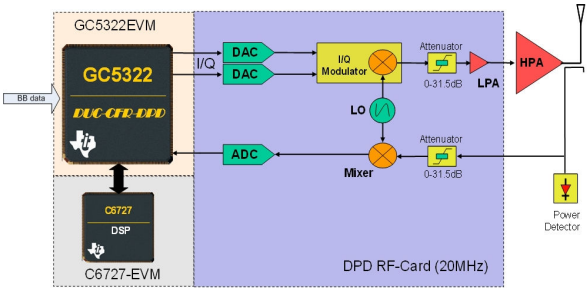


Figure 3: GC5322 evaluation platform system diagram.

The GC5322 evaluation platform (Fig. 3) was used to test the capabilities of the pre-distortion hardware. A variety of different RF architectures can be supported by the GC5322 (zero/low/high IF, analog/digital quadrature modulation, common/split LO etc.). The evaluation platform used to compile the results presented here consists of a GC5322 evaluation module (which includes a TI C6727 DSP), and two different versions of TI reference RF up-down conversion boards, a 'WiMax' and a 'WCDMA' version, both with a low IF, analog quadrature modulation and a common LO for the transmit and feedback paths. More details on the architecture are listed in Table 1.

Evaluation System Configuration		
RF Card Version	WiMax	WCDMA
DUC Input Sample Rate	11.2MSPS (WiMax)	3.84MSPS (WCDMA), 1.28MSPS(TD-SCDMA), 4.333MSPS (MC-GSM), 30.72MSPS (LTE)
CFR Sample Rate	67.2MSPS (WiMax)	61.44MSPS (WCDMA, TD-SCDMA, LTE), 69.333MSPS (MC-GSM)
DPD Sample Rate	112MSPS	122.88MSPS
DAC	DAC5682 @ 672MHz Complex	DAC5682 @ 737.28MHz Complex
ADC	ADS5444 @ 224MHz Real	ADS5444 @ 245.76MHz Real
IF Frequency	168MHz	184.32MHz
RF Frequency	2.123GHz	2.139GHz
IQ Modulator	TRF3703	
Mixer	HMC214	
LO	TRF3761	
PLL	CDCM7005	

Table 1: GC5322 evaluation platform system parameters.

The results presented below are split into 2 sections:

A] A comprehensive analysis of performance gain provided by DPD and CFR at different output power levels and peak to average ratios for a 2-carrier WCDMA configuration.

B] A comparative analysis of the flexibility and adaptability of the pre-distortion hardware and software for a variety of different air interface standards (WCDMA, WiMax, TD-SCDMA, MC-GSM, LTE), each with a different peak to average ratio, signal bandwidth and modulation type.

A 3 stage PA consisting of a 2W Sirenza pre-driver, a 45W NXP class AB driver, and a 130W NXP LDMOS Doherty PA (with a P2dB of 55dBm) at 2.1GHz was used for all these experiments.

A] 2 Carrier W-CDMA results

Standard 3GPP test model signals (TM3-32 and TM1-64) were used as baseband data in these tests. Experiments were run at different PA output power levels [42.75dBm, 44.75dBm, 46.75dBm], peak to average signal power ratios [6dB, 7dB], and signal types [TM1-64, TM3-32]. Results are encapsulated in the graphs below.

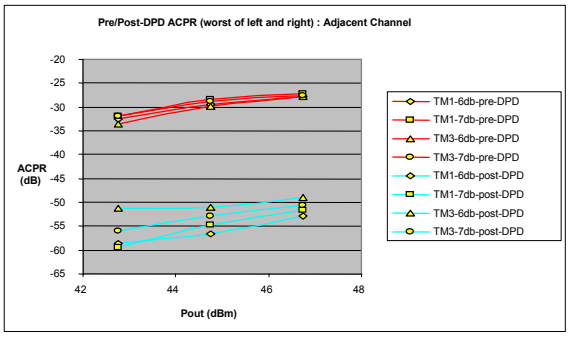


Figure 4-A: Adjacent channel ACLR Vs. Pout at different PAR levels and test signals, pre and post DPD

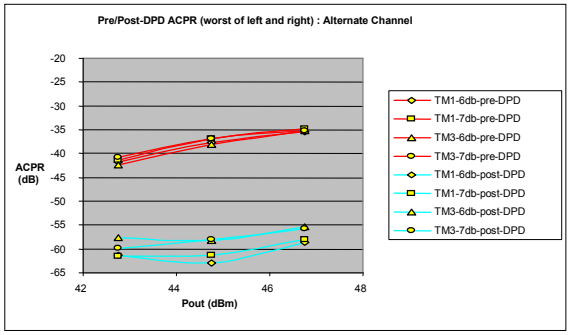


Figure 4-B: Alternate channel ACLR Vs. Pout at different PAR levels and test signals, pre and post DPD

Figures 4-A and 4-B show the adjacent and alternate channel leakage power ratios (ACLRs) before and after DPD for TM1 and TM3 test model data at 6 and 7dB PARs. Before DPD, the 3GPP ACLR requirement of 45dBc is violated by over 15dB. After DPD, these requirements are met with more than 5dB margin for all these test cases.

Figures 5-A and 5-B show the pre and post DPD spectrums for the 46.75dBm, 6dB PAR case for TM1-64 data. Worst case (of left and right sides) adjacent and alternate channel ACLR is -26dBc and -34dBc respectively before DPD. After DPD, the adjacent and alternate channel ACLRs are -53dBc and -59dBc respectively.

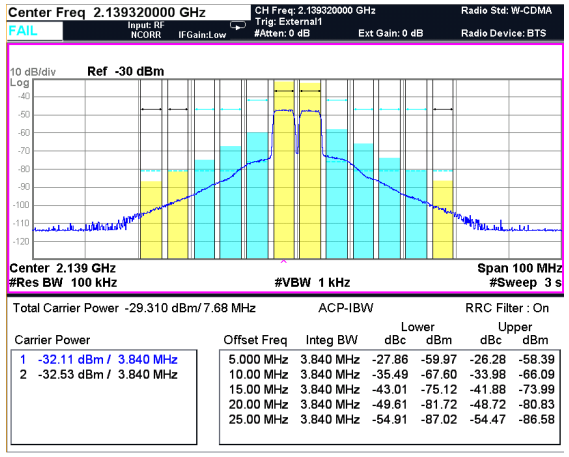


Figure 5-A: Pre-DPD spectrum at 46.75dBm Pout and 6dB PAR (TM1-64 data)

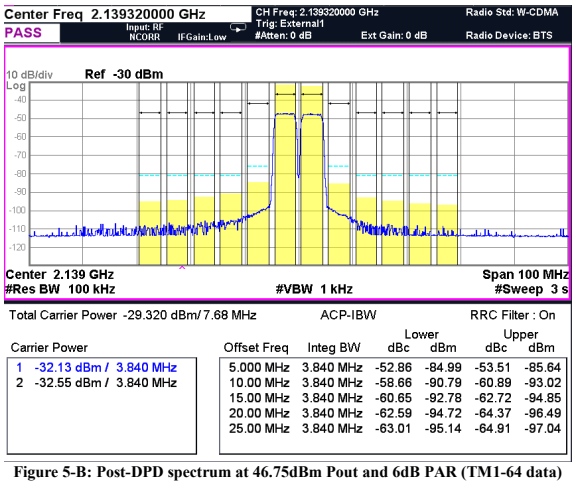


Figure 5-B: Post-DPD spectrum at 46.75dBm Pout and 6dB PAR (TM1-64 data)

Figures 6-A and 6-B show the pre and post DPD peak code domain error (PCDE) and error vector magnitude (EVM) metrics for the different output power, PAR and signal type combinations. In all cases, post DPD, we meet the 3GPP specs of -33dB and 17.5% respectively with considerable margins.

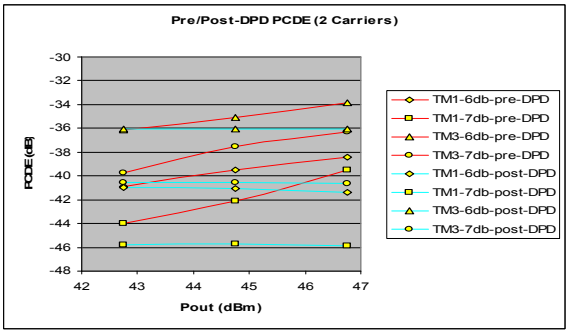


Figure 6-A: PCDE Vs. Pout at different PAR levels and test signals, pre and post DPD

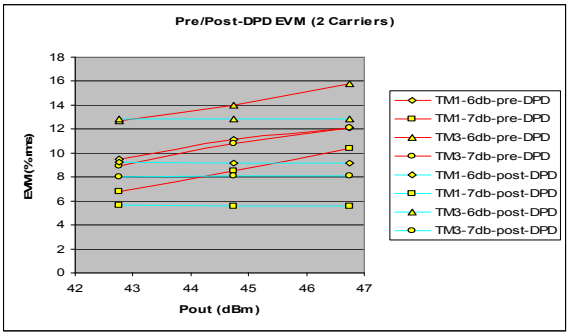


Figure 6-B: EVM Vs. Pout at different PAR levels and test signals, pre and post DPD

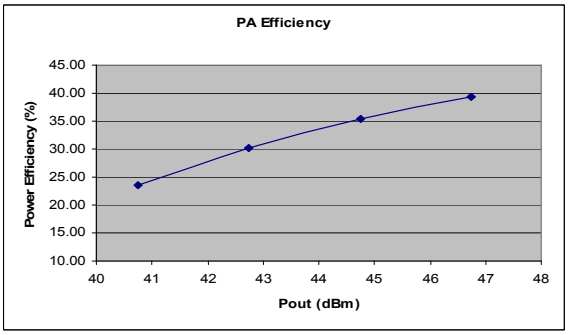


Figure 7: PA drain power efficiency Vs. output power

Figure 7 shows the drain power efficiency of the final PA stage versus the output power level. At 46.75dBm, the GC5322 pre-distorter enables this PA to be driven at close to 40% drain efficiency while still meeting all the transmit spectral mask and modulation accuracy requirements. Without DPD and CFR, this PA can only be operated up to 37dBm while still meeting these requirements. The PA efficiency drops to under 10% at this output power level.

In conclusion, with DPD and CFR, a 10x improvement in output power level and a 4x improvement in power efficiency are observed for this PA for this 2-carrier WCDMA application.

B] Comparative DPD results for WCDMA, WiMax, TD-SCDMA, MC-GSM and LTE signal types.

- **4-carrier WCDMA**

Figures 8-A and 8-B show the pre and post DPD spectrums for a 4 carrier WCDMA signal at 42.75dBm output power, 6dB PAR using TM1-64 data. Worst case adjacent and alternate channel ACLR is -31dBc and -33dBc respectively before DPD. After DPD, the adjacent and alternate channel ACLRs are -51dBc and -56dBc respectively. Post-DPD, the EVM and PCDE are at 9.2% and -40.8dB respectively.

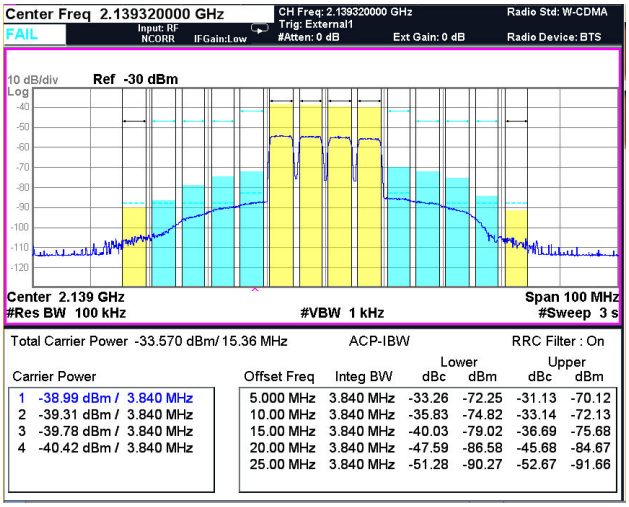


Figure 8-A: WCDMA: Pre-DPD spectrum at 42.75dBm Pout and 6dB PAR (TM1-64 data)

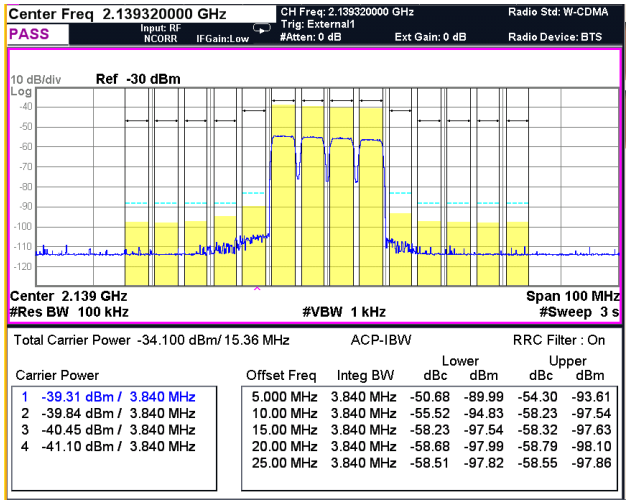


Figure 8-B: WCDMA: Post-DPD spectrum at 42.75dBm Pout and 6dB PAR(TM1-64 data)

- **2-carrier WiMax (2x10MHz)**

Figure 9-A shows the pre and post DPD spectrums for a 2x10MHz WiMax 802.11e signal configuration at the PA output for 43.75dBm output power and an 8.5dB PAR. A mix of 64QAM, 16QAM and QPSK data bursts are included in the test signals, with a TDD cycle of 60% downlink.

The worst case spectral mask requirement (of FCC, ETSI, Japanese) at 6.5MHz offset from the center of the channel is -44.5dB. At this output power level, pre-DPD, the spectral mask is violated by as much as 22dB. But post-DPD the spec is met with more than 2.5dB

margin to spare (more than 24dB improvement in the spectral performance).

Figure 9-B shows the pre-DPD (left) and post-DPD (right) EVM results for this test case. The plots on the top show the pre and post DPD constellations, and the bottom plots show the pre and post DPD error vector spectrums. The EVM improved from -19dB before DPD to -32dB after DPD for this test case. The worst case EVM requirement per the standards is -30dB, which is met with over 2dB margin post DPD.

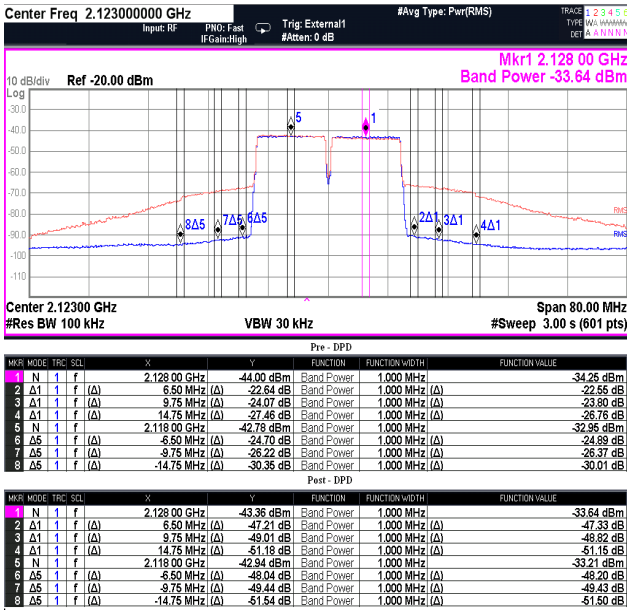


Figure 9-A: WiMax: Pre (red) and post (blue) DPD spectrums at 43.75dBm Pout and 8.5dB PAR

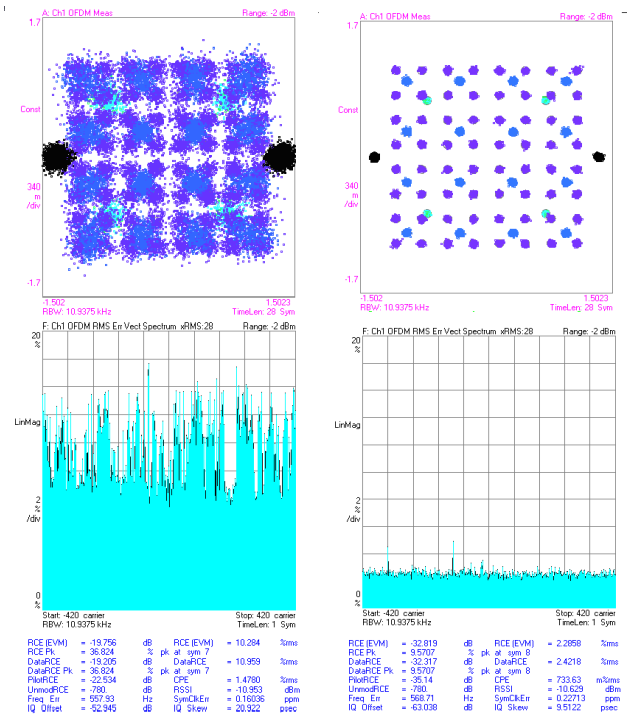


Figure 9-B: WiMax: Clockwise from top left: Pre-DPD Constellation, Post-DPD Constellation, Post-DPD Error vector spectrum, Pre-DPD Error Vector Spectrum plots for 43.75dBm Pout, 8.5dB PAR

- **6-carrier TD-SCDMA**

Figure 10-A shows the pre and post DPD spectrums for a 6 carrier TD-SCDMA signal configuration at the PA output for a 46dBm output power and an 8dB PAR. The test signals have a TDD cycle of 60% downlink. Marker results are shown at 1.6, 3.2, 4.8 and 6.4MHz offsets from the center of the last carrier. Between pre and post DPD results, we see 26-28dB improvement in the spectral response at these offset frequencies.

Figure 10-B shows the pre-DPD (left) and post-DPD (right) EVM results for this test case. The EVM improves from 11.6% before DPD to 5.3% after DPD for this test case.

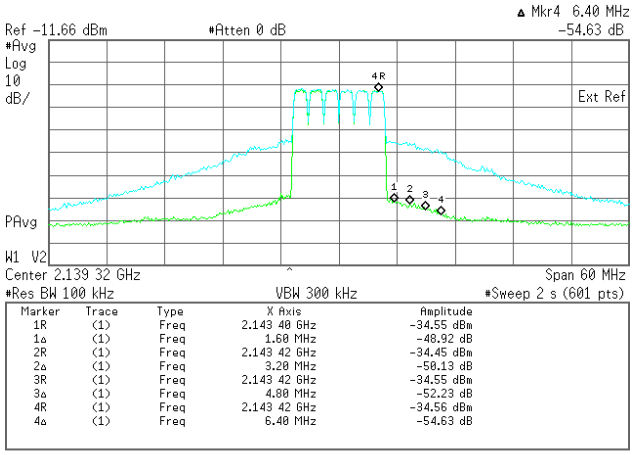


Figure 10-A: TD-SCDMA: Pre (blue) and post (green) DPD spectral plots at 46dBm Pout and 8dB PAR

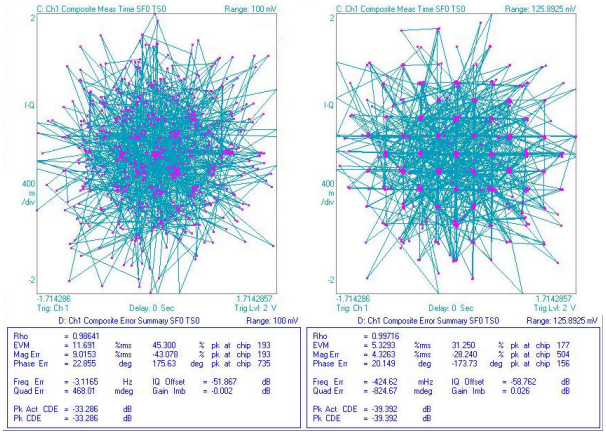
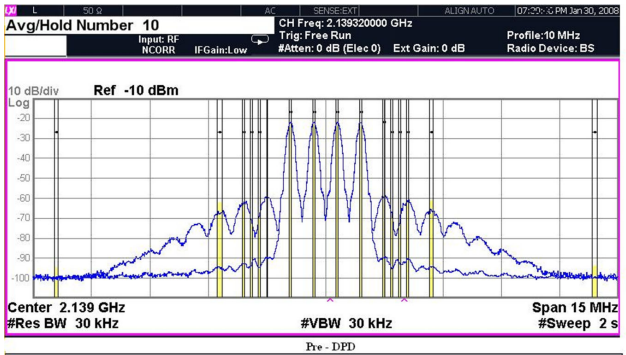


Figure 10-B: TD-SCDMA: Pre-DPD (left) and post-DPD (right) Constellation plots for 46dBm Pout, 8dB PAR

- **4-carrier MC-GSM (standard still evolving)**

Figure 11 shows the pre and post DPD spectrums for a 4 carrier MC-GSM (600kHz carrier spacing) signal configuration at the PA output for a 42dBm output power and an 6.3dB PAR. At a 600kHz offset from the center of the last carrier, we see a 33dB improvement in the spectral response between pre and post DPD results.



Pre - DPD

Total Carrier Power -16.560 dBm/ 120.00 kHz ACP-IBW RRC Filter : Off

Carrier Power	Offset Freq	Integ BW	Lower dBc	Lower dBm	Upper dBc	Upper dBm
1 -22.71 dBm / 30.00 kHz	600.0 kHz	30.00 kHz	-37.00	-59.70	-36.53	-59.24
2 -22.64 dBm / 30.00 kHz	800.0 kHz	30.00 kHz	-46.38	-69.09	-46.17	-68.88
3 -22.54 dBm / 30.00 kHz	1.000 MHz	30.00 kHz	-48.99	-71.70	-48.27	-70.97
4 -22.44 dBm / 30.00 kHz	1.200 MHz	30.00 kHz	-40.20	-62.90	-38.92	-61.63
	1.800 MHz	100.0 kHz	-39.76	-62.47	-38.57	-61.27
	6.000 MHz	100.0 kHz	-72.22	-94.93	-71.31	-94.02

Post - DPD

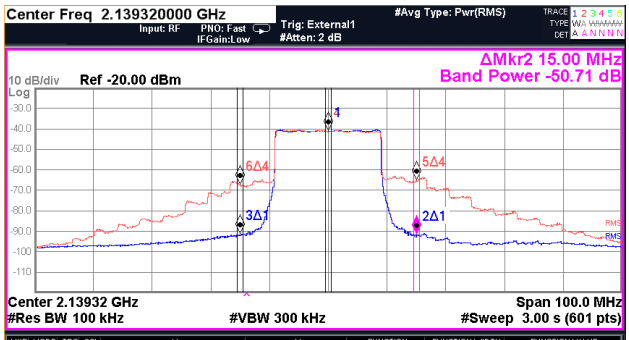
Total Carrier Power -16.370 dBm/ 120.00 kHz ACP-IBW RRC Filter : Off

Carrier Power	Offset Freq	Integ BW	Lower dBc	Lower dBm	Upper dBc	Upper dBm
1 -22.36 dBm / 30.00 kHz	600.0 kHz	30.00 kHz	-70.66	-92.04	-70.51	-92.89
2 -22.37 dBm / 30.00 kHz	800.0 kHz	30.00 kHz	-72.27	-94.66	-72.84	-95.22
3 -22.38 dBm / 30.00 kHz	1.000 MHz	30.00 kHz	-71.15	-93.54	-70.53	-92.92
4 -22.46 dBm / 30.00 kHz	1.200 MHz	30.00 kHz	-70.50	-92.88	-70.34	-92.73
	1.800 MHz	100.0 kHz	-67.24	-89.62	-66.98	-89.37
	6.000 MHz	100.0 kHz	-72.41	-94.79	-72.25	-94.64

Figure 11: MC-GSM: Pre (blue) and post (green) DPD spectral plots at 42dBm Pout and 6.3dB PAR

- **20MHz LTE (standard still evolving)**

Figure 12 shows the pre and post DPD spectrums for a 20MHz LTE signal (OFDMA, 64QAM modulation) configuration at the PA output for a 43.5dBm output power and a 7.5dB PAR. At a 15MHz offset from the center of the carrier, we see a 24dB improvement in ACPR between pre and post DPD results.



MKR	MODE	TRC	SCL	X	Y	FUNCTION	FUNCTION WIDTH	FUNCTION VALUE
1	N	1	f	2.139 32 GHz	-41.71 dBm	Band Power	1.000 MHz	-31.59 dBm
2	Δ1	1	f (Δ)	15.00 MHz (Δ)	-51.23 dB	Band Power	1.000 MHz (Δ)	-50.71 dB
3	Δ1	1	f (Δ)	-15.00 MHz (Δ)	-50.40 dB	Band Power	1.000 MHz (Δ)	-50.37 dB
4	N	2	f	2.139 32 GHz	-41.674 dBm	Band Power	1.000 MHz	-31.571 dBm
5	Δ4	2	f (Δ)	15.00 MHz (Δ)	-23.629 dB	Band Power	1.000 MHz (Δ)	-24.086 dB
6	Δ4	2	f (Δ)	-15.00 MHz (Δ)	-25.93 dB	Band Power	1.000 MHz (Δ)	-26.05 dB

Figure 12: LTE: Pre(red) and post(blue) DPD spectrums at 43.5dBm Pout and 7.5dB PAR

VI. CONCLUSION

We presented a novel hardware implementation of a flexible Volterra based pre-distorter for high power, wideband, multi-carrier RF power amplifier linearization. The pre-distortion scheme presented in this paper is shown to be highly efficient at improving power amplifier linearity and power efficiency. Lab results have shown PA power efficiency improvements of over 4x and ACPR improvements of over 20dB for a variety of PA topologies and air interface standards. The GC5322 integrated transmit solution presented here not only provides a significant environmental benefit, but also provides substantial cost savings both in capital expenditure and operational expenditure for next generation base stations. This highly flexible systems solution can be optimized for a variety of linearization applications ranging from low power Pico and Micro base stations to high power Macro base stations for CDMA/OFDM systems, with multi-mode signal bandwidths up to 30MHz. By providing an integrated DUC-CFR-DPD signal processing hardware solution, along with optimized DSP based adaptation software and a proven reference RF board design, it reduces the base-station component as well as integration costs, and enables faster time to market.

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