

# ***Amplifier Design and Topology for Microwave Applications*** ***(from LNAs to LPNAs to PAs)***

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# *Presentation Outline*



- 
- Amplifier requirements – practical view
  - Design considerations – multidisciplinary know how
  - Examples of practical amplifier designs and their performances

# *Amplifier Requirements*

## *(Wish list)*

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- High and flat gain
- Very low noise figure
- High output power and efficiency
- Extremely linear
- Very low phase noise
- No reflections or harmonics
- Super wide dynamic range
- Constant over temperature
- Very small size
- Very high MTBF

# *Practical Trade-offs*



- General:
  - Gain, NF vs BW
  - BW vs Power
  - Stability vs NF
  - BW, Gain and flatness vs practical matching
  - Linearity vs efficiency
  - Amplifier input/output protection vs NF, BW
  - Performance vs price

# *Practical Trade-offs*

## *- cont -*

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- Low Noise Amplifier:
  - Gain, VSWR, stability vs NF
  - Power, BW, linearity vs NF
- Power Amplifier:
  - Max power vs efficiency
  - Max power vs BW
  - Max power vs linearity & efficiency
  - Power vs environmental

# Meeting Specifications Dependents On:

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- \* Design:
  - Active device selection
  - Amplifier topology
  - CAD design tools
  
- \* Fab and Testing:
  - Implementation
  - Assy Processes
  - Test methodology
  - Environment

# *What Does It Take to Make a 'perfect' Amplifier ?*

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- Know device performance & limitations
  - Correct application of amplifier topologies
  - Experienced with CAD design tools
  - Understand the environmental impact
  - Posses world class processes
  - Expert in testing techniques
  - Verify data vs. environmental specs
-

# Active Devices

- **Heterojunctions:**
  - Reliable and commercially available
  - HEMTs & HBTs replace MESFETs & BJTs
  
- **Performance/Advantages depending on:**
  - compound material properties,
  - technology, mainly Gate geometry,
  - device capacitances and access resistances,
  - Attachment in the circuit
  - \$



# Material Properties Brief

	Si	GaAs	InGaAs	SiC	GaN
<b>Bandgap Energy (eV)</b>	1.1	1.4	0.8	3.2	3.4
<b>Breakdown Field (MV/cm)</b>	0.3	0.4	2	3.5	3.5
<b>Thermal Conductivity (W/cm*K)</b>	1.5	0.5	0.07	2.9	1.7
<b>Electron Mobility (cm<sup>2</sup>/ V*s)</b>	1,350	8,500	12,000	800	1,500
<b>Saturated Electron Velocity (*10<sup>7</sup> cm/s)</b>	1	0.8	0.75	2	2.4

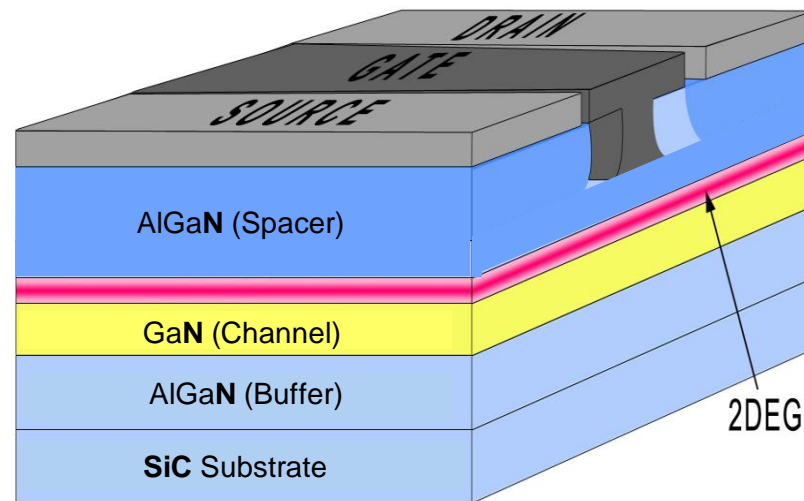
# *From MESFETs to HEMTs*



- HEMTs outperform MESFETs in NF, gain, and also operate to higher frequencies.
- “Heart of HEMT: 2DEG”
- This is due to superior electron transport properties in the channel:
  - higher mobility and density
  - higher transconductance
  - higher cut-off frequency ( $f_T$ )
  - lower layer resistances

# GaAs HEMT Basic Structure

- The electron channel is confined in a 2DEG layer, just under the Spacer layer
- Size: Channel width  $\ll$  Gate to Channel distance  $\ll$  Gate length



# From BJT's to HBT's

- BJT's: current gain ( $\beta$ ) highly dependent on doping level of Base and Emitter
- As for HBT's,  $\beta$  can be substantially increased by Base/Emitter junction bandgap engineering. Advantages:
  - low  $C_{BE}$ , thus higher frequencies
  - lower  $R_B$ , easier to match

# Amplifier Performance at X-Band vs Device



	Vds	NF	Gain	P-1dB	Phase Noise (@ 1 kHz Offset)	Psat	PAE
MESFET (GaAs)	5/10 VDC	Good, (even below 2GHz) (4 dB)	Poor (10 dB)	Good Typ 0.5W/mm (+17dBm)	Good (155dBc/Hz)	typ 2dB above P-1	<20%
PHEMT (AlGaAs/InGaAs)	3/8 VDC	Best (2.5 dB)	Good (13 dB)	Good Typ 0.65W/mm (+20dBm)	Poor (140dBc/Hz)	typ 3/5dB above P-1	35%
HEMT (AlGaN/GaN)	28/40 VDC	Good (3 dB)	Good (11 dB)	Very good 5W+/mm (+38 dBm)	Poor (140dBc/Hz)	typ 3/5dB above P-1	50% (@ Psat)
HBT (InGaP) (SiGe)	2/5 VDC	Good (4 dB)	Poor (9 dB)	Low (+16 dBm)	very good (160dBc/Hz)	typ 2dB above P-1	30%

# Amplifier Topologies

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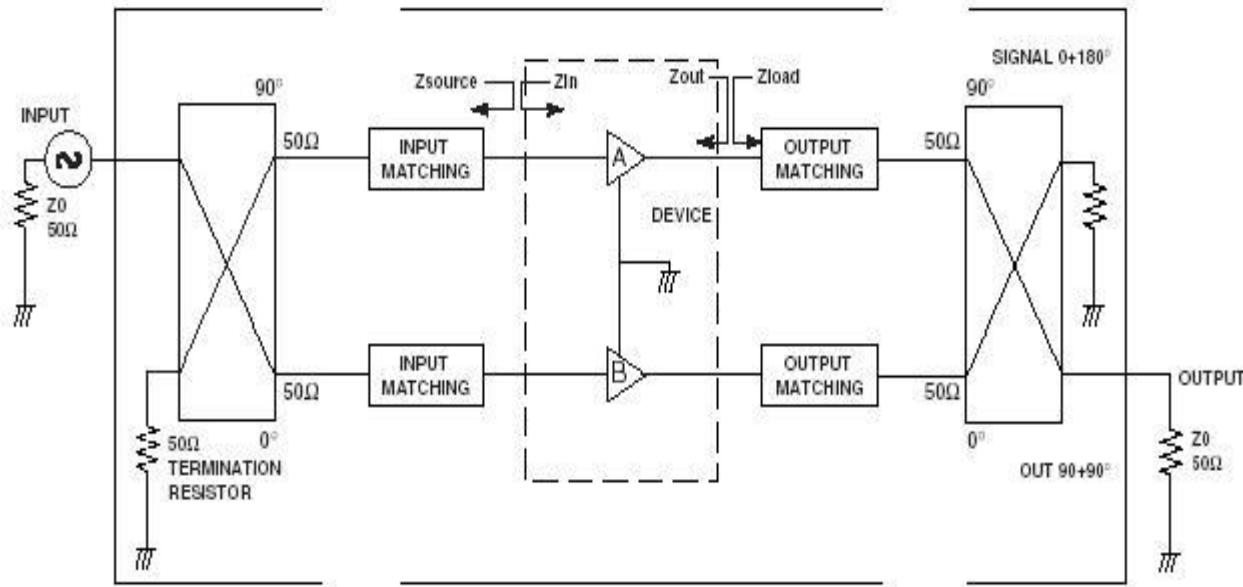
## \* **Single ended:**

- best NF, poor VSWR, nominal gain and power, narrow band, difficult to achieve stability

## \* **Balanced:**

- best VSWR, good NF, twice the power of single ended, very good stability, covers 1.5 octave, build-in redundancy

# Balanced Amplifier - basic block diagram -

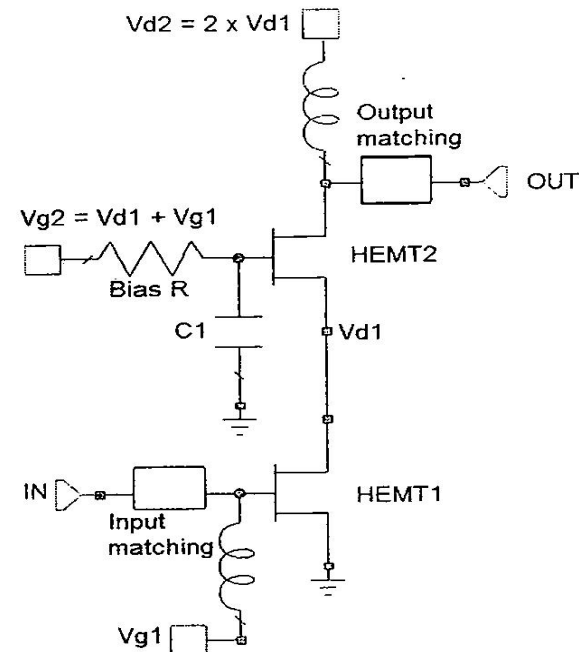


# Cascode Amplifier Topology

\* advantages:

- high reverse isolation
- higher gain and BW
- low power consumption
- higher input and output impedances vs single device

• Schematic





# *Amplifier Topologies* *(cont)*

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- **Distributed:**
  - Moderate to high flat gain over broad freqs
  - Moderate NF
  - fair power and linearity
- **Feedback amplifiers:**
  - Flat gain over many octaves
  - Good power and high linearity
  - Suppresses harmonics and spurious signals
  - Poor NF

# *Required Design Tools*



- 
- Microwave CAD: small and large S-param.
  - CAD Harmonic analysis
  - 3D EM simulation tool
  - Mechanical CAD: 2D and 3D
  - Thermal simulation tools
  - Reliability tools
  - Cascade analysis

# Amplifier Design Process



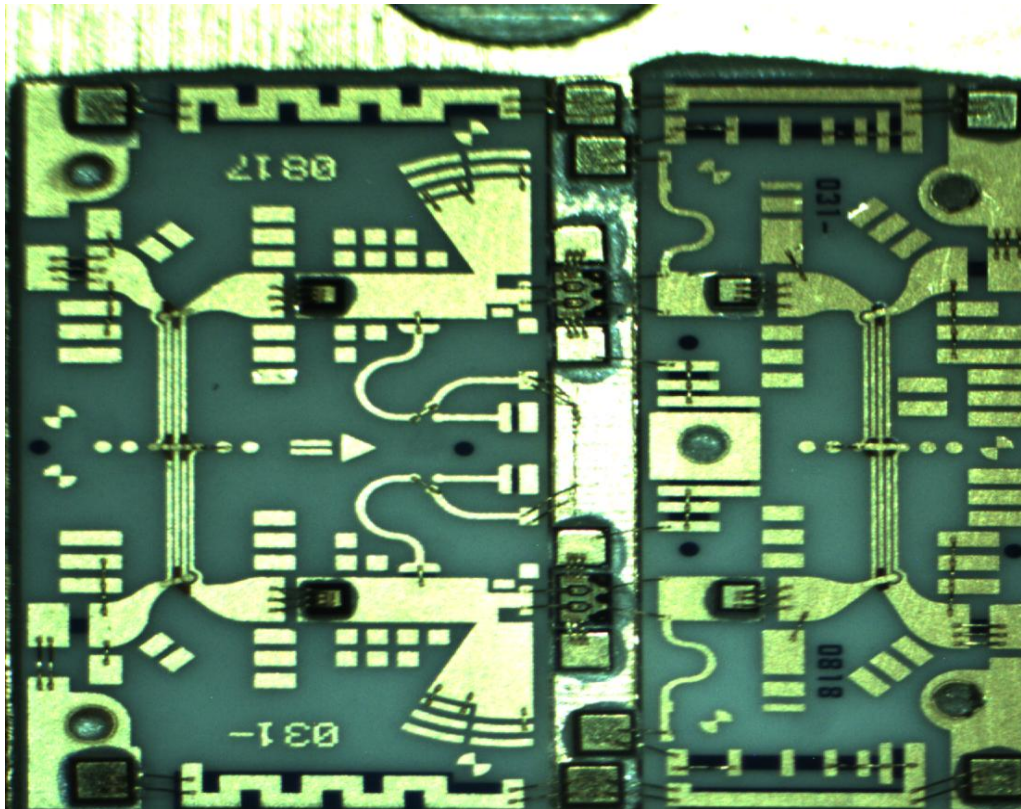
1. Select appropriate devices and topology vs requirement
2. CAD design using linear/non-linear simulation tools:
  - solve a matching problem, note that a different criteria is used for different amplifier types
  - depending on the application, optimize for gain, NF, Pout, and/or VSWR<sub>in/out</sub>
  - perform a stability simulation – it is a must!
3. Perform a sensitivity analysis and evaluate design
4. Make circuit layouts,
5. Fab and QC
6. Perform DVT/Qual
7. Implement tuning notes

# LNA Design Rules



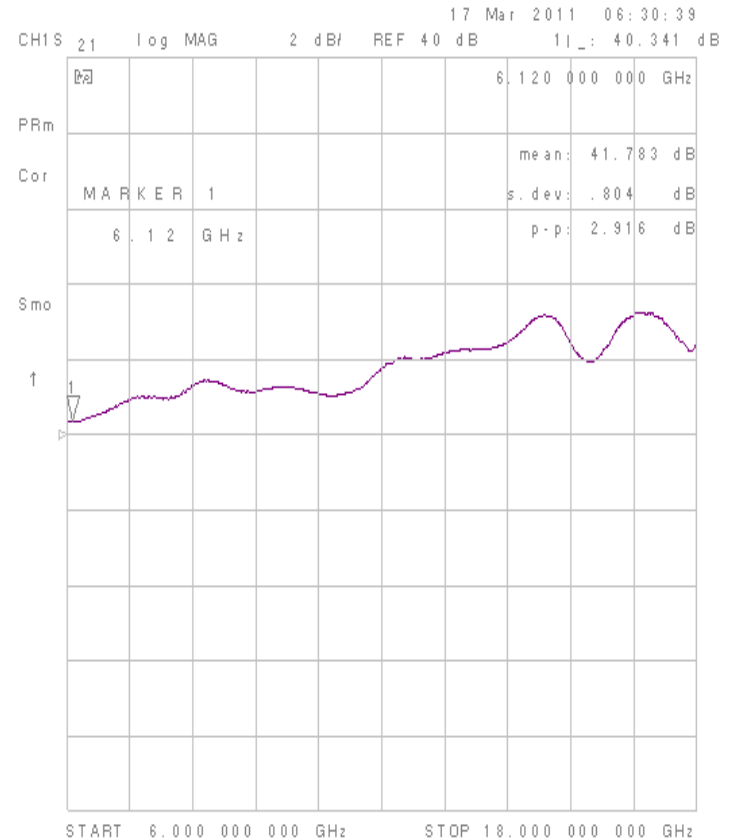
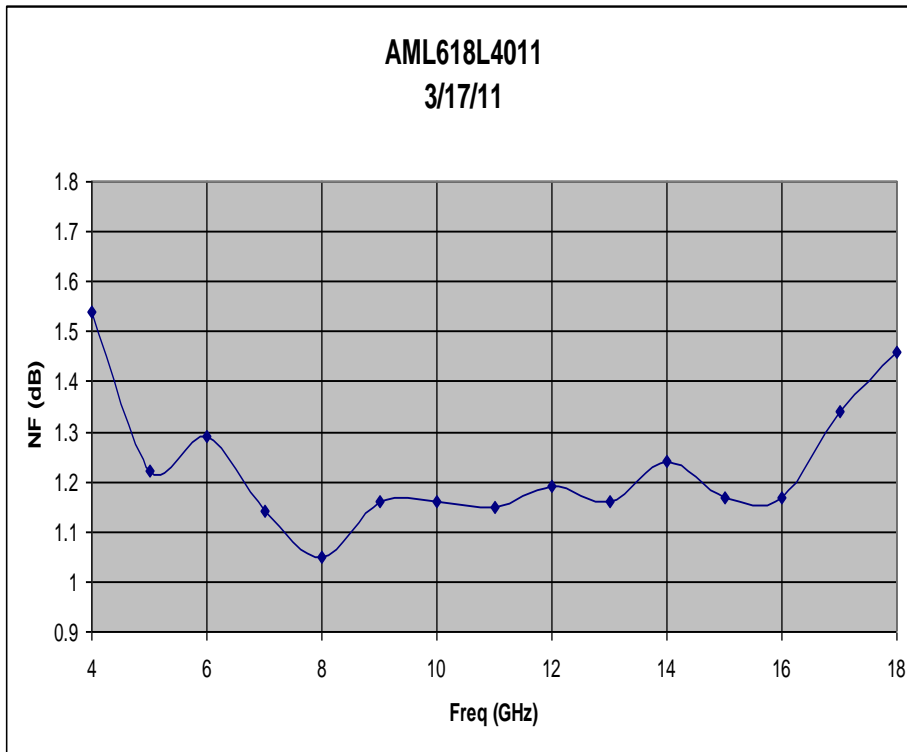
- \* Select devices that exhibit low NF, high gain, low current consumption in the band of interest
- \* Expect lower gain due to NF optimization
- \* Balanced topology is preferred, for stability and  $S_{11}$  reasons, and if no other constraints are dictated by requirements
- \* Match the input to  $G_{opt}$  for min NF and the output to  $S_{22}^*$ , using manufacturer's S-param
- \* Verify unconditional stability over a wide BW

# Example of Balanced Ku-Band LNA



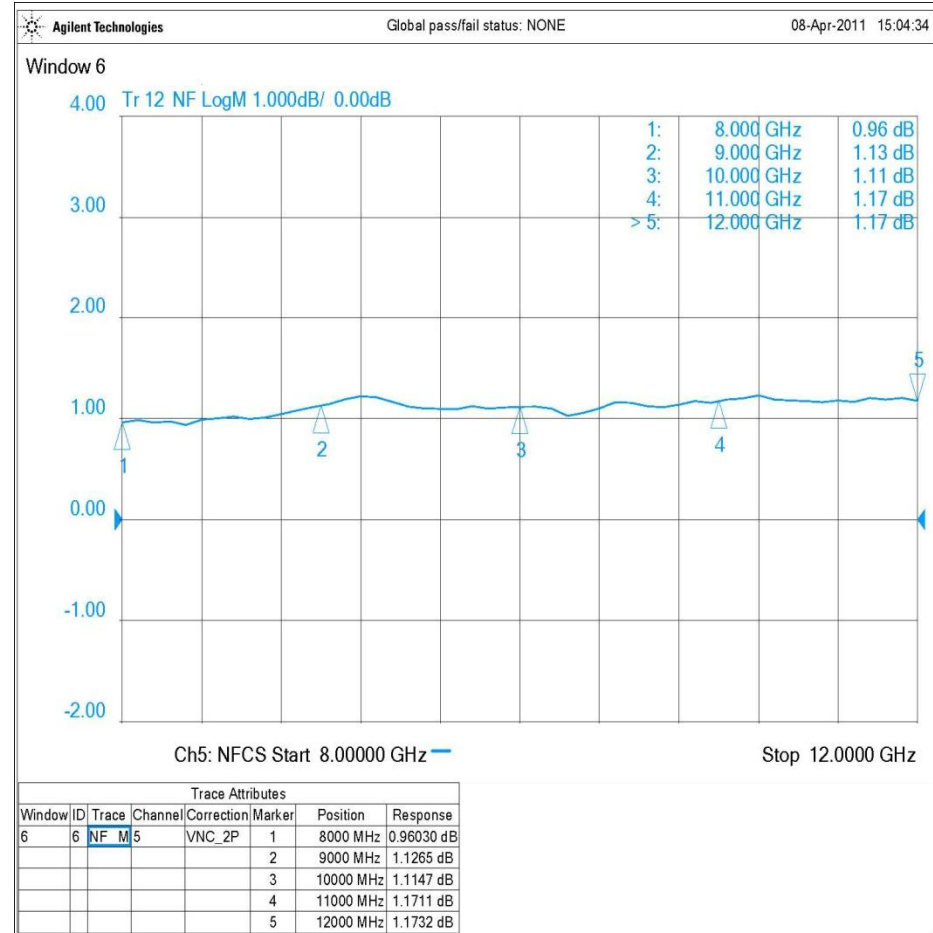
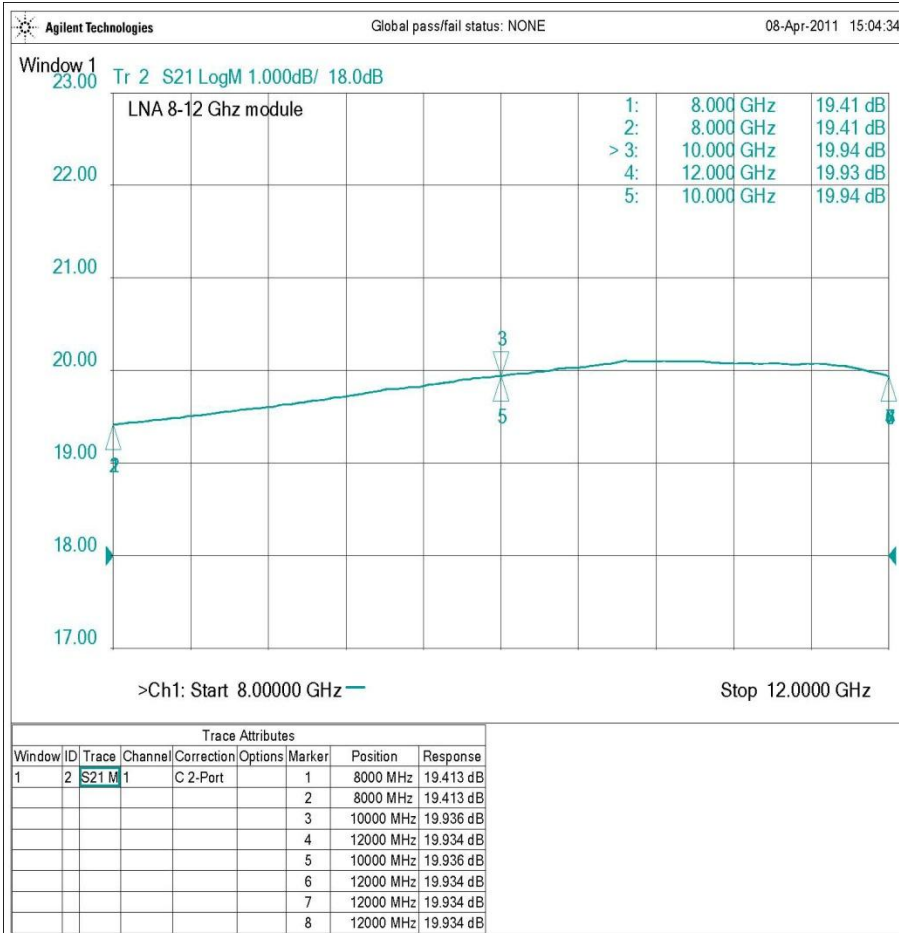
# Balanced Ku Band LNA

## - performance -



# Single Ended X Band LNA

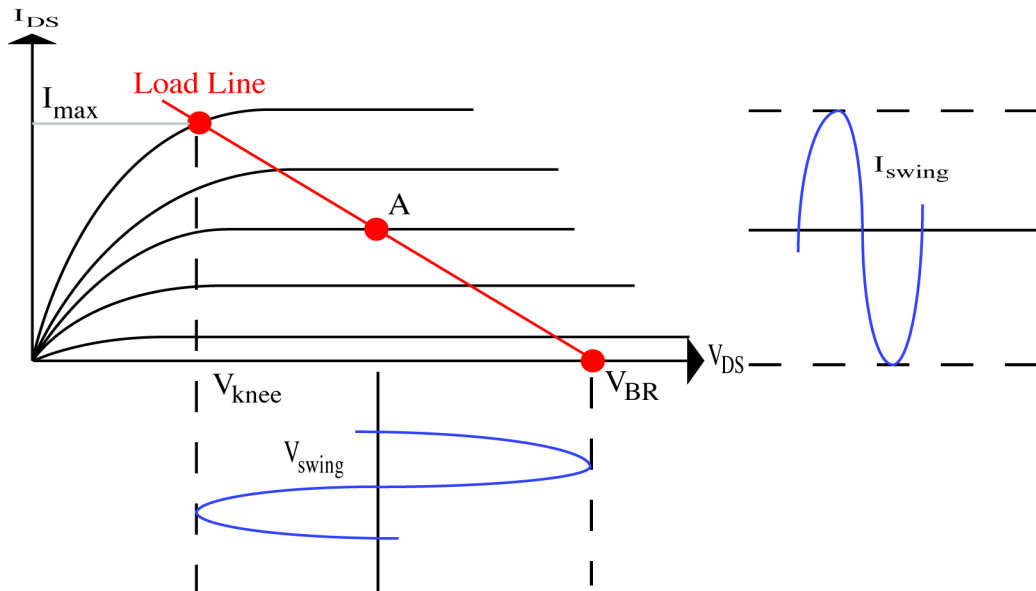
## - performance -



# GaN Power Amplifiers

## Why GaN ?

- Has higher carrier mobility (than SiC)
- Has highest power density/mm gate
- \* Reliability verified and commercially available



$$P_{out} = I_{max} \cdot (V_{BR} - V_{knee}) / 8$$
$$= (V_{BR} - V_{knee})^2 / (2 \cdot RL)$$

thus:

$P_{out}$  is maximized if the operational voltage is maximized!

**That's the key !**

- \* Other GaN Characteristics:
  - high output impedance
  - high efficiency
  - high linearity



# Example of Power Amplifier Design

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- Requirements over 9.9-10.7 GHz:
  - \*  $P_{sat} > 16W$ ;  $PAE > 45\%$
  - \*  $SSG > 11dB$ ; Power Gain  $> 9dB$
  - \*  $VSWR < 1.5:1$
  - \* DC available: 32V at 1.4A
  - \* Stable at any frequency
- Select device: TGF2023-02
- Note: it consists of two 6W unit GaN cells, 1.25mm gate
- Topology: Balanced
- Use S2p & Large Signal Device Model
- Use Gate and Drain pads S4p

# Example of Power Amplifier Design – cont.



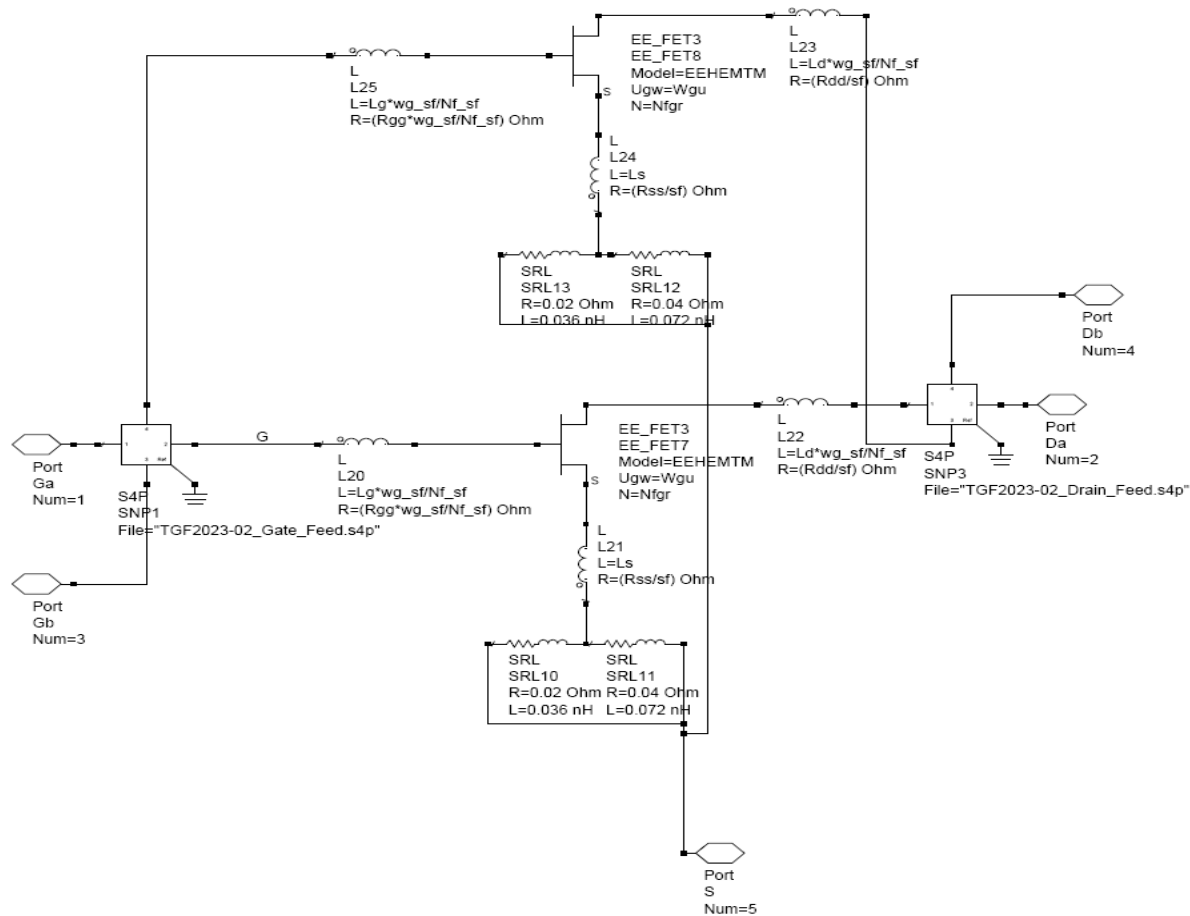
## Design Sequence:

- Create transistor circuit model: filename TGF2023-02\_32V250A
- Add Input and Output matching circuits to the above: filename TGF2023-02\_single
- Create the balanced amplifier: filename TGF2023-02\_bal

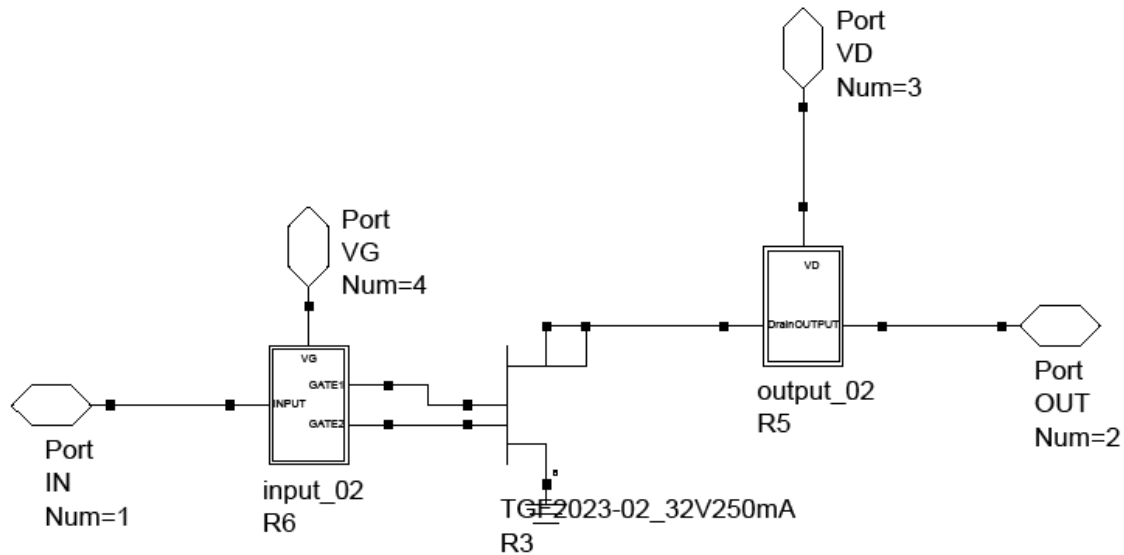
## Simulation:

1. Derive  $G_s$  using S-param for the Input circuit for, small signal (SS) gain
2. Verify  $S_{11}^*$  of FET matches  $G_s$ , and tune the input matching network if necessary; verify stability.
3. Using the load pull method derive  $G_{opt}$  vs. freq for optimum Pout and PAE ,
4. Derive  $G_L$  by looking at the output matching network,
5. Verify that  $G_{opt}$  matches  $G_L$  by using the Smith Chart in SS simulation and tune output matching network if necessary. Verify stability.
6. Check compression, Pout and PAE using HB
7. Tune circuits for  $G_s$  and  $G_L$  for trade-offs in flatness, gain, Pout and PAE in SS,
8. Re-check steps 2 and 5

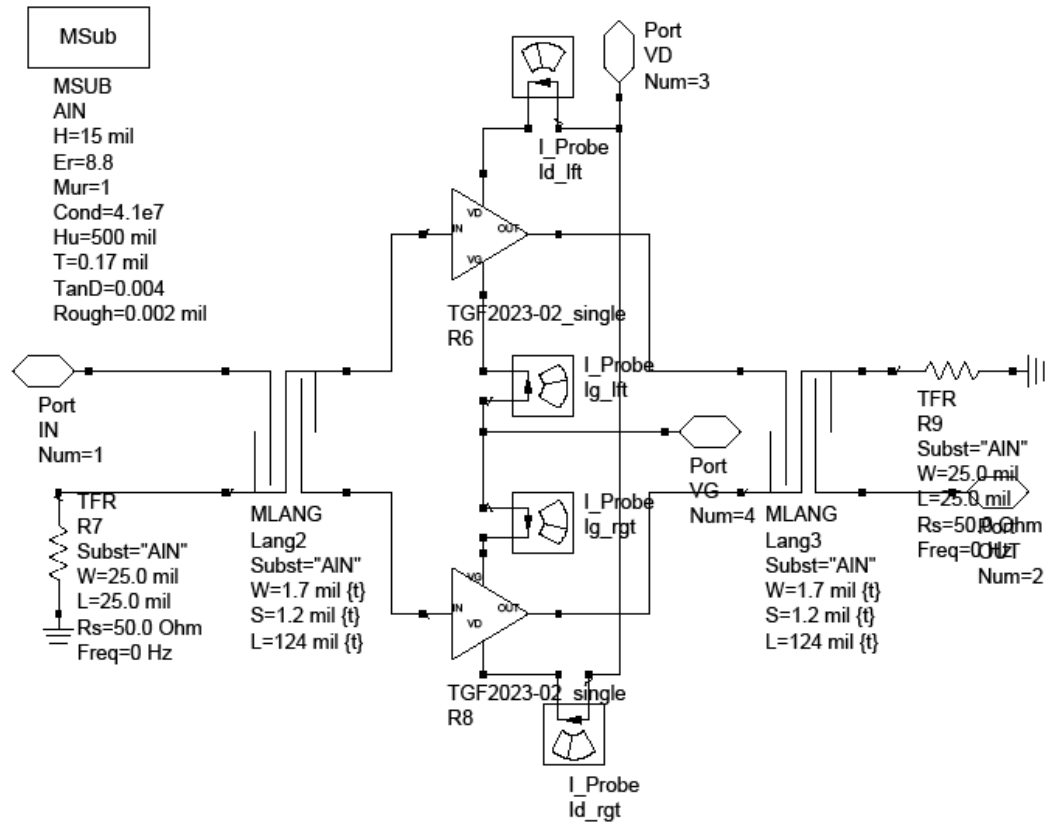
# Circuit schematic for TGF2023-02\_32V250A



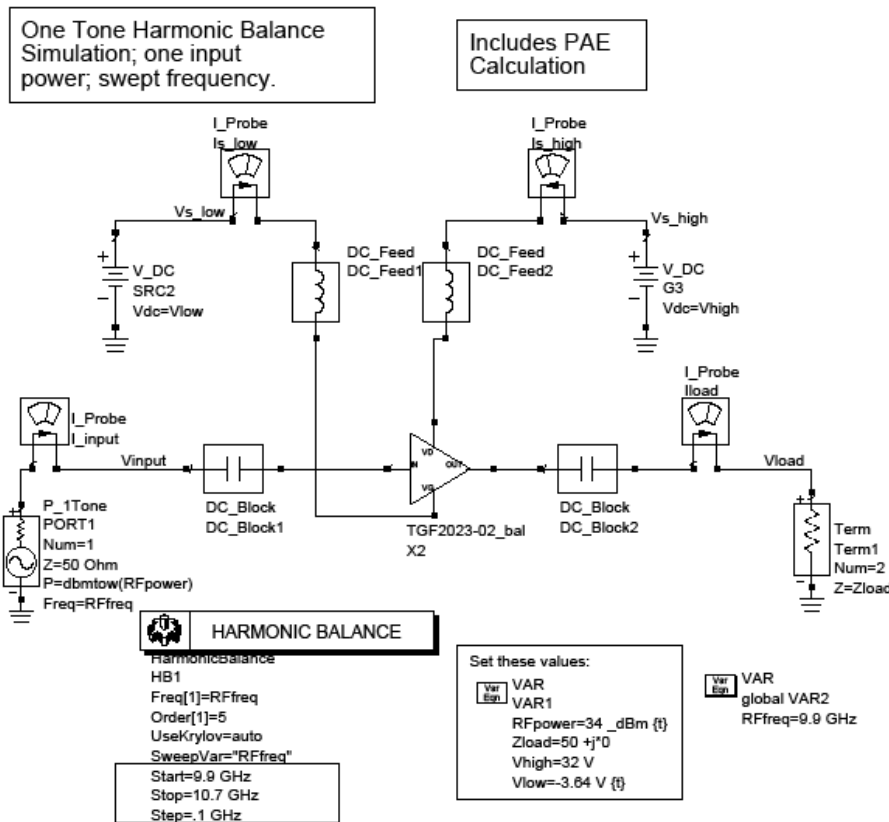
# Circuit schematic for TGF2023-02\_single



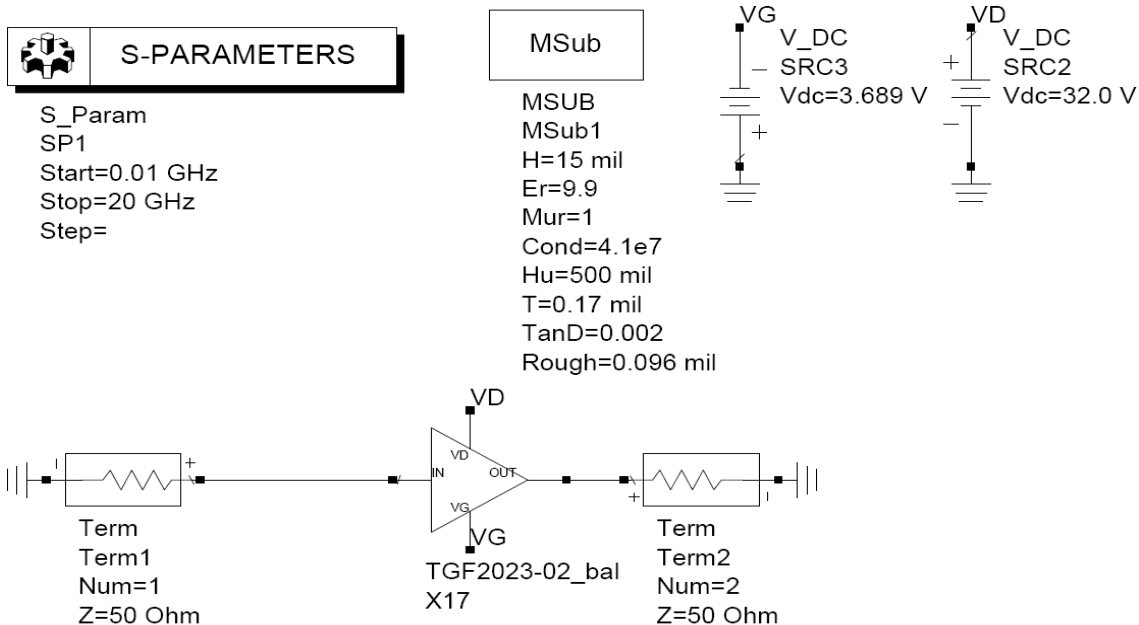
# Circuit schematic for TGF2023-02\_bal



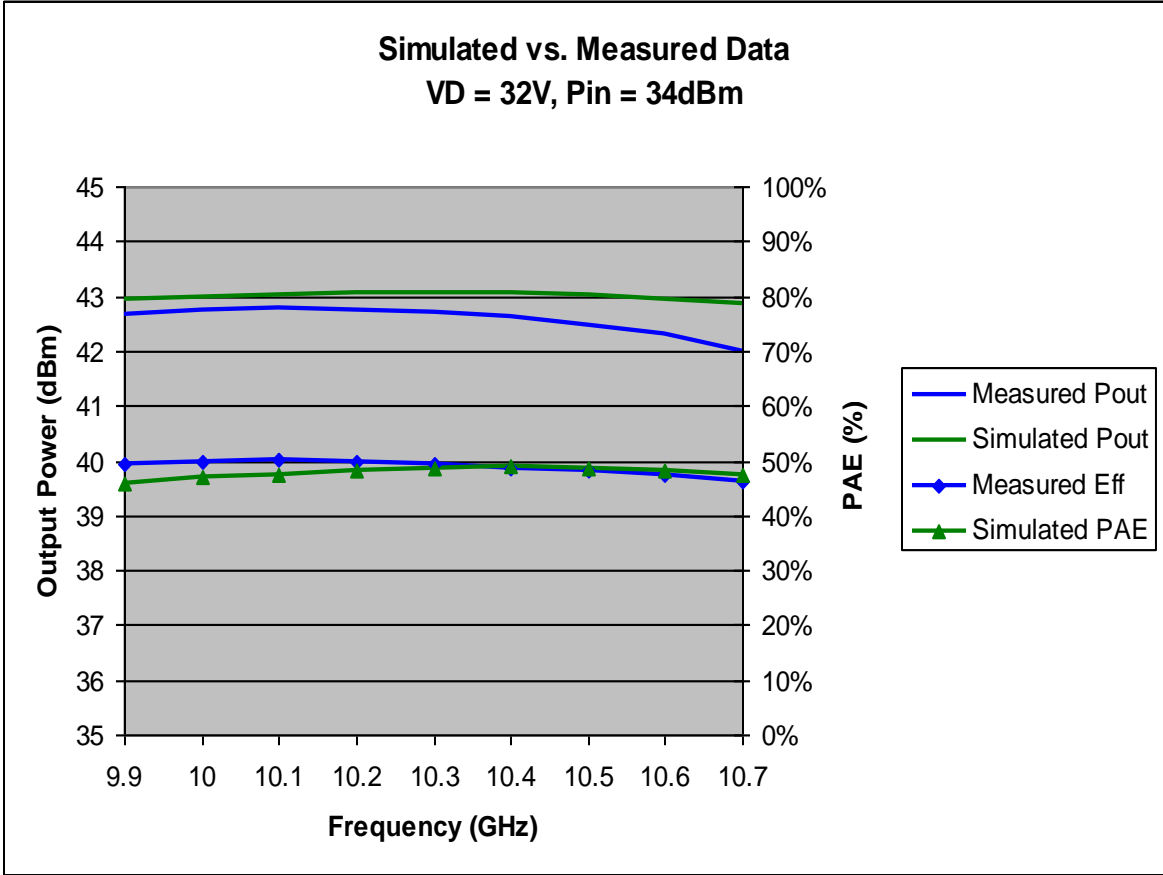
# Circuit schematic for HB simulation



# Circuit schematic for Small Signal simulation

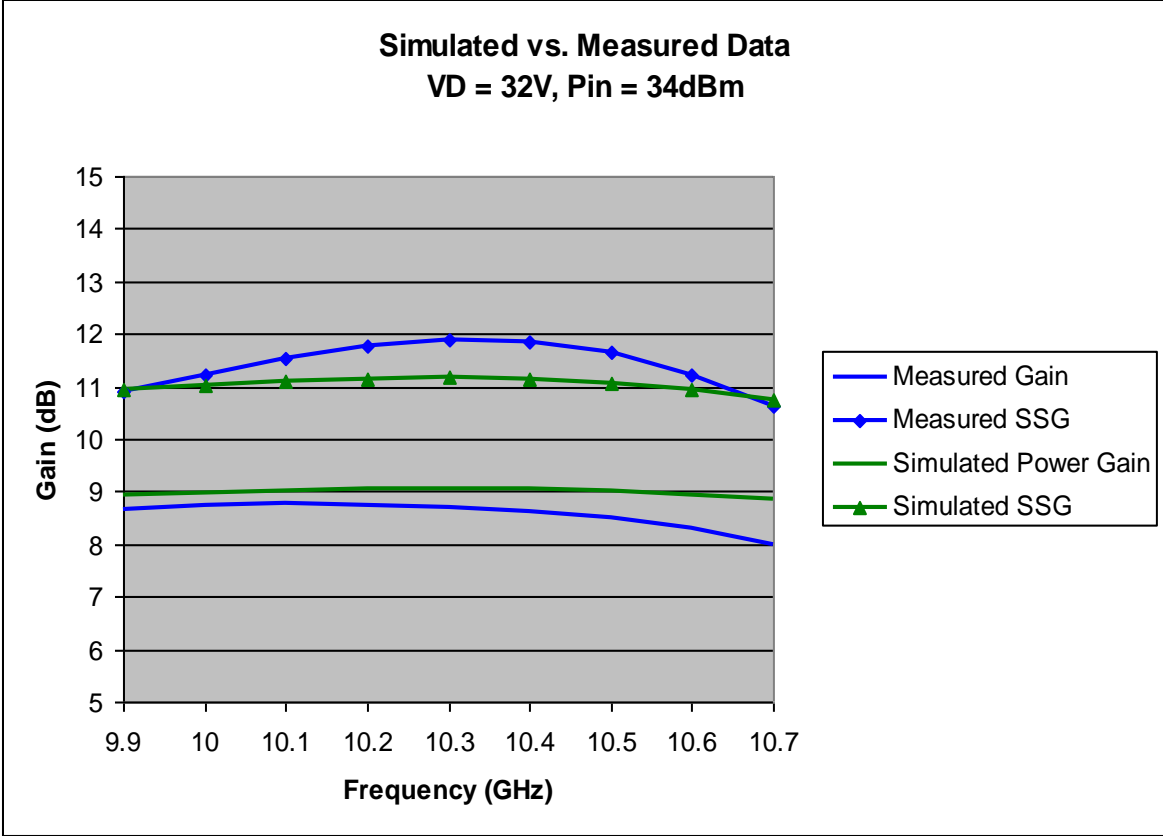


# GaN Module Simulation vs Measured Data

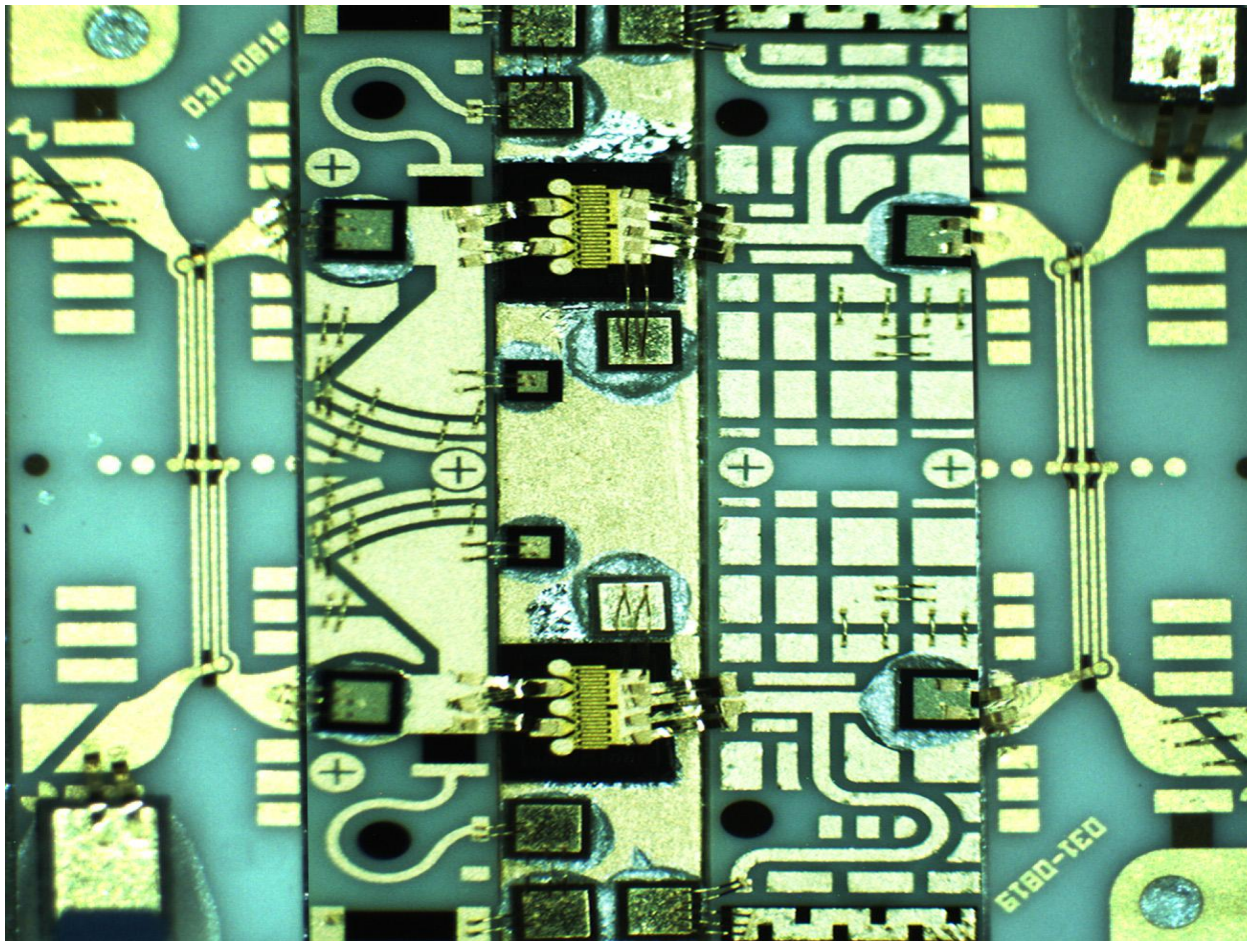




# GaN Module Simulation vs Measured Data

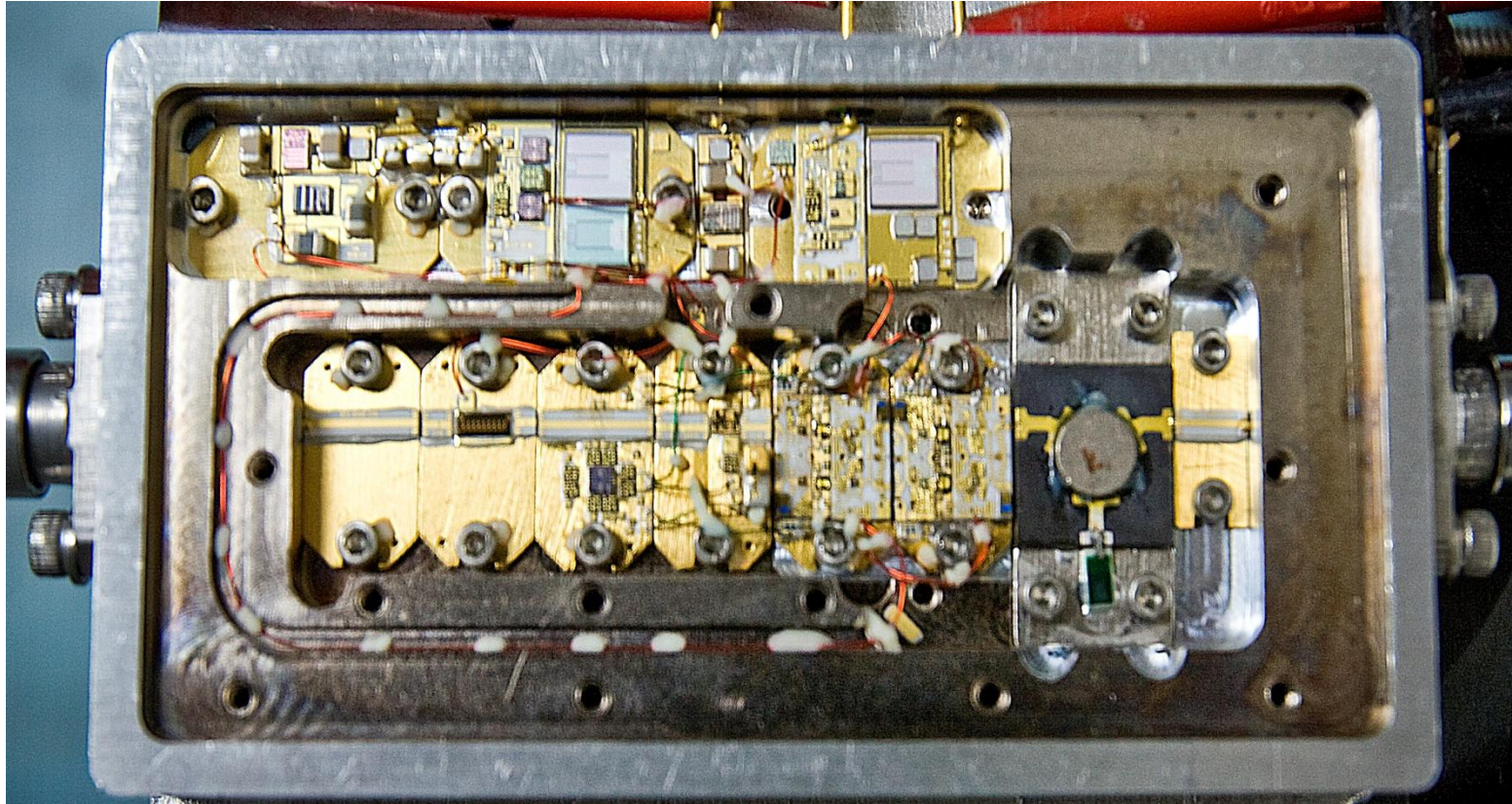


# GaN Module Image (.250x.250)

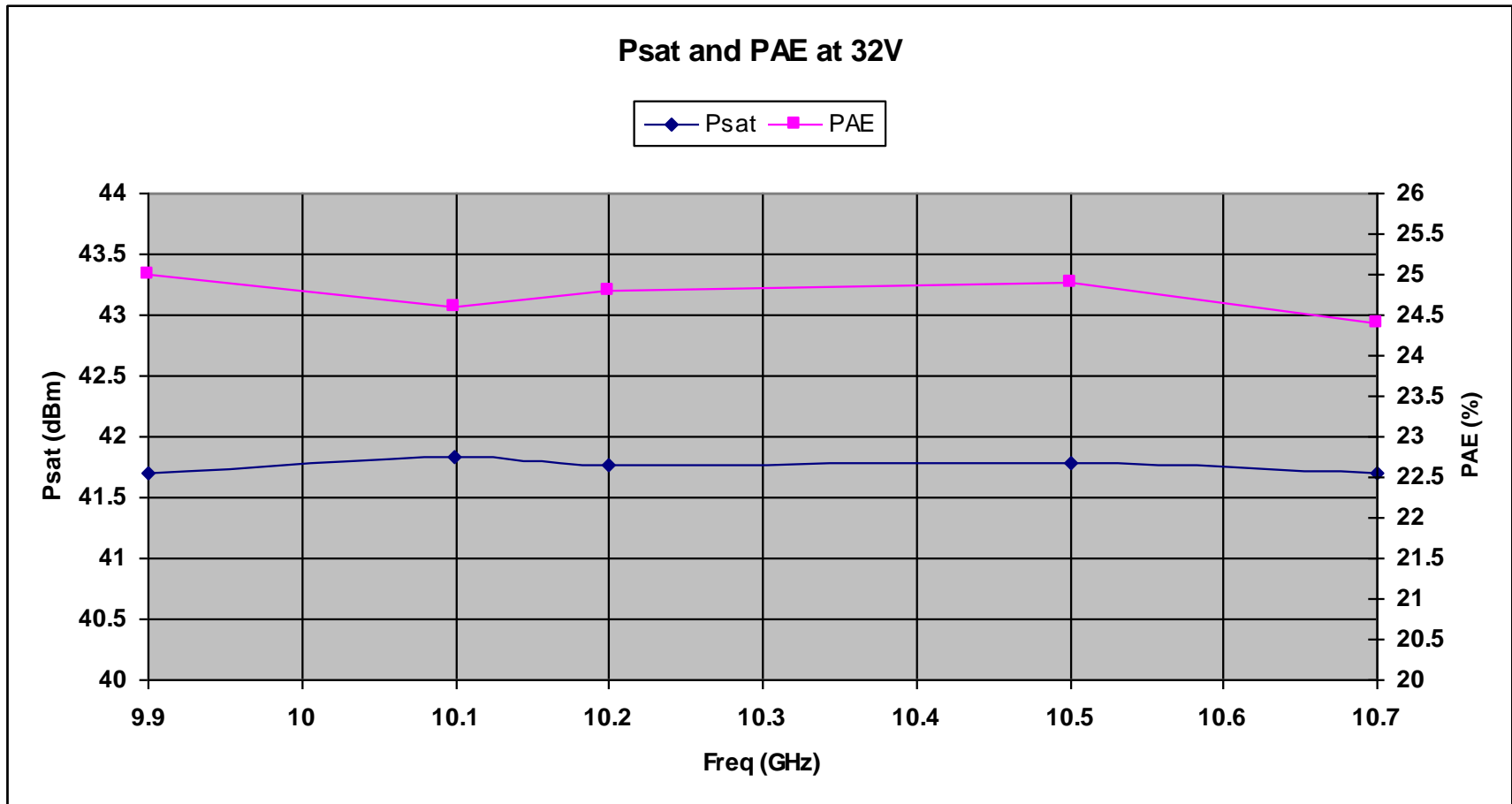




# Prototype X-Band PA with GaN modules



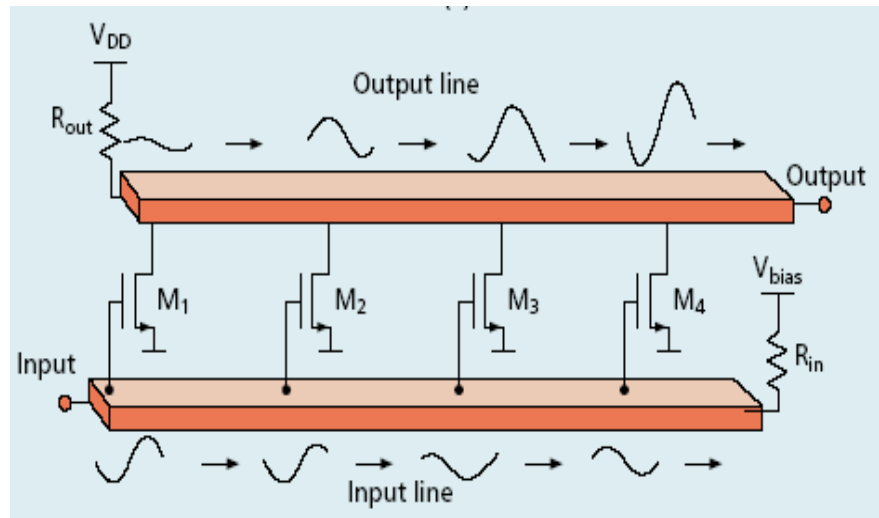
# Prototype PA Performance @ $P_{in}=0dBm$



# Distributed Amplifier (DA)

## - how it works -

- Amplification effect is dominated by the forward wave due to the FET characteristics, where each device adds power in phase at each tap point on the output line.
- The inherent attenuation in both the Gate and Drain lines forces the gain to reach maximum value given an optimum number of HEMTs in the design.



# *Distributed Amplifiers*

## *- benefits & limitations -*

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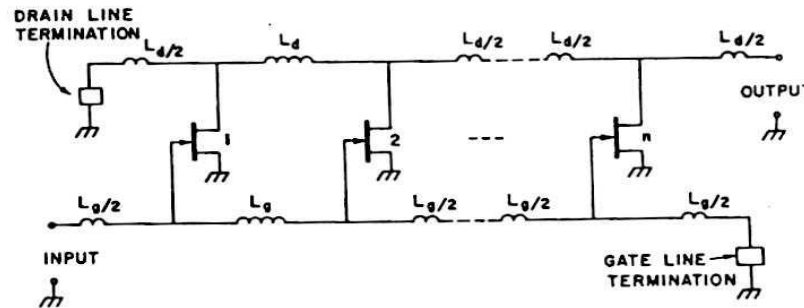


- Eliminates gain and BW trade-offs
- Less sensitive to device & ckt. variations
- Achieves flat frequency response, though the upper limit is dictated by:
  - the FETs  $f_c$  (solution: adopt non-uniform DA design topology)
  - the cutoff of the Gate line (solution: make  $C_{gs}$  smaller)
  - Drain line atten and loading (choose cascode FET approach)

# Conventional DA

## - BW & Power Limits -

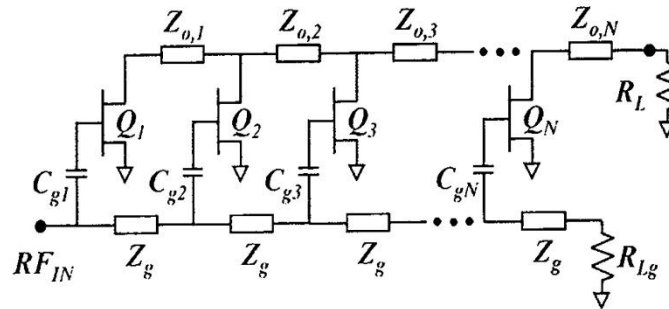
- Schematic (aka Uniform Elements DA):



- Gate and Drain lines are lossy, frequency dependent and loaded, ie both lines have a cutoff freq, and power down the lines is attenuated,
- Output power is also suffering (by 50%) because of the drain line termination,
- The load line for each cell is different due to unmatched capacitances thus power is not maximized in each cell, and not delivered to the output,
- In addition, the power vs frequency is higher or lower from each cell, ie the DA can not achieve a flat output power over the entire BW

# Non-Uniform DA

- Schematic

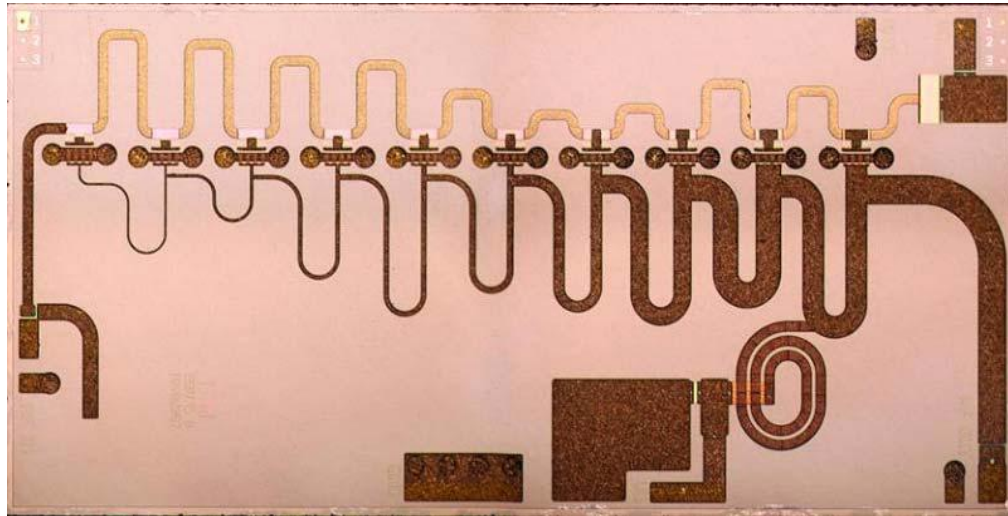


- Increase  $f_c$  by adding capacitors in series w/ each gate
- Taper drain TL from cell to cell for optimum loads.
- Impedance tapering is to force the backward travelling current to zero. In addition, adjust each drain TL length to add the forward currents in phase
- Absorb each FET output capacitance into the TL



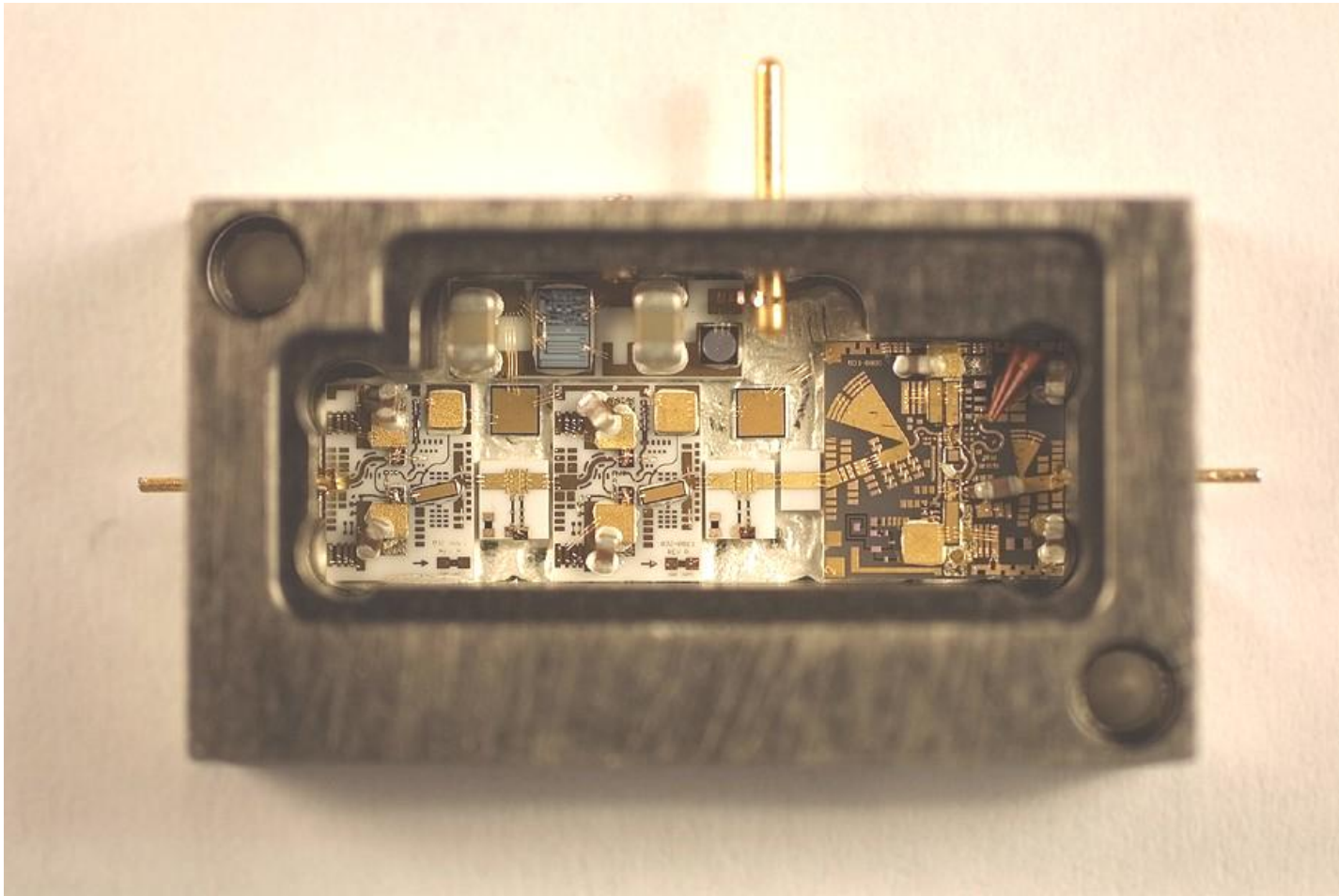
# Non-Uniform MMIC DA - example -

- Triquint TGA2570 : 1.5-17 GHz, 8W output  
GaN MMIC, size: 2.27x5.54x.10 mm



# Uniform 0.05-6 GHz DA

(1.0x0.5x0.16 inches)

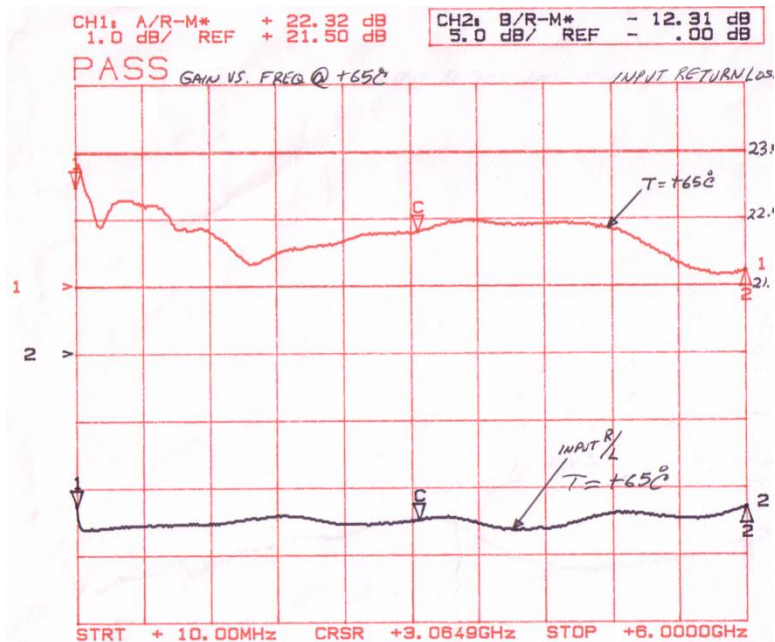


# 0.05-6 GHz DA

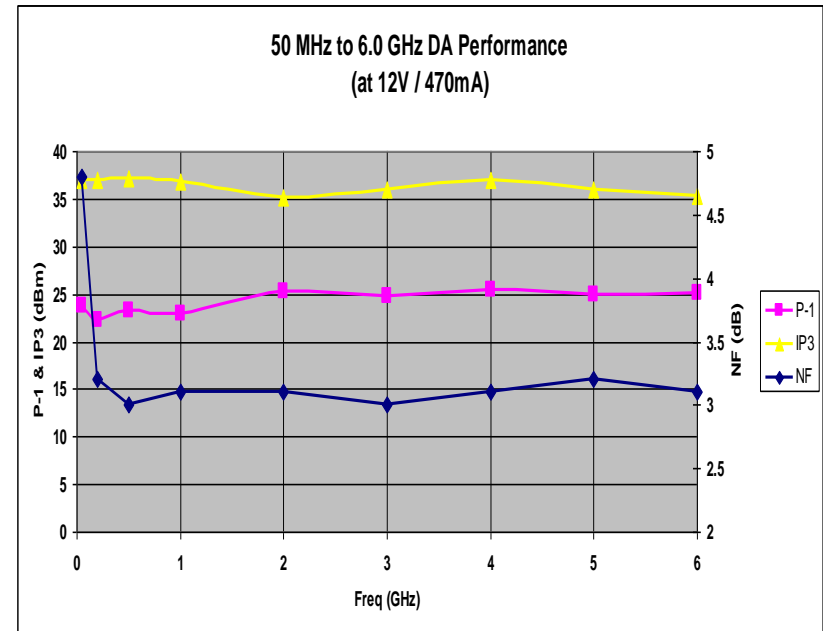
## - RF performance -



- Gain & VSWR



- NF & Power



# Low Phase Noise Amp's

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- Facts and Theory:
    - Phase noise derives from adding white noise to the RF spectrum around the carrier.
    - Amplifier phase noise is of  $1/f$  type, referred to as flicker noise and it takes place at the microscopic scale
    - By definition, phase noise is the power spectral density of the signal phase fluctuations around the fundamental carrier (PM fluctuations)
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# *Low Phase Noise Amp's - design -*

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- Experimentation is crucial
  - No dedicated CAD simulation exists since the models are developed empirically and not fully supported by experiments
  - Accurate measurements are mandatory
  - Phase noise designs require a comprehensive understanding of the active device
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# Measuring techniques

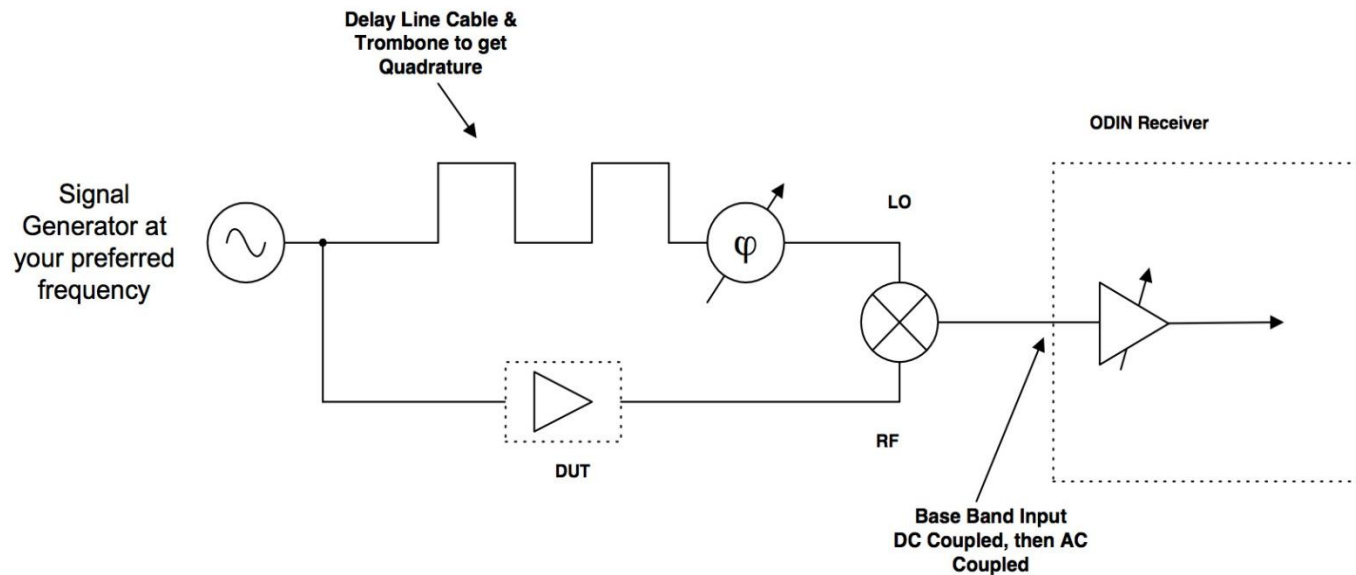
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- Residual Phase Noise single channel Measurements for amplifiers up to -155dBc/Hz at 1kHz (at X-Band)
- Dual channel Cross Correlation Phase Noise method for amplifiers with a phase noise expectation beyond the above number

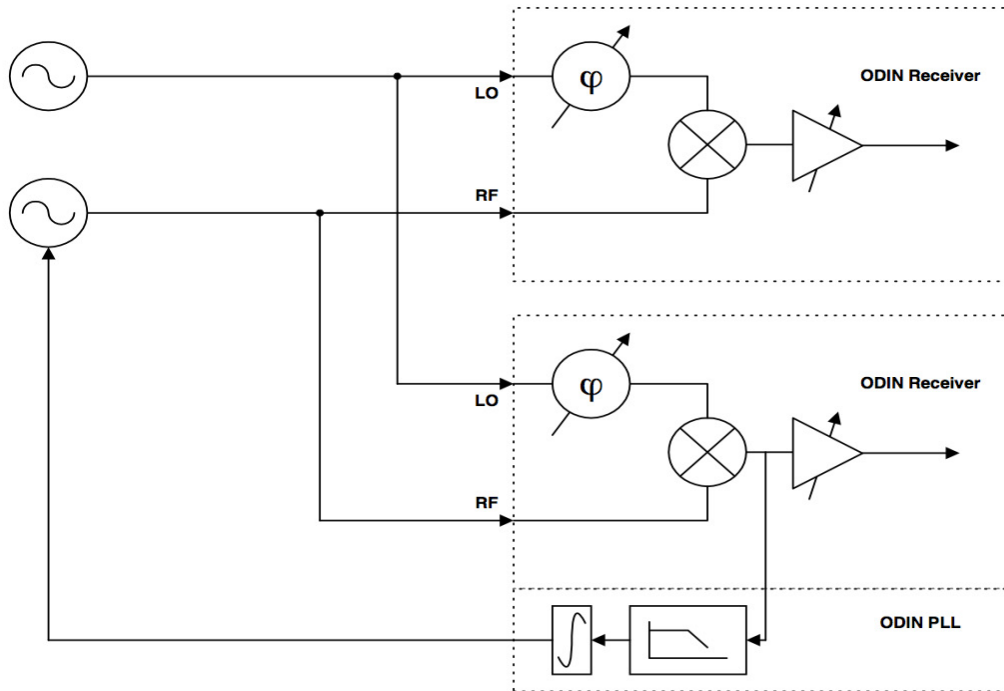
# Single channel set-up

- Using one ODIN Rcvr form PSI



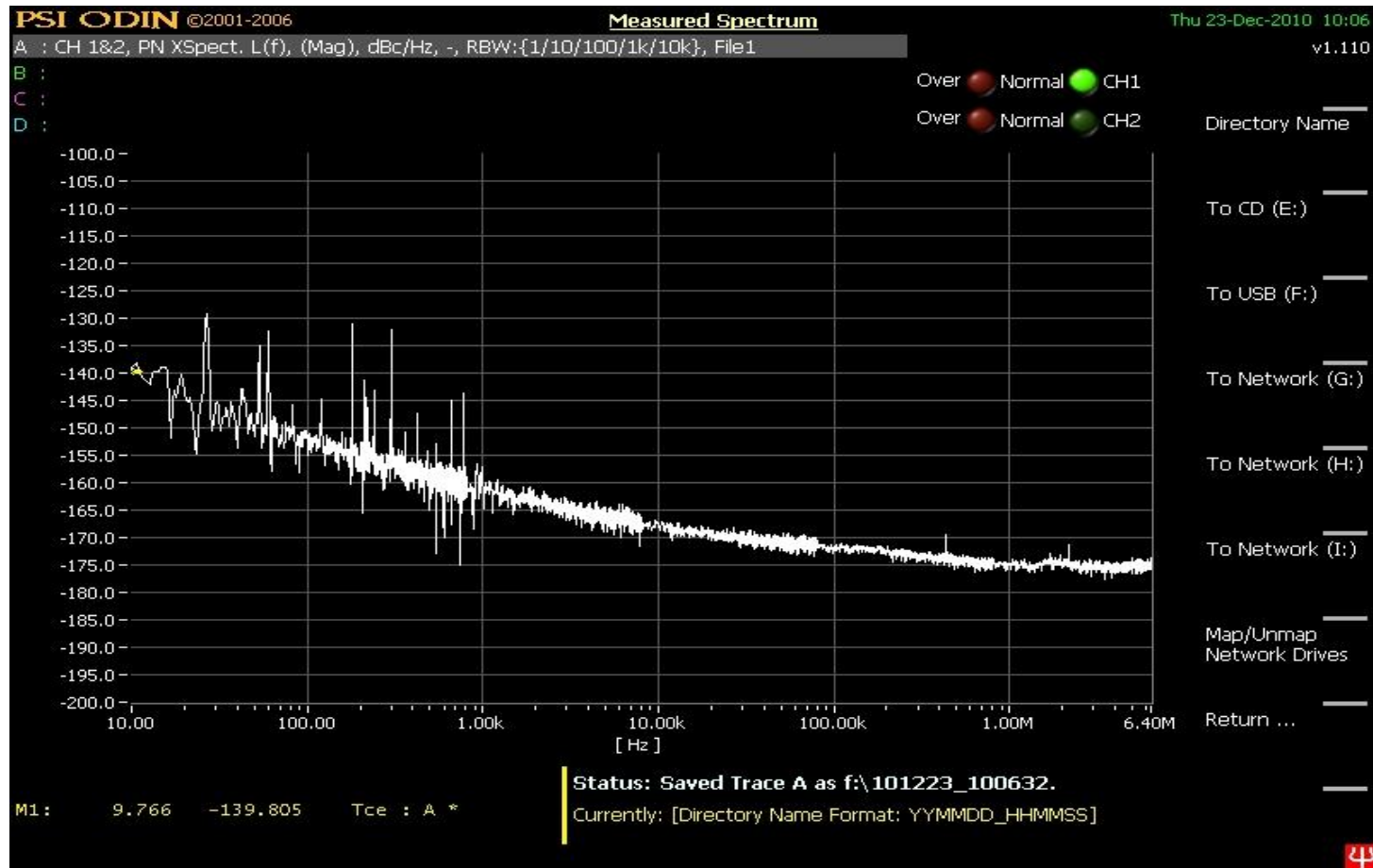
# Dual channel set-up

- Using two ODIN Rcvrs from PSI





# X-Band: 163 dBc/Hz at 1 kHz

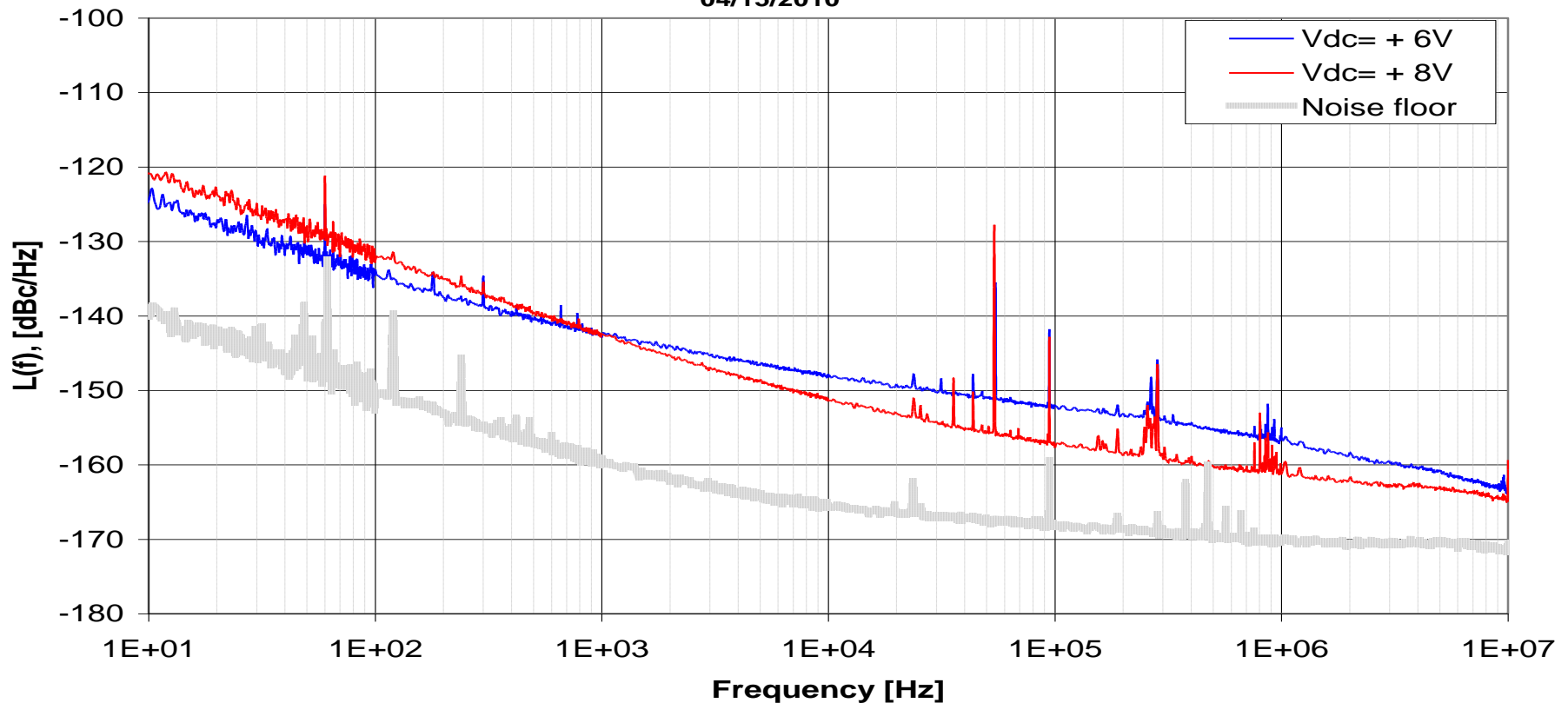


# 40GHz: 142 dBc/Hz at 1kHz

PM noise of a **PAIR** of AML amplifiers (Model No.- 4040PNB1511) at 40 GHz

Pin= +6 dBm

04/15/2010



# *AML Reference Data*



- Practiced all designs and
- Maintains reference data on 2400 amplifiers at

[www.amlj.com](http://www.amlj.com)