

# Welcome

## DPD for Everyone and by Everyone

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Sr. Member IEEE

# Agenda

## About Digital Pre-Distortion (DPD)

DPD challenges for 4G/wideband systems

Design a PA that is more linearizable

Understand the limits of the DPD algorithm

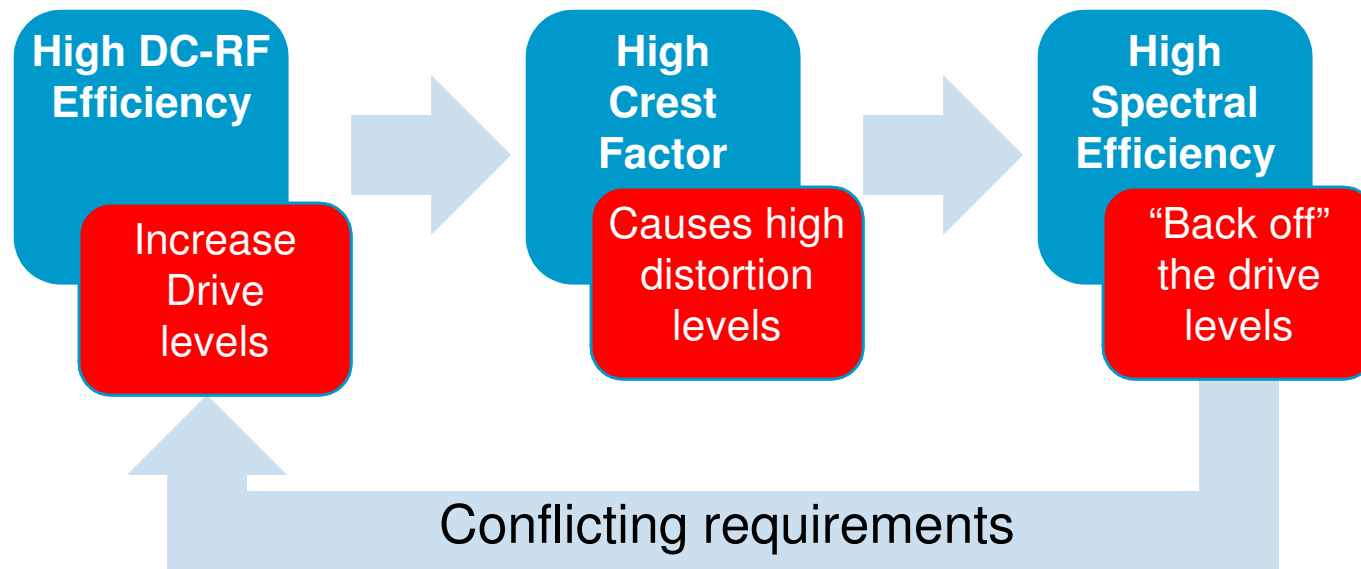
Practical implementation

Some Results

Q&A

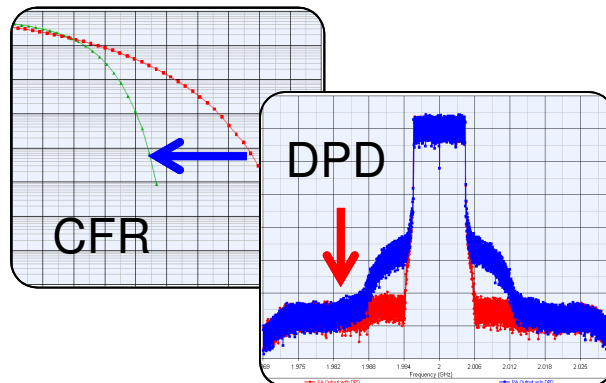
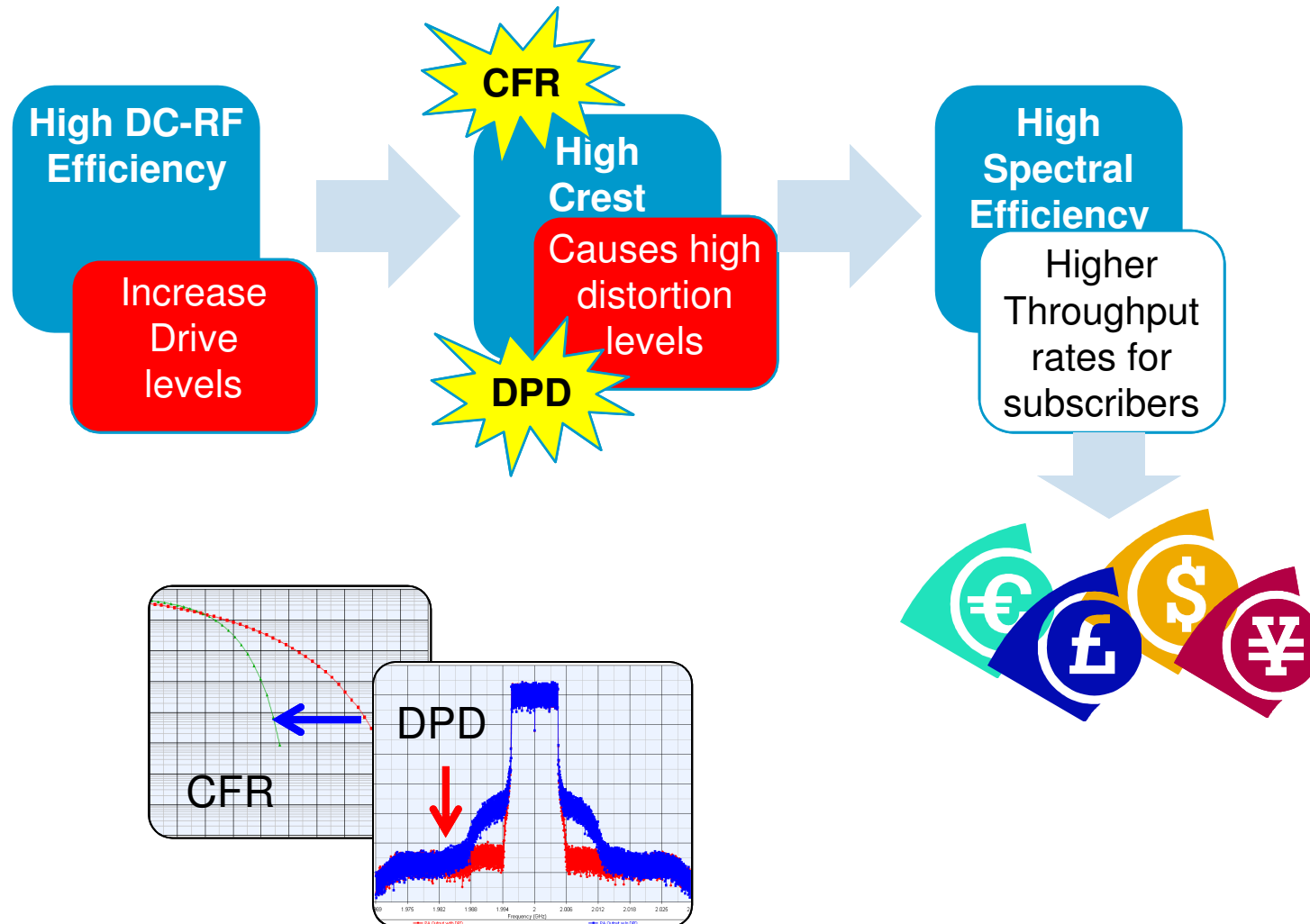


# Problem Statement

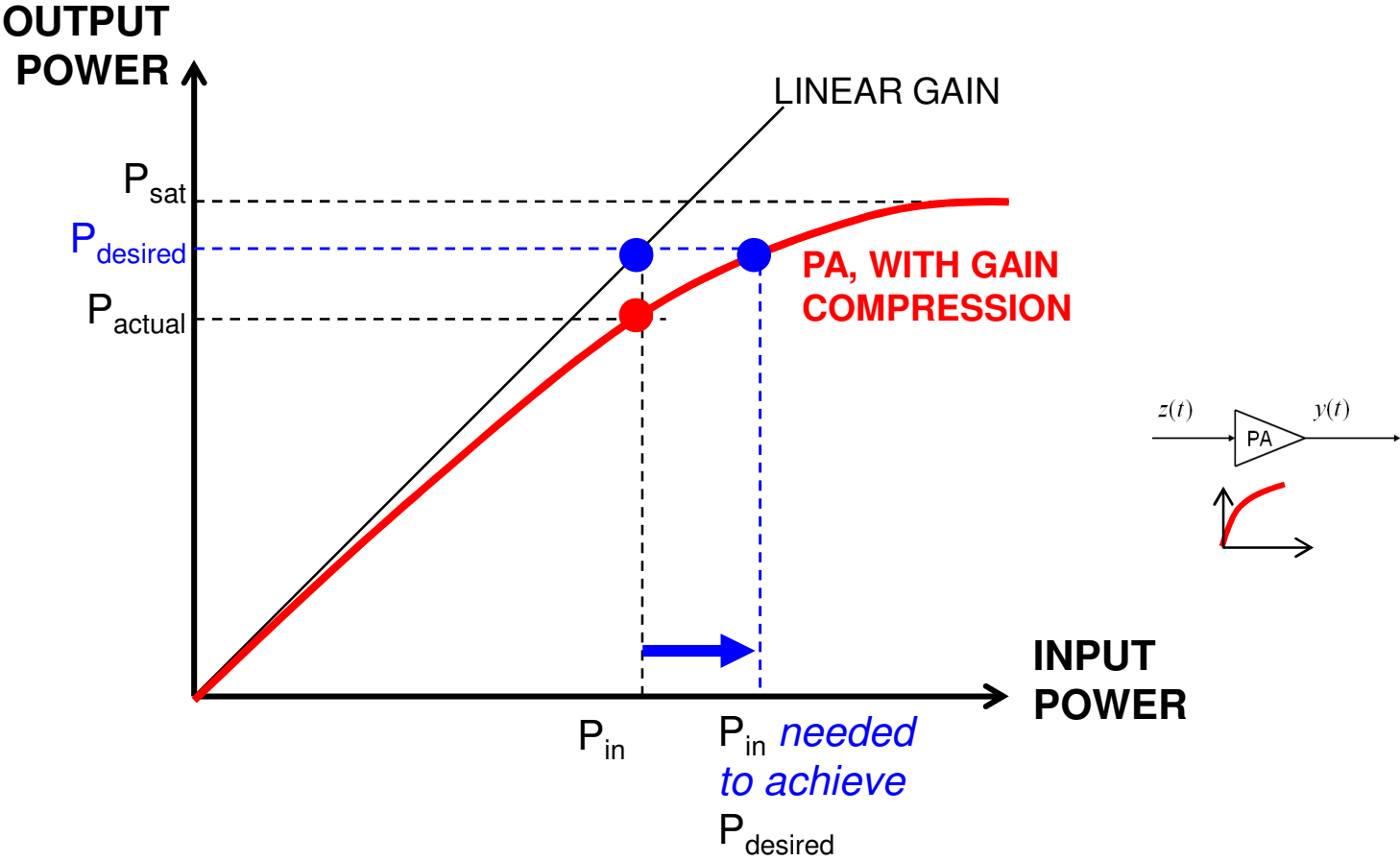


How to handle signals with high Crest Factor, while driving the PA to operate with high PAE, while also having low signal distortion?

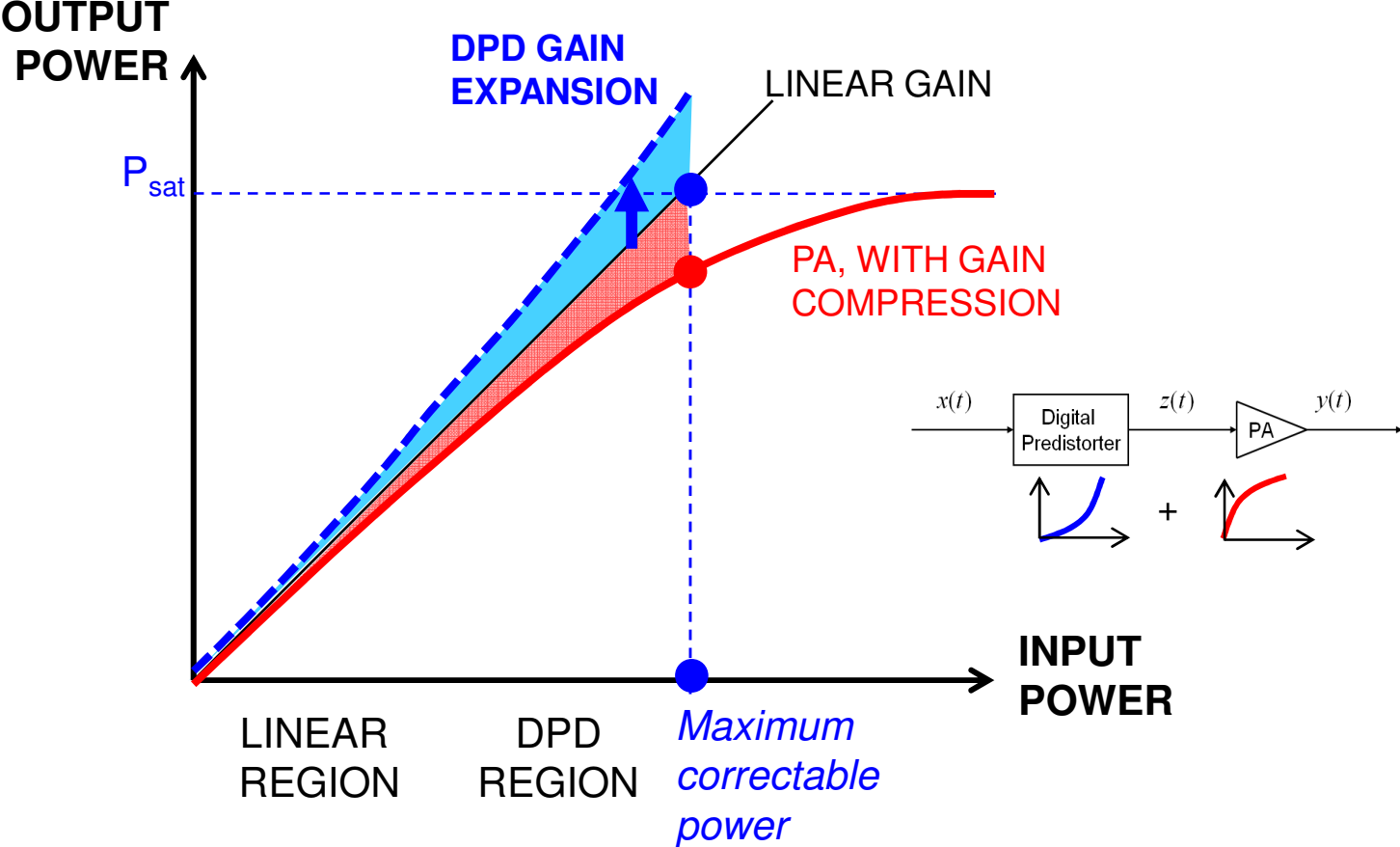
# Solution Approach



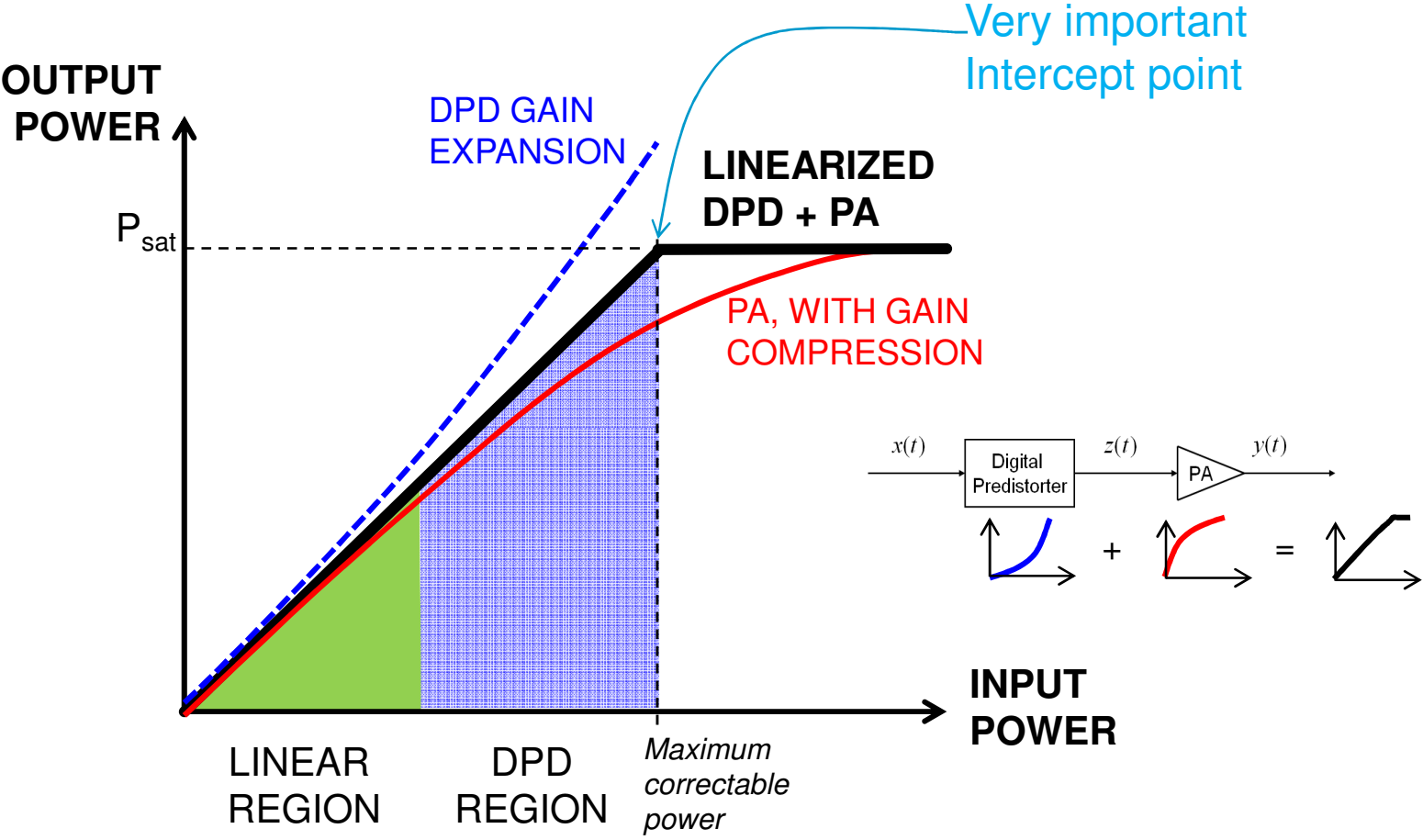
# Digital Pre-distortion Principles – Compressing PA



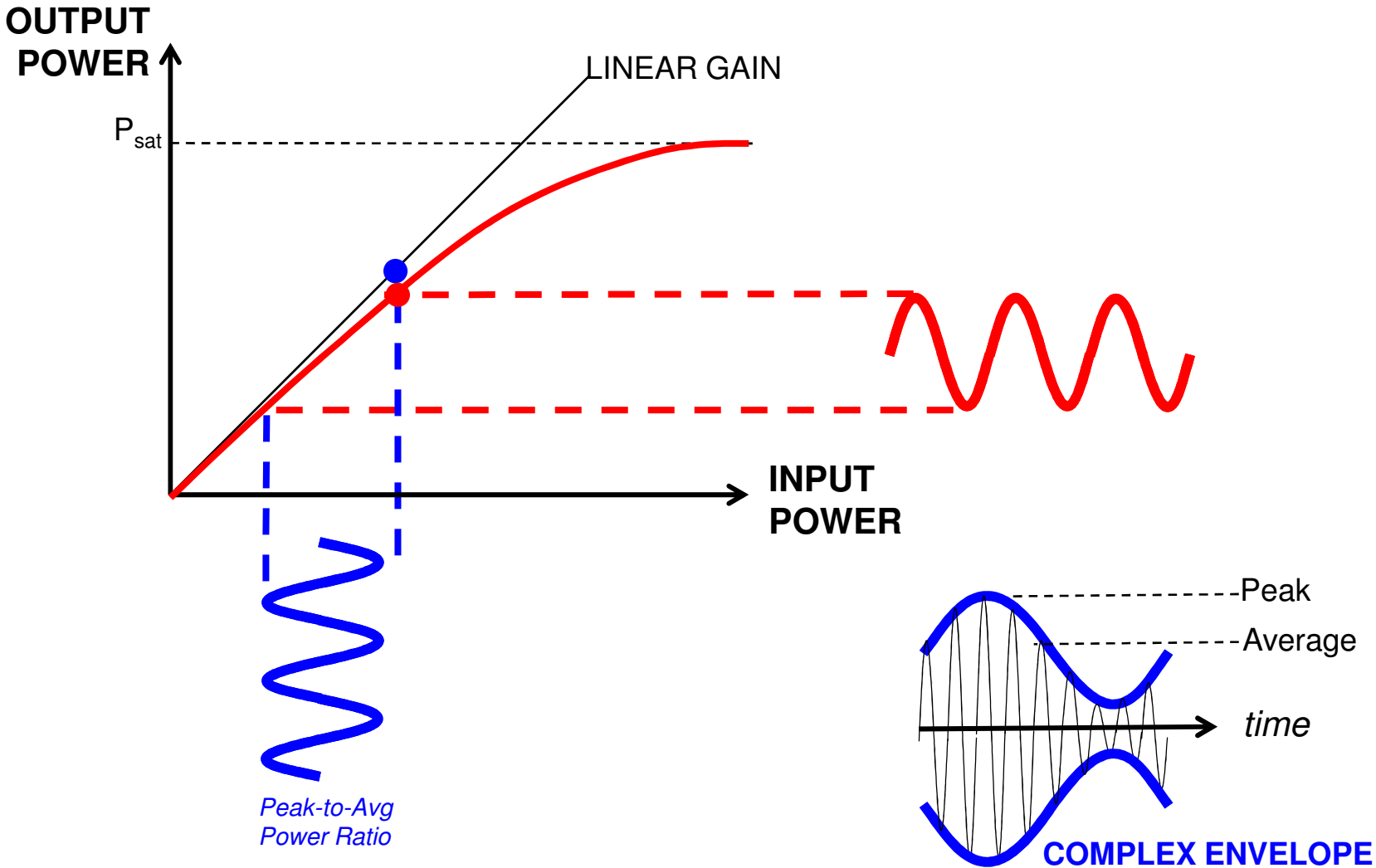
# Digital Pre-distortion Principles – Pre-expansion



# Digital Pre-distortion Principles – Linearized Result

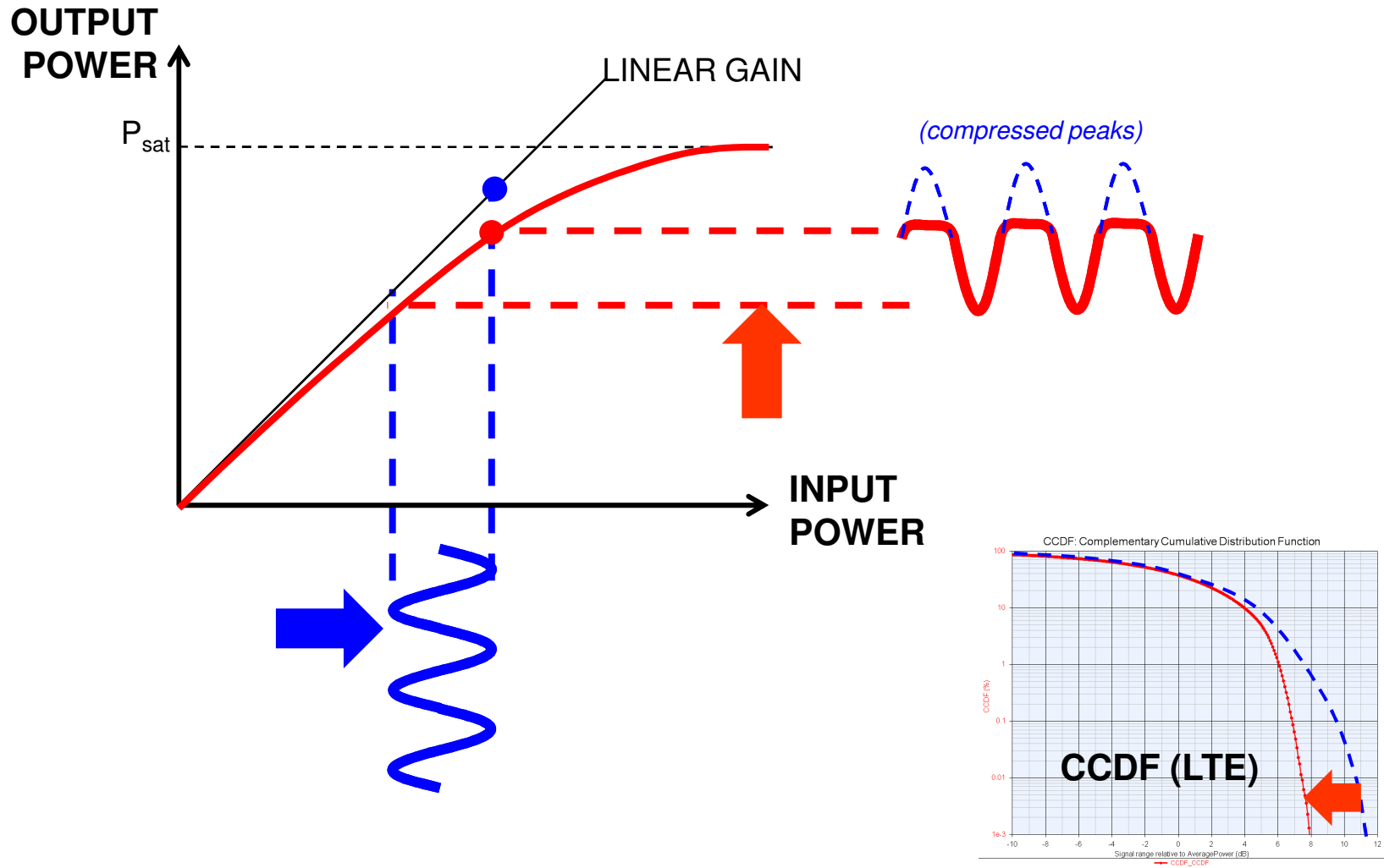


# Linear Operation with Time-varying Envelope

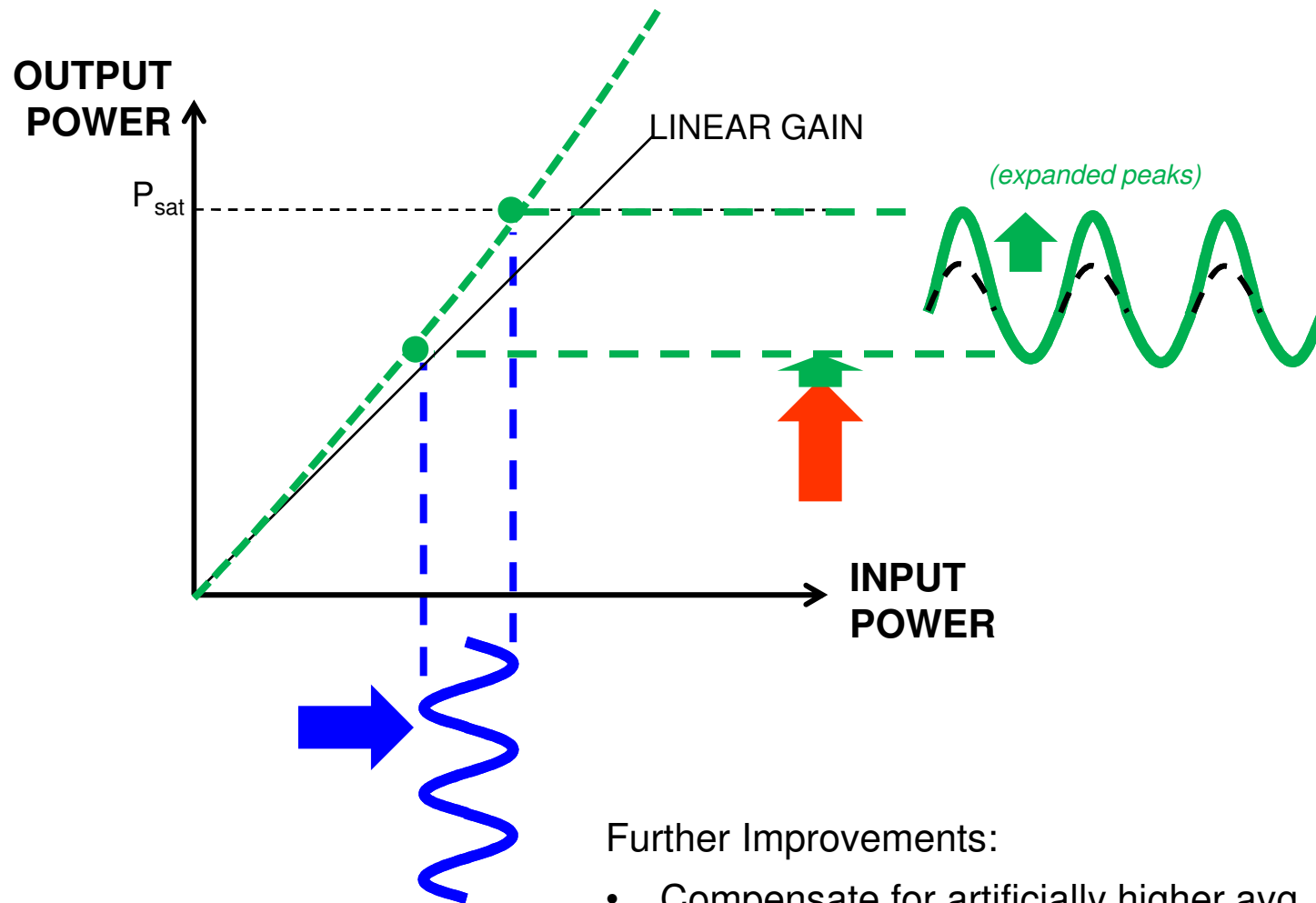




# Nonlinear Operation – Peaks are Compressed



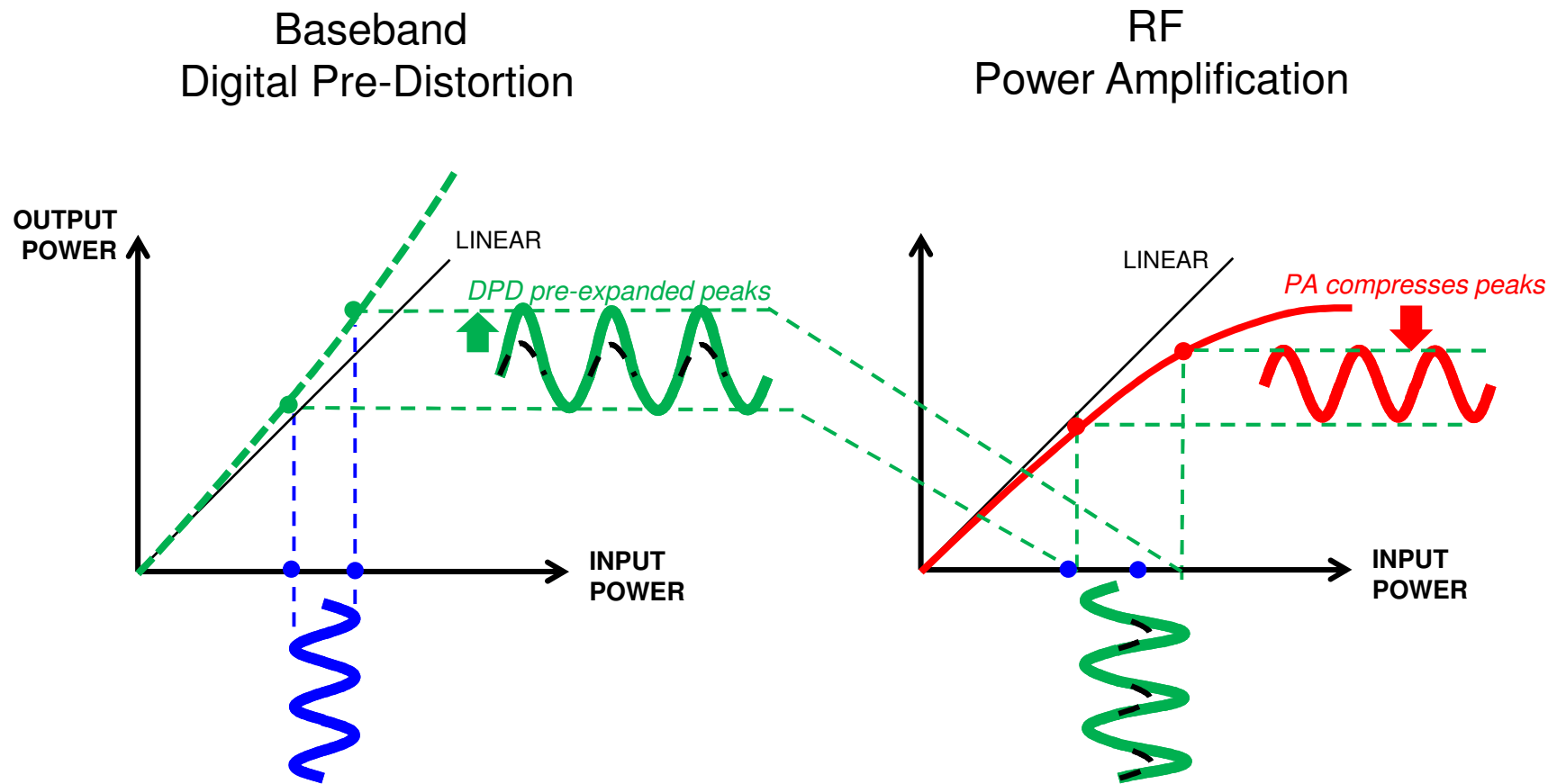
# DPD Pre-Expansion – Peaks are Exaggerated



Further Improvements:

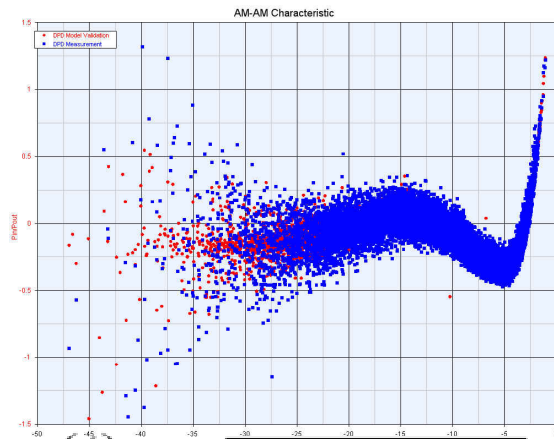
- Compensate for artificially higher avg. signal power
- Condition signal w/Crest Factor Reduction (CFR)

# DPD Net Result: *Linear Gain of Complex-valued RF Carrier Envelope Over a Specific Range of Power Levels*

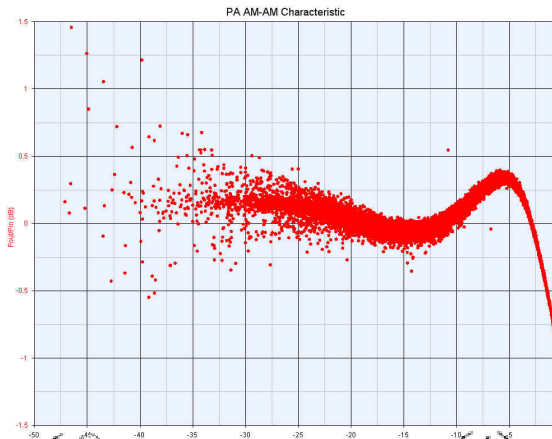


# AM-AM Effects (Change in Gain vs. Power level)

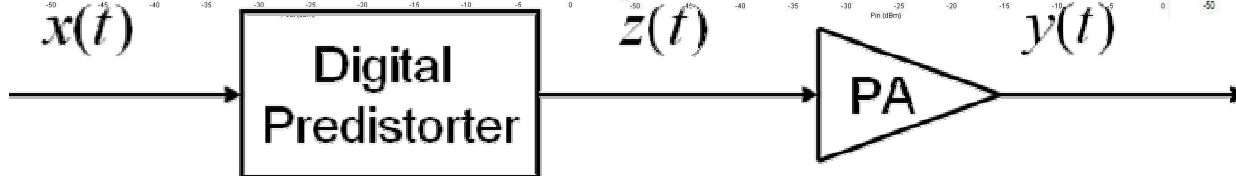
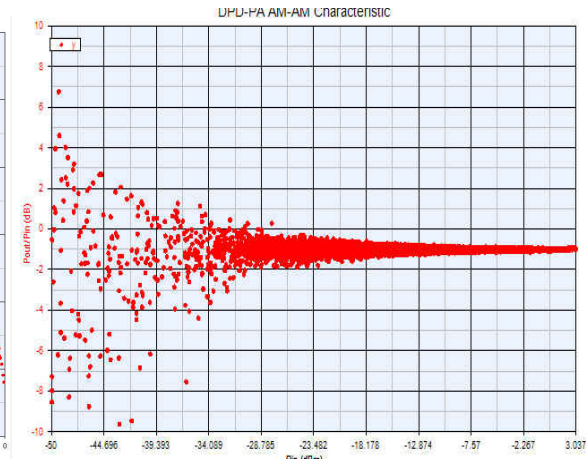
Pre-Distorter  
AM-to-AM



Power Amp  
AM-to-AM



DPD + PA  
AM-to-AM



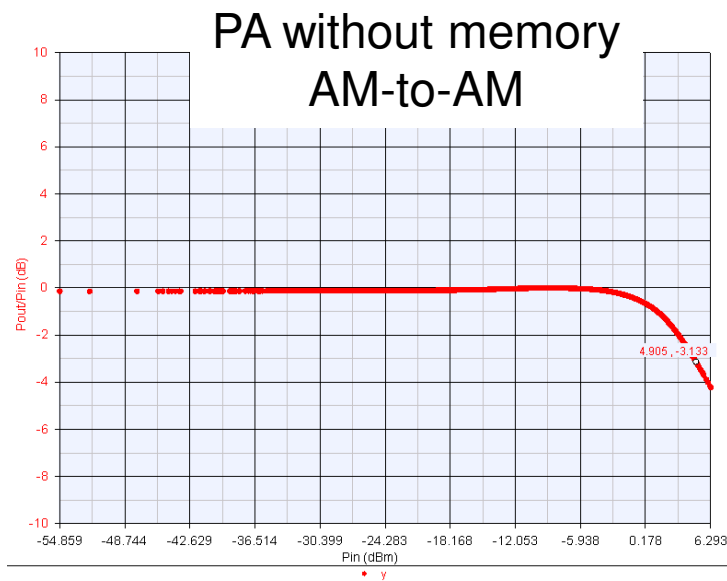
Linearized  
PA

## Definitions

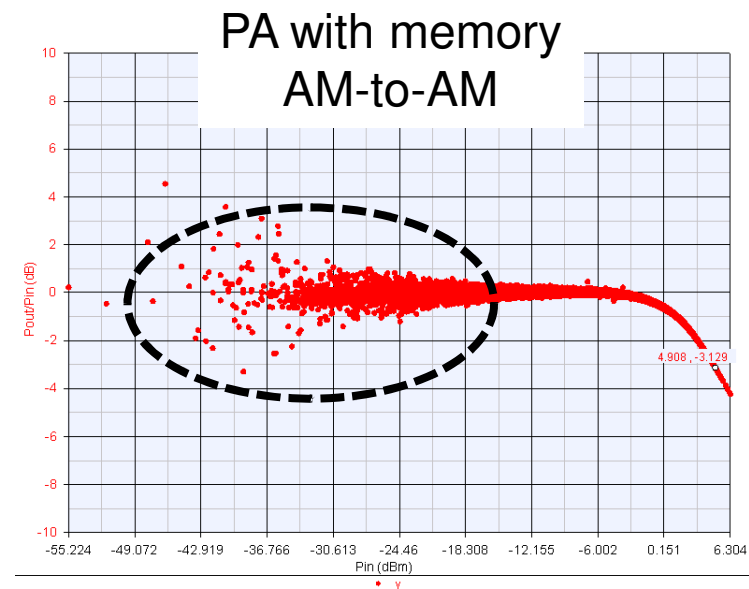
- **AM-AM** : Change in Gain vs. Power level, compared to small-signal ( $dB(S21)$ )
- **AM-PM** : Change in Transmission Phase, compared to small-signal ( $phase(S21)$ )
- **CCDF**: Percentage of time a particular amplitude level spends above avg power

# Additional issues: Memory Effects

*Output is Dependent on Previous History: "Path Dependence"*



Output waveform has an instantaneous 1:1 correspondence in time with input waveform



Output waveform depends on previous values

# What Does a DPD Look Like? (Volterra Model)

Volterra series pre-distorter can be described by

$$z(n) = \sum_{k=1}^K z_k(n) \quad \text{where} \quad z_k(n) = \sum_{m_1=0}^Q \cdots \sum_{m_k=0}^Q h_k(m_1, \dots, m_k) \prod_{l=1}^k y(n - m_l)$$

which is a 2-dimensional summation of power series & past time envelope responses

$$z(n) = h_0 + \sum_{m_1=0}^Q h_1(m_1) y(n - m_1) + \sum_{m_1=0}^Q \sum_{m_2=0}^Q h_2(m_1, m_2) y(n - m_1) y(n - m_2) + \dots$$

A memory polynomial pre-distorter uses the diagonal kernels of the Volterra series and can be viewed as a generalization of the Hammerstein pre-distorter. It is constructed using the indirect learning architecture, thereby eliminating the need for a model assumption and parameter estimation of the power amplifier. Compared to the Hammerstein pre-distorter, the memory polynomial predistorter has slightly more terms, but it is much more robust and its parameters can be easily estimated using a least-squares algorithm.

A full Volterra produces a huge computational load. People usually simplify it into:

- Wiener model
- Hammerstein model
- Wiener-Hammerstein model
- **Memory polynomial model**



# Memory Polynomial Model

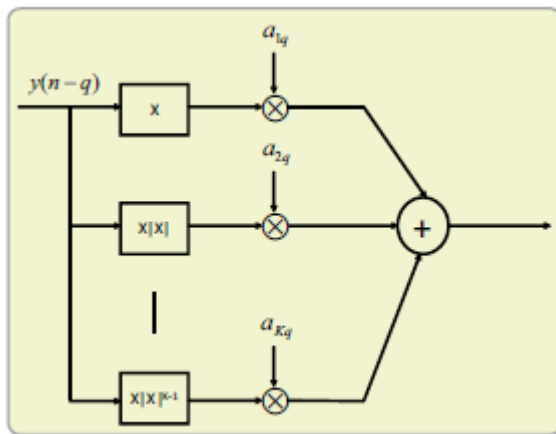
If only diagonal terms are kept in Volterra model, Volterra model becomes memory polynomial model.

$$z(n) = \sum_{k=1}^K \sum_{q=0}^Q a_{kq} y(n-q) |y(n-q)|^{k-1} \quad \text{--- 4}$$

, where,  $K$  is Nonlinearity order and  $Q$  is Memory length

If  $Q=0$ , the structure in the equation degenerates to a memoryless polynomial. Since the model in equation 4 is linear with respect to its coefficients, the predistorter coefficients  $a_{kq}$  can be directly obtained using a least-squares algorithm by defining a new sequence:

$$u_{kq}(n) = \frac{y(n-q)}{G} \left| \frac{y(n-q)}{G} \right|^{k-1}$$



At convergence, we should have

$$z = Ua$$

where

$$z = [z(0), z(1), \dots, z(N-1)]^T$$

$$U = [u_{10}, \dots, u_{K0}, \dots, u_{1Q}, \dots, u_{KQ}],$$

$$u_{kq} = [u_{kq}(0), u_{kq}(1), \dots, u_{kq}(N-1)]^T,$$

$$a = [a_{10}, \dots, a_{K0}, \dots, a_{1Q}, \dots, a_{KQ}]^T.$$

The least-squares solution for (6) is

$$\hat{a} = (U^H U)^{-1} U^H z$$

where  $(U)^H$  denotes the complex conjugate transpose matrix.

L. Ding, G. T. Zhou, D. R. Morgan, Z. Ma, J. S. Kenney, J. Kim, and C. R. Giardina, "Memory polynomial predistorter based on the indirect learning architecture," in *Proc. of GLOBECOM*, Taipei, Taiwan, 2002, vol. 1, pp. 967-971.

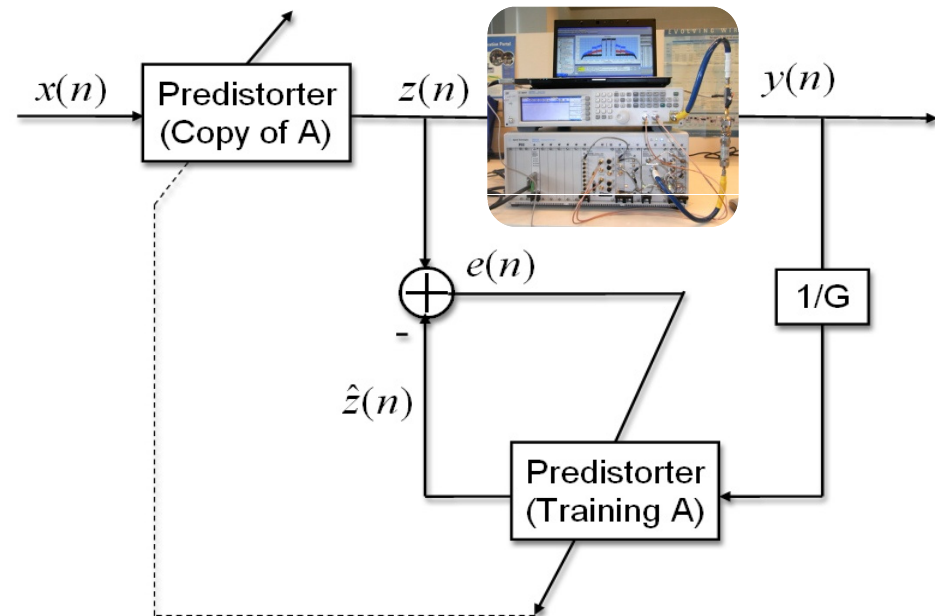
# DPD Principles – Memory Polynomial Model

How is it done in practice?

$$z(n) = \sum_{k=1}^K \sum_{q=0}^Q a_{kq} y(n-q) |y(n-q)|^{k-1}$$

Where

- $K$  is Nonlinearity order
- $Q$  is Memory length





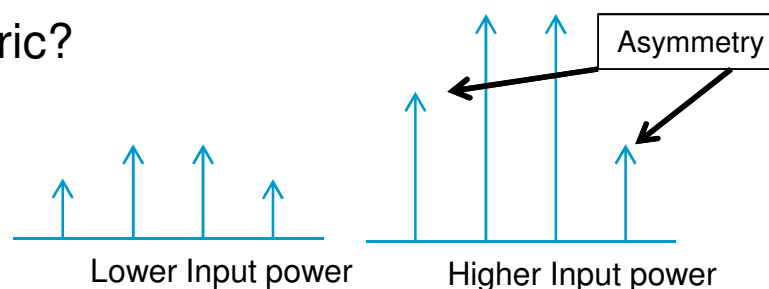
# DPD Principles – Memory Polynomial Model

How do we select K (nonlinear order) and Q (memory length)?

- K is perhaps more tangible. When do you say “this amplifier is pretty nonlinear?”
- Q There are no golden rules yet. Mostly set up by experience.

What is memory? Is there a metric?

Asymmetry in intermod products  
Indicates memory.



“the unlinearized IMD total power normalized to the IMD power obtained after optimum static linearization”<sup>1</sup>  
Is some times used as a metric for memory.

<sup>1</sup> João Paulo Martins et.al. IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, VOL. 54, NO. 12, DECEMBER 2006

# Agenda

## About Digital Pre-Distortion (DPD)

DPD challenges for 4G/wideband systems

Design a PA that is more linearizable

Understand the limits of the DPD algorithm

Practical implementation

Some Results

Q&A

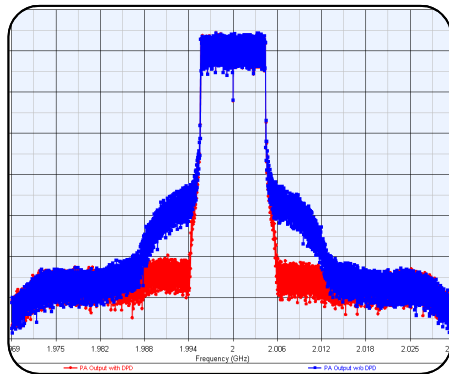


# DPD Challenges for 4G/Wideband Systems

Wider Bandwidth

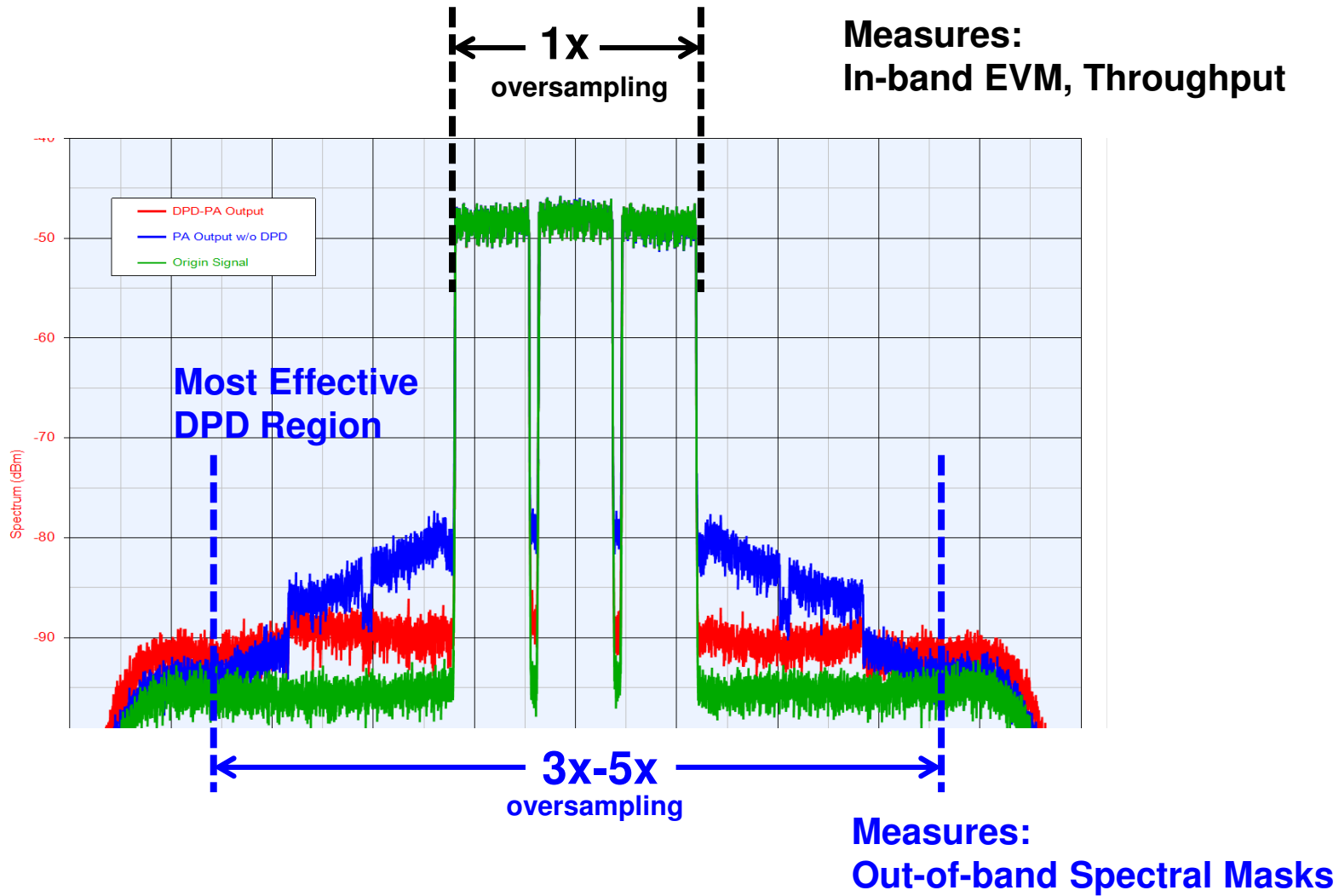
Higher Crest Factor

Rapidly changing environment



- LTE-Advanced (100MHz) and 802.11ac (160MHz) are physically 5x-8x wider than previous generation
- Oversampling increases this bandwidth an additional 3x-5x
- Drives wider ADC/DAC, data rates, test equipment, & more
- Requires powerful embedded processors : DSP/FPGA/ASIC

# Oversampling Increases the Measurement BW

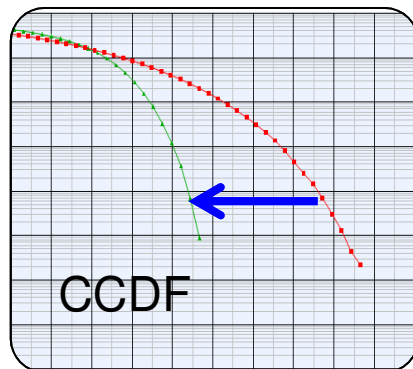


# DPD Challenges for 4G/Wideband Systems

Wider Bandwidth

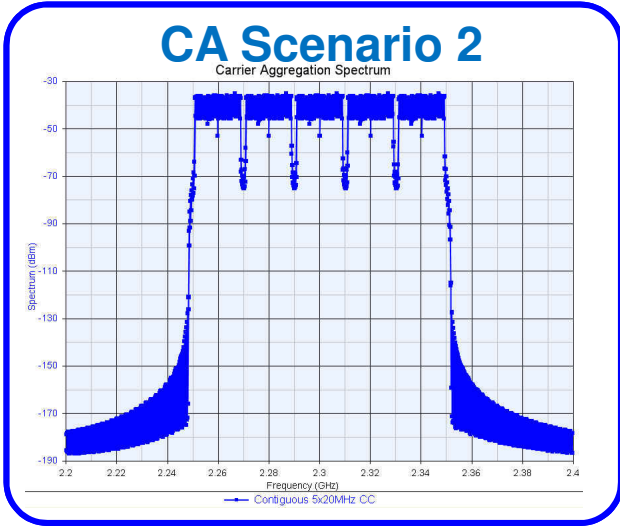
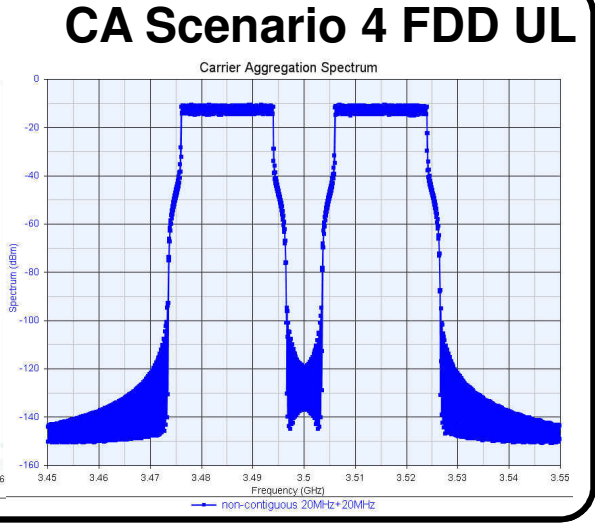
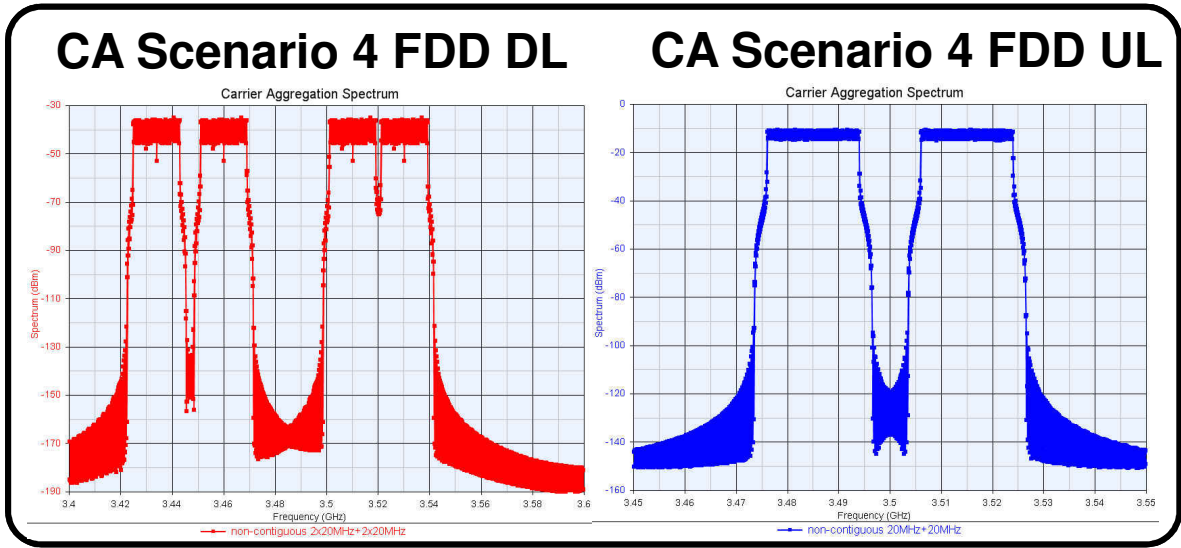
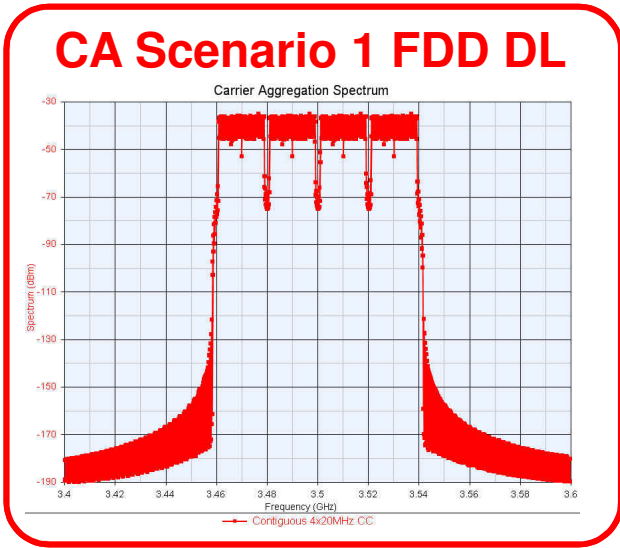
Higher Crest Factor

Rapidly changing environment



- Carrier aggregation increases PAPR (drives Efficiency down)
- Need to have compatibility with 3G signals.
- Highly-configurable signals (time-varying RBs) can lead to worst-case RF scenarios
- People apply Crest Factor Reduction differently....  
....how to estimate the effect of CFR on your PA if *someone else* is doing the DSP?

# The Effect of Carrier Aggregation on PAPR



Carrier Agg. Scenario	Link Type	Configuration	PAPR of single CC, before aggregation	PAPR with CCs, after aggregation
Scenario 1	FDD DL	4x20 MHz CCs	8.45 dB	9.98 dB
Scenario 2	TDD DL	5x20 MHz CCs	9.17 dB	11.71 dB
Scenario 4	FDD DL	2x20+2x20MHz	8.38 dB	9.58 dB
	FDD UL	20 + 20MHz	5.79 dB	6.86 dB

# DPD Challenges for 4G/Wideband Systems

Wider Bandwidth

Higher Crest Factor

Rapidly changing environment

- LTE-Advanced, 802.11ac, and other Standards still changing
- IP issues: interoperability of signals, algorithms, channels, coded performance
- Closed DPD IP (no control)
- Availability of commercial DPD solutions
- Ecosystem & vendor re-alignments
- BB/RF hardware platform neutrality for local spectral variations, vendors, standards



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# PA Linearizability

- “I have a PA, but I do not know how linearizable it is.”
- “I can not give an accurate model of my PA”
  - That captures non-linearity
  - Memory effects, short term and long term
  - Frequency response and
  - Noise
- “How do I exercise my degrees of freedom of my design?”
- “What technology/techniques are there for good PA modeling?”

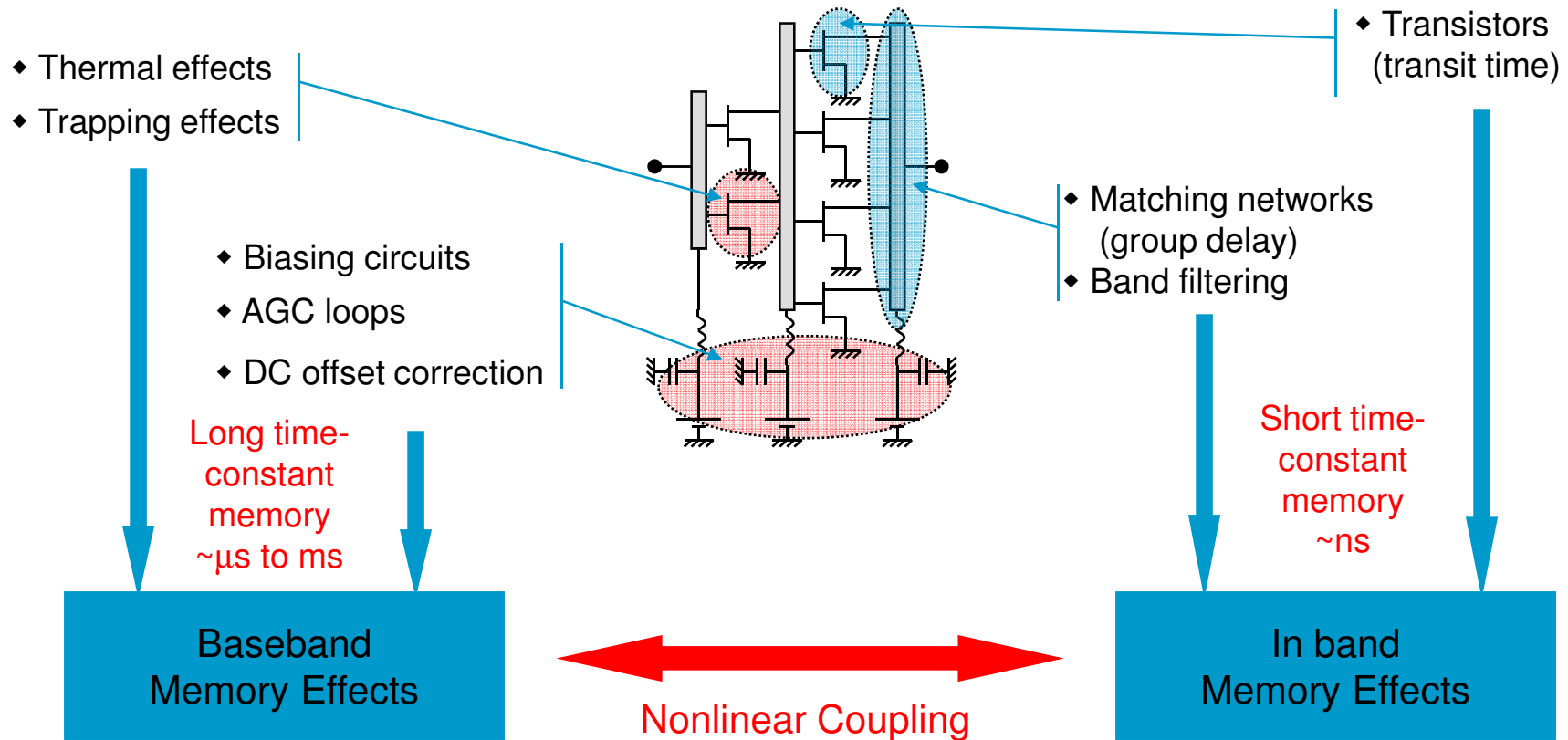
Let us review:

1. Memory effects and
2. PA modeling



# Manifestations of Memory Effects in Circuits

*Some examples*



# PA Linearizability

- PA modeling involves creating behavioral models:

Power-dependent S-parameters	Parallel Hammerstein
X-parameters current	Volterra
Static Polynomial	Radial Basis-function neural Network
Hammerstein	

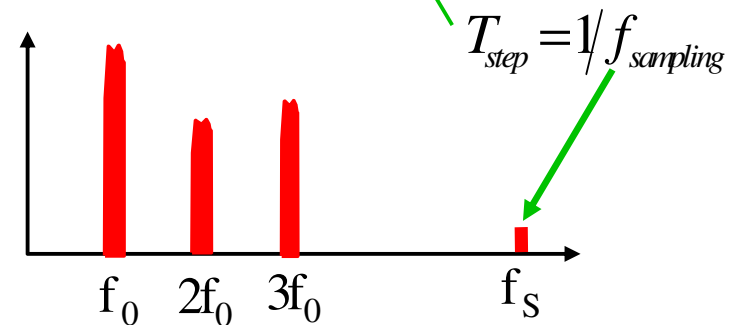
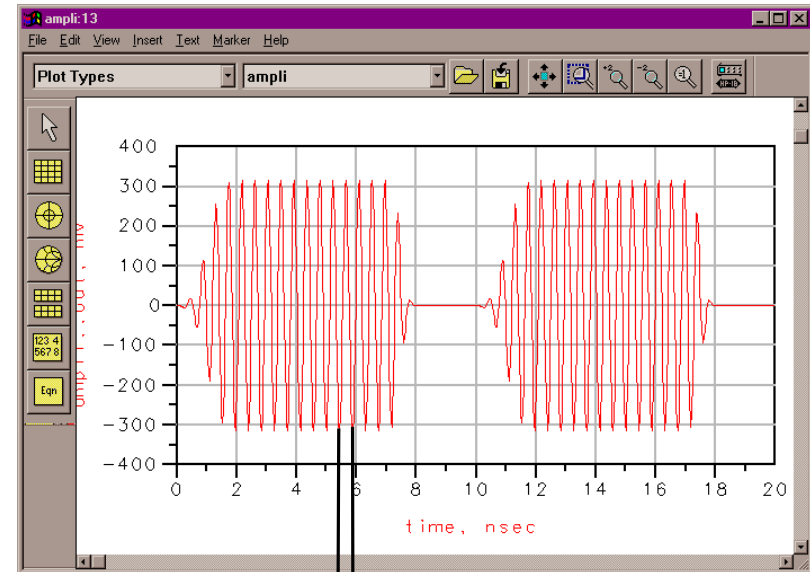
- All the above have either limitations or work for certain signals or too complex.

- Best two alternatives:

- Fast Circuit Envelope (FCE) model -- limited to RFIC world (and not covered in this presentation).
- Direct co-simulation – avoid intermediate modeling altogether!

# Time Domain Simulation

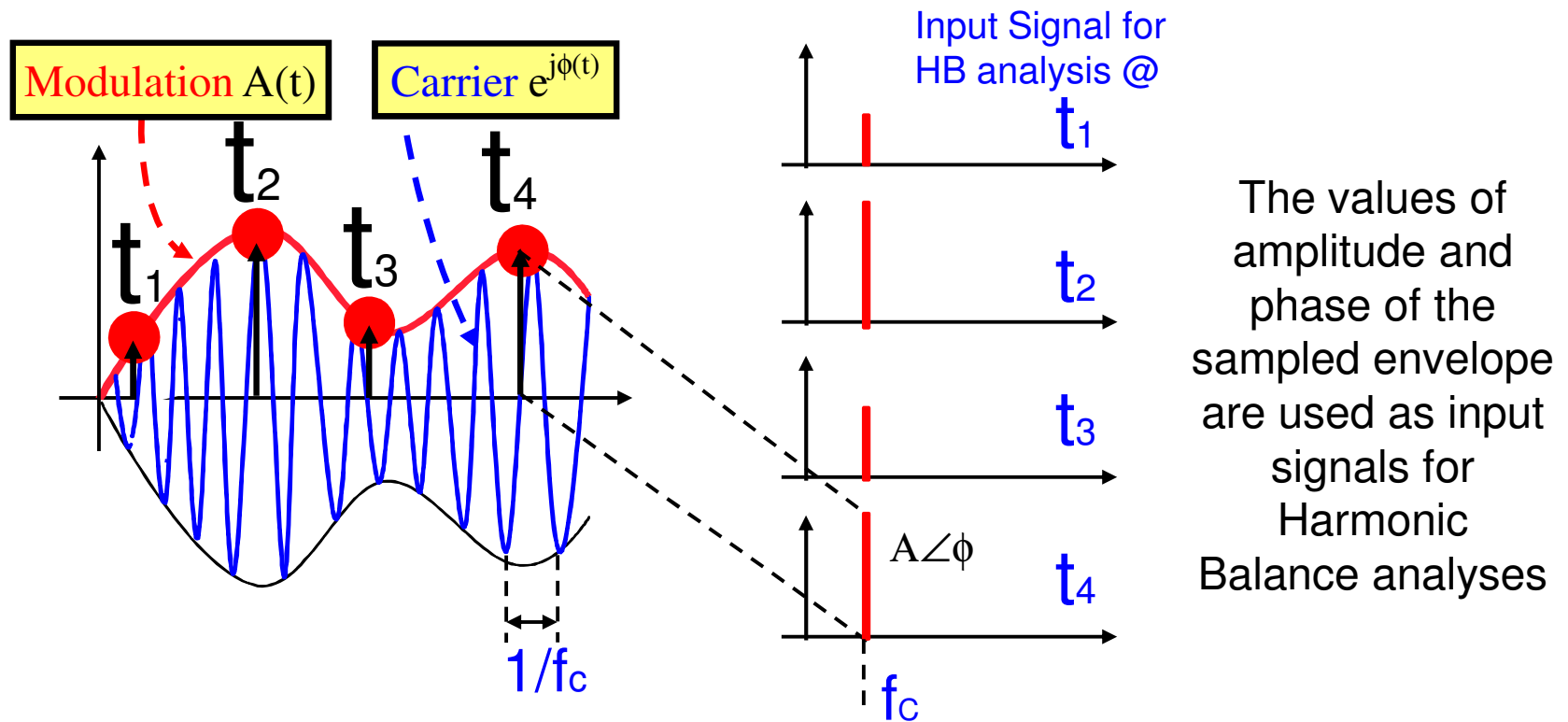
- Must sample the carrier frequency over at least one period of the modulation signal
  - Very small time steps
  - Long simulation time
  - Don't know if settled
- To display spectrum must compute FFT of large number of sample points
  - Long computation
- No frequency-domain models (microstrip, S-parameters, etc.)



# Circuit Envelope Technique

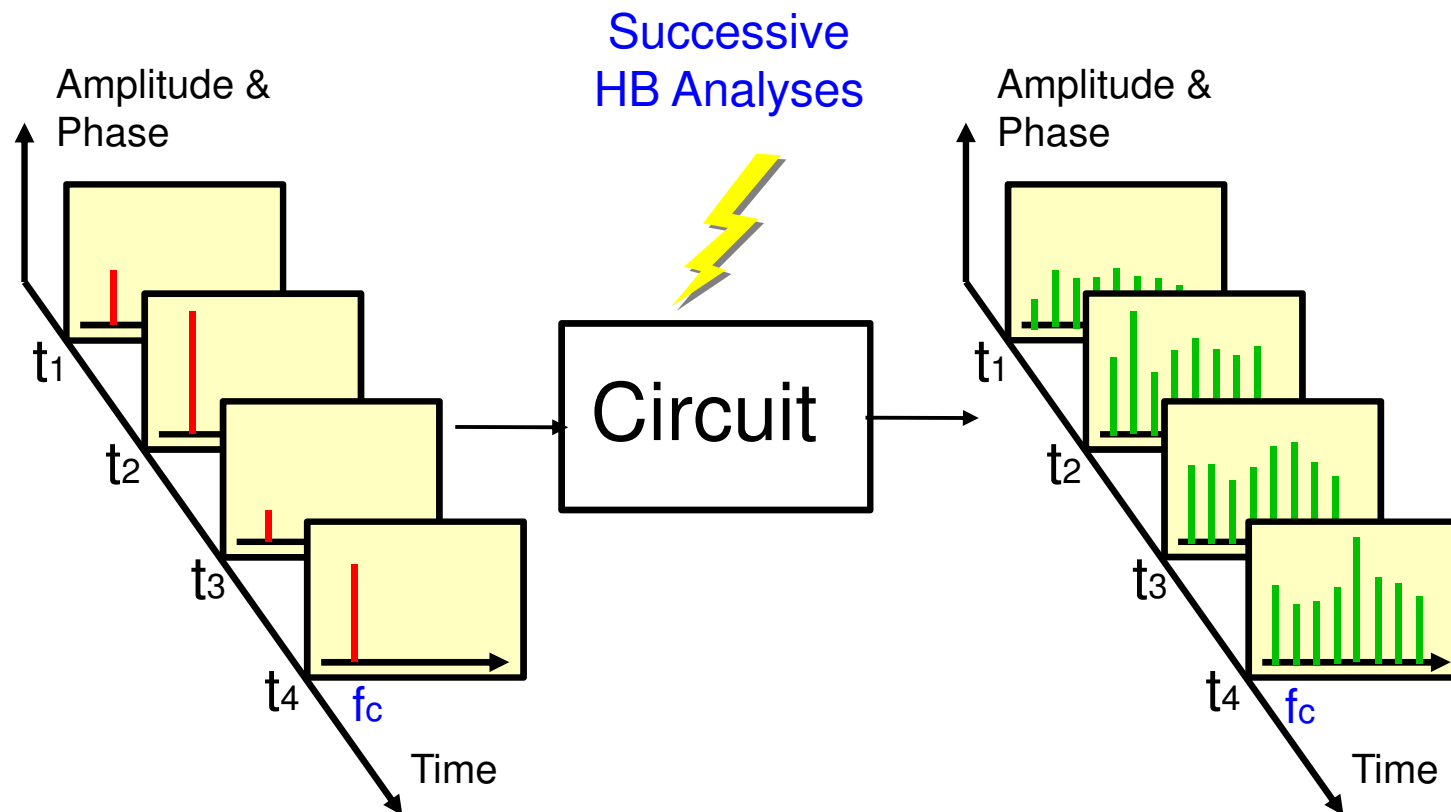
## Step 1 - Transform input signal

Each modulated signal can be represented as a carrier modulated by an envelope -  $A(t) \cdot e^{j\phi(t)}$



# Circuit Envelope Technique

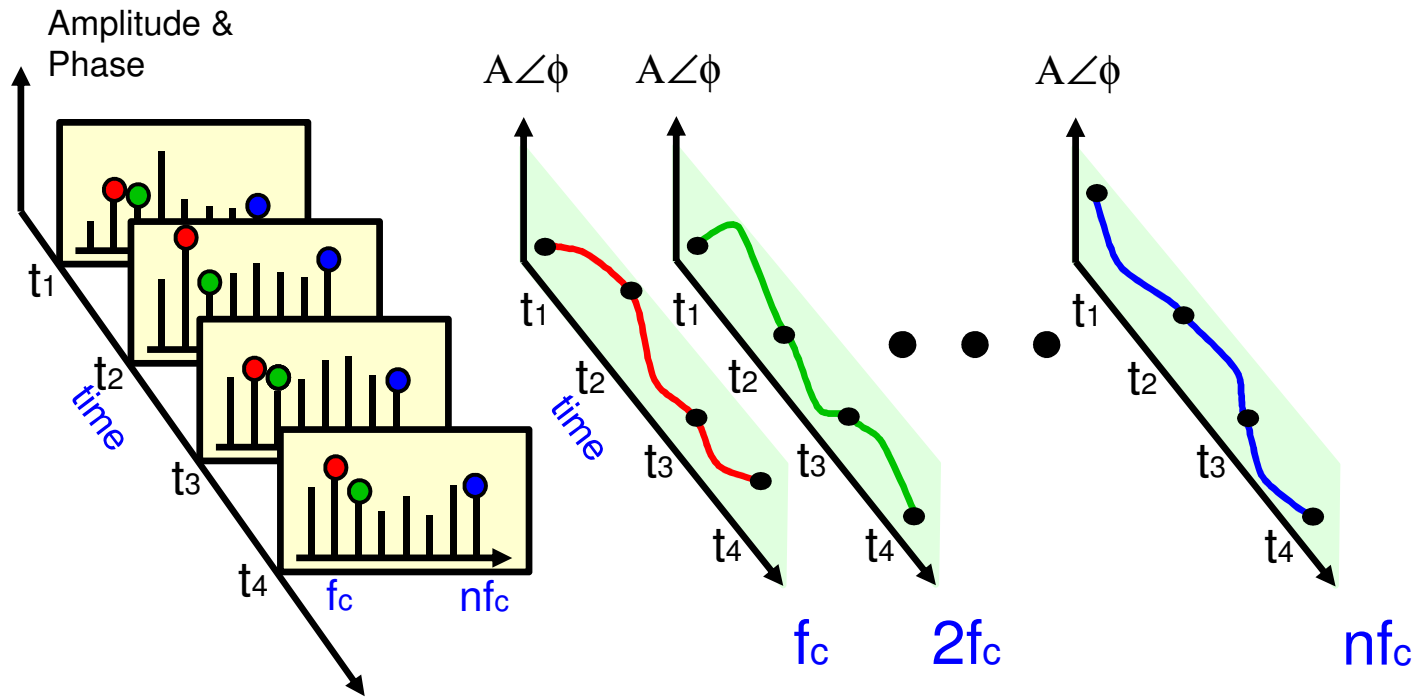
## Step 2 - Frequency Domain Analysis



An Harmonic Balance analysis is performed at each time step. This process creates a succession of spectra that characterize the response of the circuit at the different time steps.

# Circuit Envelope Technique

## Step 3 - Time domain Analysis

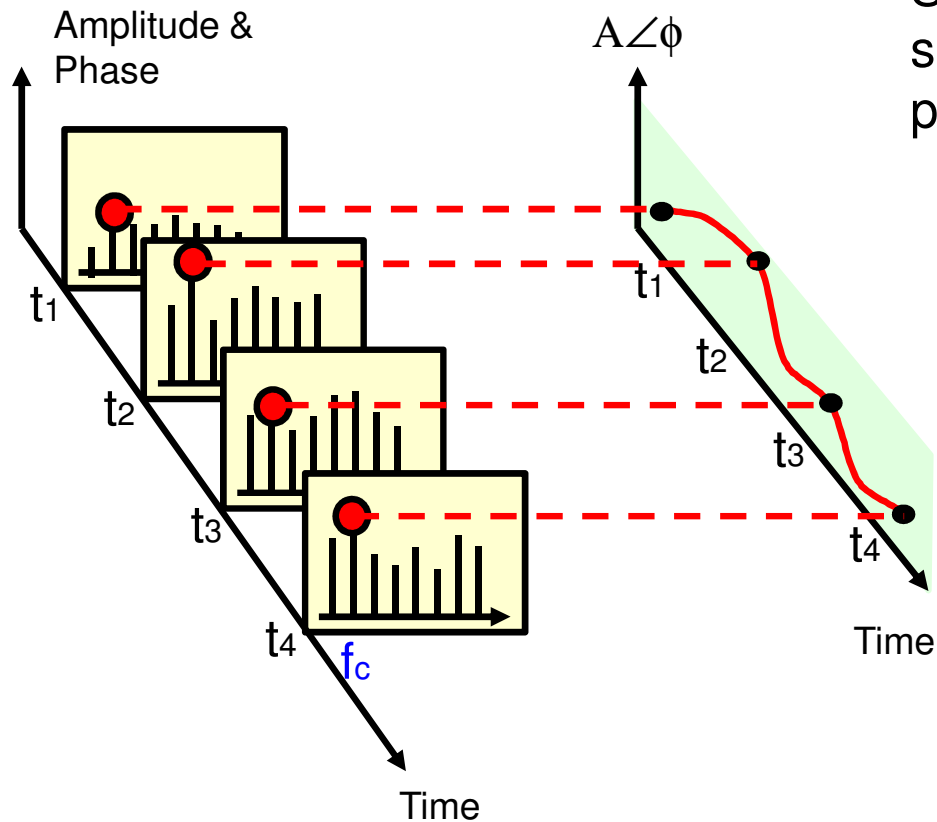


Circuit Envelope provides a complete non steady-state solution of the circuit through a Fourier series with time-varying coefficients

$$v(t) = \text{real} \left[ \sum_{k=0}^N V_k(t) e^{j\omega_k t} \right]$$

# Circuit Envelope Technique

## *Extracting Information From Time Domain Data*



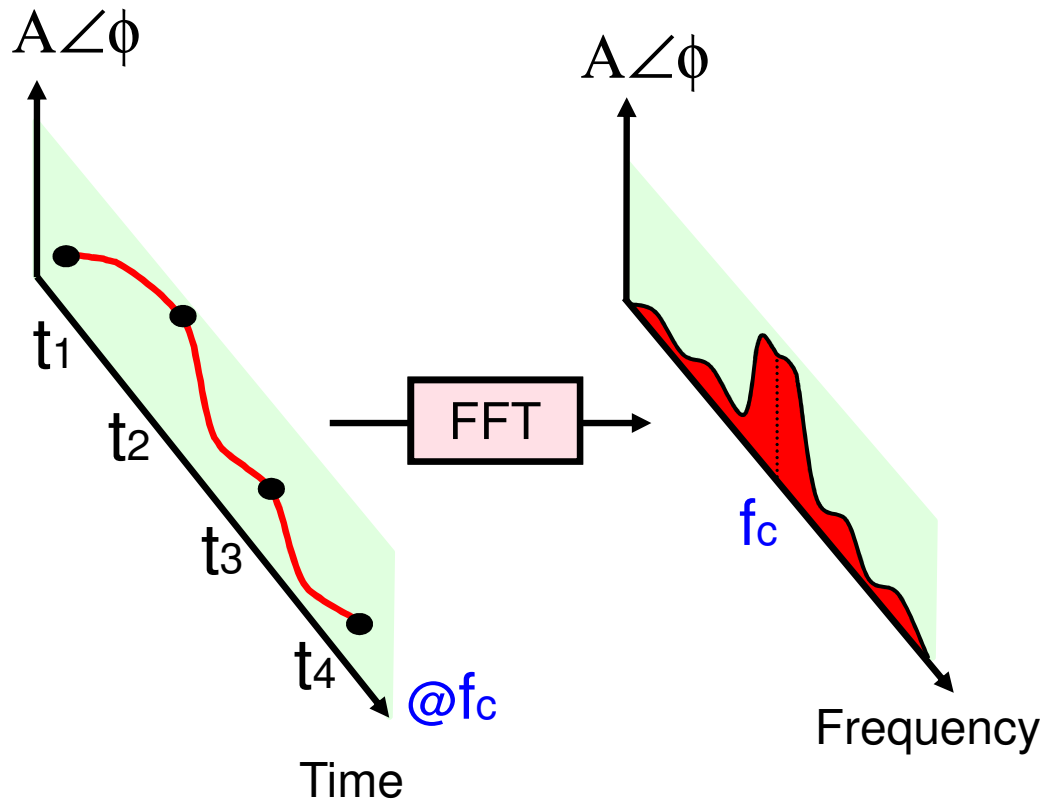
Selecting the desired harmonic spectral line ( $f_c$  in this case), it is possible to analyze:

- Amplitude vs. Time
  - Oscillator start up
  - Pulsed RF response
  - AGC transients
- Phase ( $\phi$ ) vs. Time ( $\tau$ )
  - VCO instantaneous frequency ( $\delta\phi/\delta\tau$ ), PLL lock time
- Amplitude & phase vs. time
  - Constellation plots
  - EVM, BER



# Circuit Envelope Technique

## *Extracting Information From Frequency Domain Data*



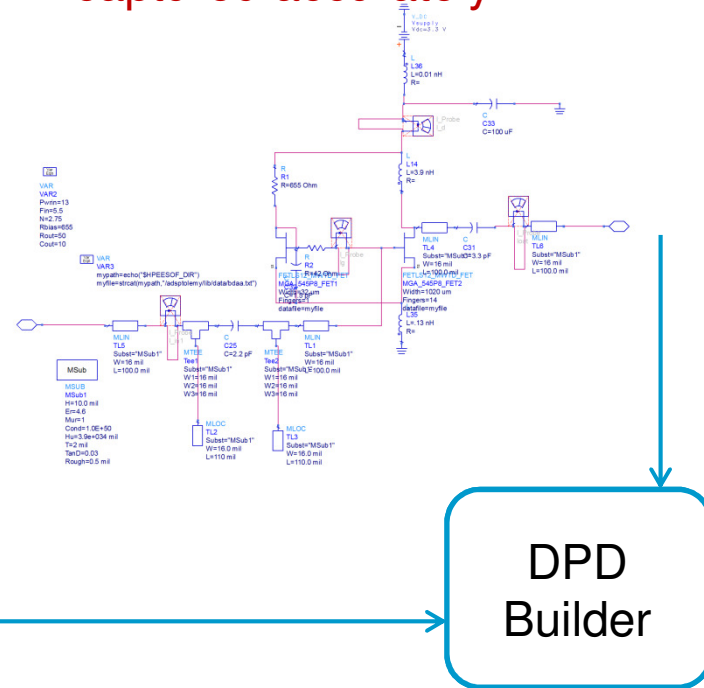
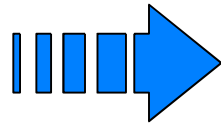
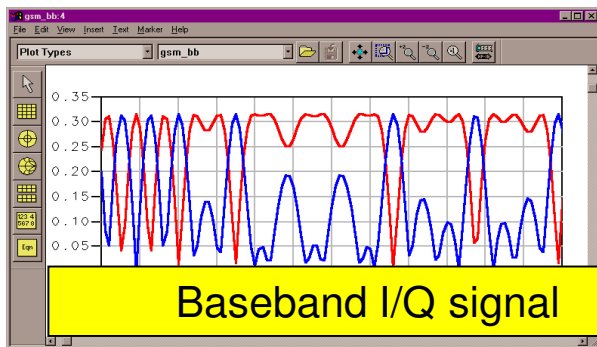
By applying FFT to the selected time-varying spectral line it is possible to analyze:

- Adjacent Channel Power Ratio (ACPR)
- Noise Power Ratio (NPR)
- Power added efficiency
- Reference frequency feed through in PLL
- Mixer intermod:
  - 3<sup>rd</sup>, 5<sup>th</sup>, 7<sup>th</sup>, 9<sup>th</sup> etc.

# PA Modeling: A Direct Co-simulation Approach

Instead of modeling  
– use the circuit directly!

Memory effects and non-linearity  
captured accurately



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About Digital Pre-Distortion (DPD)

DPD challenges for 4G/wideband systems

Design a PA that is more linearizable

Understand the limits of the DPD algorithm

Practical implementation

Some Results

Conclusion

Q&A



# How to optimize the DPD algorithm?

## **DPD + Behavioral**

- Potentially ignores memory effects and may not give best results

## **DPD + HW Amplifier**

- How do we know the measurement set up is not the limiting factor?

## **DPD + Actual circuit simulation**

- Opportunity to optimize circuit as well as the DPD algorithm concurrently

## **DPD (fixed point) + Actual circuit simulation**

- Tells how much realistic efficiency is achieved that takes the DPD HW current consumption also.

Next --- Some Results

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# Step by step to do DPD on a HW amplifier Presentation & Demonstration

# Five Easy Steps!

But lot of details

The screenshot shows the Agilent DPD software interface with the following configuration details:

- Current Iteration:** 1
- FCarrier:** 836e6 Hz
- SamplingRate:** 34.666e6 Hz
- Clipping Parameters:**
  - ClippingThreshold: 1
  - Maximum Order: 300
  - Pass Frequency: 4.5e6 Hz
  - Pass Ripple: 0.1 dB
  - Stop Frequency: 5e6 Hz
  - Stop Ripple: 50 dB
- I Branch Browse:** C:\Users\mupmaka\Documents\
- Q Branch Browse:** C:\Users\mupmaka\Documents\
- Download Parameter:**
  - RFPower: -17.51014 dBm
  - PrimAddress: 141.121.206.110
  - TimeStart: 0 ms
  - TimeStop: 10 ms
- Customized Waveform:** SystemVue 2010 icon with an arrow pointing to an MXG/ESG icon.
- Buttons:** Download Waveform, Go To ESG Web Control, CCDF, PAPR.

## Before you start DPD builder

1. Know the signal
2. Know your Power amplifier
3. Know the instruments
  - A. Signal Source
  - B. Signal Analyzer
4. Cable losses
5. DC bias source



# Know CCDF of your signal

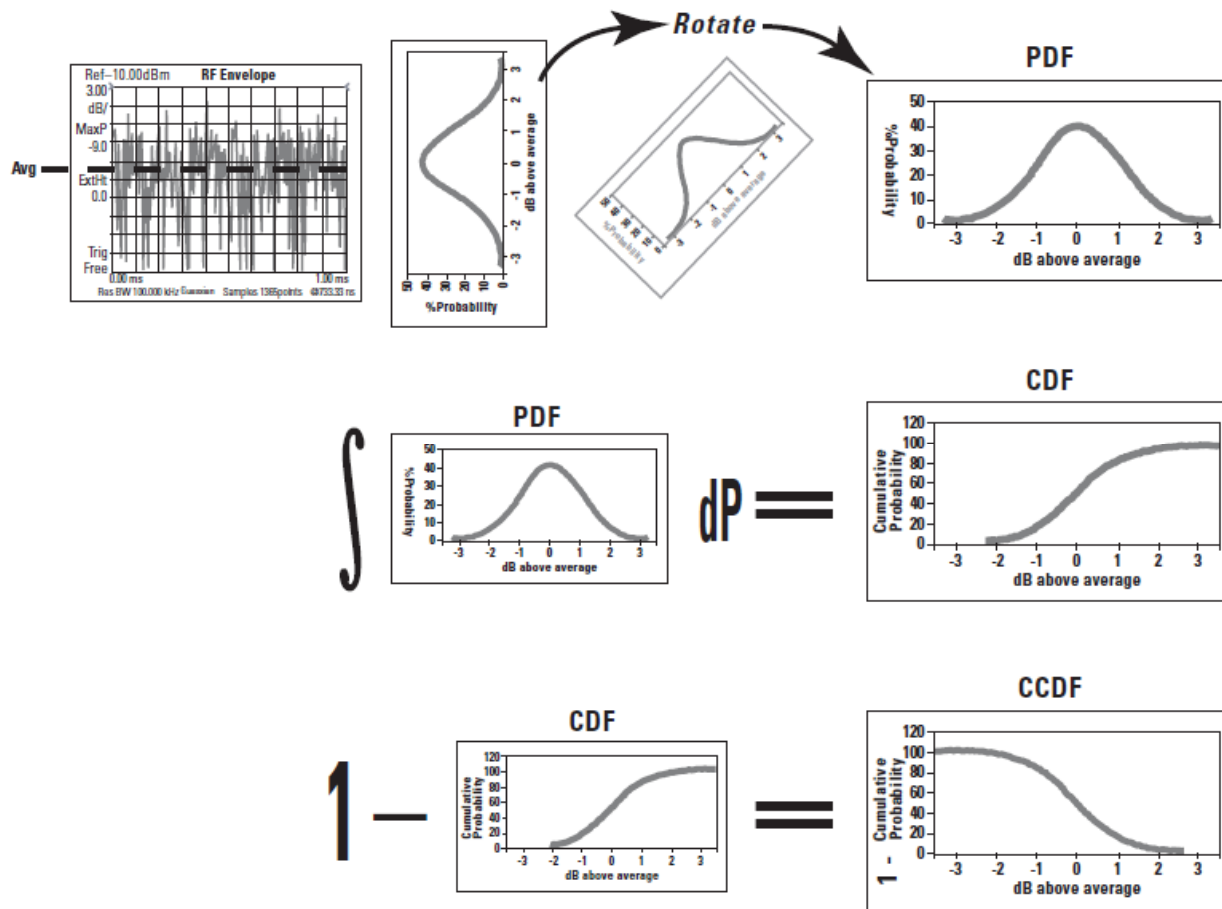
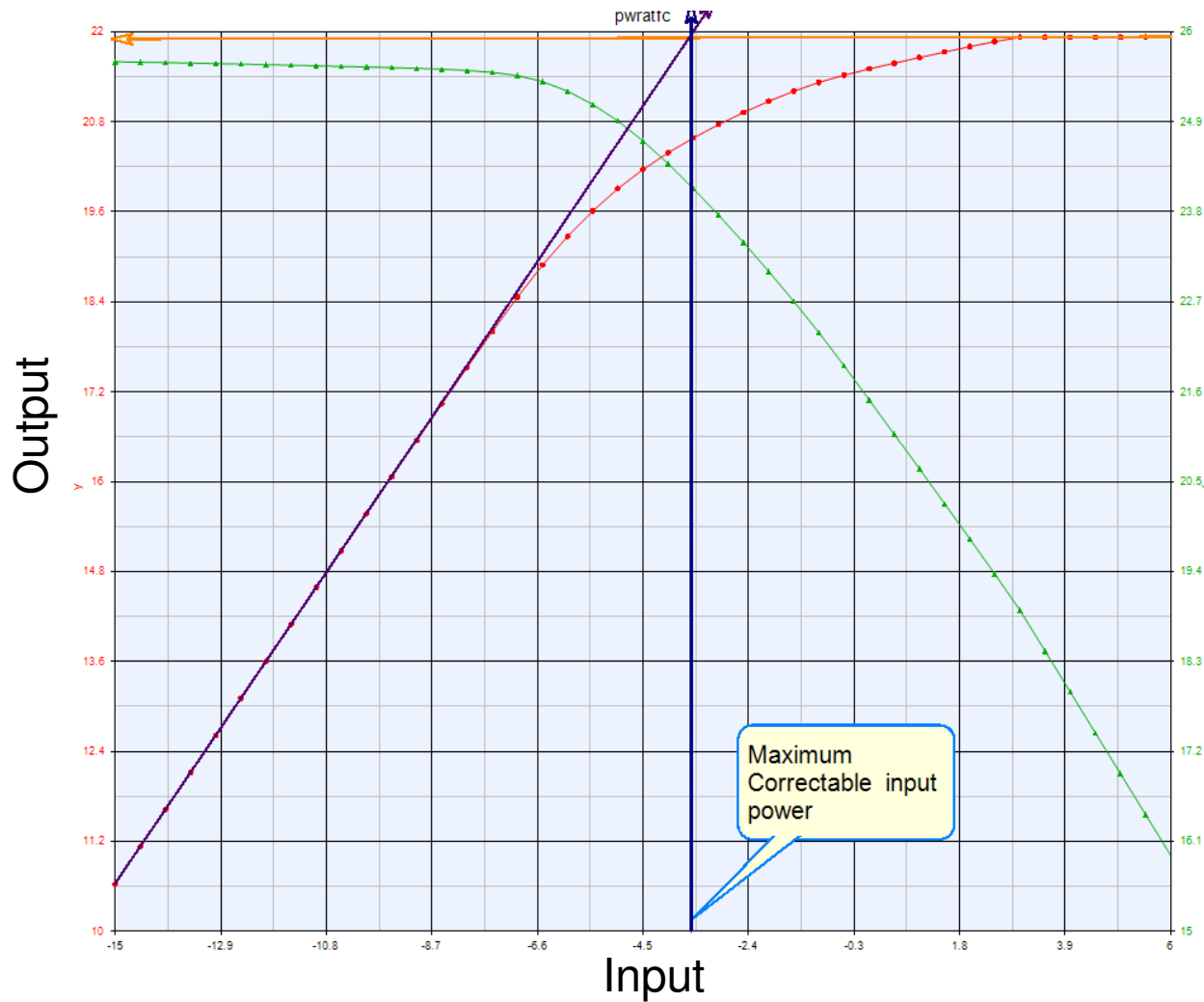


Figure 2: Mathematical origin of CCDF

# Know your Amplifier

## Gain and Gain compression



## Before you start DPD builder

1. Know the signal
2. Know your Power amplifier
3. Know the instruments
  - A. Signal Source
  - B. Signal Analyzer
4. Cable losses
5. DC bias source
6. VSA (89600) software.

# Five Easy Steps!

But lot of details

DPD

1: Create DPD Stimulus 2: Capture DUT Response 3: DUT Model Extraction 4: DPD Response 5: Verify DPD Response

Current Iteration

FCarrier  Hz

SamplingRate  Hz

Clipping Parameters

ClippingThreshold

Maximum Order

Pass Frequency  Hz

Pass Ripple  dB

Stop Frequency  Hz

Stop Ripple  dB

I Branch Browse  ...

Q Branch Browse  ...

Download Parameter

RFPower  dBm

PrimAddress

TimeStart  ms

TimeStop  ms

Customized Waveform

MXG/ESG

Download Waveform

Go To ESG Web Control

CCDF

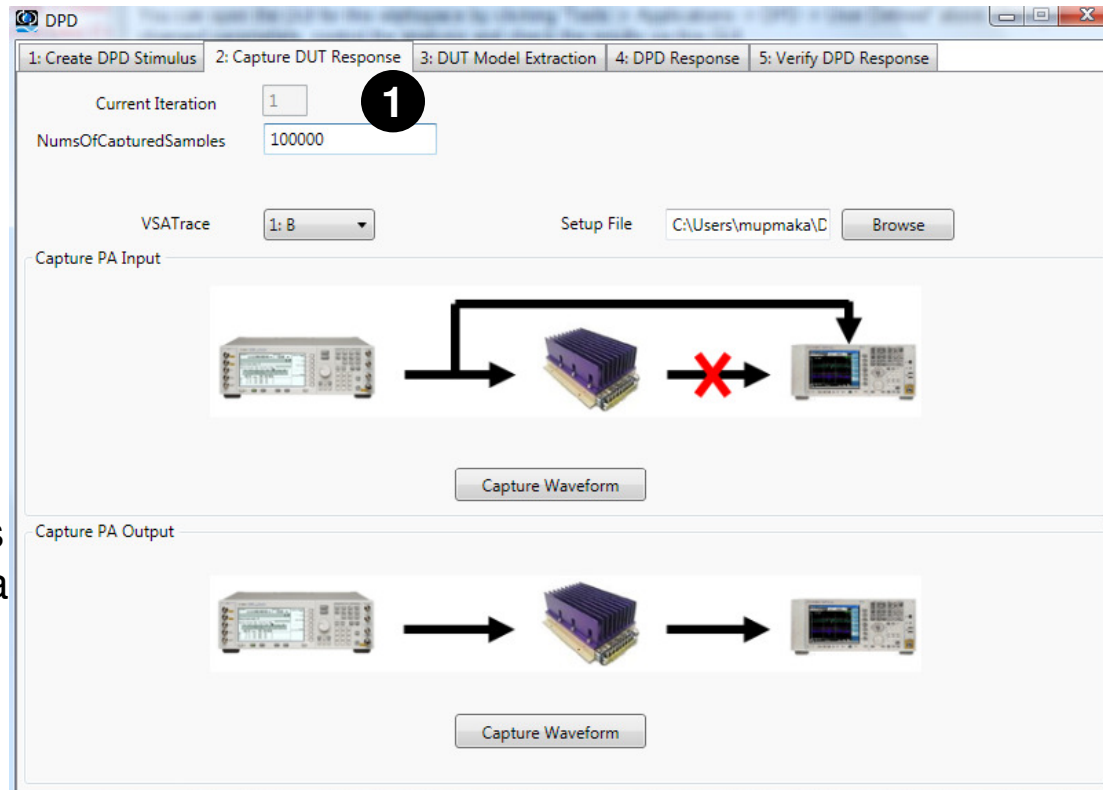
PAPR

# Capture: configure the measurement samples

## Iteration-1

**1**  
Configure the number of samples to capture.

Whereas SystemVue talks *directly* to the ESG/MXG, it talks to the Analyzer via the 89600 VSA software.



Do you have enough time points for a statistically valid extraction?

Before you go any further, the VSA software must be able to make a standalone hardware measurement. Once VSA configured, then SystemVue's task is very simple. It just talks to the VSA, and anything the VSA can control.

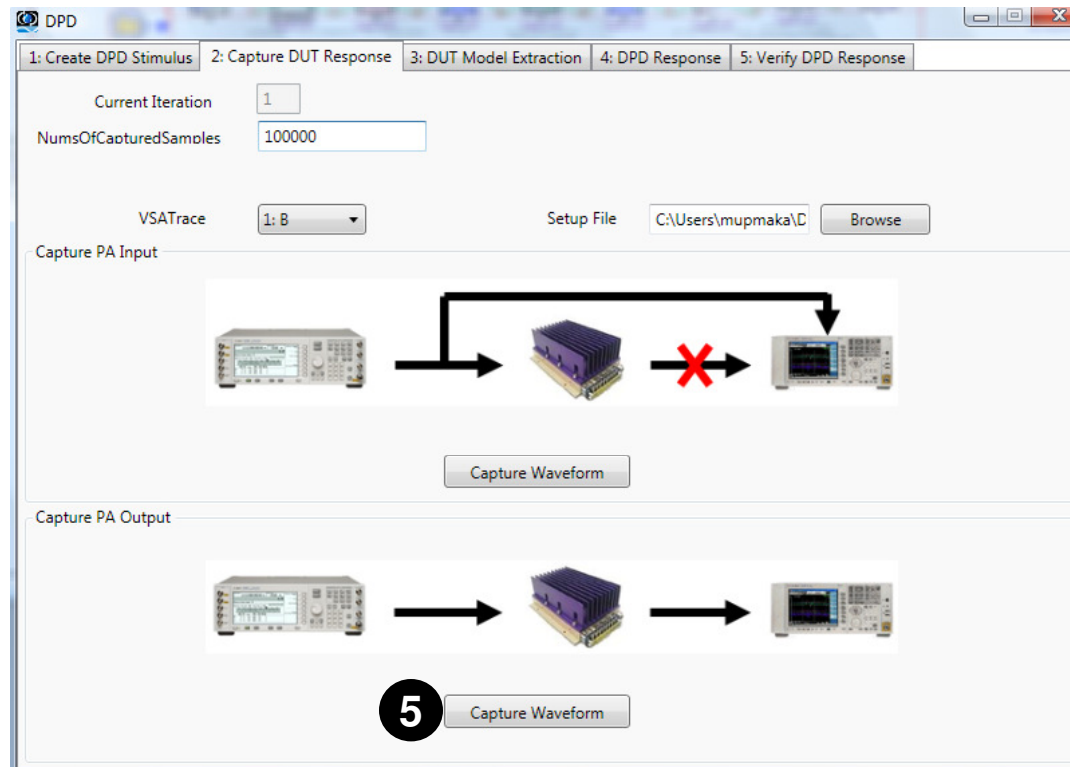
# Capture the PA output waveform

## Iteration-1

**5** Connect the PA into the measurement system.

Do a quick local measurement with the VSA to make sure that your PA is really operating.

Verify the true output power using the “Integrated BW Markers”



**IMPORTANT**  
Make sure that you have enough attenuation on the spectrum analyzer to prevent the PA from overloading the receiver front end.



**5** FILES STORED:  
Step2\_PAOutputdata\_Imag\_Iter1.txt  
Step2\_PAOutputdata\_Real\_Iter1.txt

# Iteration-1

The screenshot displays the 'DPD Model Extractor and Verifier' software interface. The top navigation bar shows five steps: 1: Create DPD Stimulus, 2: Capture DUT Response, 3: DUT Model Extraction, 4: DPD Response, and 5: Verify DPD. Step 2 is highlighted with a black circle and the number '1'. Step 5 is highlighted with a black circle and the number '2'. The main configuration area includes the following settings:

- Current Iteration: 1
- NumOfInputSamples: 30000
- Model Type: 0: Memory Polynomial
- Model Identification Algorithm: 0: LSE using QR
- MemoryOrder: 4 (circled in red)
- NonlinearOrder: 9

A block diagram illustrates the model structure. The input signal  $y(n)$  is processed through a series of delay elements ( $z^{-1}$ ) and summed with its magnitude raised to the power of 4, as shown in the equation blocks:

$$\sum_{k=1}^K a_k y(n-k) |y(n-k)|^{k-1}$$

The outputs of these blocks are summed to produce the final signal  $z(n)$ . Below the diagram, there are buttons for 'DPD Model Extraction' and 'Show DPD Coefficients'. The 'Show Results' section includes a 'Normalize' checkbox (checked) and several analysis buttons: 'PA AM-AM', 'DPD AM-AM', 'PA AM-PM', and 'DPD AM-PM'. The 'Power Alignment' button is highlighted in blue. The results display shows a value of 0.375177350895535 and an NMSE of -49.625061020684 dB.

# Iteration-1

The screenshot displays the 'DPD Model Extraction and Verification' software interface. The top navigation bar shows five steps: 1: Create DPD Stimulus, 2: Capture DUT Response, 3: DUT Model Extraction, 4: DPD Response, and 5: Verify DPD Response. The 'Current Iteration' is set to 1. The 'NumOfInputSamples' is 30000, 'MemoryOrder' is 4, and 'NonlinearOrder' is 9. The 'Model Type' is '0: Memory Polynomial' and the 'Model Identification Algorithm' is '0: LSE using QR'. A block diagram shows the signal flow from  $y(n)$  through delay elements ( $z^{-1}$ ) and nonlinear blocks to produce  $z(n)$ . The 'Show Results' section includes a 'Normalize' checkbox and buttons for 'PA AM-AM', 'DPD AM-AM', 'PA AM-PM', 'DPD AM-PM', 'Spectrum', and 'Power Alignment'. The 'Power Alignment' button is active, and the 'NMSE' result is -49.625061020684 dB, which is circled in red.

Current Iteration: 1  
NumOfInputSamples: 30000  
MemoryOrder: 4  
NonlinearOrder: 9  
Model Type: 0: Memory Polynomial  
Model Identification Algorithm: 0: LSE using QR

DPD Model Extraction  
Show DPD Coefficients

Show Results

Normalize

PA AM-AM    DPD AM-AM    PA AM-PM    DPD AM-PM

Spectrum    Power Alignment    0.375177350895535    NMSE: -49.625061020684 dB



# Iteration-1

1: Create DPD Stimulus 2: Capture DUT 3: DUT Model Extraction 4: DPD 5: Verify DPD Response

Current Iteration: 1

Power Alignment: 0.3751773508955 Default Do Power Alignment AM-AM

Download Parameters

RFPower: -1.0 dBm Default PrimAddress: 192.168.0.102

Time Start: 0 s Time Stop: 20 ms

Customized Waveform Pre-Distorter MXG/ESG

Please "Do power search" in MXG/ESG by clicking "Amplitude\Do Power Search" after downloading.

Download Waveform Go To ESG Web Control Spectrum

Capture Waveform Normalize DPD-PA AM-AM DPD-PA AM-PM

# End--Iteration 1

The screenshot shows the DPD software interface with the following elements:

- Progress Bar:** 1: Create DPD Stimulus | 2: Capture DUT Response | 3: DUT Model Extraction | 4: DPD Response | 5: Verify DPD Response
- Current Iteration:** 1
- Download Parameters:**
  - RFPower: -1.0 dBm
  - PrimAddress: 192.168.0.102
  - Time Start: 0 ms
  - Time Stop: 20 ms
- Workflow Diagram:**
  - Step 1:** A diagram showing a 'Customized Waveform' (SystemVue 2010) being downloaded to an 'MXG/ESG' device. A button labeled 'Download Waveform' is circled with a '1'. A button labeled 'Go To ESG Web Control' is also present.
  - Step 2:** A diagram showing the 'MXG/ESG' device connected to a 'DUT' (Device Under Test) and then to a spectrum analyzer. A button labeled 'Capture Waveform' is circled with a '2'.
  - Step 3:** A button labeled 'Show Results' is circled with a '3', with a 'Spectrum' button below it.
- Text:** A blue text box on the right states: "This step is to download the original signal (without DPD) with the same RF power as step 4. You may also use the downloaded waveform in step 1 and change the power in MXG/ESG."

Ideally the DPD spectrum should coincide with the original signal spectrum excepting a gain difference. If the DPD has not improved the out put spectrum then we have to go back to step1.

# Begin--Iteration 2

The screenshot shows the 'Create DPD Stimulus' software window. The top navigation bar includes five steps: 1: Create DPD Stimulus, 2: Capture DUT Response, 3: DUT Model Extraction, 4: DPD Response, and 5: Verify DPD Response. The 'Current Iteration' is set to 2, indicated by a circled '1'. The 'FCarrier' is 835.6e6 Hz and 'SamplingRate' is 2.1666e6 Hz. The 'Clipping Parameters' section includes: ClippingThreshold (1), Maximum Order (300), Pass Frequency (4.5e6 Hz), Pass Ripple (0.1 dB), Stop Frequency (5e6 Hz), and Stop Ripple (50 dB). The 'I Branch Browse' and 'Q Branch Browse' fields both point to 'C:\Users\mupmaka\Documents\'. The 'Download Parameter' section includes: RFPower (-1.0 dBm), PrimAddress (192.168.0.102), TimeStart (0 ms), and TimeStop (20 ms), with a circled '2' next to the PrimAddress field. At the bottom, there is a 'Customized Waveform' section with a 'SystemVue 2015' icon and an 'MXG/ESG' icon connected by an arrow. To the right are buttons for 'Download Waveform', 'Go To ESG Web Control', 'CCDF', and 'PAPR'.

## Iteration 2

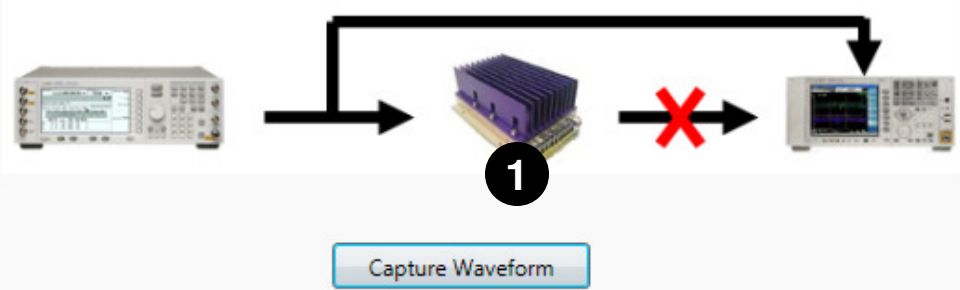
DPD

1: Create DPD Stimulus 2: Capture DUT Response 3: DUT Model Extraction 4: DPD Response 5: Verify DPD Response

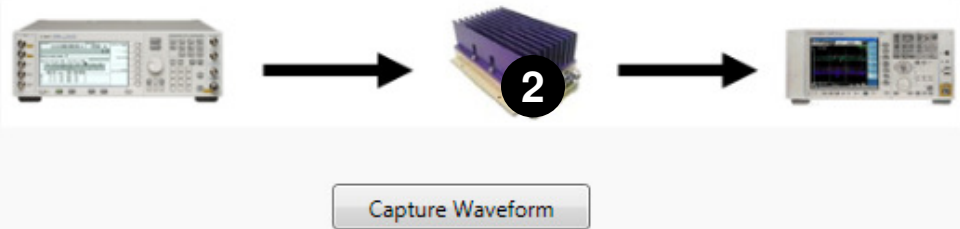
Current Iteration: 2  
NumsOfCapturedSamples: 100000

VSATrace: 1: B Setup File: C:\Users\mupmaka\D Browse

Capture PA Input



Capture PA Output



# Iteration 2

DPD

1: Create DPD Stimulus 2: Capture DUT Response 3: DUT Model Extraction 4: DPD Response 5: Verify DPD Response

Current Iteration: 2

NumOfInputSamples: 30000

MemoryOrder: 4

NonlinearOrder: 9

Model Type: 0: Memory Polynomial

Model Identification Algorithm: 0: LSE using QR

DPD Model Extraction **1**

Show DPD Coefficients

Show Results

Normalize

PA AM-AM **2**

DPD AM-AM

PA AM-PM

DPD AM-PM

Spectrum

Power Alignment **3** 0.375177350895535

NMSE **4** -49.625061020684 dB

## Iteration 2

The screenshot shows the DPD software interface with the following components:

- Progress Bar:** 1: Create DPD Stimulus | 2: Capture DUT Response | 3: DUT Model Extraction | 4: DPD Response | 5: Verify DPD Response
- Current Iteration:** 2
- Power Alignment:** 0.375177350895535, Default, Do Power Alignment, AM-AM
- Download Parameters:**
  - RFPower: -1.0 dBm, Default
  - PrimAddress: 192.168.0.102
  - Time Start: 0 s
  - Time Stop: 20 ms
- Step 1:** Customized Waveform (SystemVue 2010) → Pre-Distorter → MXG/ESG. Includes buttons: Download Waveform, Go To ESG Web Control, Spectrum. Text: "Please 'Do power search' in MXG/ESG by clicking 'Amplitude\Do Power Search' after downloading."
- Step 2:** MXG/ESG → PA → Analyzer. Includes buttons: Capture Waveform,  Normalize, DPD-PA AM-AM, DPD-PA AM-PM.

## End--Iteration 2

DPD

1: Create DPD Stimulus 2: Capture DUT Response 3: DUT Model Extraction 4: DPD Response 5: Verify DPD Response

Current Iteration

Download Parameters

RFPower  dBm PrimAddress

Time Start  ms Time Stop  ms

**1** Customized Waveform → MXG/ESG

Download Waveform Go To ESG Web Control

This step is to download the original signal (without DPD) with the same RF power as step 4. You may also use the downloaded waveform in step 1 and change the power in MXG/ESG.

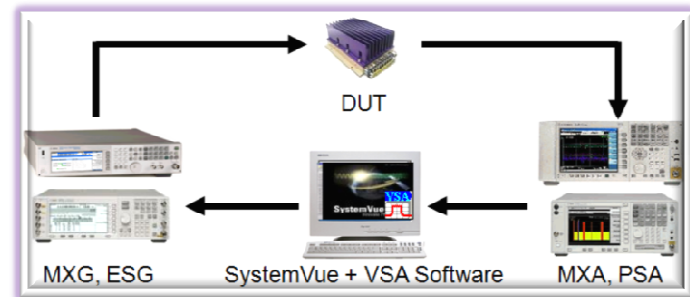
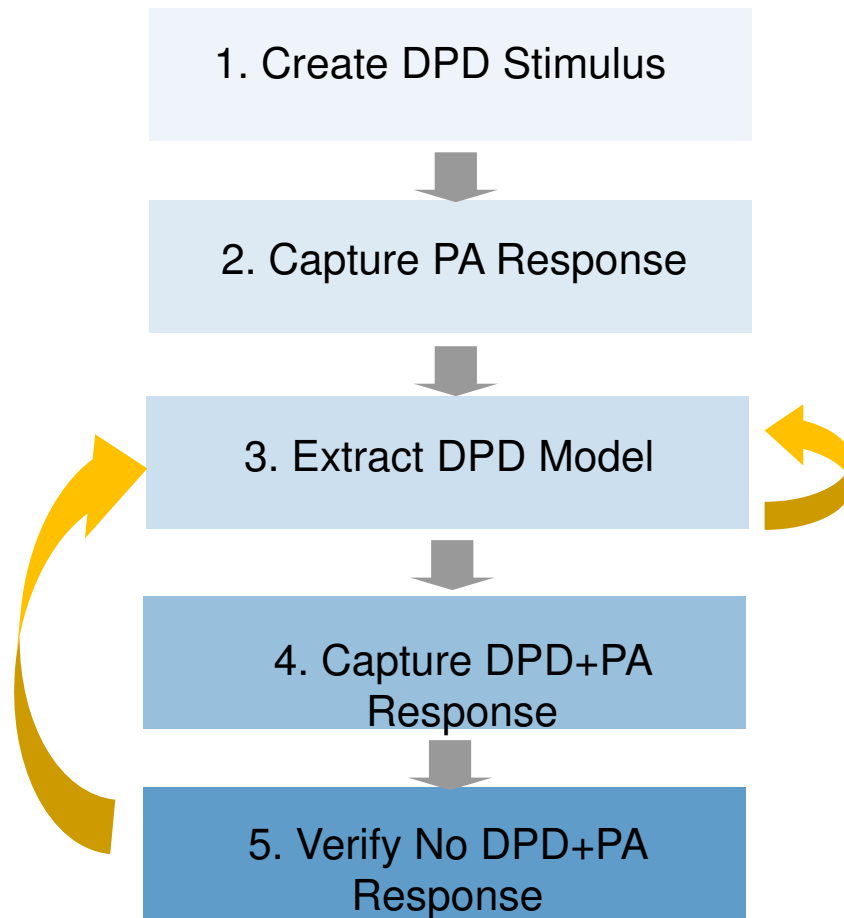
**2** MXG/ESG → DUT → Spectrum Analyzer

Capture Waveform

**3** Show Results

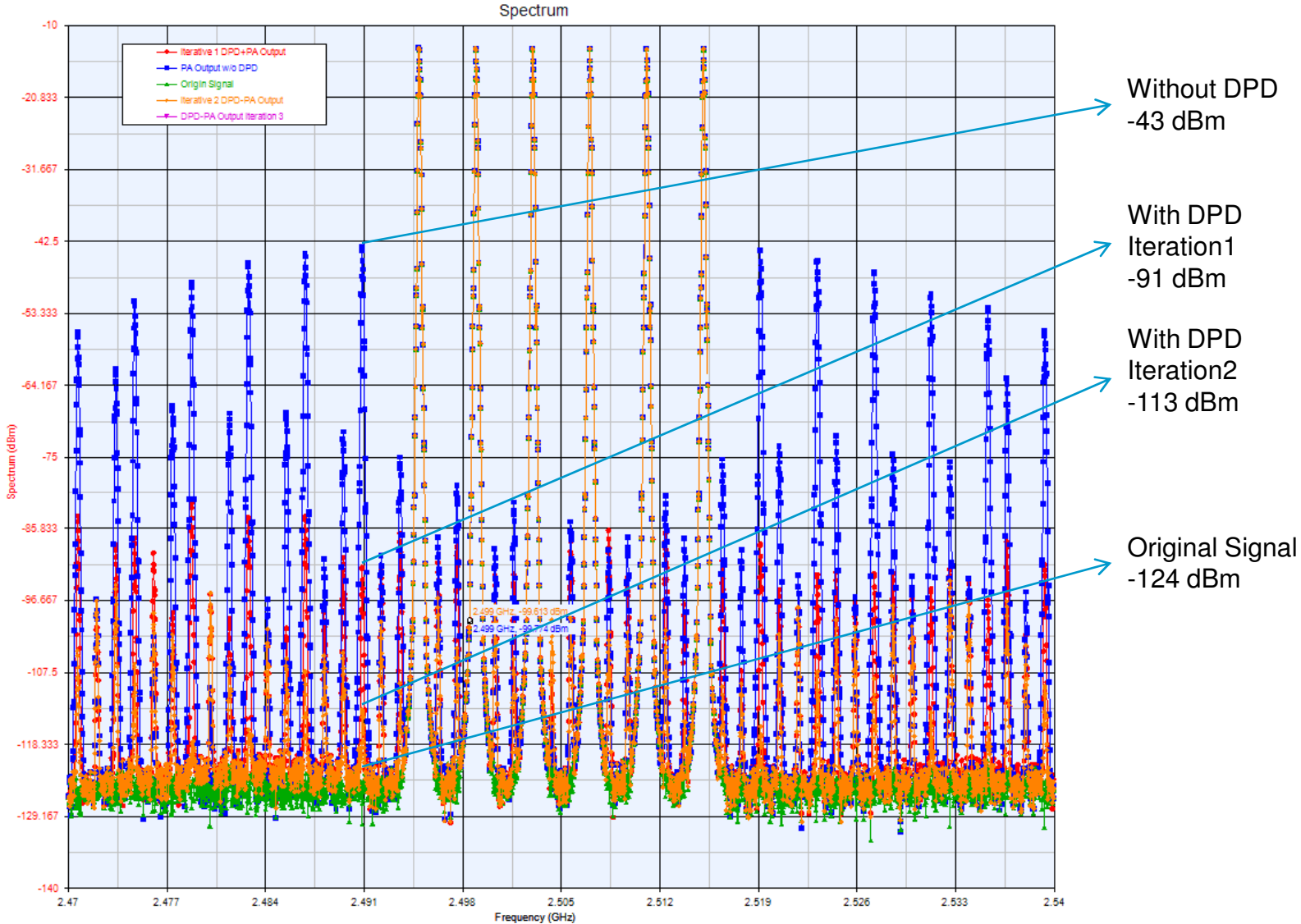
Spectrum

# Let us review the steps



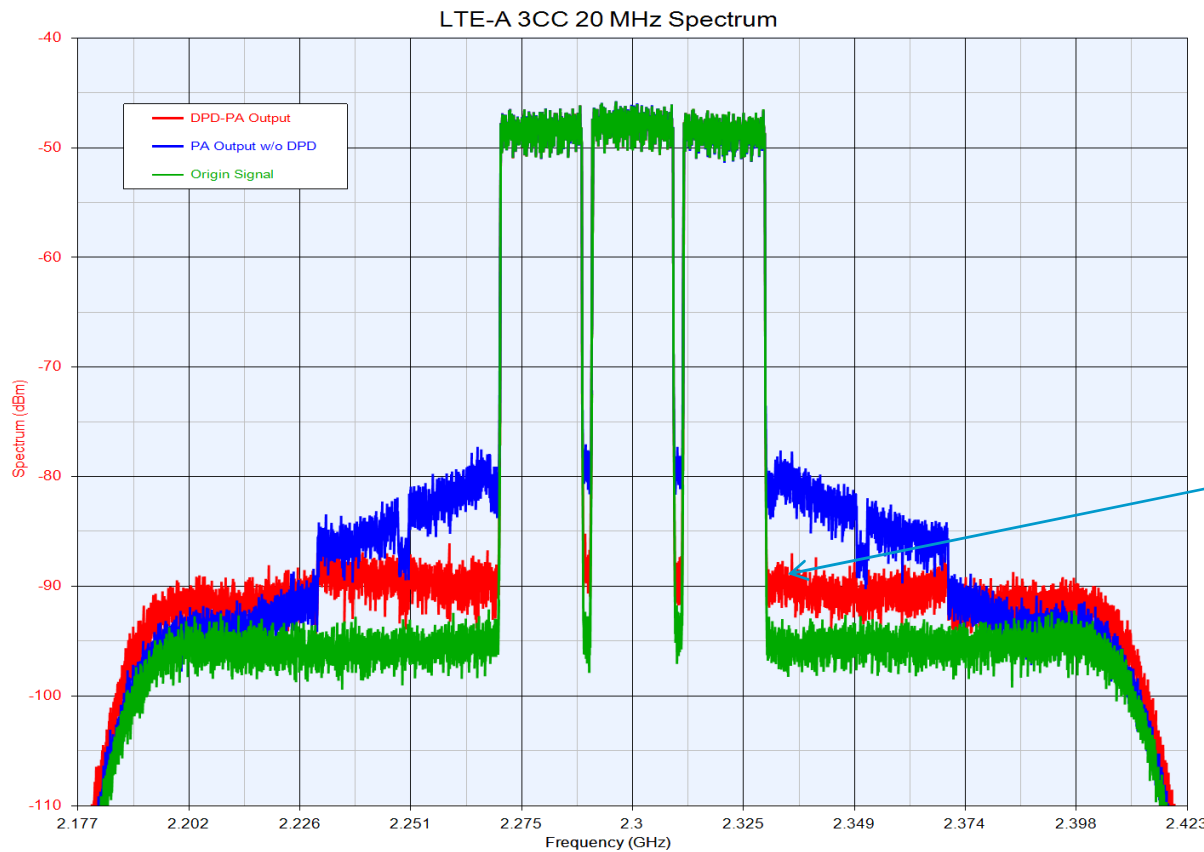


# PA Circuit - DPD Algorithm in Simulation



# Wideband platform

*SystemVue with Modular PXI Instruments (Bandwidth ~250 MHz)*



**~10 dB  
improvement  
in spectral  
leakage  
(1<sup>st</sup> iteration)**

# DPD of LTE-Advanced, Using M9330A/M9392A

## 4 x 20 MHz Contiguous CCs (80 MHz Signal BW)

Source = M9330A AWG

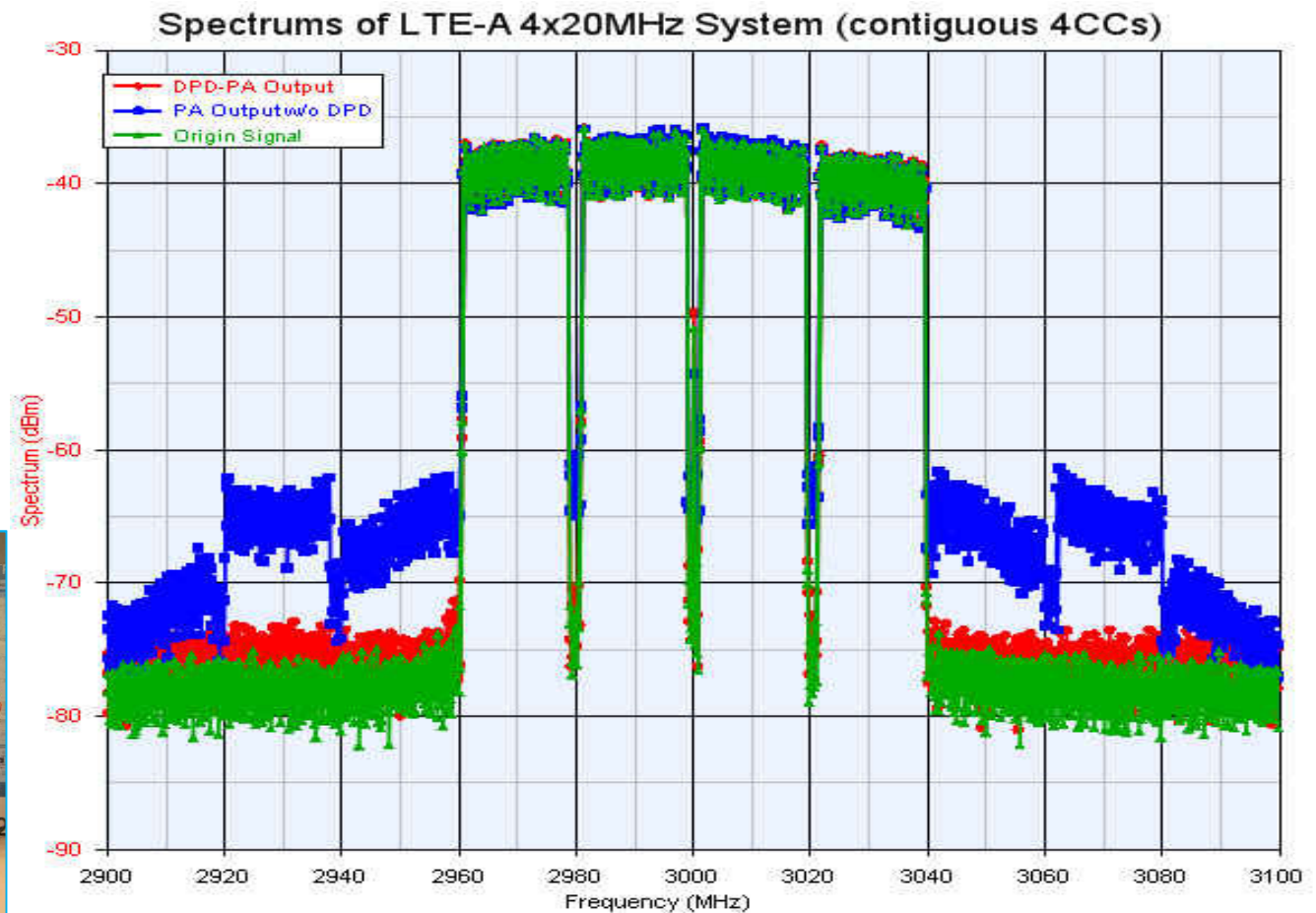
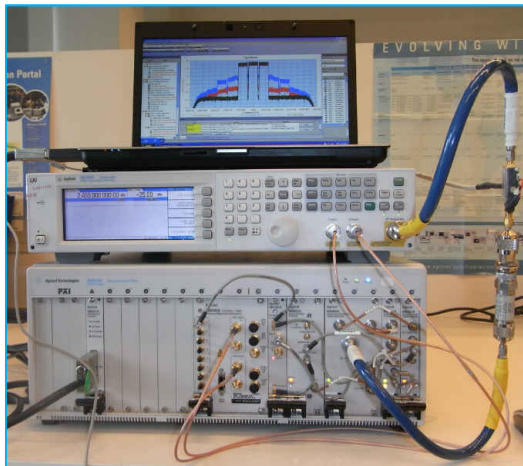
Vector Analyzer= M9392A

- 12bits ADC
- up to 250 MHz bandwidth

PA Output Spectrum (Blue)

PA+DPD Spectrum (Red)

PA Input Spectrum (Green)



# DPD of LTE-Advanced, Using M9330A/M9392A

## *2 x 20 MHz + 20 MHz Non-contiguous CA (80 MHz Signal BW)*

**Source** = M9330A AWG

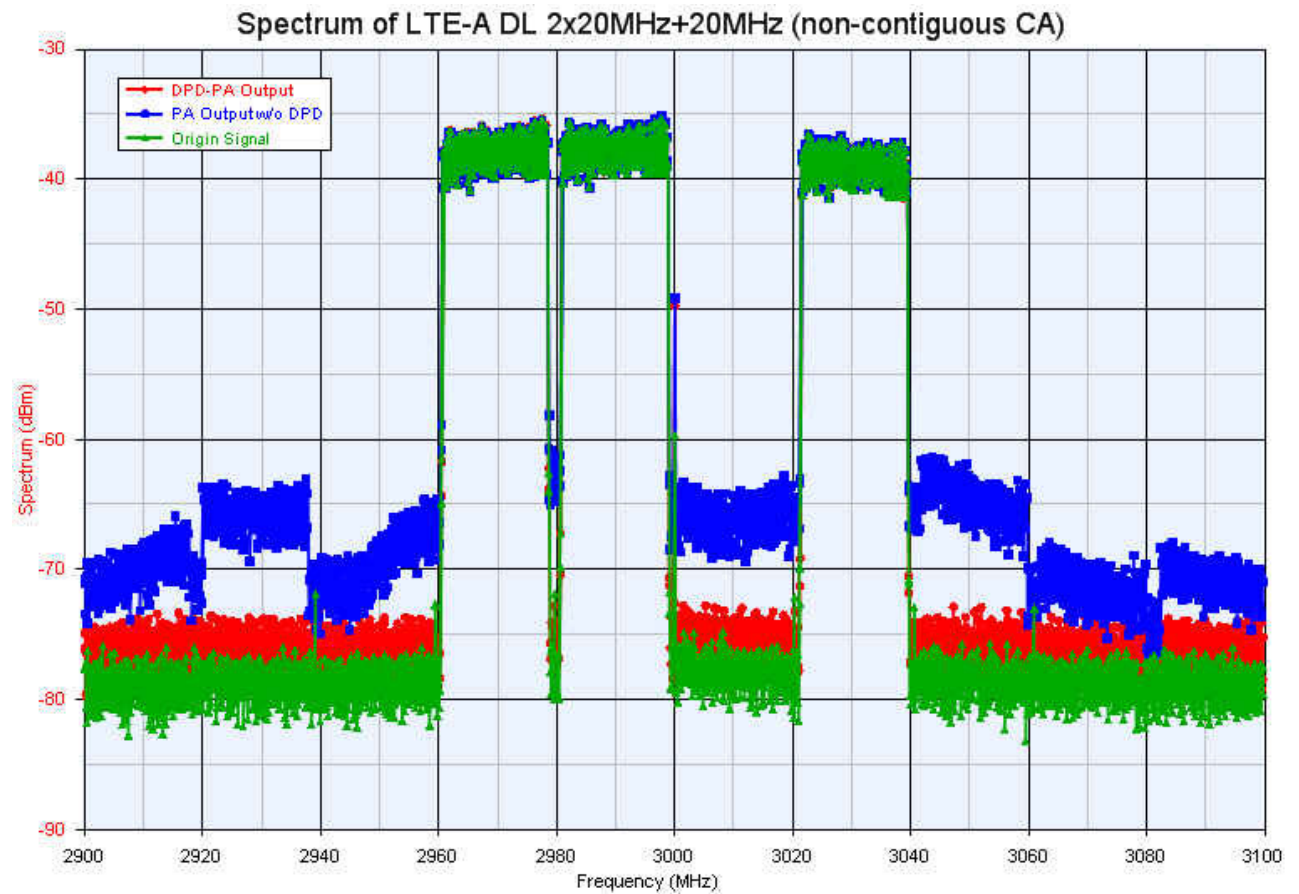
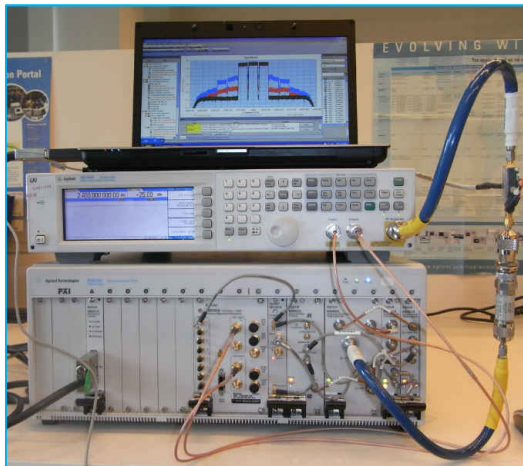
**Vector Analyzer**= M9392A

- 12bits ADC
- up to 250 MHz bandwidth

**PA Output Spectrum** (Blue)

**PA+DPD Spectrum** (Red)

**PA Input Spectrum** (Green)



# DPD of 802.11ac, Using M9330A/M9392A (80 MHz Option)

Source = M9330A AWG

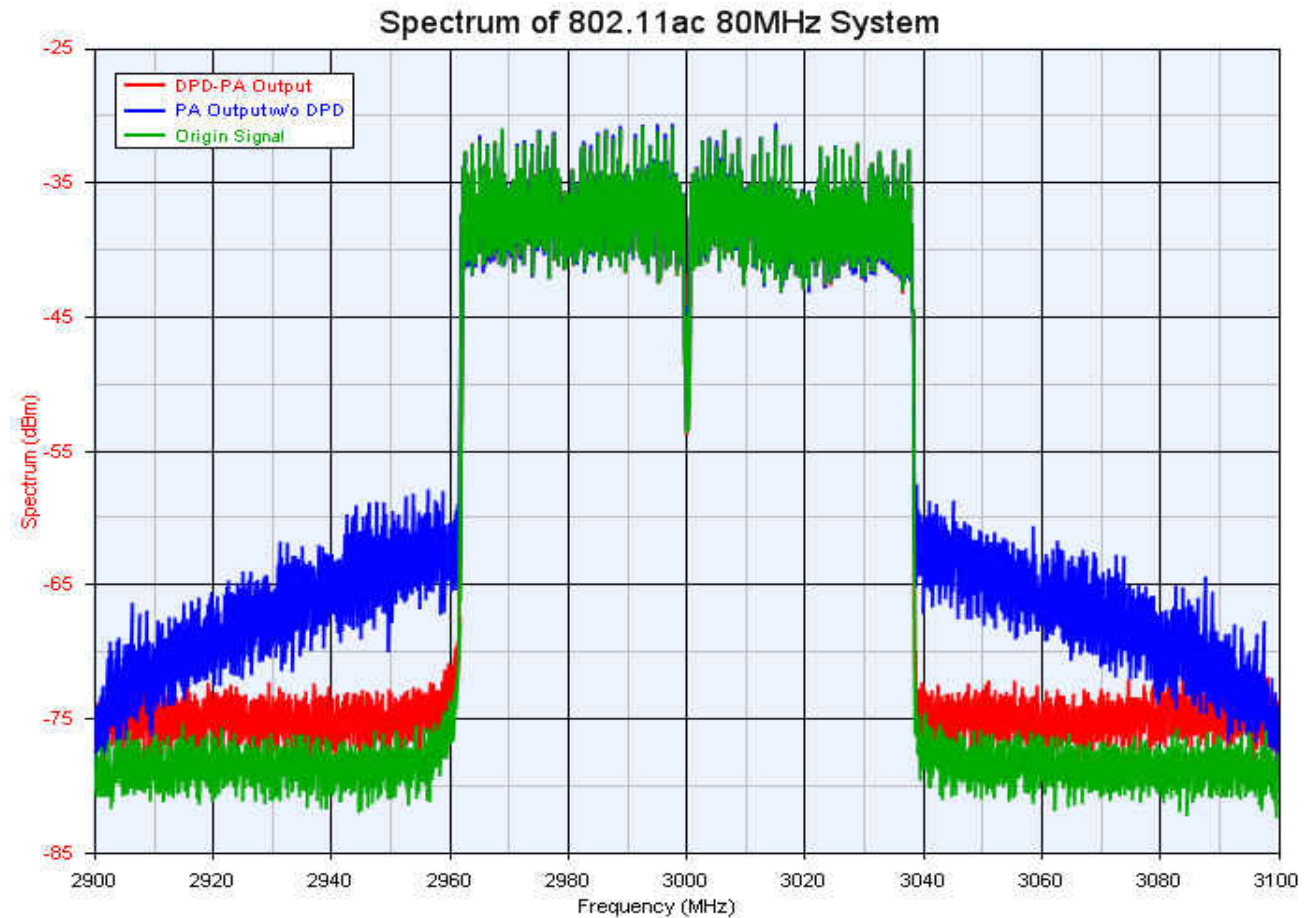
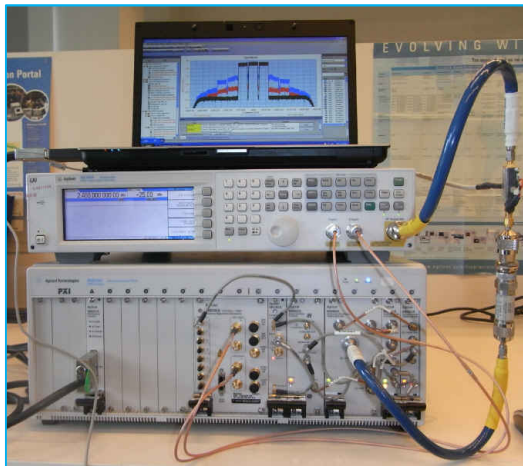
Vector Analyzer= M9392A

- 12bits ADC
- up to 250 MHz bandwidth

PA Output Spectrum (Blue)

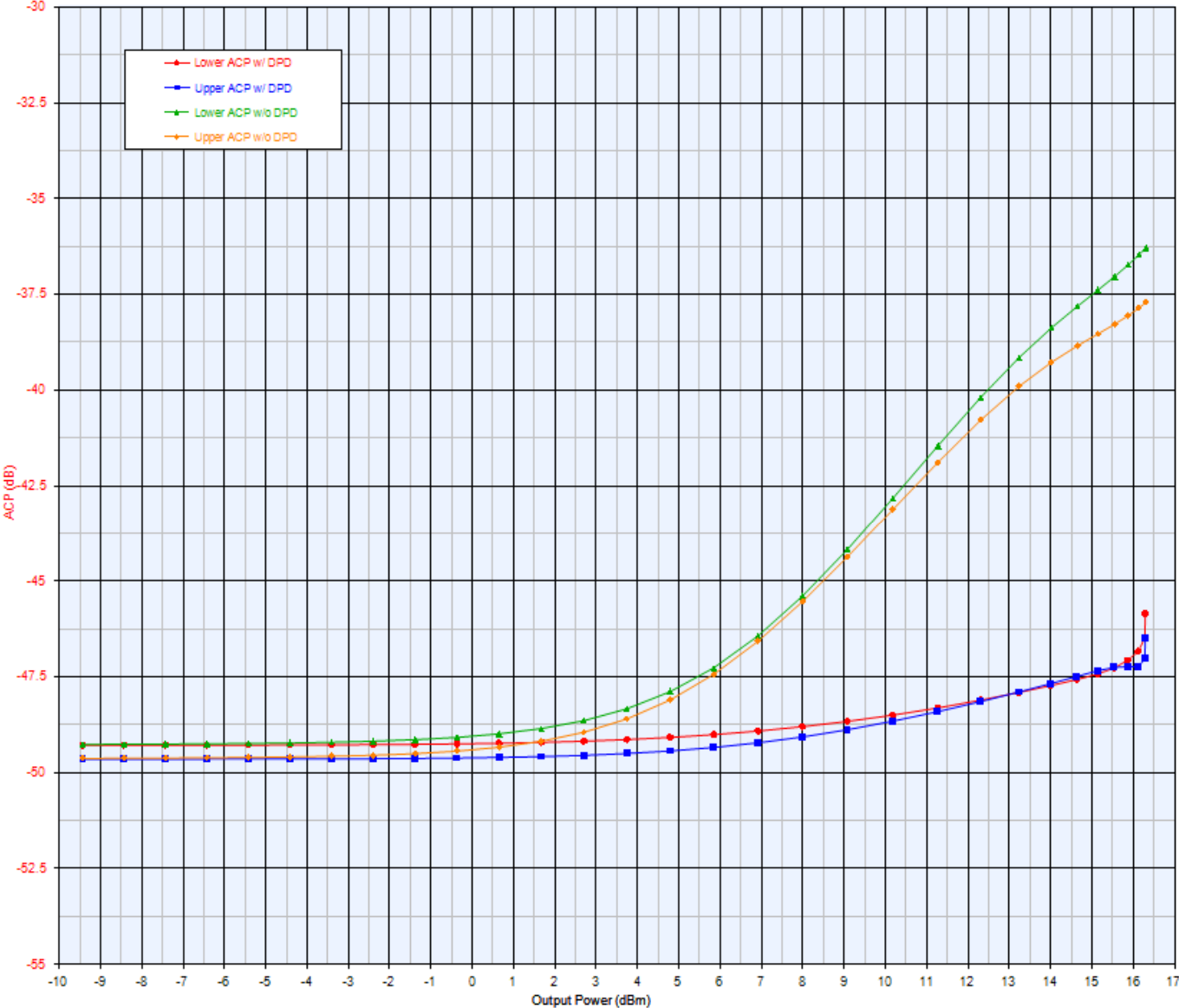
PA+DPD Spectrum (Red)

PA Input Spectrum (Green)

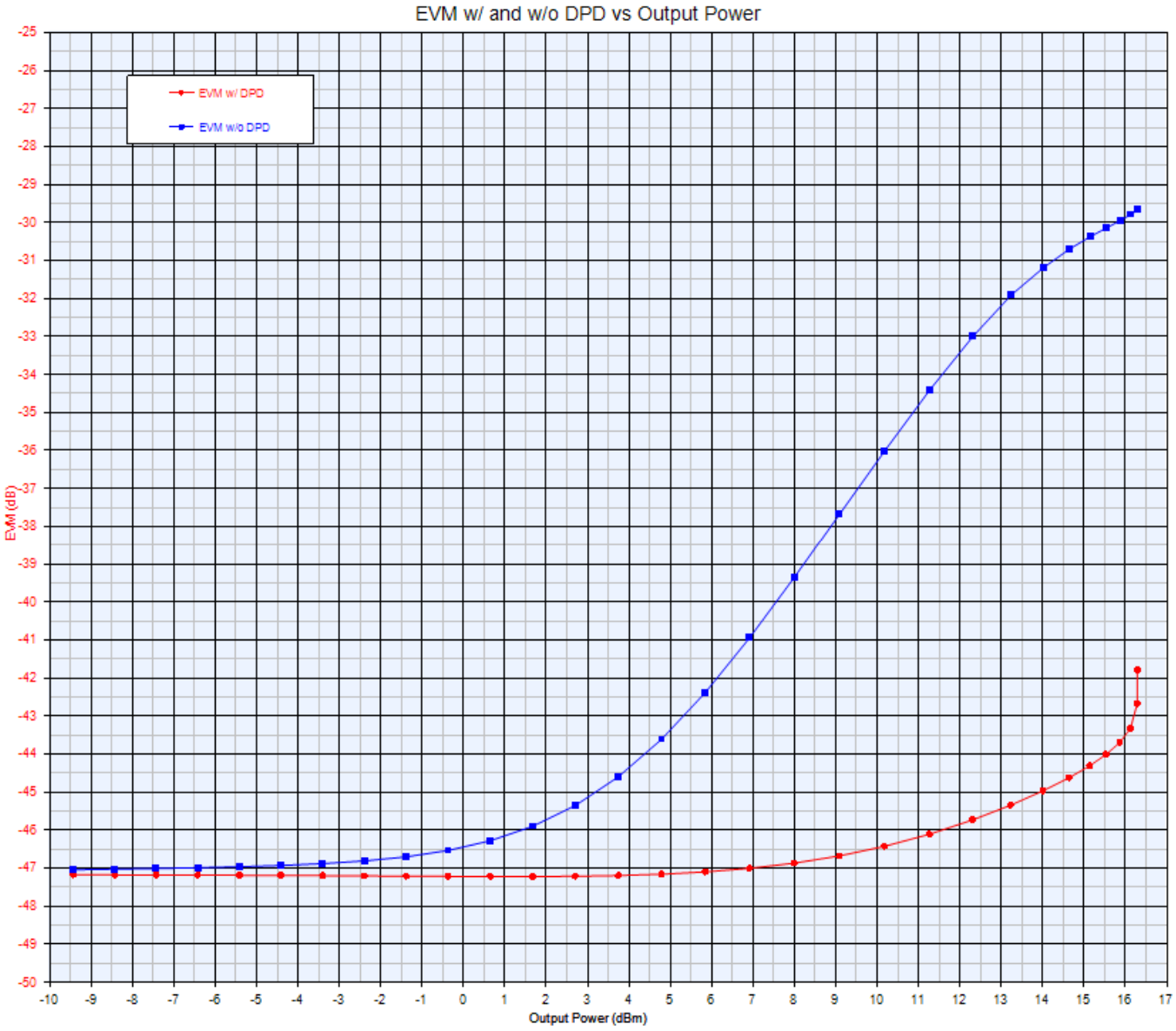


# DPD of 802.11ac - Simulation

ACPR w/ and w/o DPD vs Output Power



# DPD of 802.11ac - Simulation



# Agenda

About Digital Pre-Distortion (DPD)

DPD challenges for 4G/wideband systems

Design a PA that is more linearizable

Understand the limits of the DPD algorithm

Some Results

Conclusion

Q&A





# Conclusion

- New bandwidth and linearity requirements are driving 4G designers to spec DPD earlier in their system designs
- The velocity of the industry is pushing DPD activity in-house, where designers are taking a more active role
- Cosimulation with actual circuit gives the ability to capture Memory effects
- Establishes the boundaries of DPD algorithm
- Enables good business decision on the selection of instrumentation

# Further Information

## About Wideband DPD

– *Watch a demo:*

<http://www.youtube.com/watch?v=bocF6P74T9E>

– *Read an app note:*

<http://cp.literature.agilent.com/litweb/pdf/5990-8883EN.pdf>

## About Agilent Products

– <http://www.agilent.com/find/eesof-systemvue-dpd-builder>

– <http://www.agilent.com/find/modular>



# Selected DPD References

1. Lei Ding, Zhou G.T., Morgan D.R., Zhengxiang Ma, Kenney J.S., Jaehyeong Kim, Giardina C.R., “*A robust digital baseband predistorter constructed using memory polynomials*”, [Communications, IEEE Transactions on](#), Jan. 2004, Volume: 52, Issue:1, page 159-165.
2. Lei Ding, “*Digital Predistortion of Power Amplifiers for Wireless Applications*”, PhD Thesis, March 2004.
3. Roland Sperlich, “*Adaptive Power Amplifier Linearization by Digital Pre-Distortion with Narrowband Feedback using Genetic Algorithms*”, PhD Thesis, 2005.
4. Helaoui, M. Boumaiza, S. Ghazel, A. Ghannouchi, F.M., “*Power and efficiency enhancement of 3G multicarrier amplifiers using digital signal processing with experimental validation*”, [Microwave Theory and Techniques, IEEE Transactions on](#), June 2006, Volume: 54, Issue: 4, Part 1, page 1396-1404.
5. H. A.Suraweera, K. R. Panta, M. Feramez and J. Armstrong, “*OFDM peak-to-average power reduction scheme with spectral masking*,” Proc. Symp. on Communication Systems, Networks and Digital Signal Processing, pp.164-167, July 2004.
6. Zhao, Chunming; Baxley, Robert J.; Zhou, G. Tong; Boppana, Deepak; Kenney, J. Stevenson, “*Constrained Clipping for Crest Factor Reduction in Multiple-user OFDM*”, Radio and Wireless Symposium, 2007 IEEE Volume , Issue , 9-11 Jan. 2007 Page(s):341- 344.
7. Olli Vaananen, “*Digital Modulators with Crest Factor Reduction Techniques*”, PhD Thesis, 2006
8. Boumaiza, et a, “*On the RF/DSP Design for Efficiency of OFDM Transmitters*” , *IEEE Transactions on Microwave Theory and Techniques*, Vol. 53, No. 7, July 2005, pp 2355-2361.
9. Boumaiza, Slim, “*Advanced Memory Polynomial Linearization Techniques*,” IMS2009 Workshop WMC (Boston, MA), June 2009.

# Recent DPD Resources from Agilent

## App Notes

- <http://cp.literature.agilent.com/litweb/pdf/5990-8883EN.pdf> (Wideband DPD)
- <http://cp.literature.agilent.com/litweb/pdf/5990-7818EN.pdf> (3G/4G)
- <http://cp.literature.agilent.com/litweb/pdf/5990-6742EN.pdf>
- <http://cp.literature.agilent.com/litweb/pdf/5990-6534EN.pdf> (algorithms used)

## Demonstration Videos

- <http://www.youtube.com/watch?v=bocF6P74T9E> (Wideband DPD)

## Webcasts

*“High Performance Digital Pre-Distortion (DPD) for Wideband Systems” (Sept 2011)*

<http://www.home.agilent.com/agilent/eventDetail.jspx?ckey=2021229&pid=1475688&nid=-34360.0&lc=eng>

*“4G For Everyone: Extended RF Performance with DPD” (June 2010)*

<http://www.home.agilent.com/agilent/eventDetail.jspx?cc=US&lc=eng&ckey=1842093&nid=-11143.0.00&id=1842093>

# Q&A

