InterDigital®

Smart Technologies™

A Direct Conversion, All Digital Gain Control Radio Receiver Suitable For User Equipment Applications

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Abbreviations

- DC-AAGC: Direct conversion, all analog gain control
- DC-ADGC: Direct conversion, all digital gain control receiver.
- EP-DC-ADGC: Enhanced performance, direct conversion, all digital gain control receiver
- RC-DC-ADGC: Reduced complexity, direct conversion, all digital gain control receiver.
- IP3: Third order intercept point
- IIP3: Input referred IP3
- IP2: Second order intercept point
- IIP2: Input referred IP2
- ACS: Adjacent channel selectivity
- SFDR: Spurious free dynamic range
- WCDMA: Wideband CDMA
- TDD: Time division duplex
- FDD: Frequency division duplex
- RRC: Root raised cosine
- UE: User equipment
- LNA: Low noise amplifier
- AGC: Automatic gain control
- NF : noise figure (dB)
- G_p : Processing gain
- E_b/N_t : Signal to noise and interference ration
- ESL: Effective sensitivity level, 10log(KT*BW*NF)
- IMD: Inter modulation distortion

Outline

- Emerging standards and UE receiver design challenges
  - UE receiver design challenges associated with popular standards
  - Features of the DC-ADGC receiver that meet these design challenges
- Introduction
  - A brief description of the DC-ADGC receiver
  - A brief description of the benchmark receiver
  - Common front end requirements
- DC-ADGC receiver theory of operation
  - Derivation of back end IP3 and measured results
  - Derivation of back end noise figure
  - Derivation of the receiver SFDR
  - Trading SFDR for analog selectivity
- Performance comparison
  - SFDR
  - AGC Complexity Comparison
  - Enhancements for a closed loop AGC scheme
- Conclusions

Market Trends, Emerging Standards and UE Receiver Design Challenges

Mobile Communications Market Trends

- WCDMA TDD
  - Time Division Duplexing, built on a packet switched network and must support high mobility (velocity exceeding 120km/h) users.
- WCDMA FDD HSDPA
  - High speed downlink packet access. The base station, upon receiving a request downloads large volumes of digital multimedia data in short bursts to the user equipment.

Mobile Communications Market Trends

- Other Present & Future Generation (3G, 4G, etc.) Systems
  - Completely built on packet-switched networks.
  - Will have to support time multiplexed data traffic.
  - Will have to support high data rate (20Mbps) traffic.
  - Will have to support high mobility (velocity up to 250km/h) users.

UE Receiver Design Challenges

- In the case of burst packet reception, or a high mobility scenario (fast fading channel) the UE receiver AGC will have to handle large instantaneous jumps in received power.

- In the case of Time Division Duplex (TDD) systems the receiver AGC will have to handle large variations in received power from one timeslot to another.

UE Receiver Design Challenges

- Due to spectrum congestion, often different standards are deployed in frequency bands adjacent to one another. Therefore, modern UE receivers must be able to tolerate higher interferer power levels for a given adjacent channel selectivity.

Features of the DC-ADGC Receiver

- Employs an open loop, low latency, all digital gain control mechanism and avoids stability, settling time and overshoot issues associated with a closed loop AGC.
- Delivers a large instantaneous dynamic range with no radio adjustments required by employing a logarithmic amplifier in the analog baseband and a low latency, all digital gain control mechanism.
- Simultaneously delivers high IP3 and good noise figure.
- Delivers superior spurious free performance at high interferer power levels.

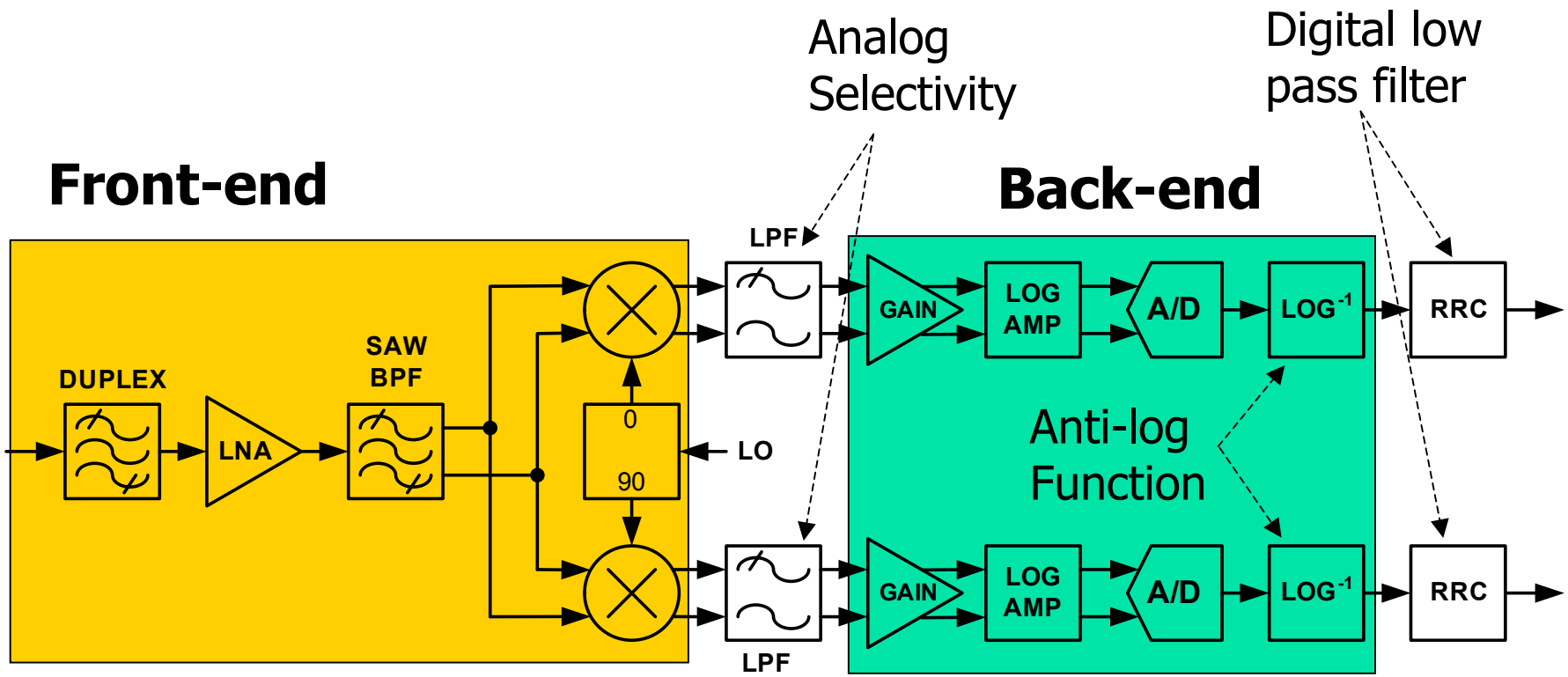
Introduction

DC-ADGC Receiver

- The receiver front-end employs a direct conversion architecture.
- The receiver employs a logarithmic amplifier in the analog baseband to compress the incoming signal before the analog to digital converter. As a result, the DC-ADGC receiver is able to deliver a large instantaneous dynamic range.
- The enhanced performance implementation of the DC-ADGC receiver employs a digital anti-log function and the reduced complexity version omits the digital anti-log function.
- A simple, low latency, all digital received power normalizer is used in place of a complex AGC loop.

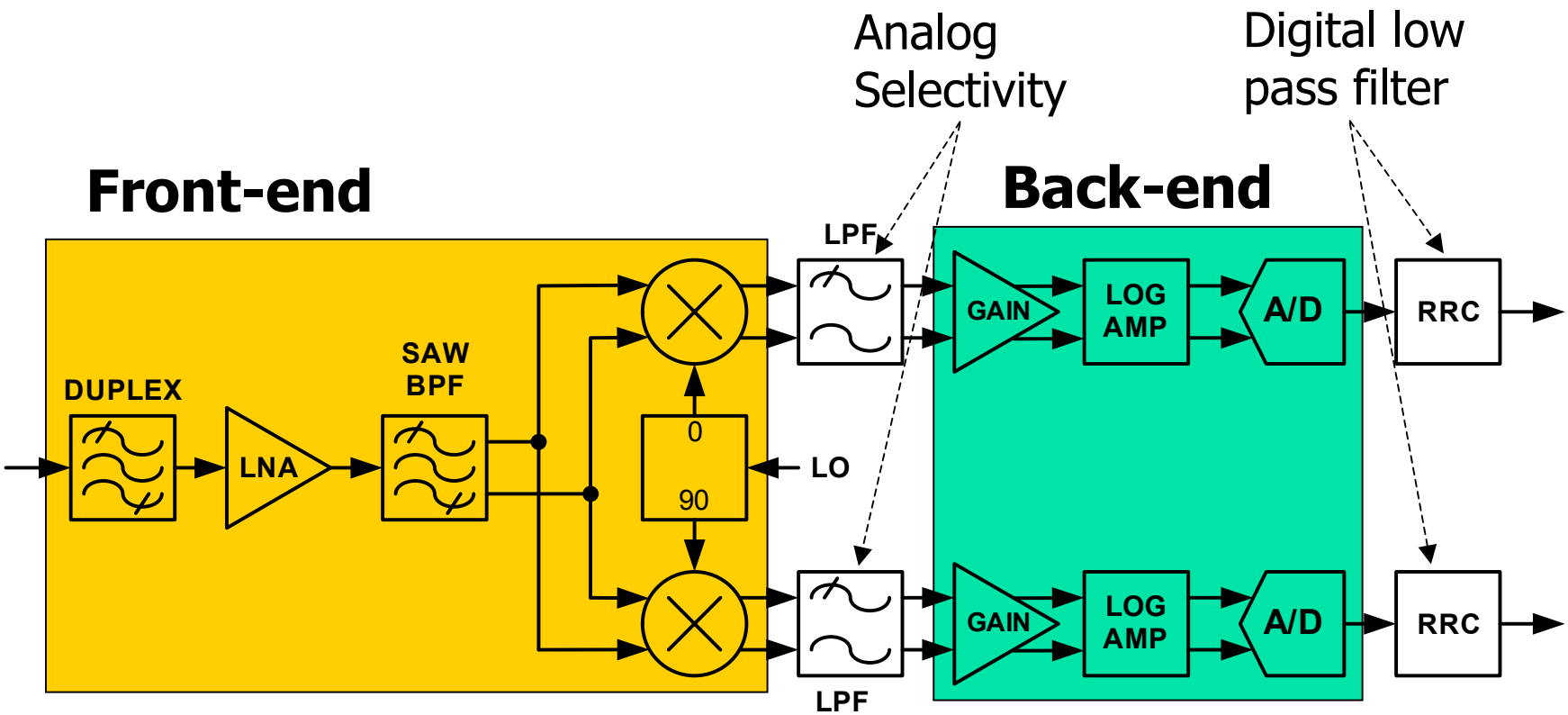
DC-ADGC Receiver

Enhanced Performance Implementation



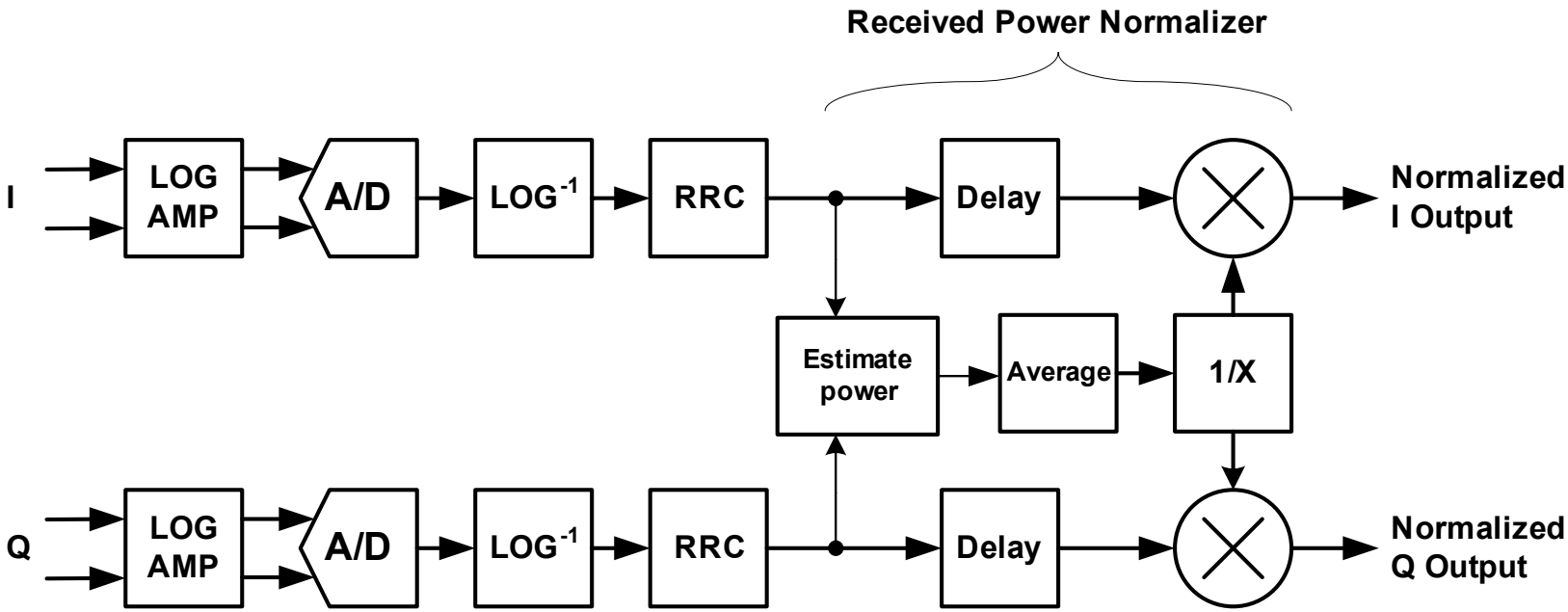
DC-ADGC Receiver

Reduced Complexity Implementation



DC-ADGC Receiver Backend

Digital Gain Control Scheme

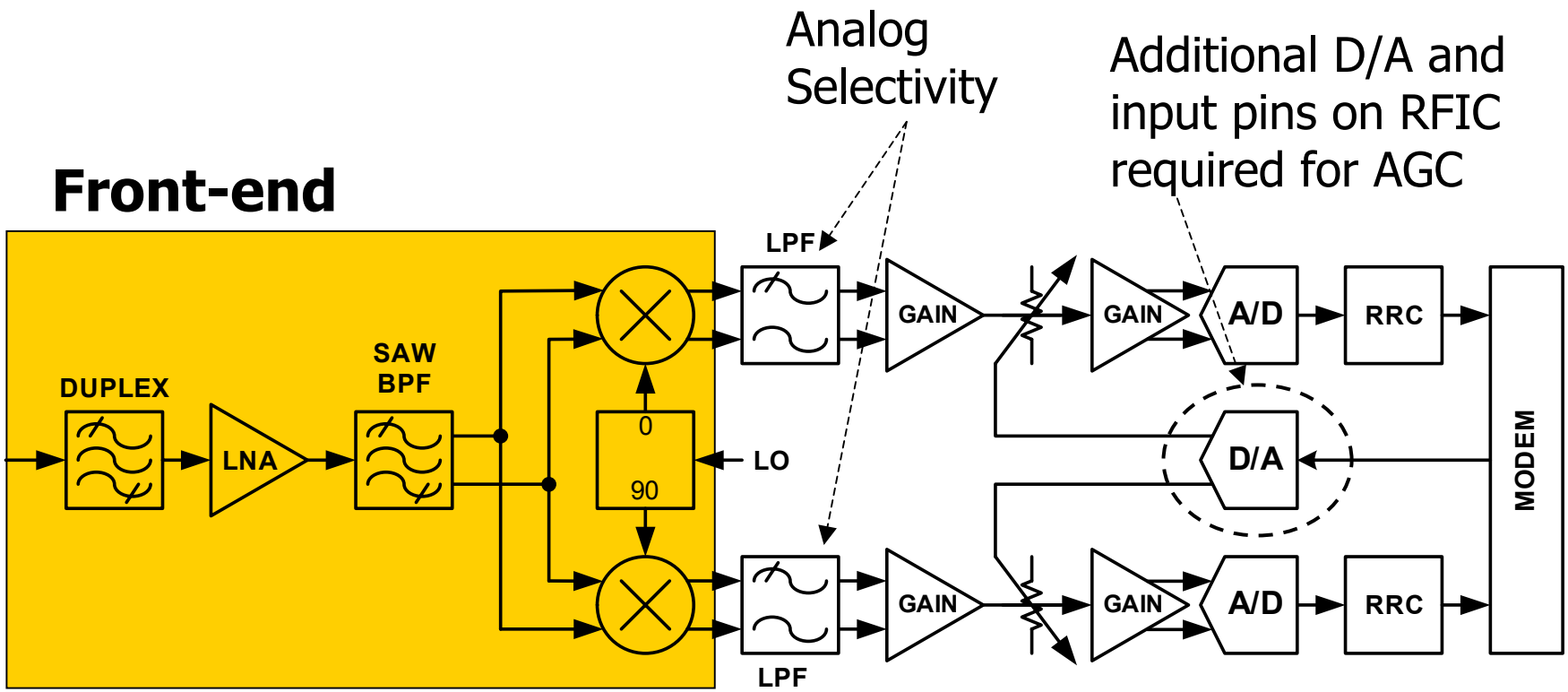


DC-AAGC Benchmark Receiver

- The receiver front-end employs a direct conversion architecture.
- The receiver employs variable gain amplifiers (attenuators) in the analog baseband to implement the AGC function.
- A feedback loop is employed to implement the AGC scheme.

DC-AAGC Benchmark Receiver

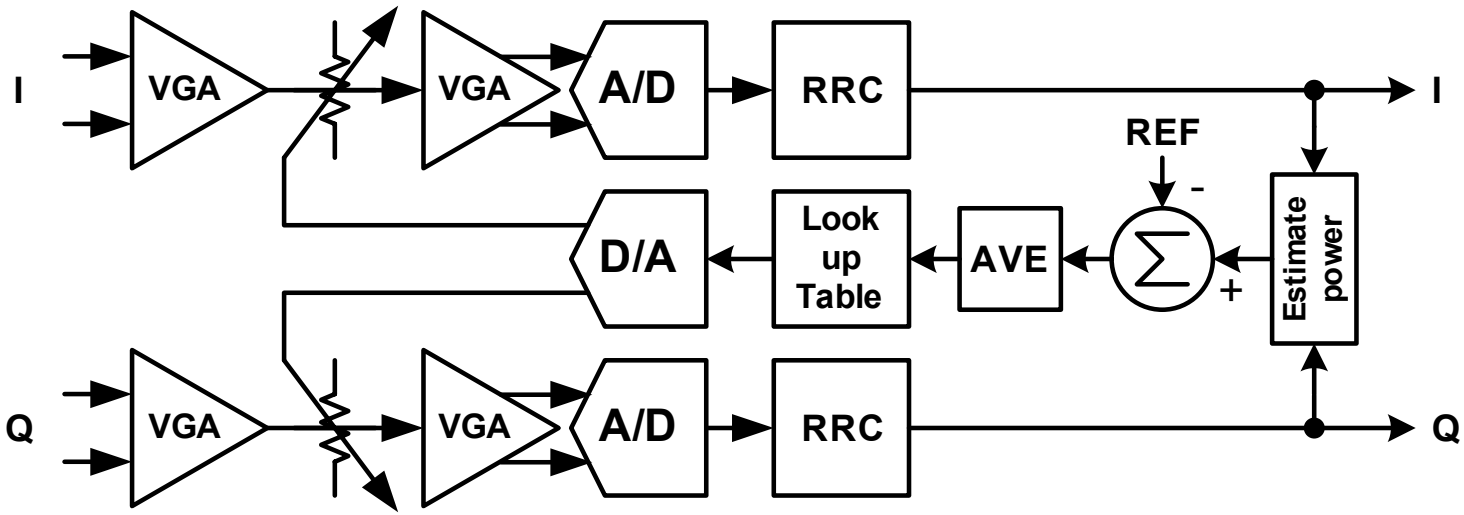
Direct Conversion with Analog Gain Control



DC-AAGC Receiver

Closed Loop, Automatic Gain Control Scheme

- Loop stability, settling time, overshoot, etc. are of concern.
- Trade off is made between NF and IP3.



Performance Comparison Rules and Criteria

- The DC-AAGC receiver is used as benchmark for performance comparisons.
- Measures like IP3, NF and SFDR are used as performance gauges.
- All receivers under consideration are assumed to employ the same front-end (LNA, down converter).
- All receivers employ the same number of bits in the analog to digital converters.
- All receivers employ digital RRC filters with the same ACS and ultimate rejection.
- All receivers employ a fully differential analog baseband.

Front-end Requirements
Derived from 3GPP WCDMA-FDD Standards

- Receiver front-end requirements are derived from the 3GPP WCDMA FDD standards.
- The following assumptions are made in deriving the front-end requirements:
  - Processing Gain = 25 dB
  - Required Signal to Noise and Interference ratio = 7 dB

Receiver Parameter	Required Performance
Receiver total NF	< 9 dB
Front-end NF	4 ~ 6 dB
Front-end IIP3	> -17 dBm
Front-end IIP2	> +10 dBm
ACS	> 33 dB
1st alternate channel selectivity	> 45 dB
2nd alternate channel selectivity	> 57 dB

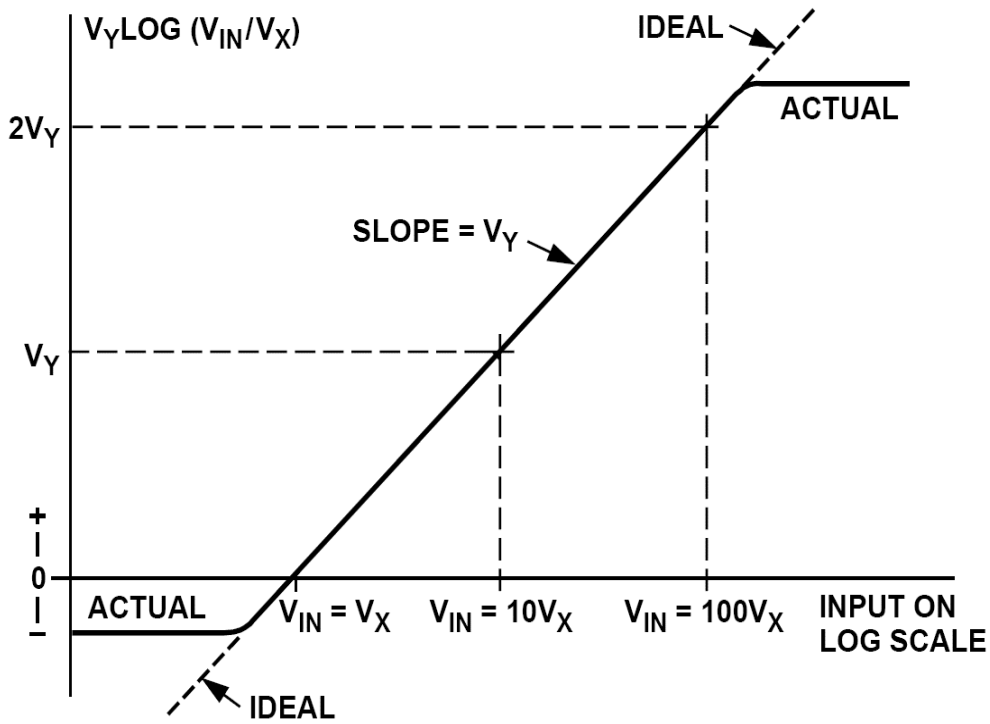
DC-ADGC Receiver Theory of Operation

A Typical Logarithmic Amplifier Transfer Function

$$V_{OUT} = V_Y \log_{10}\left(\frac{V_{IN}}{V_X}\right)$$

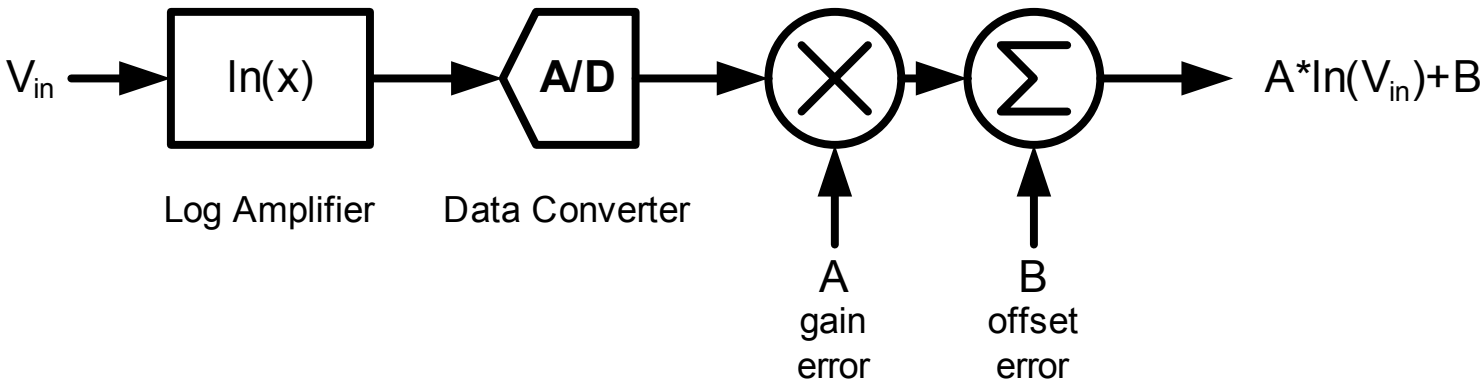
Analog Devices AD641

- V_Y: slope voltage
- V_X: intercept voltage
- Input domain: $1<(V_{IN}/V_X)<10^N$
- Output range: $0<V_{OUT}<V_Y*N$



Reduced Complexity DC-ADGC Receiver

Backend IIP3 Derivation



- The logarithmic amplifier and the data converter are assumed ideal. All sources of gain and offset error are applied to points A and B.
- Both A and B may vary with the input level. It is assumed that the input signal range may be divided into a finite number of small enough sections within which A and B remain constant.

Reduced Complexity DC-ADGC Receiver

Backend IIP3 Derivation

$$V_{OUT,Backend} = A\ln(V_{in}) + B = \alpha_0 + \alpha_1 V_{in} + \alpha_2 V_{in}^{\ 2} + \alpha_3 V_{in}^{\ 3} + \ldots$$

Taylor series expansion around $\overline{V_{in}}$

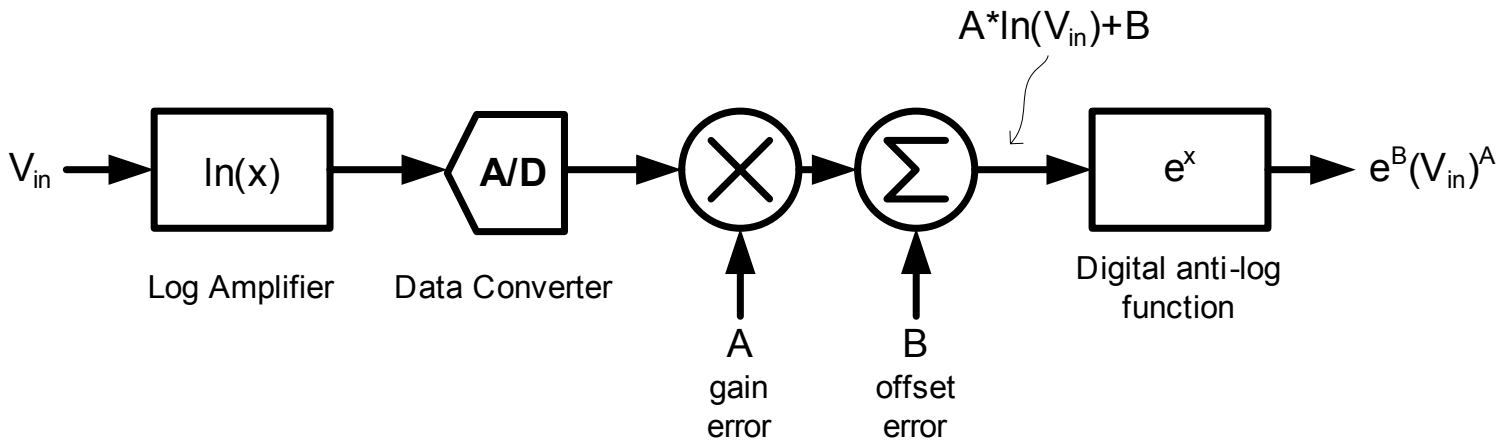
$$V_{OUT,Backend} = A\{\ln(\overline{V_{in}}) + \frac{(V_{in} - \overline{V_{in}})}{\overline{V_{in}}} - \frac{(V_{in} - \overline{V_{in}})^2}{2\overline{V_{in}}^2} + \frac{(V_{in} - \overline{V_{in}})^3}{3\overline{V_{in}}^3} - \frac{(V_{in} - \overline{V_{in}})^4}{4\overline{V_{in}}^4} + \ldots\} + B$$

$$\alpha_1 = \frac{4A}{\overline{V_{in}}}, \alpha_3 = \frac{4A}{3(\overline{V_{in}})^3}, IIP3 = 20\log_{10}\sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|}$$

$$IIP3_{RC-DC-ADGC} = 10\log_{10}(4) + 10\log_{10}(V_{in})^2$$

Enhanced Performance DC-ADGC Rx

Backend IIP3 Derivation



- The DC offset, B is removed by the digital gain normalizer and therefore B is set equal to zero. A signifies a gain mismatch and is bounded in the following manner.

  $(1-r)<A<(1+r)$ where $|r|<1$

- The quantity |A-1| signifies the percentage gain mismatch between the log amplifier transfer function and the digital antilog transfer function.

Enhanced Performance DC-ADGC Rx

Backend IIP3 Derivation

- The primary source of 3rd order distortion in the backend is assumed to be the gain mismatch between the log amplifier transfer function and the digital antilog transfer function.
- It will be shown that the IIP3 of the backend is a function of the gain mismatch (|A-1|) between the log amplifier transfer function and the digital anti-log transfer function.

Enhanced Performance DC-ADGC Rx

Backend IIP3 Derivation

$$(V_{in})^A = \alpha_0 + \alpha_1 V_{in} + \alpha_2 V_{in}{}^2 + \alpha_3 V_{in}{}^3 + \ldots$$

The Taylor Series expansion around $\overline{V_{in}}$

$$f(V_{in}) = (V_{in})^A = f(\overline{V_{in}}) + f^{(1)}(\overline{V_{in}})(V_{in} - \overline{V_{in}}) + f^{(2)}(\overline{V_{in}})\frac{(V_{in} - \overline{V_{in}})^2}{2} + f^{(3)}(\overline{V_{in}})\frac{(V_{in} - \overline{V_{in}})^3}{3!} + \ldots$$

$$\alpha_0 = (\overline{V_{in}})^A\left[1 - A + \frac{A(A-1)}{2} - \frac{A(A-1)(A-2)}{3!} + \frac{A(A-1)(A-2)(A-3)}{4!} - \ldots\right]$$

$$\alpha_1 = (\overline{V_{in}})^A \frac{A}{\overline{V_{in}}}\left[1 - (A-1) + \frac{(A-1)(A-2)}{2} - \frac{(A-1)(A-2)(A-3)}{3!} + \ldots\right]$$

$$\alpha_2 = (\overline{V_{in}})^A \frac{A(A-1)}{2\overline{V_{in}}^2}\left[1 - (A-2) + \frac{(A-1)(A-2)}{2} - \ldots\right]$$

$$\alpha_3 = (\overline{V_{in}})^A \frac{A(A-1)(A-2)}{(3!)\overline{V_{in}}^3}\left[1 - (A-3) + \ldots\right]$$

Enhanced Performance DC-ADGC Rx

Backend IIP3 Derivation

$$IIP3 = 20\log_{10}\sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|}$$

The following simplification is made based on the assumption that A is close to 1:

$$\left|\frac{\alpha_1}{\alpha_3}\right| = 2(V_{in})^2\frac{[1-\frac{11}{6}(A-1)]}{(A-1)} \approx \frac{2V_{in}^{\ 2}}{(A-1)}$$

$$IIP3_{EP-DC-ADGC} = 10\log_{10}(4) + 10\log_{10}(V_{in})^2 - 10\log_{10}(\frac{3}{2}|A-1|)$$

$$IIP3_{EP-DC-ADGC} = IIP3_{RC-DC-ADGC} - 10\log_{10}(\frac{3}{2}|A-1|)$$

DC-ADGC Receiver Backend IIP3

Reduced Complexity DC-ADGC Receiver:

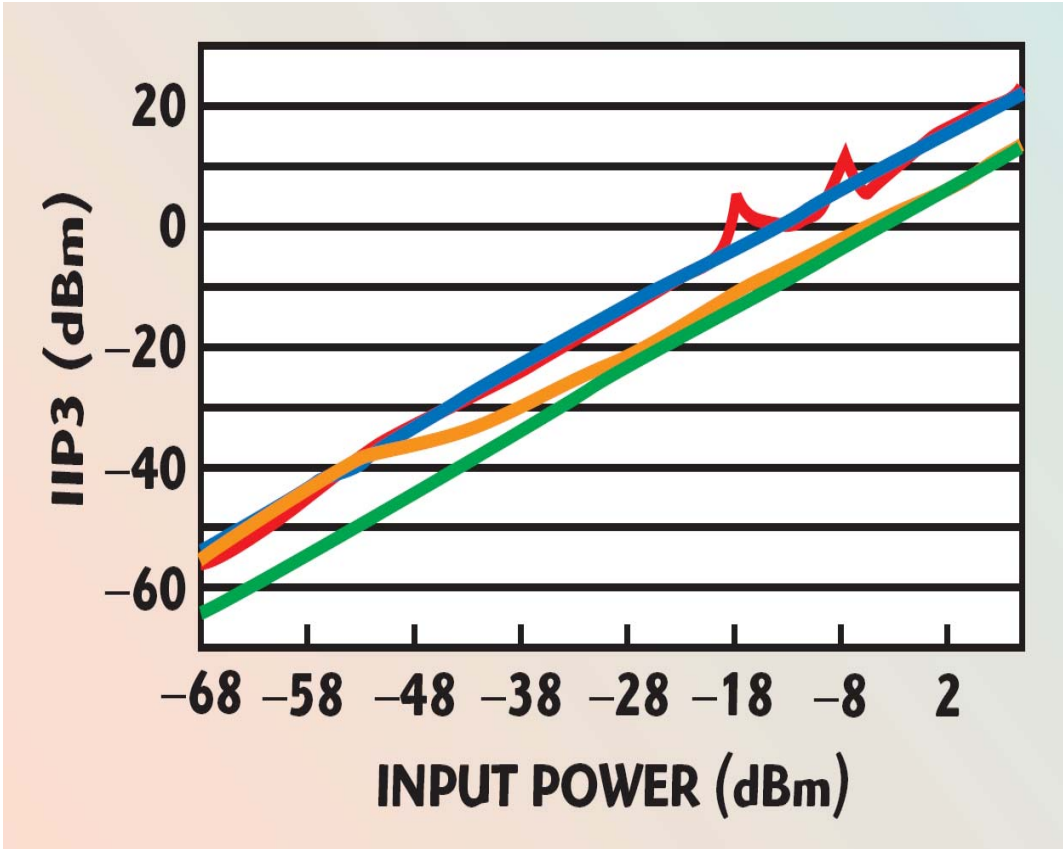
$$IIP3_{RC-DC-ADGC} = 10\log_{10}(4) + 10\log_{10}(V_{in})^2$$

Enhanced Performance DC-ADGC Receiver:

$$IIP3_{EP-DC-ADGC} = IIP3_{RC-DC-ADGC} - 10\log_{10}(\frac{3}{2}|A-1|)$$

DC-ADGC Receiver Backend IIP3
Predicted and Measured

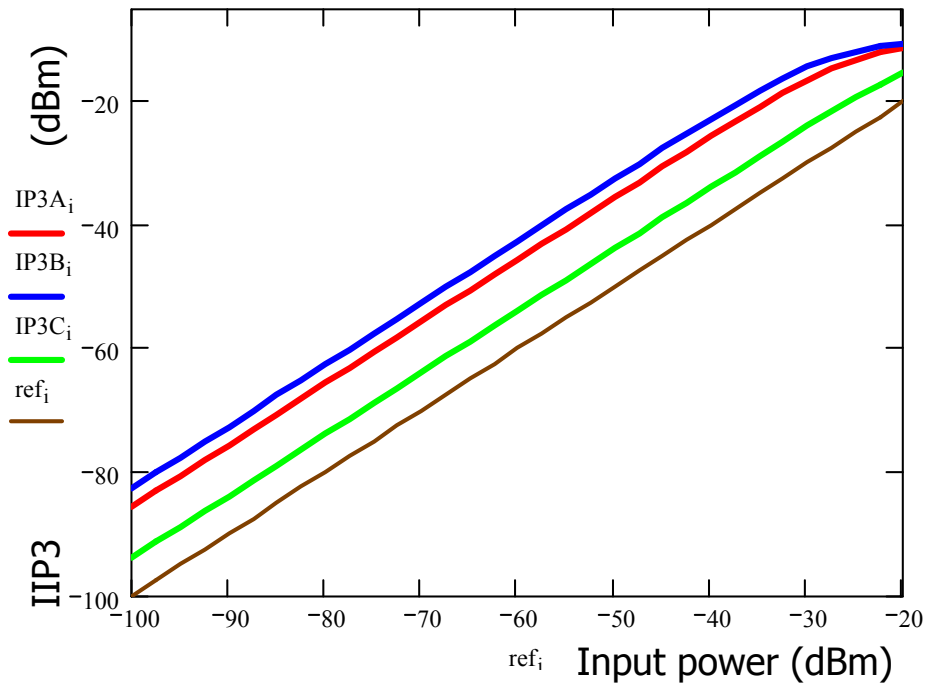
- Predicted EP-DC-ADGC receiver backend IIP3, 10% mismatch: |A-1|=0.1
- Predicted RC-DC-ADGC receiver backend IIP3, no digital antilog function
- Measured EP-DC-ADGC receiver backend IIP3, 10% mismatch: |A-1|=0.1
- Measured RC-DC-ADGC receiver backend IIP3, no digital antilog function



DC-ADGC Receiver (FE+BE) IIP3

$$\frac{1}{IIP3^2} = \frac{1}{IIP3_{FE}{}^2} + \frac{\alpha_{FE}{}^2}{IIP3_{BE}{}^2}$$

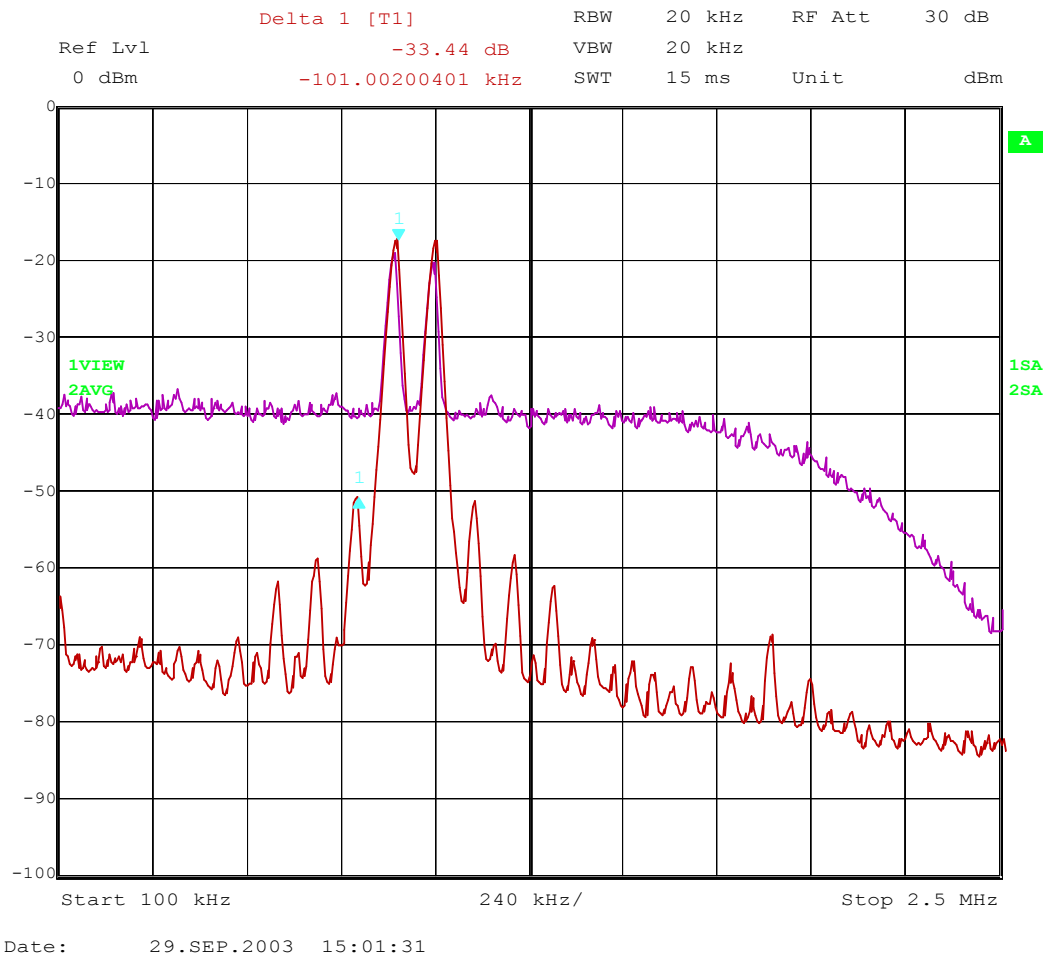
- EP-DC-ADGC Rx IIP3, 5% mismatch
- EP-DC-ADGC Rx IIP3, 10% mismatch
- RC-DC-ADGC Rx IIP3, no antilog function
- Reference line (input power)



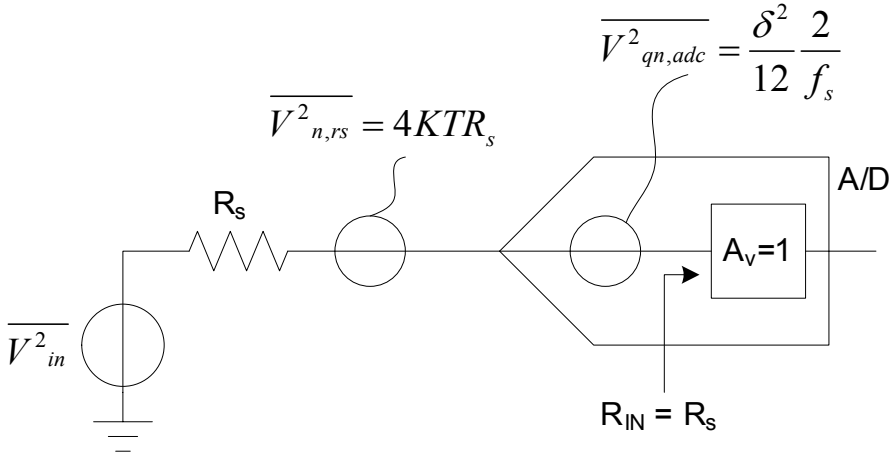
DC-ADGC Receiver IP3 Performance

(More than 60dB spurious free dynamic range demonstrated)

- |A-1|=0.1, 10% mismatch, IIP3 = input power+15dB, 3RD order IMD terms -30dBc over an input power range of 60dB.
- The combination of a logarithmic amplifier at analog baseband, and a low latency digital power normalizer, enables the receiver to follow a 60dB instantaneous jump in received power with no radio adjustments.



DC-ADGC Receiver Backend NF Derivation
A/D Noise Figure



$f_s = 40MHz$

$\delta = \frac{1}{2^N}$

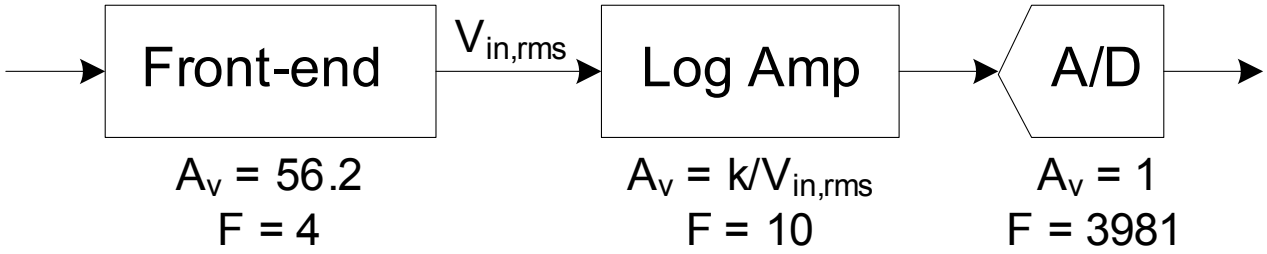
$N = 8$

$R_S = 1000$

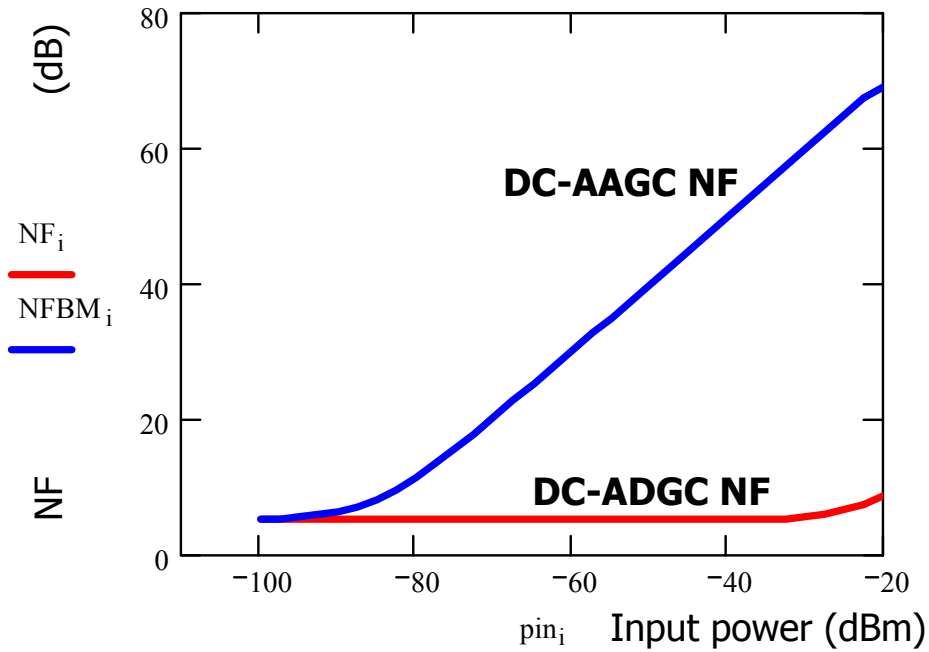
$$F = \frac{SNR_{IN}}{SNR_{OUT}} = 1 + \frac{\overline{V^2_{qn,adc}}}{4KTR_S} = 1 + \frac{\delta^2}{12}\frac{2}{f_S}\frac{1}{4KTR_S}$$

$$NF = 10\log_{10}(F) = 36dB$$

DC-ADGC Receiver Noise figure



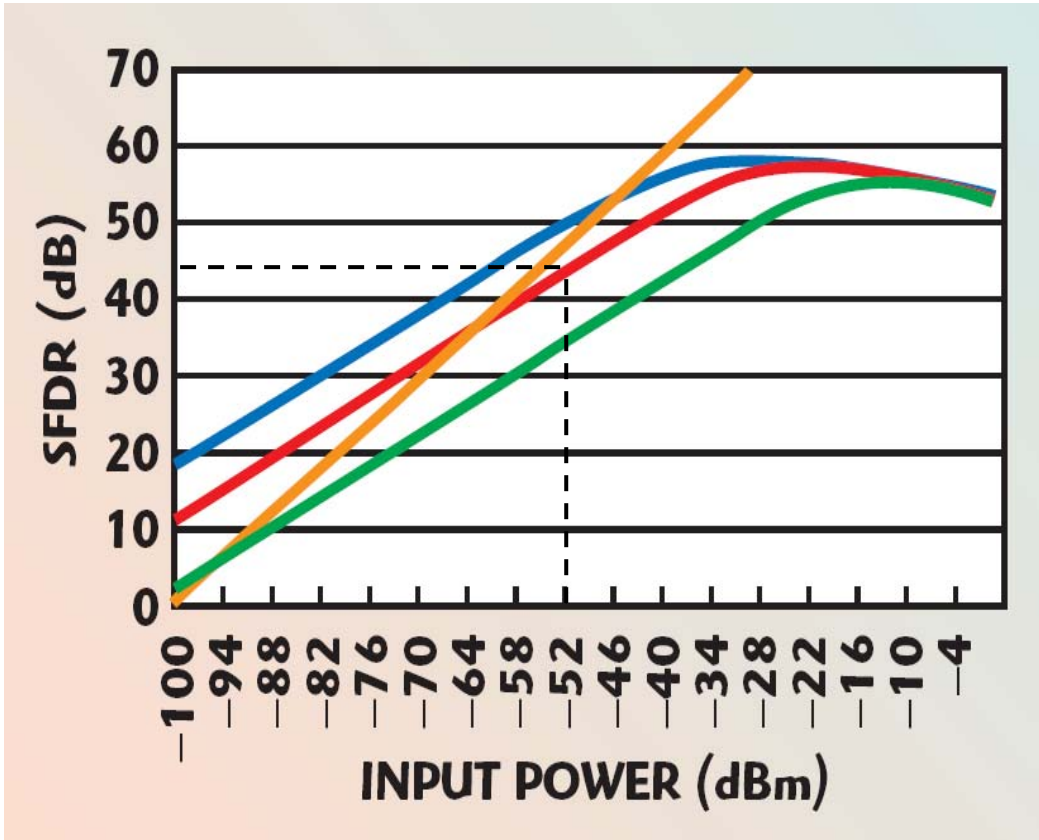
- DC-AAGC Rx NF (Backend + Frontend)
- DC-ADGC Rx NF (Backend + Frontend)



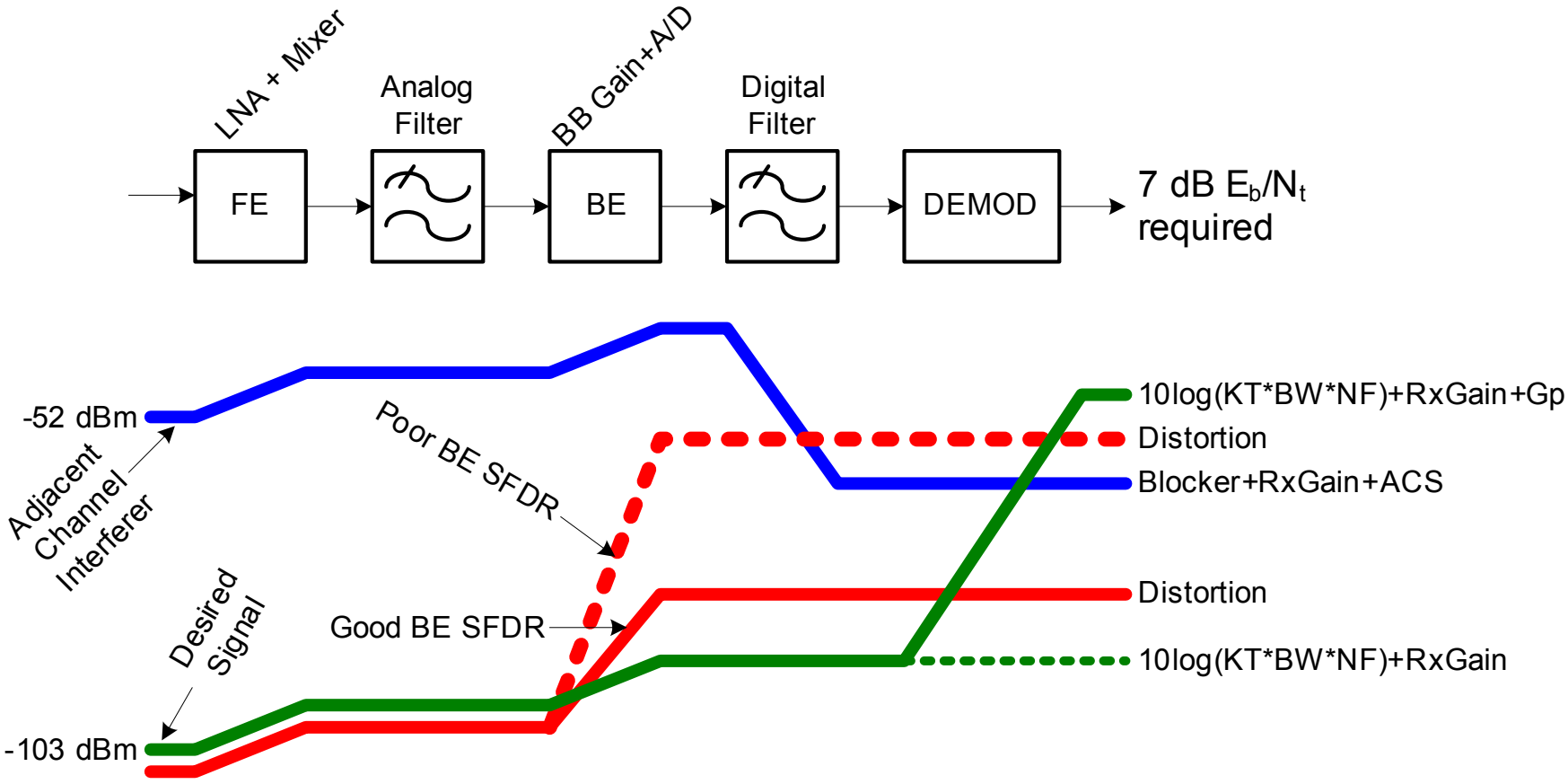
DC-ADGC Receiver SFDR

$$SFDR = \frac{2}{3}[IIP3 - NF - 10\log(KT) - 10\log(BW)]$$

- EP-DC-ADGC Rx SFDR, |A-1|=0.005 0.5% mismatch
- EP-DC-ADGC Rx SFDR, |A-1|=0.05 5% mismatch
- RC-DC-ADGC Rx SFDR, no antilog function
- Reference line, unity slope on log-log scale

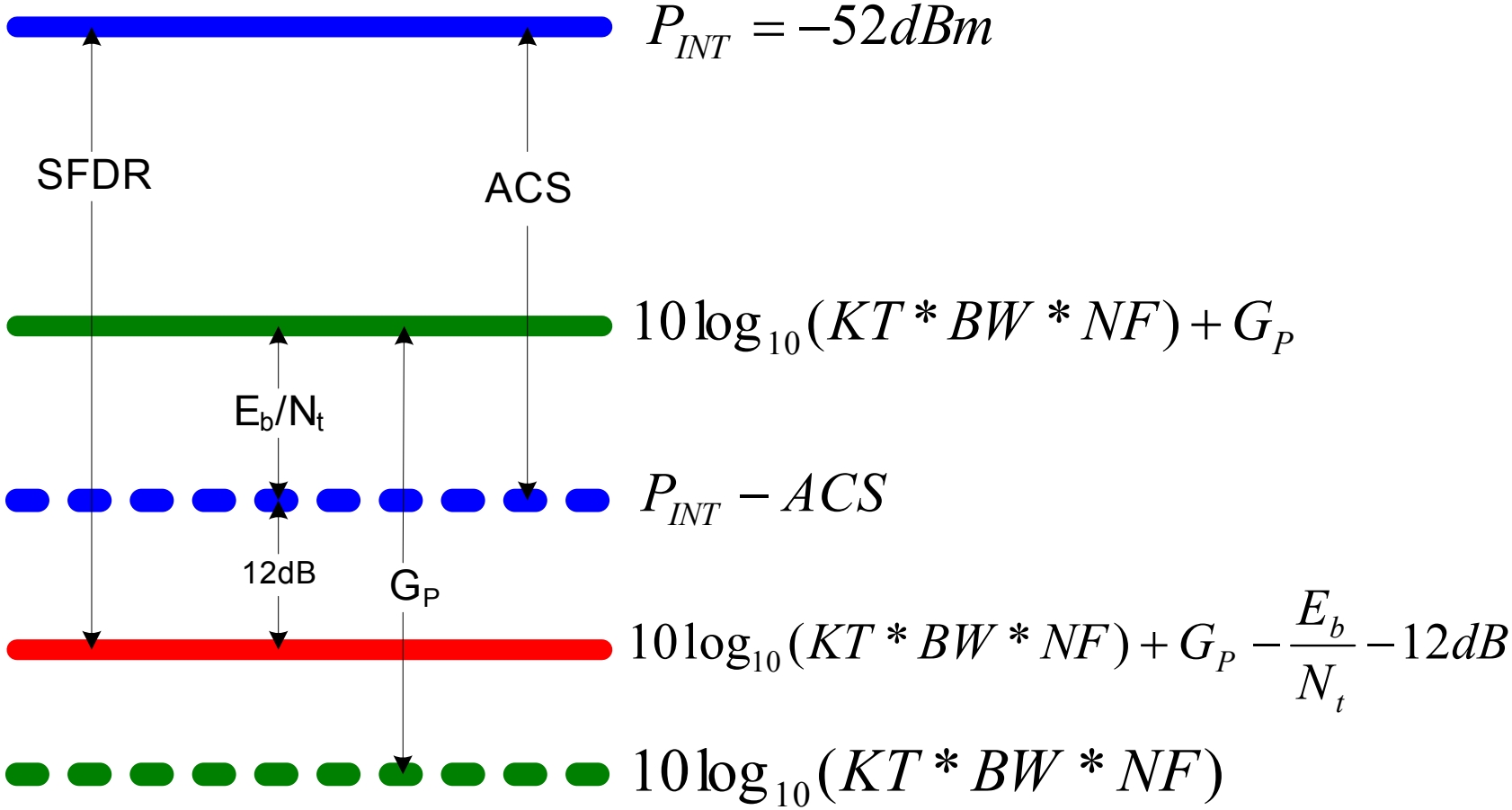


Receiver Analog Selectivity Requirement



Receiver Signal Level Diagram

Receiver Analog Selectivity Requirement



Input Referred Receiver Signal Level Diagram

Trading SFDR for Analog Selectivity (DC-ADGC Receiver)

$$IIP3_{RX} = P_{IN,RX} + 10\log_{10}(4) - 10\log_{10}\left|\frac{3}{2}(A-1)\right|$$

$$SFDR(P_{INT}) = \frac{2}{3}[IIP3(P_{INT}) - 10\log_{10}(KT * BW * NF)]$$

$$P_{DIST} = P_{INT} - SFDR(P_{INT})$$

$$ESL + G_P - \frac{E_b}{N_t} - 12dB = ESL + 6dB = P_{INT*} - SFDR(P_{INT*})$$

$$(P_{INT} - P_{INT*}) = 3[P_{DIST} - (ESL + 6dB)]$$

Trading SFDR for Analog Selectivity
(DC-ADGC Receiver)

$$ACS = 3[P_{DIST} - (ESL + 6dB)]$$

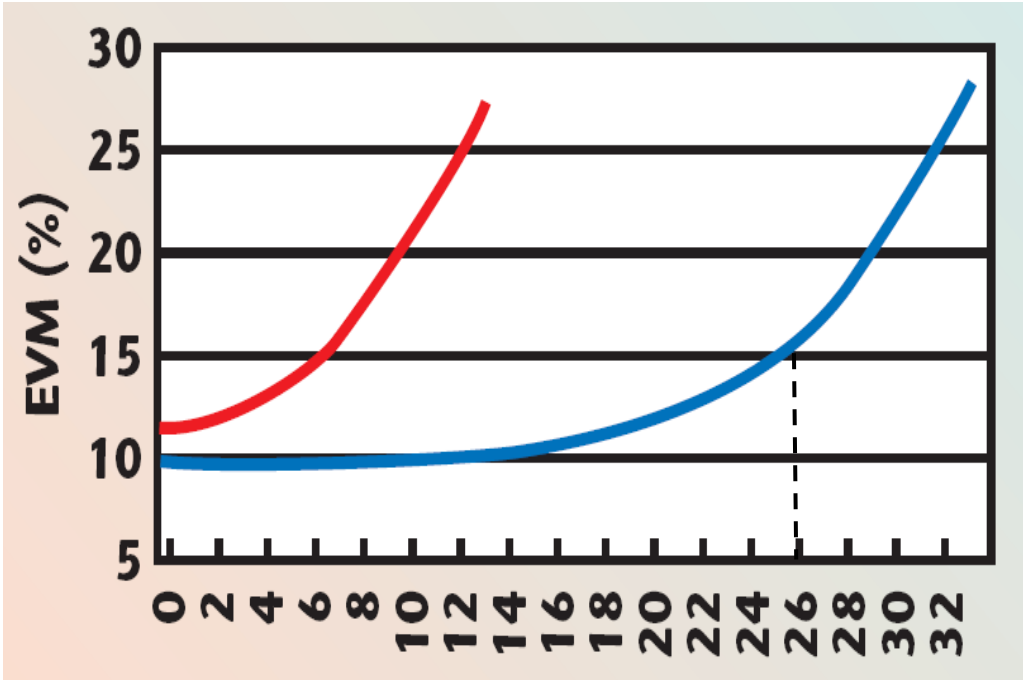
Log-Antilog Mismatch%	DC-ADGC RX SFDR	Distortion Level	Required ACS
(No Anti-log function)	36 dB	-88 dBm	27 dB
10%	41 dB	-93 dBm	12 dB
5%	43 dB	-95 dBm	6 dB
2.5%	45 dB	-97 dBm	0 dB

DC-ADGC Receiver EVM vs Interferer Power

Test Scenario:

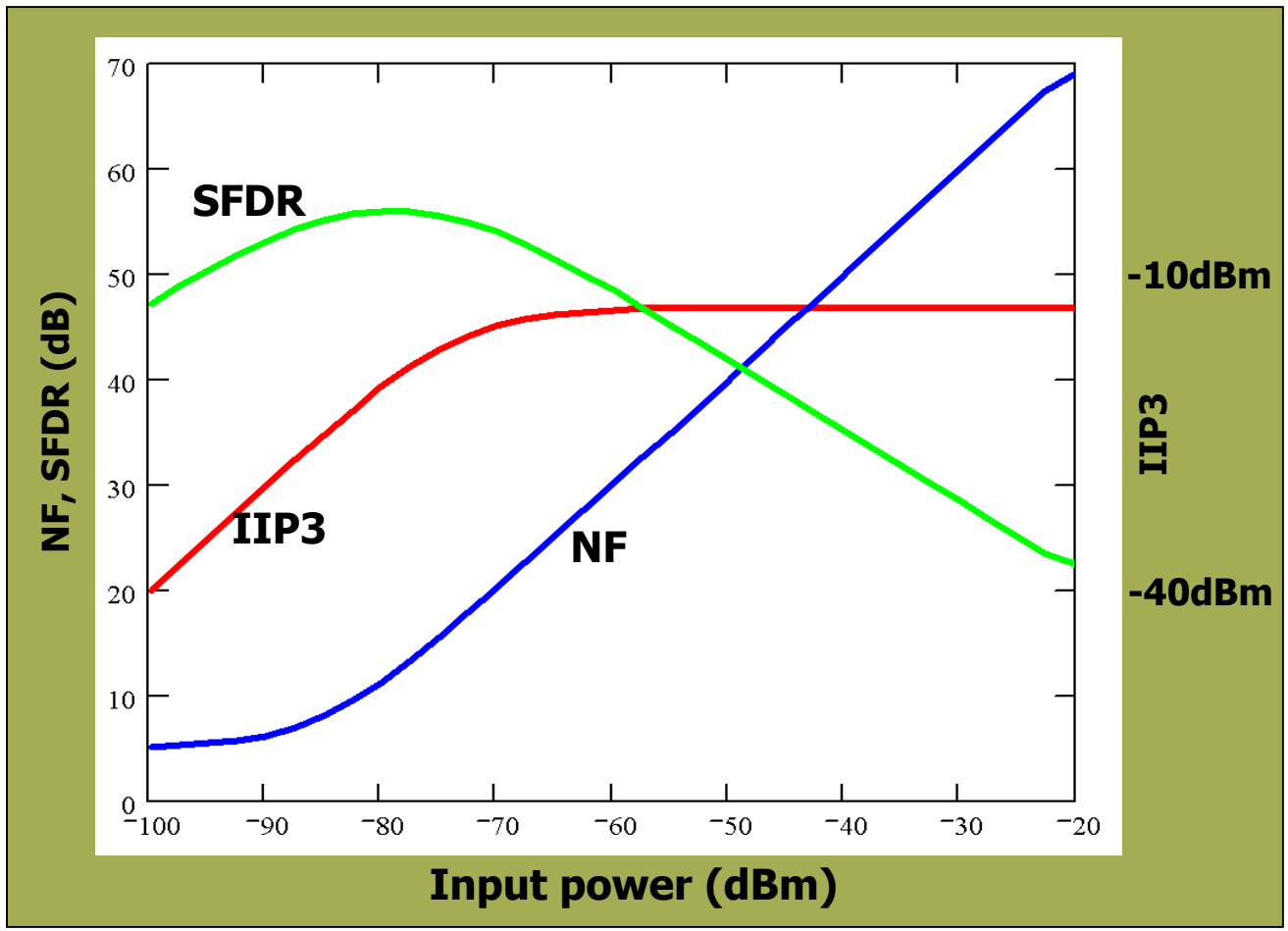
Analog selectivity: linear phase low pass filter, ACS < 6dB
Received signal: 1 code, forward link, FDD-WCDMA
Adjacent Channel Interferer: 2 code, FDD-WCDMA

- Enhanced Performance DC-ADGC Rx EVM (as a function of blocker power), |A-1|=0.1
  10% mismatch
- Reduced Complexity DC-ADGC Rx EVM (as a function of blocker power), no antilog function



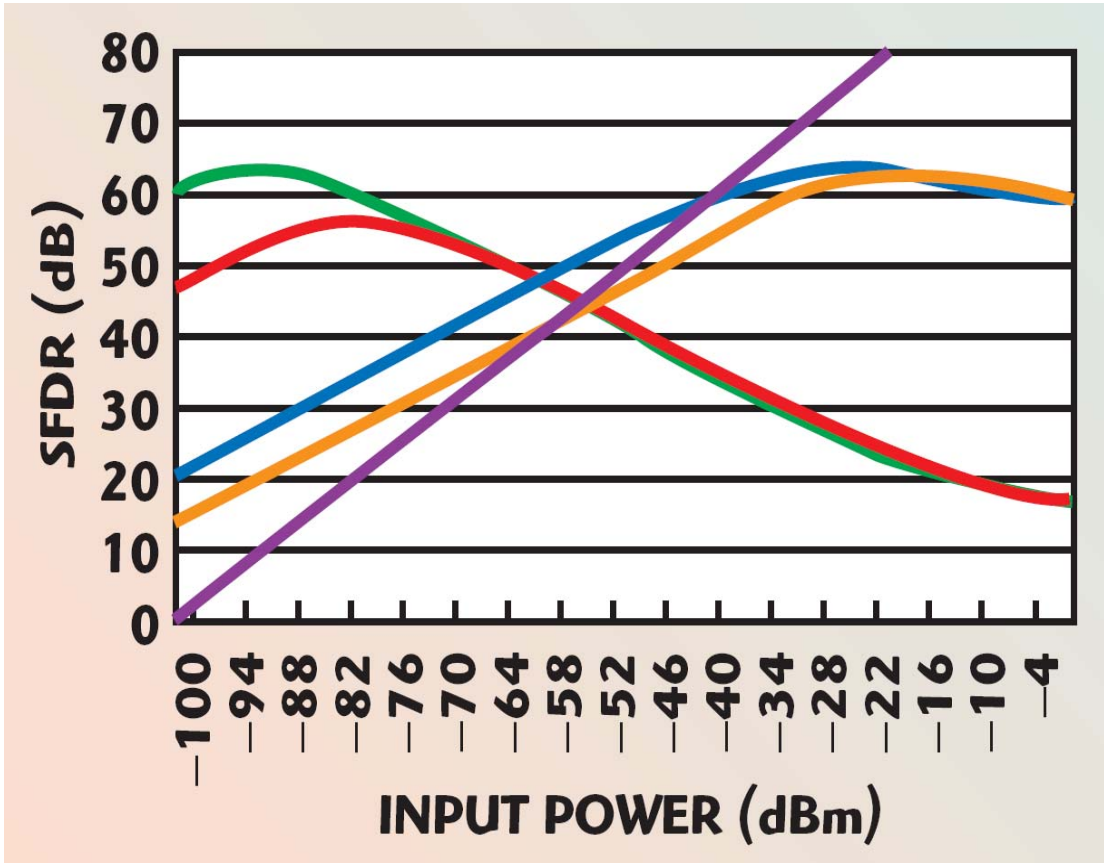
A Performance Comparison:
DC-ADGC vs DC-AAGC

DC-AAGC (Benchmark) Receiver NF, IP3 and SFDR



DC-ADGC and the DC-AAGC (Benchmark) Receiver SFDR Comparison

- EP-DC-ADGC Rx SFDR, |A-1|=0.005 0.5% mismatch
- EP-DC-ADGC Rx SFDR, |A-1|=0.05 5% mismatch
- Benchmark receiver with high IP3 final baseband stage
- Benchmark receiver with poor IP3 final baseband stage
- Reference line



DC-AAGC (Benchmark) Receiver Properties

- The IP3 at low power levels is determined by the final baseband stage IP3.
- The IP3 at high power levels is determined by the front-end IP3.
- The noise figure of the receiver increases with increasing signal power levels due to the AGC action.

∴ **The SFDR is limited by the final baseband stage IP3 at low input levels and begins to drop with increasing input power levels due to increasing noise figure caused by the AGC action.**

DC-ADGC (Benchmark) Receiver Properties

- The IP3 is low at low power levels, but increases with increasing input power.
- The IP3 at high power levels is determined by the front-end IP3.
- The noise figure remains relatively constant throughout the signal input power range.

∴ **The SFDR is delivered where it is needed – at high (blocker) power levels.**

∴ **Simultaneous delivery of noise figure and IP3 is possible.**

DC-ADGC and the DC-AAGC (Benchmark) Receiver AGC Complexity Comparison

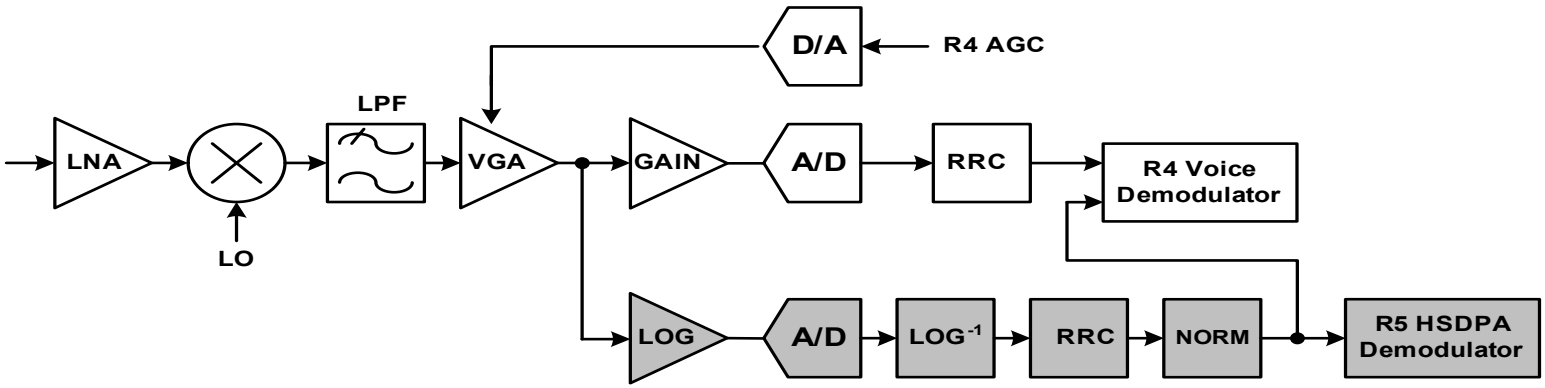
DC-ADGC Receiver Gain Control Mechanism	DC-AAGC Receiver Gain Control Mechanism
Open loop implementation	Complex closed loop implementation – stability, settling time, overshoot
Log amplifier and a low latency power normalizer is employed – can handle large instantaneous input power variations	Large loop settling time – does not respond to instantaneous input power variations and as a result A/D may saturate
No mixed signal components required to implement the gain control mechanism	Requires additional mixed signal components and input pins on the receiver IC to implement the gain control loop.

The 3GPP WCDMA-FDD Release 4 AGC

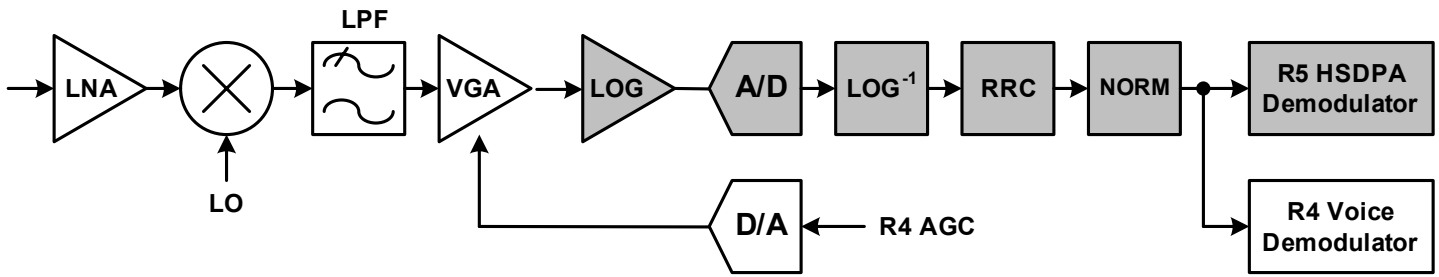
(Drawbacks of the Legacy Release 4 AGC approach)

- Closed loop AGC implementation suitable for circuit switched voice data reception. High loop settling time (typically from hundreds of microseconds to tens of milliseconds).
- 3GPP WCDMA-FDD R5 includes HSDPA (high speed downlink packet data access). Future FDD receiver must handle both R4 and R5.
- R4 AGC will not respond to packet data burst intended for the user or a neighboring UE receiver and as a result the receiver A/D may saturate.
- Commonly adopted remedy is to increase receiver overhead (increase number of bits on the A/D) or to design a fast (higher order) AGC.

Proposed FDD R4 AGC Enhancements Suitable for HSDPA



Add-on to Legacy R4 AGC



R4 AGC Redesigned for R4+R5 Operation

Conclusions

Important Features of the DC-ADGC Receiver

- The DC-ADGC receiver radio delivers a large instantaneous dynamic range by employing logarithmic amplifiers in the analog baseband.

- The DC-ADGC receiver automatic gain control function is implemented in its digital backend. A low latency, all digital gain normalizer is used. No AGC loop, analog variable gain amplifiers or gain control D/A converters are required.

Important Features of the DC-ADGC Receiver

- The combination of a radio with a large instantaneous dynamic range and a low latency, all digital gain normalizer allows the DC-ADGC receiver to handle large instantaneous variations in the received power.

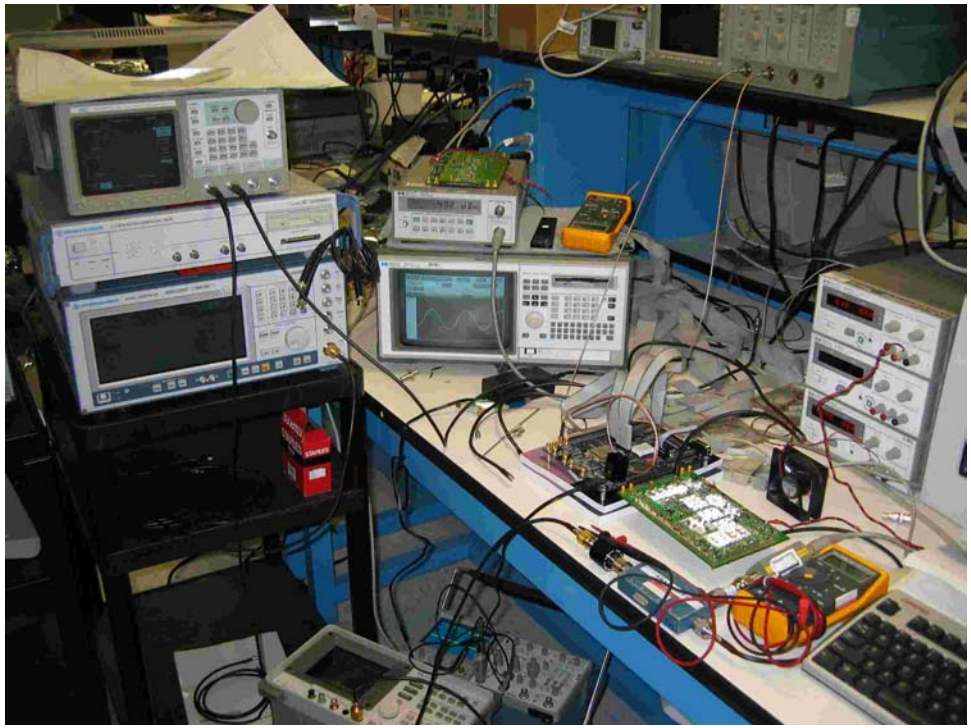
- The DC-ADGC receiver simultaneously delivers IP3 and noise figure performance. Therefore, superior SFDR performance is available large interferer power levels.

Important Features of the DC-ADGC Receiver

- The DC-ADGC receiver allows the designer to trade SFDR for Analog Selectivity by improving the gain mismatch between the logarithmic amplifier and the digital antilog function. In the case of a 2.5% maximum gain mismatch, the DC-ADGC receiver analog baseband need only provide the required 1st alternate channel selectivity.

DC-ADGC Receiver Development Platform

Hardware development platform



Hardware development bench

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List of References

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