GaN Power Amplifier Design
Presented to IEEE Long Island MTT Chapter
June 18, 2014

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GaN Power Amplifier Design

- **This lecture introduces attendees to the GaN transistor, its properties, various structures, including the latest GaN power amplifier (PA) design techniques.**
- **The properties of GaN will be presented showing the advantage of these devices over GaAs and Si. GaN HEMT transistors will be shown delineating the various geometries, semiconductor processes and structures with associated performance.**
- **Guidelines for reliable operation will be presented considering device junction temperature including thermal management techniques.**
- **The nonlinear models of GaN HEMT devices necessary for the CAD of PAs will be presented.**
- **Design considerations for both constant amplitude envelope signals as well as the non-constant amplitude envelope signals will be presented.**
- **Step-by-step design procedures will be shown for various GaN PA examples including different classes of operation as well as the popular Doherty PA.**

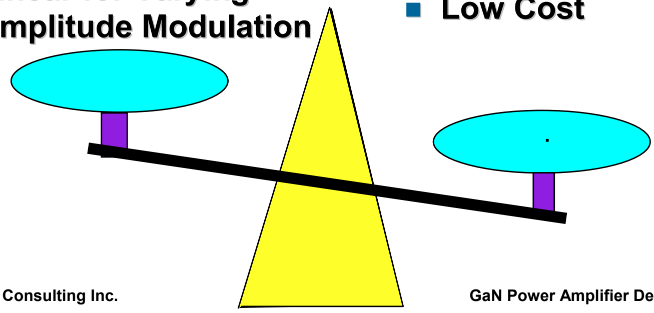
EDWARD C. NIEHENKE, Ph.D., PE, Consultant, Baltimore, Maryland, USA.

- Niehenke has pioneered the development of state-of-the-art RF, microwave, and millimeter wave components at Westinghouse/Northrop Grumman for 34 years. Circuits include low noise amplifiers, low noise oscillators, mixers, power amplifiers, phase shifters, attenuators, limiters, frequency multipliers, low-phase noise millimeter wave fiber optical links, and miniature integrated assemblies and subsystems. He previously worked in cryogenic electronics research at Martin-Marietta. He now consults and lectures on linear/nonlinear and wireless transmit/receive circuits and systems. Since 1983 he lectured to over 3000 professionals throughout the world for Besser Associates and the Continuing Education of Europe. He holds nine patents, one George Westinghouse Innovation Award, and has authored numerous papers on RF, microwave, and millimeter wave circuits.
- Niehenke is active in IEEE MTT-S activities serving on three technical committees and is their Ombudsman . He was technical program chair of the 1998 IMS, chair 1986 IMS, 1986/87 IEEE Distinguished Microwave Lecturer, and served as a member of ADCOM for 9 years Niehenke taught electricity and magnetism for 3 years at Johns Hopkins University. He was a recipient of the IEEE Centennial and Millennium Medals, is a fellow of the IEEE, and is a registered professional engineer in the State of Maryland.

What is Important for a Power Amplifier

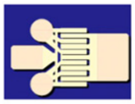
- High Power
- High Efficiency
- High Reliability
- Good Frequency Range
- Non Complex Matching with wide bandwidth
- Linear for Varying Amplitude Modulation

- Low Cost

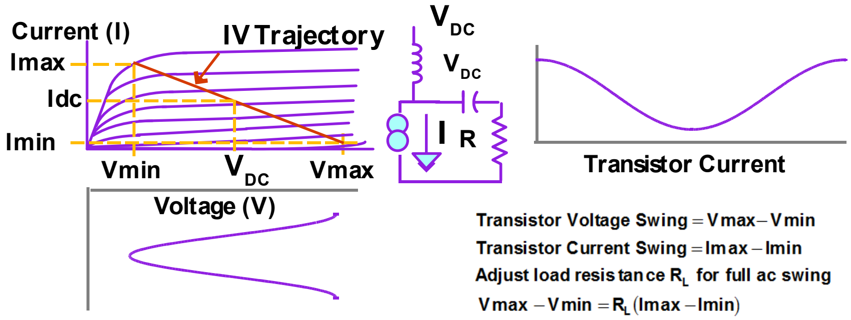


Lets Examine a Transistor

- To see to see what parameters are important
  - For Output Power
  - For Efficiency



Power and Efficiency Class A



Transistor Voltage Swing = Vmax − Vmin

Transistor Current Swing = Imax − Imin

Adjust load resistance R_L for full ac swing

$$V\max - V\min = R_L(I\max - I\min)$$

$$R_L = \frac{V\max - V\min}{(I\max - I\min)}$$

$$V_{DC} = \frac{V\max + V\min}{2}; \quad I_{DC} = \frac{I\max + I\min}{2}$$

$$P_{DC} = \frac{(V\max + V\min)(I\max + I\min)}{4}$$

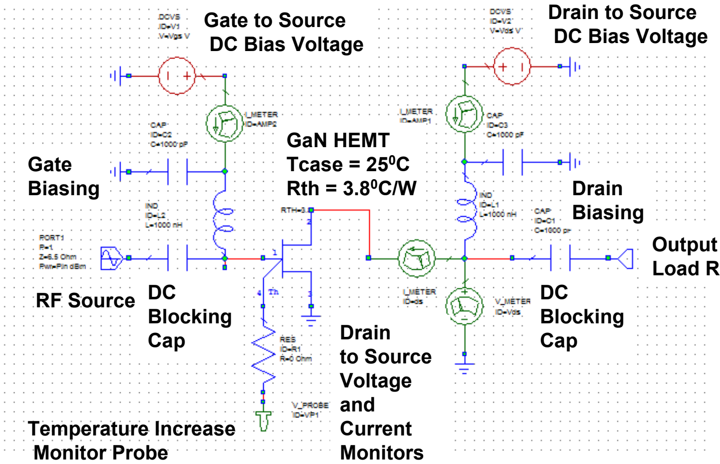
$$V_{RMS} = \frac{V\max - V\min}{2\sqrt{2}}$$

$$I_{RMS} = \frac{(I\max - I\min)}{2\sqrt{2}}$$

$$P_{LOAD} = V_{RMS} I_{RMS} = \frac{(V\max - V\min)(I\max - I\min)}{8}$$

$$\eta = \frac{P_{RF}}{P_{DC}} = 0.5\frac{(V\max - V\min)(I\max - I\min)}{(V\max + V\min)(I\max + I\min)}$$

GaN HEMT Basic Transistor Circuitry



Gate to Source
DC Bias Voltage

Drain to Source
DC Bias Voltage

GaN HEMT
Tcase = 25^{0}C
Rth = 3.8^{0}C/W

Gate
Biasing

Drain
Biasing

Output Port
Load Resistance

RF Source

DC
Blocking
Cap

DC
Blocking
Cap

Drain
to Source
Voltage
and
Current
Monitors

Temperature Increase
Monitor Probe

Material Properties Comparison

RF Power = (Vmax – Vmin)Imax/8

Material	Band Gap Energy (eV)	Critical Breakdown Field (MV/cm)	Thermal Conduc-tance (W/cm-^{0}K)	Mobility (cm^2/V-s)	Saturated Velocity (10^7 cm/s)	Relative Dielectric Constant ε_r
Si	1.1	0.3	1.5	1300	1	11.9
GaAs	1.4	0.4	0.5	6000	1.3	12.9
4H SiC	3.2	3.3	3.7	610	2	9.7
6H SiC	3.0	3.0	4.9	310	2.0	9.7
GaN	3.4	3.0	1.5	1500	2.7	9.0

High
Temperature
Operation

High Power
(High Vmax)

High Power
(High Imax)

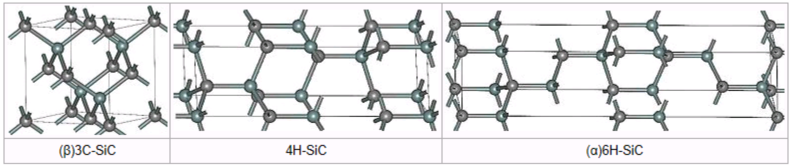
High Power GaN on 4H SiC
(Low Thermal Heating)

GaN mobility enhanced with HEMT structure for higher gain and frequency operation

Differences Between 4H and 6H SiC Substrates

- 4H and 6H SiC are different crystalline structures of the material with different properties
- 6H SiC is conductive and used for LED's (one contact)
- 4H Semi-insulating, better crystalline matched to GaN, and easier to make

Structure of major SiC polytypes.

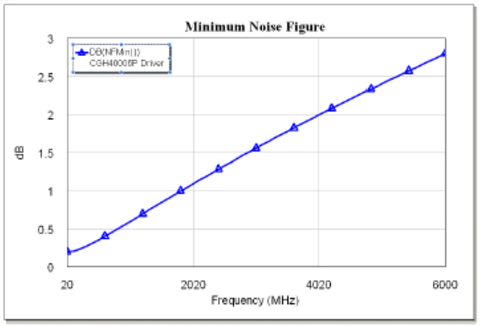


Properties of major SiC polytypes[2][22]

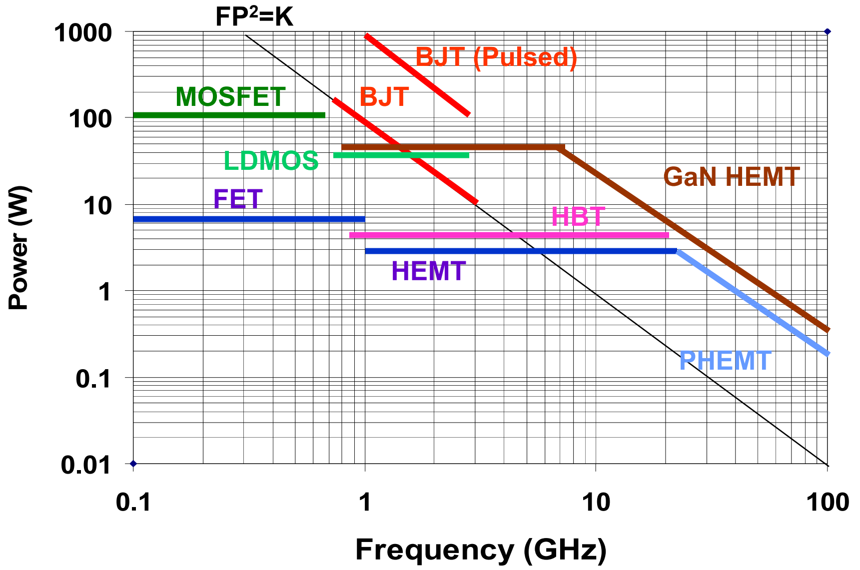
Polytype	3C (β)	4H	6H (α)
Crystal structure	Zinc blende (cubic)	Hexagonal	Hexagonal
Space group	T^2_d-F43m	C^4_{6v}-P6₃mc	C^4_{6v}-P6₃mc
Pearson symbol	cF8	hP8	hP12
Lattice constants (Å)	4.3596	3.0730; 10.053	3.0730; 15.11
Density (g/cm^3)	3.21	3.21	3.21
Bandgap (eV)	2.36	3.23	3.05
Bulk modulus (GPa)	250	220	220
Thermal conductivity (W/cm·K)	3.6	3.7	4.9

GaAs Low Noise Operation

- The mobility of GaN is so much lower than GaAs. For Ultra Low Noise GaAs PHEMTs are used over GaN.
- The mobility shown is for GaN but GaN HEMT's have higher mobility. The noise figure is very good for these devices not as low as the GaAs PHEMTs. For example the Crey 0.4 mm device:
- Where the GaN HEMT will shine is to have reasonable NF with high power capability so a receiver protector could be eliminated also they would have a high IP3



Power vs. Frequency for Solid State Devices



Silicon LDMOS Versus GaN HEMT Transistor

- The bandgap energy of silicon is only 1.1eV but Si LDMOS are used for high power applications.
- Silicon as used in LDMOS can be run at 150^0C for high reliability, not 180 to 225^0C for GaN (Higher bandgap).
- LDMOS has good breakdown voltages and also can use a large device to get the current for power. However is typically limited to use around 3 GHz. The GaN HEMT is a much higher frequency device.
- Cost is the issue and GaN price is now coming down.

High Efficiency (η)

- η = k (Vmax – Vmin)/(Vmax + Vmin)
  - k = 50% Class a, 78.5% Class b and higher for class c, d, e, f, and f^{-1}
- We will discuss later in the lecture all the details of the various classes of operation
- With high voltage operation (high Vmax), and reasonable low Vmin (knee voltage) the ratio of (Vmax – Vmin)/(Vmax + Vmin) will close to unity as opposed to low voltage operation where the ration takes a big hit on efficiency

Operation with high standing waves

- With a highly mismatched load, the transistor will see a higher voltage depending on the phase of the mismatch, so for the worse case the breakdown voltage must be larger than normal for this condition.

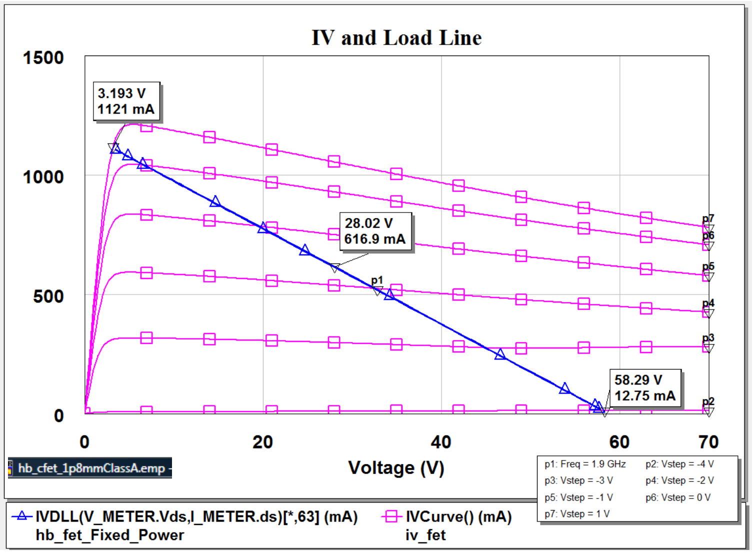
GaN Transistor Meets Objectives

- High Power
  - High breakdown voltage
  - High peak current, (Saturated velocity)
  - High current capability
- Good efficiency
  - Low knee voltage (Vmin)
  - High Vmax --- High breakdown voltage
  - Can cutoff current at high voltage – low Imin
  - Low semiconductor and circuit losses
- High Reliability
  - High temperature operation (High band gap material)
  - High reliability process
  - Low thermal resistance

Lets Look at a GaN Device to See How it Performs Compared to the Calculated Performance

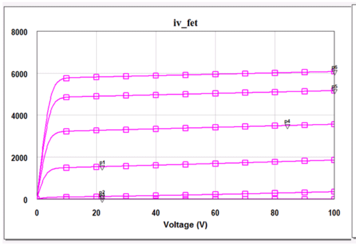
- 1.9 GHz
- 28V DC operation
- GaN HEMT Device on 100 μm of 4H SiC
- 0.25 Gate Length
- 1.8 mm Wide
- Nonlinear Model Developed by Dr. Walter Curtice
- Load the file cfet9.dll into AWR model directory
- Open up the file hb_cfet_1p8mmClassA.emp for class A operation and hb_cfet_1p8mmClassB.emp for class B operation

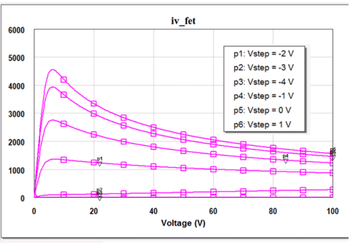
1.8 mm GaN HEMT



Note that the IV has a Negative Slope In the Saturated Region

- **This is due to self heating of the transistor. As the transistor heats up the current decreases**

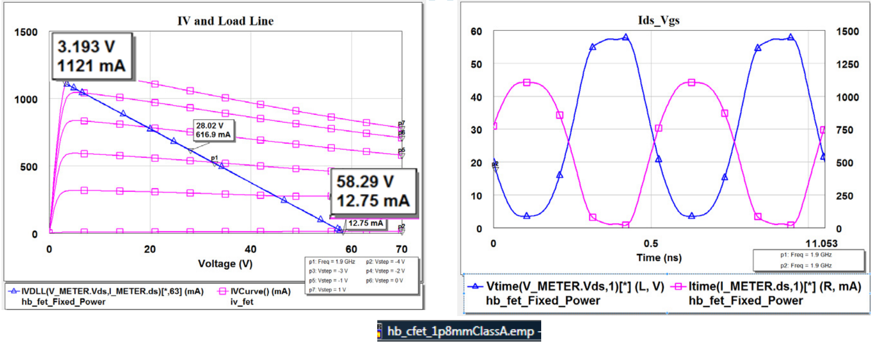




Self heating turned off

With self heating

1.8 mm GaN HEMT Class A



- Vmax = 58.29, Vmin =0
- Vmin = 3.2 V, I max = 1.12 A
- RL = (Vmax – Vmin)/Imax
- RL = (58.29 – 3.2)/1.12 = 49.2Ω
- P = (58.29 – 3.2) (1.12)/8
- P = 7.72 W or 38.9 dBm
- Pdc = 28 * 0.62A = 17.36 W
- η= 7.72/17.36 = 45%
- η= 0.5 * (58.28-.2)/(58.28+3.2)
- η= 45%

- PAE = (Pout – Pin)/Pdc
- PAE = η (1 – 1/G)
- G = Gain
- For high gain PAE = η

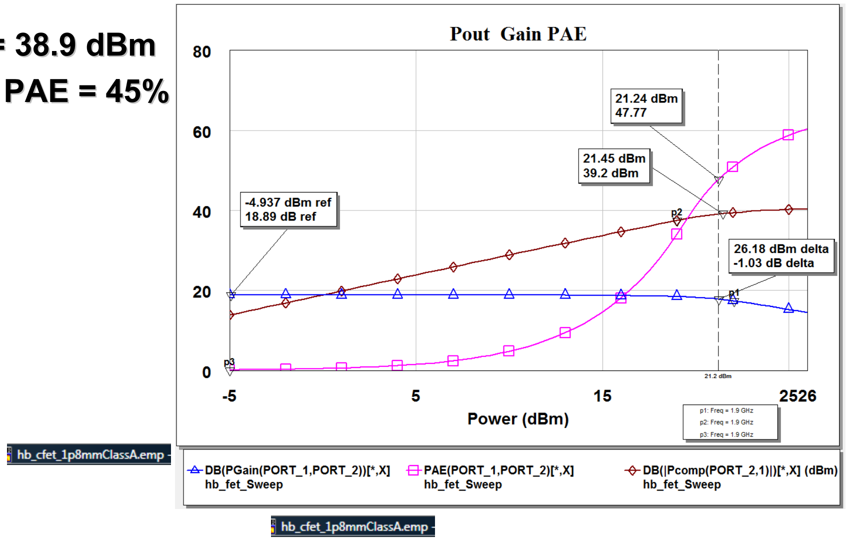
Load Line Selection

- Examine the load line and adjust Pin, Vgs and RLoad until you get simultaneously a good voltage and current swing.
- There are many answers so you should also look at the data of Pout, PAE, Gain and Gain Compression and choose the best.
- When choosing possibilities, always compare possibilities with the same gain compression amount
- I chose a condition is where the gain is compressed about 1 dB in comparing the various possibilities.
- You can also do an optimization procedure.

1.8 mm GaN HEMT Class A

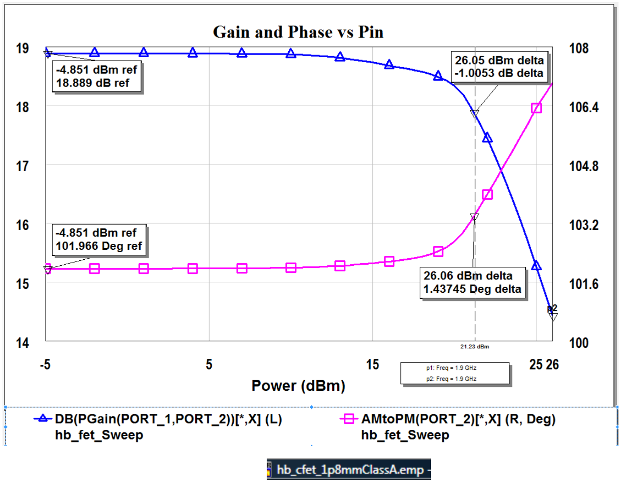
Calculated parameters similar to Harmonic Balance results

- **P = 38.9 dBm**
- **η= PAE = 45%**

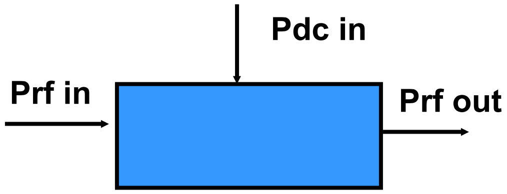


1.8 mm GaN HEMT Class A
Gain and Phase VS Pin

- **Note low Gain and Phase variation versus Pin ideal for low ACPR and EVM for digitally amplitude variant modulated signals**



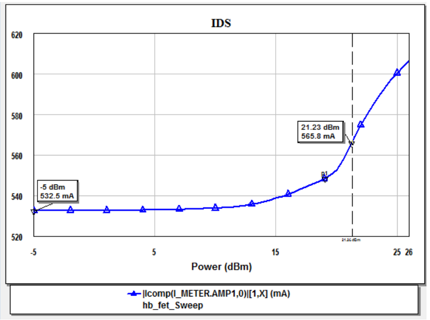
Thermal Considerations



Pdc in

Prf in

Prf out



- Tj = Ths + P dissipated * θ
- Tj = Junction temperature
- Ths = heat sink temperature
- θ = Thermal resistance
- Pdiss = Pdc in + Prf in – Prf out
- Class a has high temperature when not obtaining output power because dc power and inputs power are the heat inputs.
- With higher input powers, significant power is extracted, reducing the dissipated power and junction temperature rise

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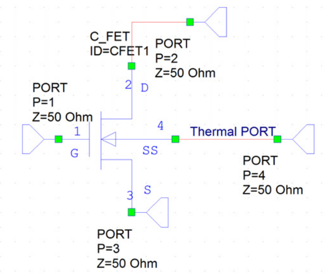
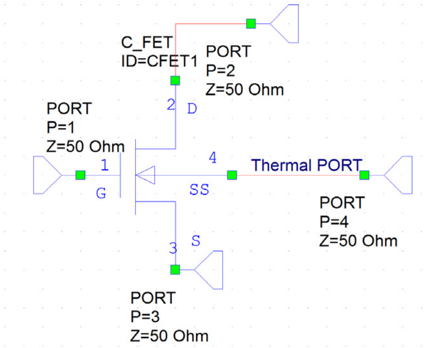
Thermal Port Voltage

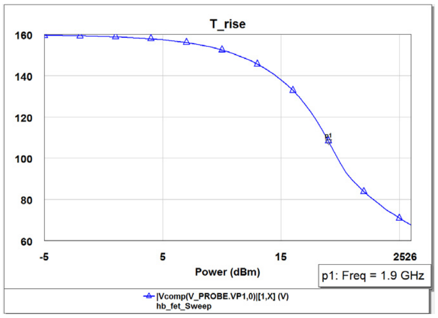
- The thermal port voltage is calibrated to read the junction temperature rise over heat sink temperature. The heat sink temperature is an input to the model.
- You just put a voltage monitor on it and read the voltage value and change volts to 0^{C}.



1.8 mm GaN HEMT Class A Thermal Considerations

- **Models of transistors include a thermal port to check thermal rise as part of nonlinear program and also vary RF modeling parameters as a function of heating**
- **Note high thermal rise for class a for low input powers**
- **Lets work in class b and examine properties**

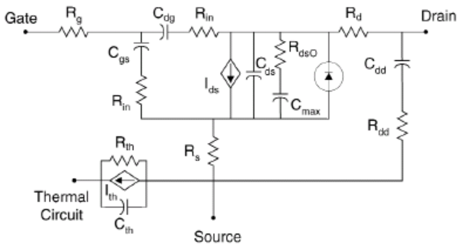




hb_cfet_1p8mmClassA.emp -

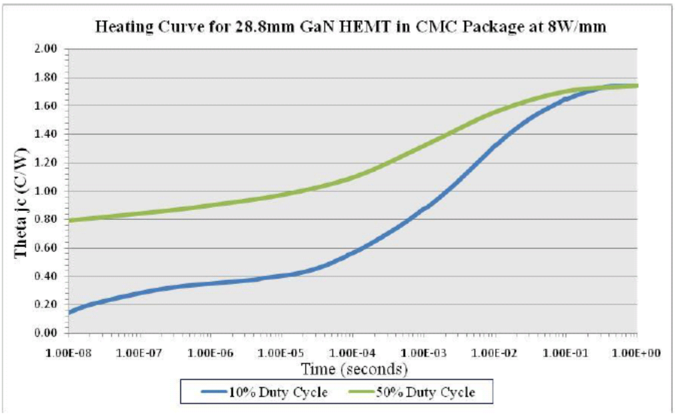
Operation under Pulsed Conditions

- **Some transistor models have the capability to consider pulsed conditions.**
- **In the model below, the current source represents the instantaneous power in the transistor.**
- **The RC represents the thermal time constant of the device.**
- **The voltage out is the temperature rise above the heat sink.**
- **So you can run pulsed conditions with specific duty cycles to determine the temperature**



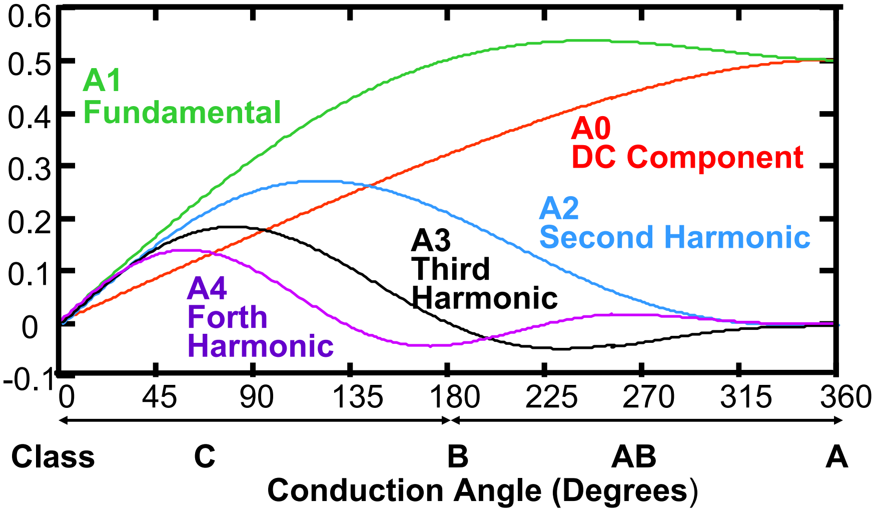
Thermal resistance vs time

- **Crey device**

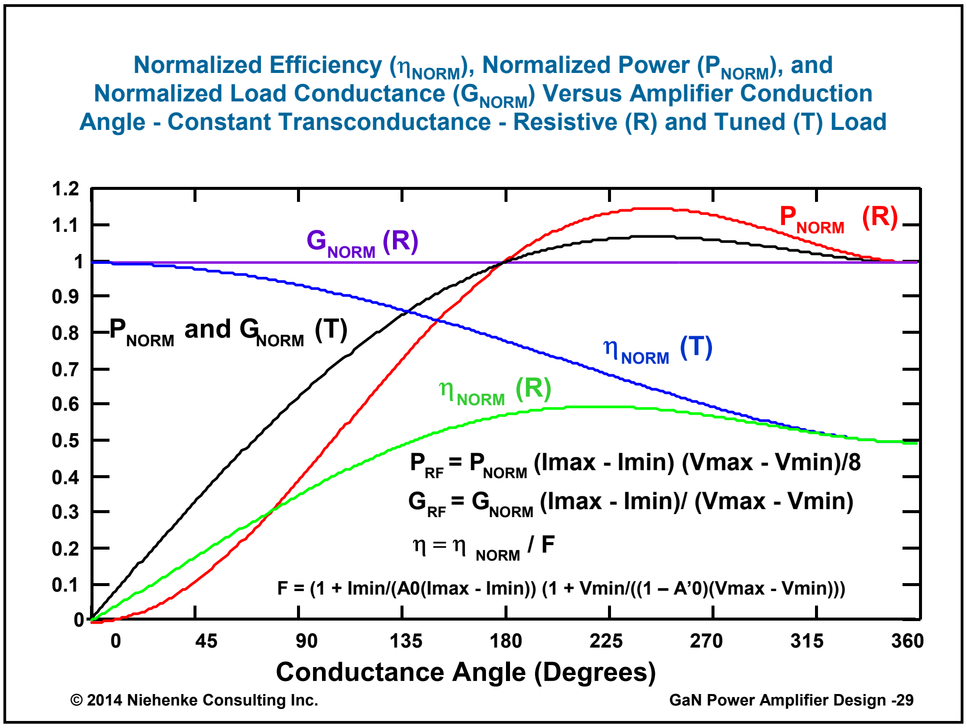


Effect of Conduction Angle on An’s

An Coefficients Normalized to Imax = 1A **Constant Gm**



ECN FT11.MCD



Normalized Efficiency (η_{NORM}), Normalized Power (P_{NORM}), and Normalized Load Conductance (G_{NORM}) Versus Amplifier Conduction Angle - Constant Transconductance - Resistive (R) and Tuned (T) Load

$P_{RF} = P_{NORM}$ (Imax - Imin) (Vmax - Vmin)/8

$G_{RF} = G_{NORM}$ (Imax - Imin)/ (Vmax - Vmin)

$\eta = \eta_{NORM} / F$

F = (1 + Imin/(A0(Imax - Imin)) (1 + Vmin/((1 – A’0)(Vmax - Vmin)))

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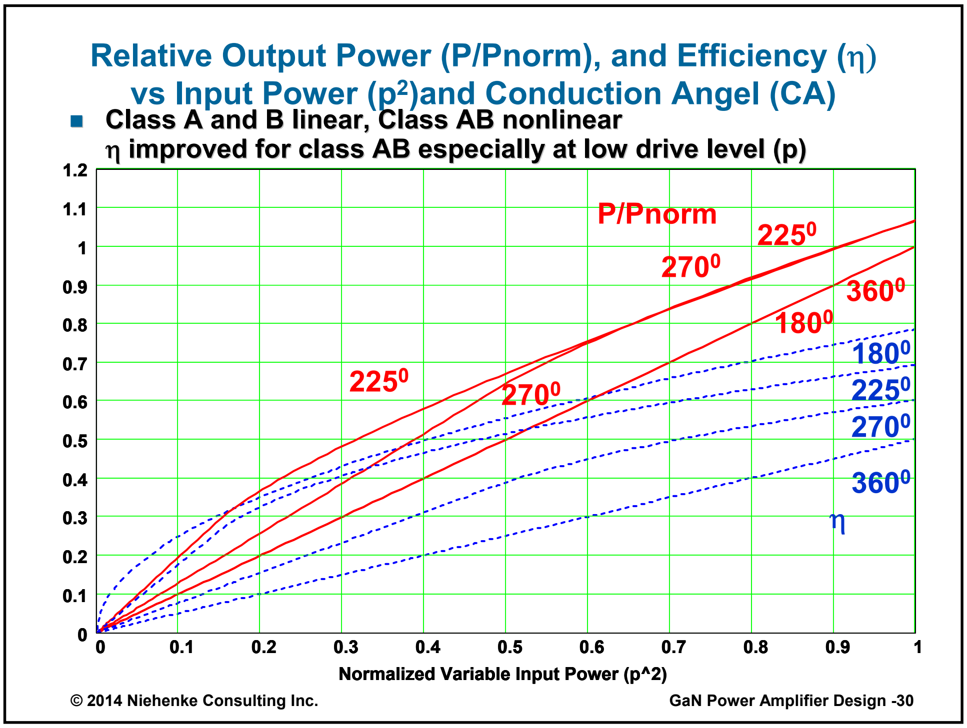
GaN Power Amplifier Design -29



Relative Output Power (P/Pnorm), and Efficiency (η) vs Input Power (p^2)and Conduction Angel (CA)

- Class A and B linear, Class AB nonlinear

η improved for class AB especially at low drive level (p)

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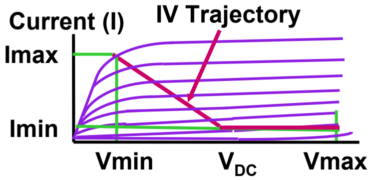
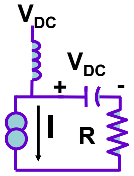
GaN Power Amplifier Design -30

Class B Operation - Tuned Load, 78.5%η

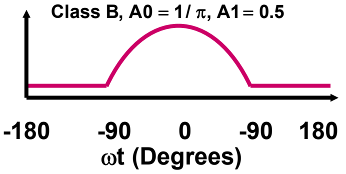


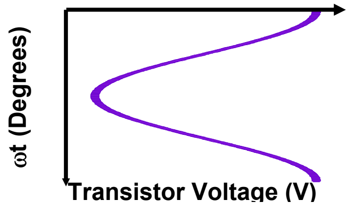


Transistor Current (I)

$$I = Imin + (Imax - Imin)\sum_{n=0}^{n=\infty} An\cos(n\omega t)$$

Class B, $A0 = 1/\pi$, $A1 = 0.5$





$$V_{RMS} = \frac{Vmax - Vmin}{2\sqrt{2}}$$

$$I_{RMS} = \frac{A1(Imax - Imin)}{\sqrt{2}} = \frac{(Imax - Imin)}{2\sqrt{2}}$$

$$P_{LOAD} = V_{RMS} I_{RMS} = \frac{(Vmax - Vmin)(Imax - Imin)}{8}$$

Transistor Voltage Swing $= Vmax - Vmin$

Transistor Current Swing $= Imax - Imin$

Output Load Current $= 2A1\,(Imax - Imin)$

Adjust load resistance R_L for full ac swing

$$Vmax - Vmin = R_L\,2A1(Imax - Imin)$$

$$R_L = \frac{Vmax - Vmin}{2A1(Imax - Imin)} = \frac{Vmax - Vmin}{(Imax - Imin)}$$

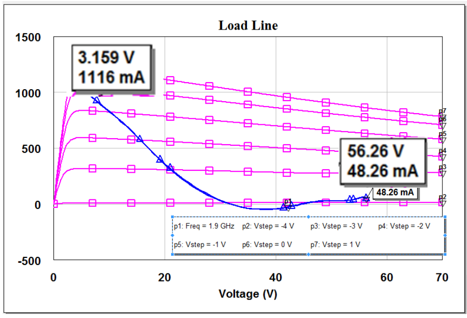
$$V_{DC} = \frac{Vmax + Vmin}{2}; \quad I_{DC} = Imin + A0(Imax - Imin)$$

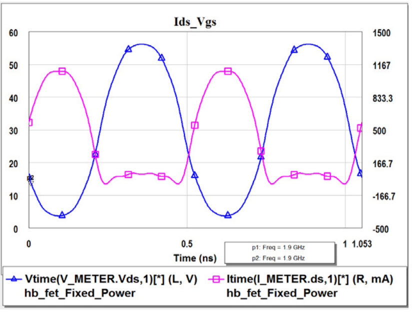
$$P_{DC} = \frac{(Vmax + Vmin)Imax}{2\pi}, \; Imin = 0$$

$$\eta = \frac{P_{RF}}{P_{DC}} = \frac{\pi}{4}\frac{(Vmax - Vmin)}{(Vmax + Vmin)}, \; Imin = 0$$

1.8 mm GaN HEMT Class B

hb_cfet_1p8mmClassb.emp





Frequency (GHz)	DB(Re(Pcomp(POR… hb_fet_Fixed_Power	DB(PGain(PORT_1,… hb_fet_Fixed_Power	PAE(PORT_1,PORT_2) hb_fet_Fixed_Power
1.9	39.039	15.239	67.907

- Second harmonic short added to circuit for good class b efficiency
- Power same for class a and b
- Efficiency better, η = 78.5 (56.26 – 3.2)/(56.26+3.2) = 70%

1.8 mm GaN HEMT Class B

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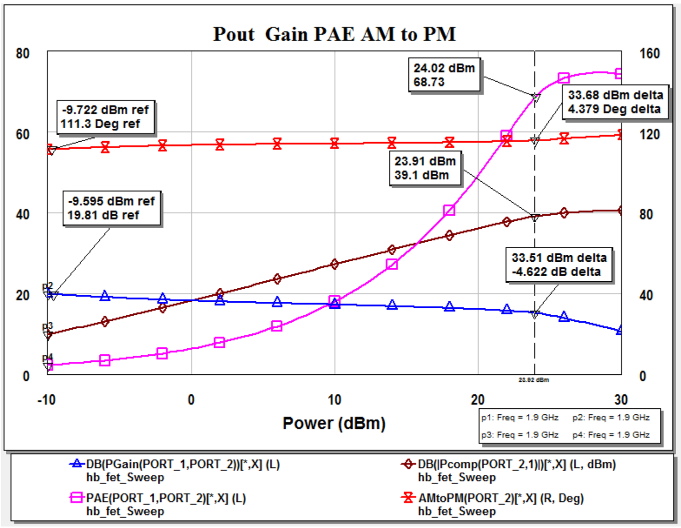

- **Gain and phase varying VS Pin for class B**
- **May need redesign for better linearity**

Gain Compression with GaN Devices

- **Some GaN HEMTs devices show a soft compression, so in my example I took the performance where I got the Pout**
- **If the product is used for a constant envelop, then work the PA where the PAE is maximum**
- **If the PA is used for varying envelop device, then design the semiconductor process and matching techniques for low AM/AM and AM/PM characteristics, and you have a winner**

AM to PM of Power Amplifiers

- AM/PM is caused by a nonlinear parameter or temperature parameter changing with input power.
- For example the transistor has nonlinear capacitors (varactors) which vary depending on the input power to the device.
- Also as the temperature changes (input power), this can cause a phase shift

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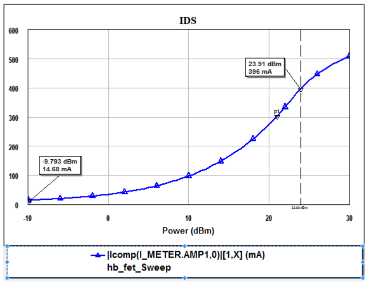
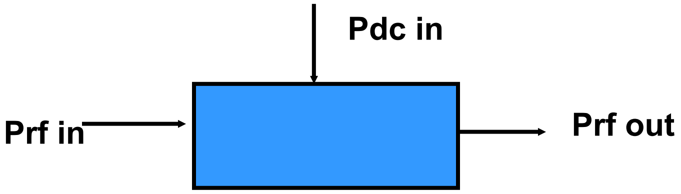
Thermal Considerations

- For Class b, current low at low output power



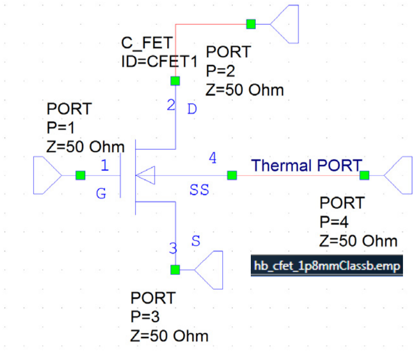

Pdc in

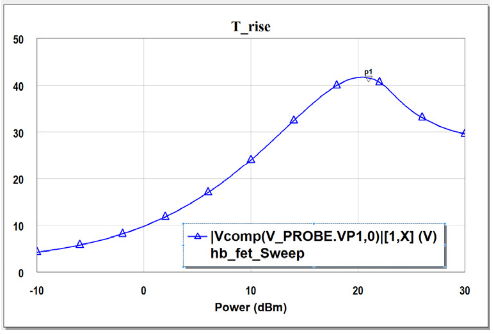
Prf in

Prf out

1.8 mm GaN HEMT Class B Thermal Considerations

- Models of transistors include a thermal port to check thermal rise as part of nonlinear program and also vary RF modeling parameters as a function of heating
- Temperature rise only 42^{0}C now not 160^{0}C rise



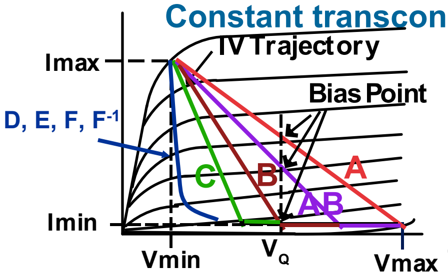


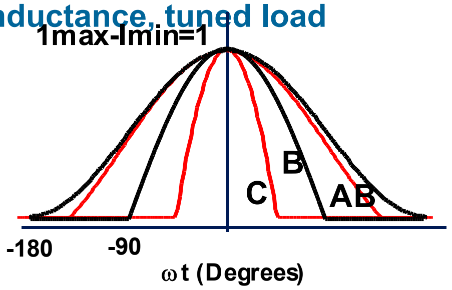
GaN Transistor Meets Objectives

- High Power
  - High breakdown voltage
  - High peak current, (Saturated velocity)
  - High current capability
- Good efficiency
  - Low knee voltage (Vmin)
  - High Vmax --- High breakdown voltage
  - Can cutoff current at high voltage – low Imin
  - Low semiconductor and circuit losses
- High Reliability
  - High temperature operation
  - High reliability process
  - Low thermal resistance
- Thermal management critical because of the very high power density in a small area and heat must be removed with low thermal resistance

Class A, B, AB, C, D, E, F, and F^{-1} Operation

Constant transconductance, tuned load



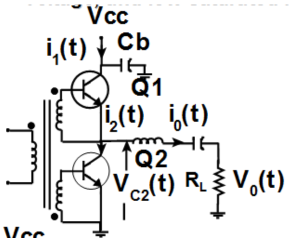


θ is angle from origin where current is at Imin
Conduction angle is 2θ

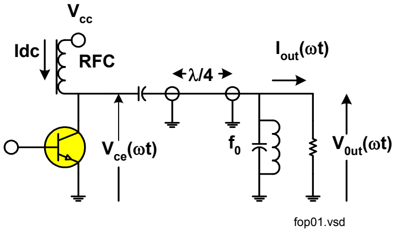
Class	Conduction Angle	Efficiency	Gain	Linearity
A	360^0	50 %	High	Good
AB	$180 - 360^0$	50 - 78.5%	-3 - -6 dB	Harmonics
B	180^0	78.5 %	-6 dB	Harmonics
C, D, E, F, F^{-1}	180^0	>78.5 %	Low	Harmonics

Class D, E, F, and F^{-1}

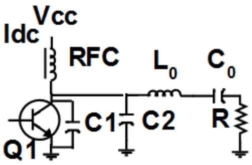
Class D



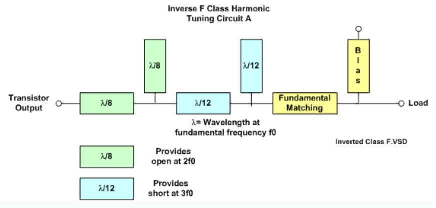
Class F



Class E

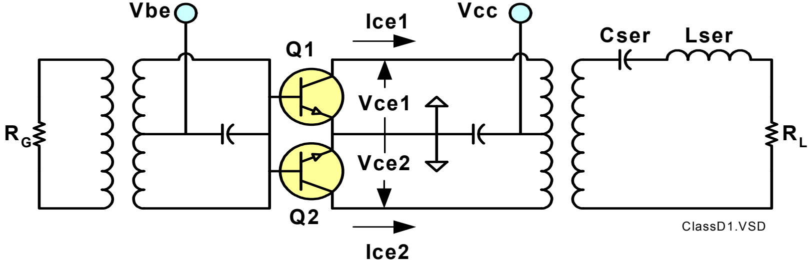


Class F^{-1}



Class D1 (Push-Pull)

- Odd mode balance places virtual short circuit in symmetry plane providing low Z at second harmonic
- Series L-C provides open at harmonics especially important for 3rd and 5th harmonic
- This enhances Vce to look like square wave with value when Icd = 0 and Vce = 0 with current value
- Result: very high efficiency



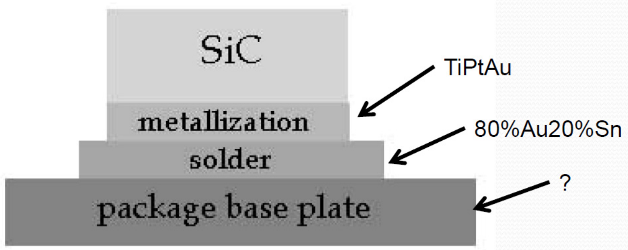
Power Amplifier Operating Class Summary

Operating Class			A	AB	B	C	D	E	F	D1	F Inverse
Conduction Angle	Θ	Degrees	360	180 to 360	180	<180	180				
Gain Reduction To Class A		dB		3	6	8	6	6	6	6	6
Ideal Efficiency	η	%	50	65	78	85	100	100	100	100	100
Efficiency Reduction	k		1-Vo/Vcc				1-2Vo/Vcc	See Notes	1-Vo/Vcc	1-Vo/Vcc	1-Vo/Vcc
Efficiency at Reduced Power			Poor	Good	Very Good	Poor	Poor, Class D, D1, E, and F need to be driven hard to obtain square wave pulse required for high η				
Frequency	fo	GHz	<≈100				<≈20 MHz KW P <≈2 GHz Watts P		<≈20		
Harmonic Suppression	nfo			Short 2f0		Short All nf0	Series LC circuit resonant at fo		Short even n Open odd n		Open even n Short odd n
Peak Transistor Voltage	Vmax	Volts	2Vcc-Vo				Vcc-Vo	3.5Vcc-2.5Vo	2Vcc-Vo		V0+(Vcc-Vo)π
Pout/Pin Gain Linearity			Good	Fair	Good	Poor	Poor (Good with system solution)				
Supply Voltage	Vcc	Volts									
Knee Voltage	Vo	Volts									

Conclusions

- We have seen that the GaN HEMT meets theoretical performance limits
- Lets now examine substrates for the GaN HEMT
- Transistor Configurations
  - With and without field plate
- Packaging for high density transistors
- Cree Devices, on 4HSiC
  - Pout, PAE, Reliability, Thermal Improvements
- Nitronex Devices on high resistivity Silicon

Packaging of High Power Density Transistors



- Package flange material needs to have high thermal conductivity but also have a coefficient of expansion that is close to SiC
- Unfortunately there a limited number of choices to get both right simultaneously!

“GaN-on-SiC MEMT Transistors and MMICs Enter the Mainstream, ”
Ray Pengelly, Cree RF and Microwave Products
Presented to IEEE AP/MTT Chapter, November 3, 2011

Properties of Relevant Materials

Material	Structure	Thermal Conductivity W/mK	Coefficient of Thermal Expansion ppm/K
Cu	Pure	393	17
Diamond		1500	1.4
Silicon		136	4.1
SiC	4H-SI	430	4
AlSiC	63%SiC	>175	7.9
W90Cu	90% W	185	6.5
W75Cu	75% W	225	9
Mo70Cu	70% Mo	185	9.1
Mo50Cu	50% Mo	250	11.5
CuMoCu	1:4:1	220	6
CuMoCu	1:1:1	310	8.8
Cu/Mo70Cu/Cu	1:4:1 laminate	340	8

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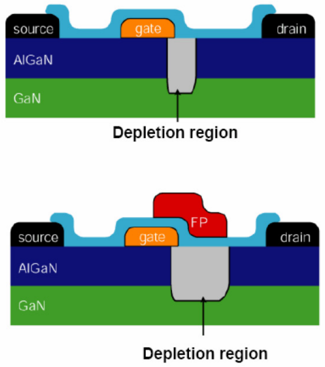
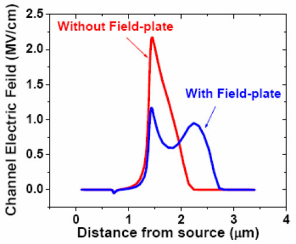
Cree





Field-plate reduces electric field

- Increase breakdown voltage
- lower electron injection into traps ➡ less dispersion

Field plate is connected to source. This reduces the gate to drain capacitance due to field plate insertion

"GaN-on-SiC MEMT Transistors and MMICs Enter the Mainstream, "
Ray Pengelly, Cree RF and Microwave Products
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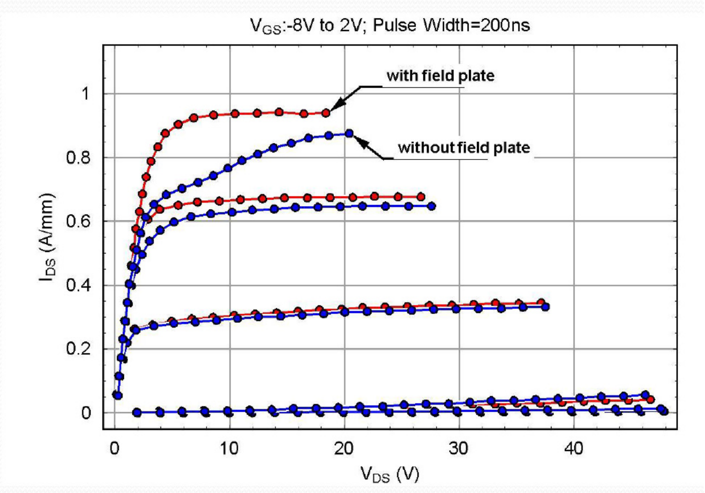
Double Recess Process to Increase Breakdown Voltage

- Many GaN HEMTs employ a double recess process to increase the breakdown voltage similar to GaAs HEMTs.
- Also many GaN HEMTs employ a field plate similar to many LDMOS transistors

---

Cree GaN Devices with and without Field Plate



"GaN-on-SiC MEMT Transistors and MMICs Enter the Mainstream, "
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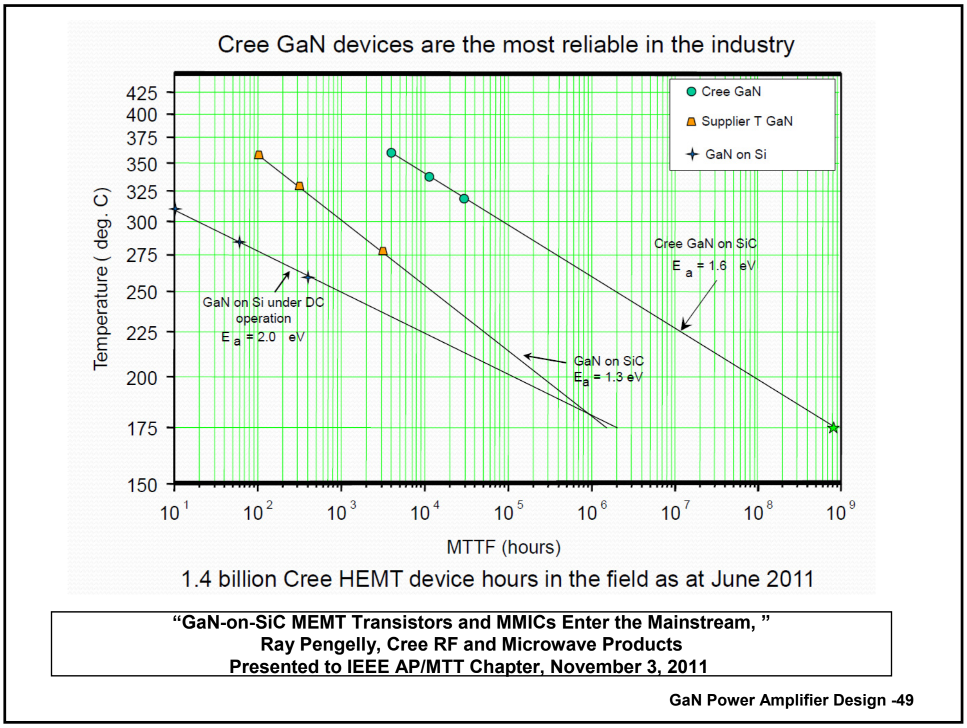
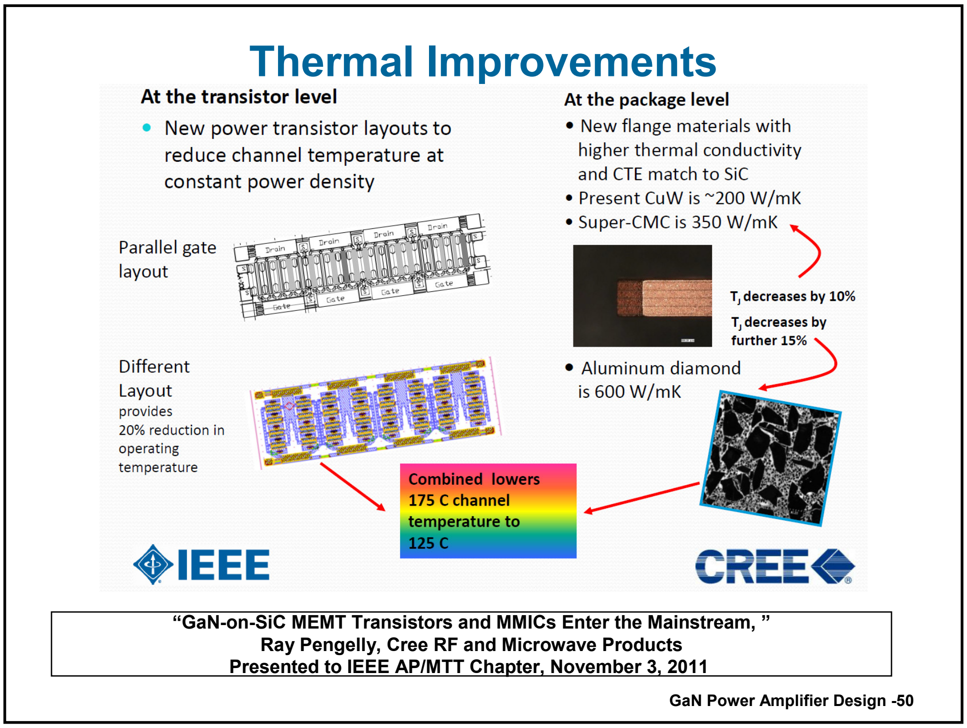


Cree GaN devices are the most reliable in the industry

1.4 billion Cree HEMT device hours in the field as at June 2011

“GaN-on-SiC MEMT Transistors and MMICs Enter the Mainstream, ”
Ray Pengelly, Cree RF and Microwave Products
Presented to IEEE AP/MTT Chapter, November 3, 2011

GaN Power Amplifier Design -49



Thermal Improvements

At the transistor level

- New power transistor layouts to reduce channel temperature at constant power density

Parallel gate layout

Different Layout provides 20% reduction in operating temperature

At the package level

- New flange materials with higher thermal conductivity and CTE match to SiC
- Present CuW is ~200 W/mK
- Super-CMC is 350 W/mK
- Aluminum diamond is 600 W/mK

T_j decreases by 10%

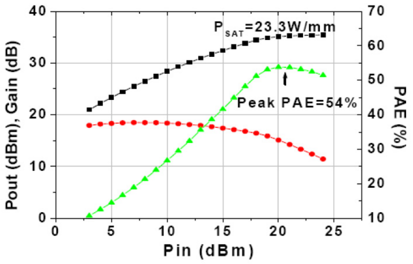
T_j decreases by further 15%

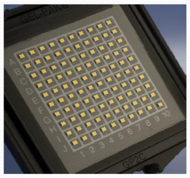
Combined lowers 175 C channel temperature to 125 C

“GaN-on-SiC MEMT Transistors and MMICs Enter the Mainstream, ”
Ray Pengelly, Cree RF and Microwave Products
Presented to IEEE AP/MTT Chapter, November 3, 2011

GaN Power Amplifier Design -50

Typical Performance of Cree Field Plate HEMTs

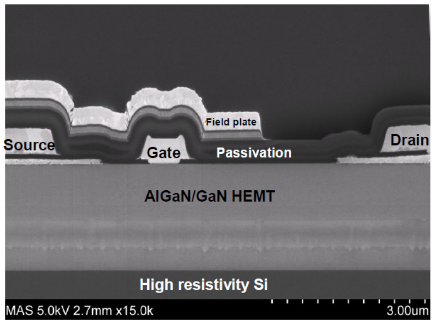


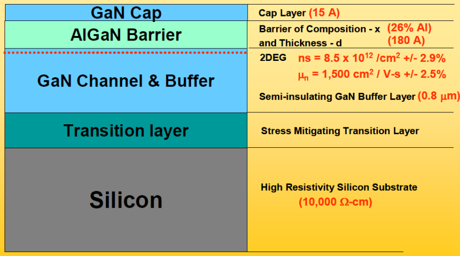


- Field-plated
- On SiC substrate. Biased at V_D=80V.
- 23.3W/mm with a peak PAE of 54% at 4GHz.

"GaN-on-SiC MEMT Transistors and MMICs Enter the Mainstream, "
Ray Pengelly, Cree RF and Microwave Products
Presented to IEEE AP/MTT Chapter, November 3, 2011

GaN ON Si HEMT Devices Nitronex



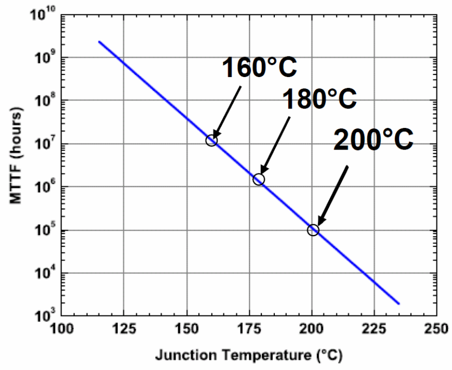


- >600 NRF1 Baseline Wafers processed since October 2005

- **The AlGaN/GaN HEMT structure results higher current and mobility compared to a FET structure**
- **The field plate improves the breakdown voltage**
- **Metal organic chemical vapor deposition (MOCVD) is the preferred method of producing GaN-based thin films on Si or SiC for RF applications.**
- **GaN-based devices and structures have been mass-produced using MOCVD for lighting applications and the same supporting high volume epitaxial manufacturing infrastructure can be leveraged for RF applications.**

GaN HEMT Devices Nitronex

- **Can operate at 180^{0}C with MTBF of 10^6**



MTTF of NRF1 Devices as a Function of Junction Temperature

Nitronex GaN on Si HEMT Device

NPTB00004 Datasheet

NITRONEX CORPORATION

Gallium Nitride 28V, 5W RF Power Transistor

Built using the SIGANTIC® NRF1 process - A proprietary GaN-on-Silicon technology

FEATURES
- Optimized for CW, pulsed, WiMAX, W-CDMA, LTE, and other applications from DC to 6GHz
- 100% RF Tested at 2500MHz
- 5W P3dB CW Power
- 15.5dB Power Gain
- Low cost, surface mount SOIC package
- High reliability gold metallization process
- Lead-free and RoHS compliant
- Subject to EAR99 Export Control

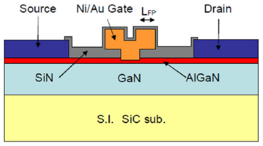
DC - 6000MHz
5 Watt, 28 Volt
GaN HEMT

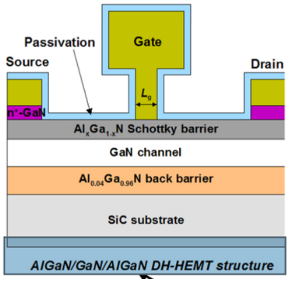
RoHS

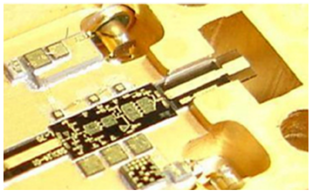
RF Specifications (CW): V_{DS} = 28V, I_{DQ} = 50mA, Frequency = 2500MHz, T_C = 25°C, Measured in Nitronex Test Fixture

Symbol	Parameter	Typ	Units
P_{3dB}	Average Output Power at 3dB Compression	5.1	W
P_{1dB}	Average Output Power at 1dB Compression	2.9	W
η	Drain Efficiency at 3dB Compression	56	%

GaN HEMT Structures Higher Frequencies

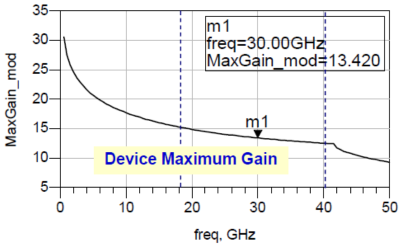


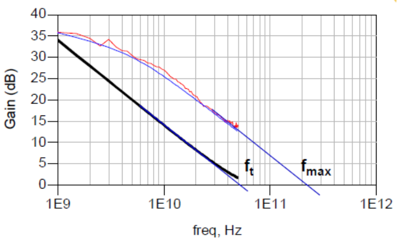


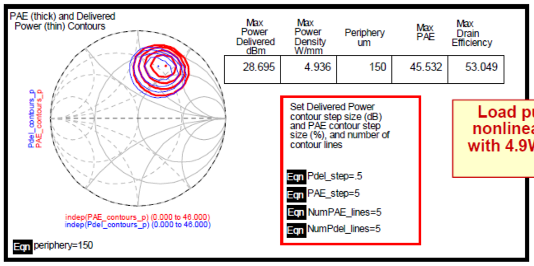


BAE Non Field Plate 0.2 μm Gate MMIC Process

- ft = 50 GHz, fmax = 220 GHz, 5W/mm, 46% PAE at 30 GHz







PAE (thick) and Delivered Power (thin) Contours

Max Power Delivered dBm	Max Power Density W/mm	Periphery um	Max PAE	Max Drain Efficiency
28.695	4.936	150	45.532	53.049

Set Delivered Power contour step size (dB) and PAE contour step size (%), and number of contour lines

Eqn Pdel_step=.5
Eqn PAE_step=5
Eqn NumPAE_lines=5
Eqn NumPdel_lines=5

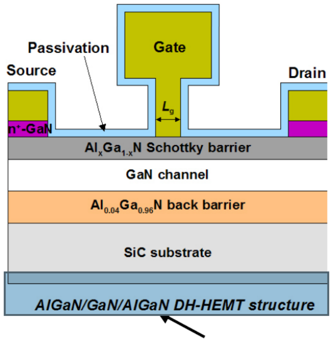
Eqn periphery=150

Load pull result based on nonlinear model – 46% PAE with 4.9W/mm power density at 30GHz

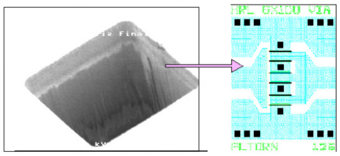
"High Efficiency Ka/Q Band PHEMT Power Amplifier MMICs" Dr. James J. Komiak, BAE Systems, IMS2011 Workshop

HRL’s Baseline T Gate Structure

HRL T-gate GaN device cross section



Source via (30um x 30um)



50µm (2mil) thick Semi-insulating SiC

-Back side dry etch vias enable microstrip designs

“GaN T-Gate and Field Plate Technology for Applications Below 45 GHz” Harris Moyer, HRL Laboratories, IMS2011 Workshop, “Introduction to GaN MMIC Design”

HRL’s Baseline T Gate Structure

Characteristics of HRL’s Baseline T-Gate Process

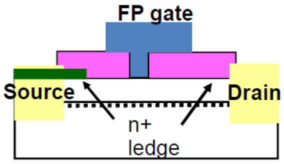
State of the art GaN device technology

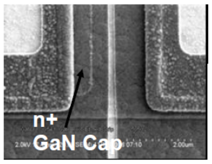
- Double Heterojunction Structure (DHFET)
  - Improves electron confinement
  - Alleviates short channel effects
- T-gate device
  - Lg ~ 0.15um, S/D spacing ~ 1.7um
  - Drain voltage range: 1V to 14V (Breakdown ~ 40V)
- Low Ohmic contact resistance and access resistance
  - Low Ron < 1.6 ohm-mm
- High f_T and f_{max}, low Fmin
  - f_T of 90 GHz
  - f_{max} of >190 GHz. *(at Vds=10V)*
  - Fmin of < 1.6 dB at 26 GHz *(at Vds=5V)*

“GaN T-Gate and Field Plate Technology for Applications Below 45 GHz” Harris Moyer, HRL, IMS2011 Workshop, “Introduction to GaN MMIC Design”

HRL’s Baseline T Gate Structure

GaN HFET with Lateral-scaling, BV> 100V

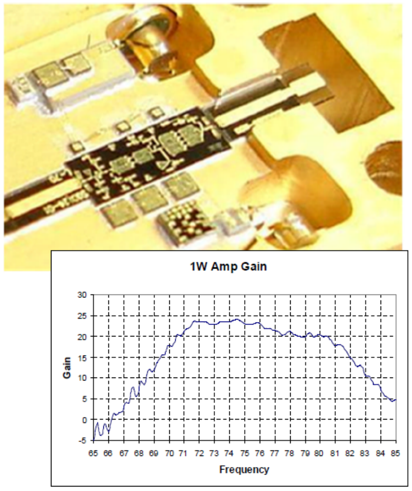




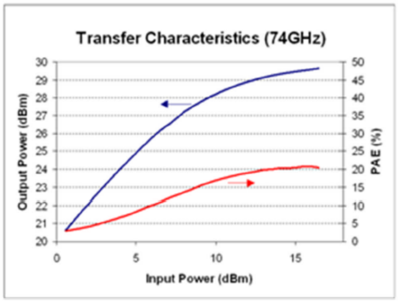
- 25 % reduction in R_on
- > 20% increase in Imax
- Keep Breakdown voltage high
- gm and ft improved by ~20%
- ft = 55 – 60 GHz
- Gain (35GHz) = 12.5 dB

“GaN T-Gate and Field Plate Technology for Applications Below 45 GHz” Harris Moyer, HRL, IMS2011 Workshop, “Introduction to GaN MMIC Design”

E-Band Test Fixture with HRL MMIC



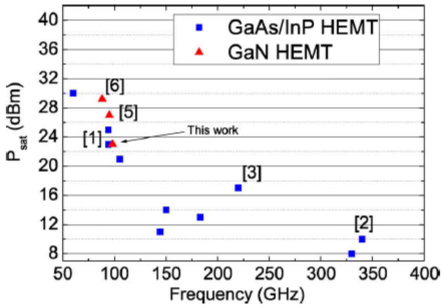
Power & PAE Measurements at 74 GHz



- **GaN MMIC**
- **3-Stages**
- **600um Output Gate Width Pout = ~1W**
- **Gain = 20 dB**

MMIC: B. Kim et al., “A Linear, High-Efficiency GaN Power Amplifier Operating at 74 GHz,” GOMAC 2011, March 2011
Presentation: IMS2011 Workshop WMA, Q/V-Band Linear Power Amplifiers using Envelope Tracking and Digital Pre-distortion James Schellenberg, QuinStar Technology, Inc., Contributors: Bumjin Kim, Jonmei Yan*, Donald Kimball* *University of California, San Diego, CA, USA 92093

Millimeter Wave Results

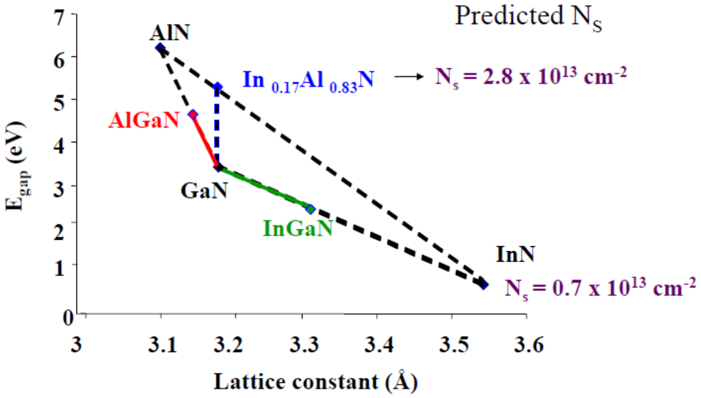


This Work
Dual-Gate GaN MMICs for MM-Wave Operation
Ruediger Quay, *Senior Member, IEEE*, A. Tessmann, R. Kiefer, S. Maroldt, C. Haupt, U. Nowotny, R. Weber, H. Massler, D. Schwantuschke, M. Seelmann-Eggebert, A. Leuther, M. Mikulla, and O. Ambacher
IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS, VOL. 21, NO. 2, FEBRUARY 2011, pp. 95-97

[1] L. A. Samoska, “Towards terahertz MMIC amplifiers: Present status and trends,” in *IEEE MTT-S Int. Dig.*, San Francisco, 2006, pp. 333–336.
[2] W. R. Deal, “Solid-state amplifiers for terahertz electronics,” in *IEEE MTT-S Int. Dig.*, Anaheim, CA, 2010, pp. 1122–1125.
[3] V. Radisic, K. M. Leong, X. Mei, S. Sarkozy, W. Yoshida, P. Liu, J. Uyeda, R. Lai, and W. R. Deal, “A 50 mW 220 GHz power amplifier module,” in *IEEE MTT-S Int. Dig.*, Anaheim, CA, 2010, pp. 45–48.
[5] M. Micovic *et al.*, “GaN MMIC PAs for E-band (71 GHz–95 GHz) radio,” in *Proc. IEEE CSICs’08*, Monterey, CA, 2008, pp. 1–4.
[6] M. Micovic *et al.*, “W-Band GaN MMIC with 842mWoutput power at 88 GHz,” in *IEEE MTT-S Int. Dig.*, Anaheim, CA, 2010, pp. 237–239.
.

New Epitaxial Material for GaN

- **Less Strain using $IN_{0.17}Al_{0.83}N$ on GaN compared to existing AlGaN on GaN**
- **Higher Reliability, Higher Power, Less short channel effects meaning can use shorter gate lengths for higher frequency operation**



$\mathrm{IN_{0.17}Al_{0.83}N}$ on GaN

- InAlN/GaN heterojunction structures offer several potential advantages over AlGaN/GaN. These include
- 1) a improved lattice matched structure with much reduced lattice stress
- 2) higher reliability and robustness due to the improved lattice match
- 3) higher output current and current density and thus higher output power where the breakdown condition is preserved
- 4) potentially higher chemical and thermal stability due to the higher temperature the structure can withstand
- 5) potentially improved control of surface instabilities
- 6) thinner barrier and shorter gate structures which will lead to higher power performance at higher frequencies into the millimeter range.
- Addressed in IMS2013 Workshop WMA: Advancements in InAlN/GaN Device and Microwave/MMW Circuit Technology

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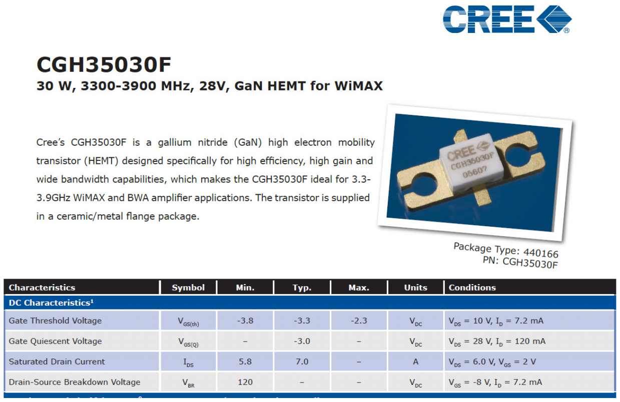
Design a 30 W (P1dB) PA using the Crey CGH35030F GaN HEMT at 1.9 GHz



CGH35030F

30 W, 3300-3900 MHz, 28V, GaN HEMT for WiMAX

Cree's CGH35030F is a gallium nitride (GaN) high electron mobility transistor (HEMT) designed specifically for high efficiency, high gain and wide bandwidth capabilities, which makes the CGH35030F ideal for 3.3-3.9GHz WiMAX and BWA amplifier applications. The transistor is supplied in a ceramic/metal flange package.

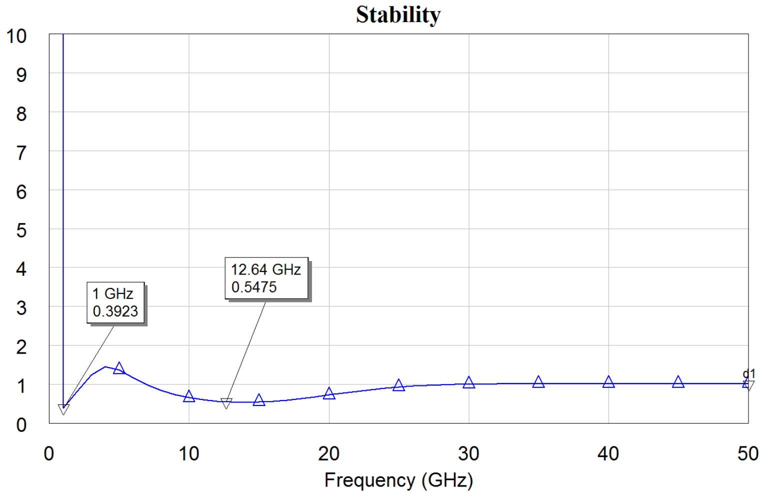
Package Type: 440166
PN: CGH35030F

Characteristics	Symbol	Min.	Typ.	Max.	Units	Conditions
DC Characteristics[1]						
Gate Threshold Voltage	$V_{GS(th)}$	-3.8	-3.3	-2.3	V_{DC}	V_{DS} = 10 V, I_D = 7.2 mA
Gate Quiescent Voltage	$V_{GS(Q)}$	–	-3.0	–	V_{DC}	V_{DS} = 28 V, I_D = 120 mA
Saturated Drain Current	I_{DS}	5.8	7.0	–	A	V_{DS} = 6.0 V, V_{GS} = 2 V
Drain-Source Breakdown Voltage	V_{BR}	120	–	–	V_{DC}	V_{GS} = -8 V, I_D = 7.2 mA

Operate at 28 Vds and design for Class a and Class b

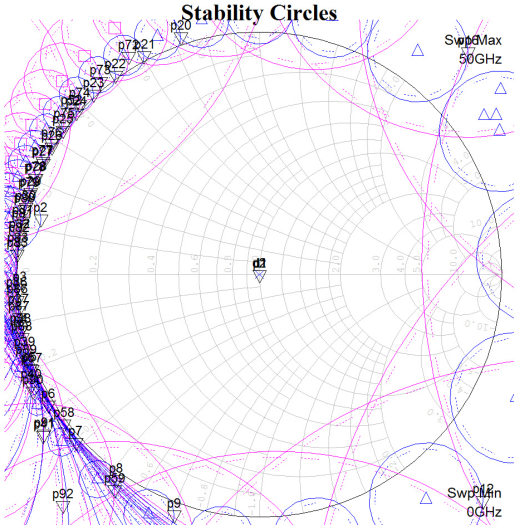
Stability

- **For stable operation k>1**
- **Amplifier unstable**


Stability

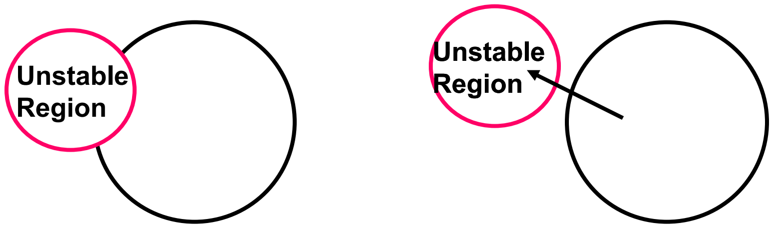
Stability

- **For stable operation No Circles in Smith chart**

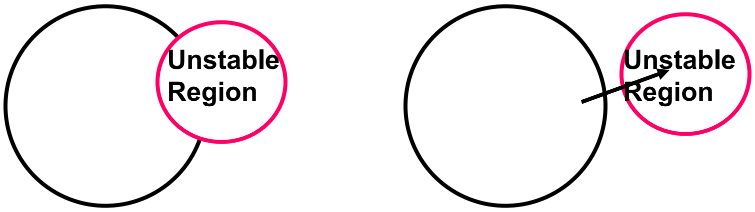

Stability Circles

Stabilization

Add Series Resistance



Add Shunt Resistance



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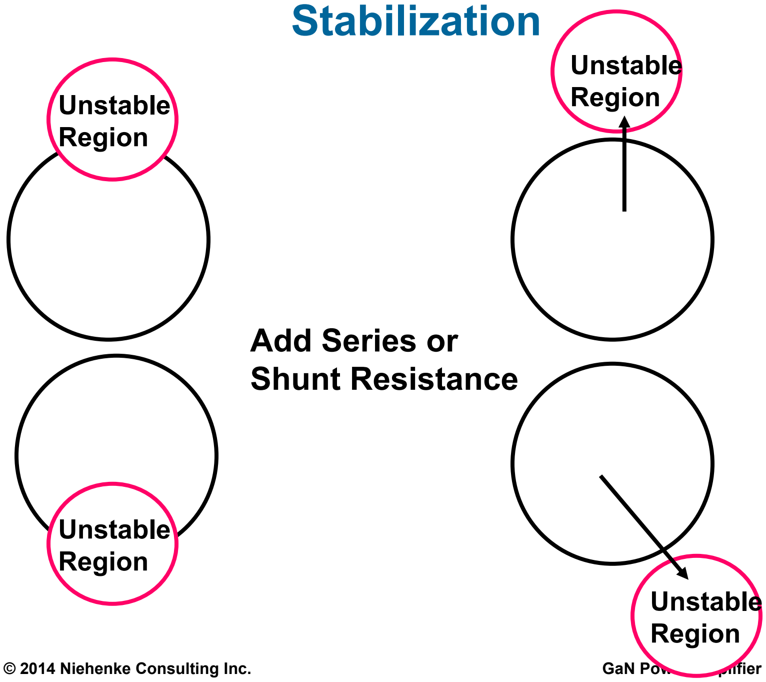
Stabilization



Add Series or Shunt Resistance

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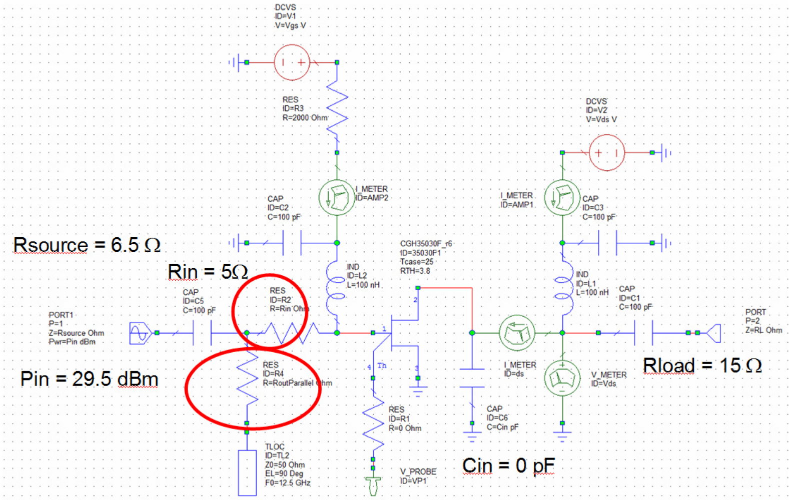
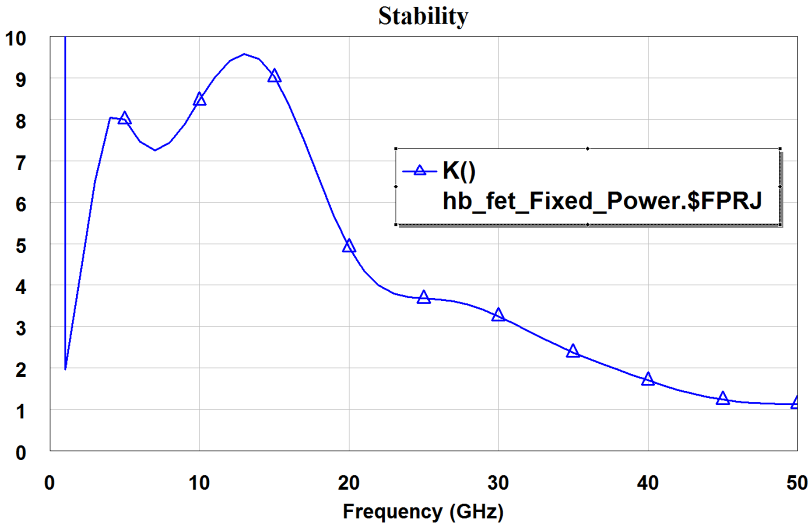
AWR Schematic Class A

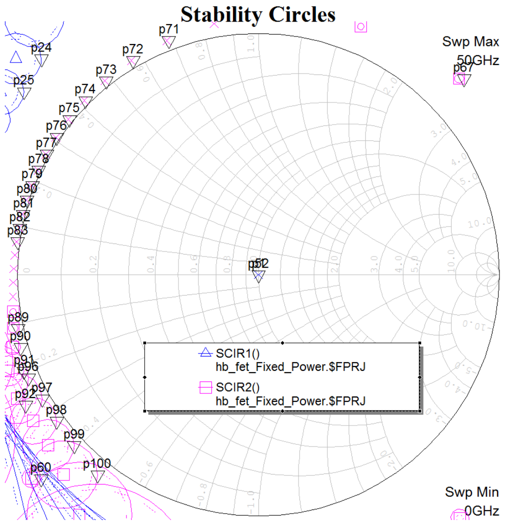
Stability achieved by placing a series resistor and a parallel resistor on the input



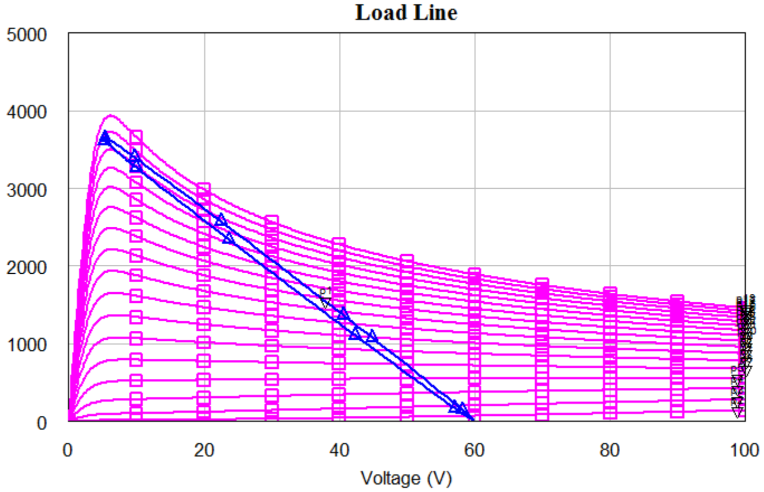
Unconditionally Stable (K>1)



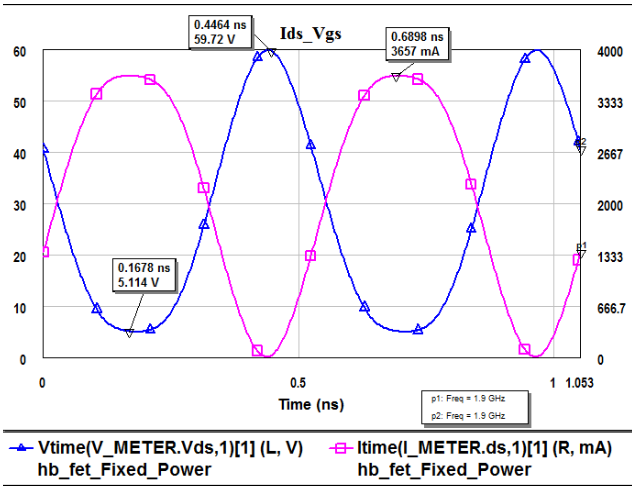
Unconditionally Stable

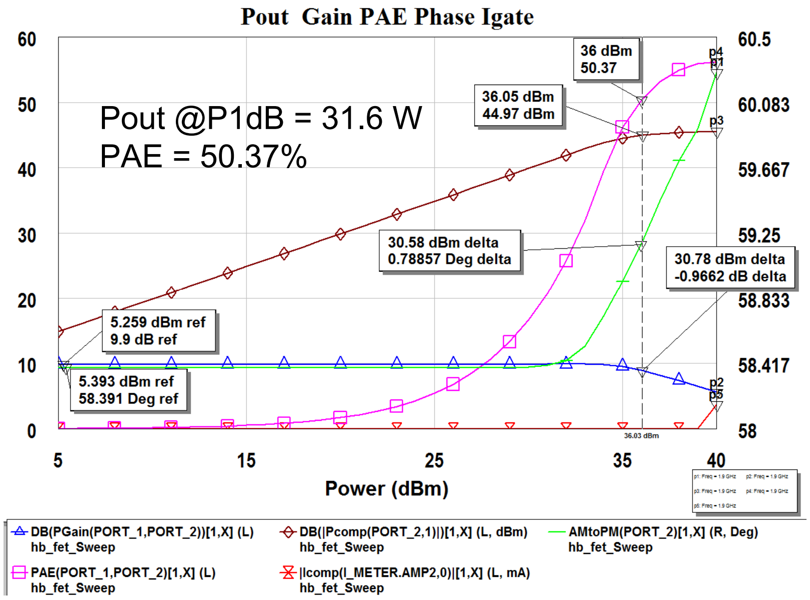


Load Line
Vgs = -1.17 V, RL = 15 Ω. Pin = 34.2 dBm

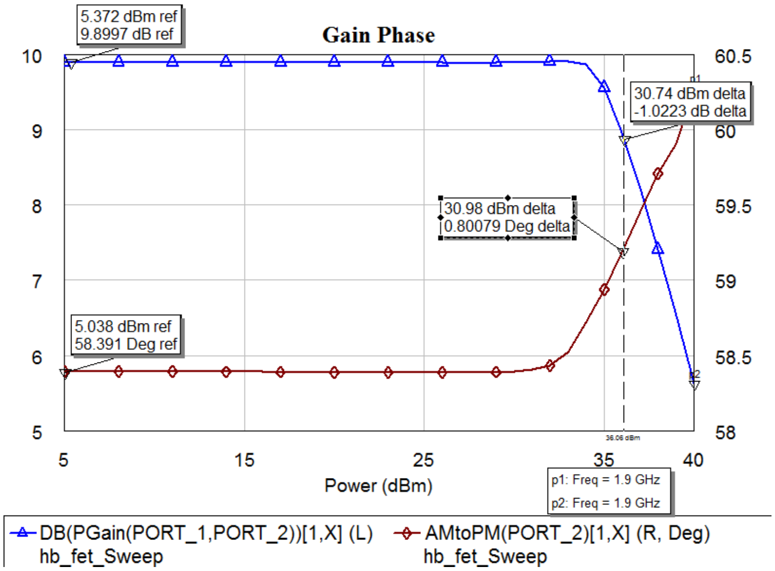


AWR Current Voltage Class A



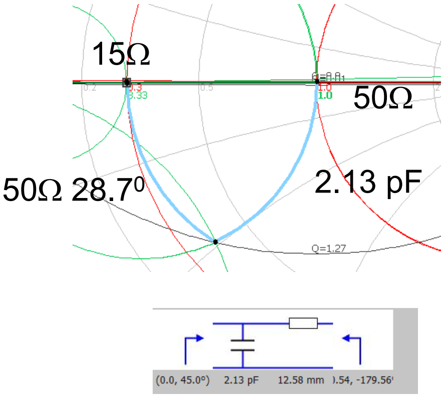

Pout @P1dB = 31.6 W
PAE = 50.37%

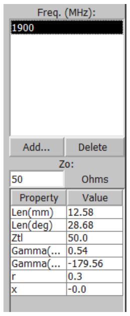
Low AM/AM and AM/PM



Output Match

- **Output needs to see 15 Ω**



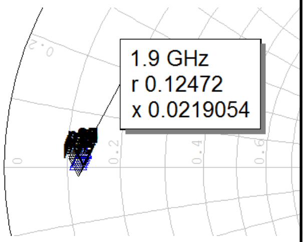


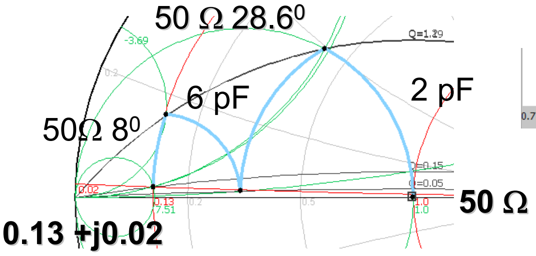
Zo: 50 Ohms

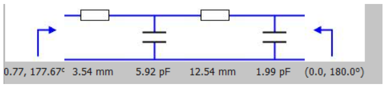
Property	Value
Len(mm)	12.58
Len(deg)	28.68
Ztl	50.0
Gamma(...	0.54
Gamma(...	-179.56
r	0.3
x	-0.0

Input Match

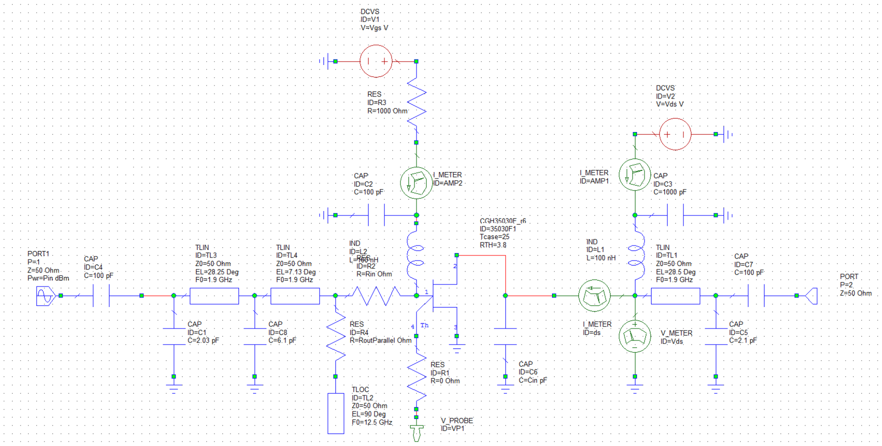
- **0.13 +j0.02 to 1**







Match Input and Output with Low Pass Matching Circuits

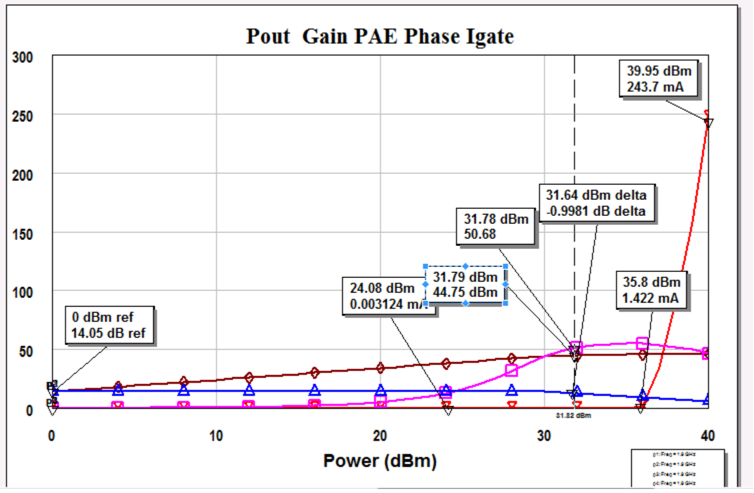


Gate Current and Reliability

- High gate current leads to metal migration which can open circuit the gate. With GaAs devices, the rule of thumb is not to exceed 1 ma per mm of gate periphery.
- So under normal operation the gate current is low, but when driven with higher power than normal, gate current is experienced.
- One way to reduce gate current with higher powers is to place a resistor in the DC portion of the gate bias circuitry
- Many times the manufacturer will suggest a gate resistor for their device.
- The metal migration process does not happen immediately, and it takes time to develop.
- Always monitor the gate current for your PA design.
- As a precaution, do not overdrive the PA, an place a resistor in the gate dc portion of the DC bias circuit.

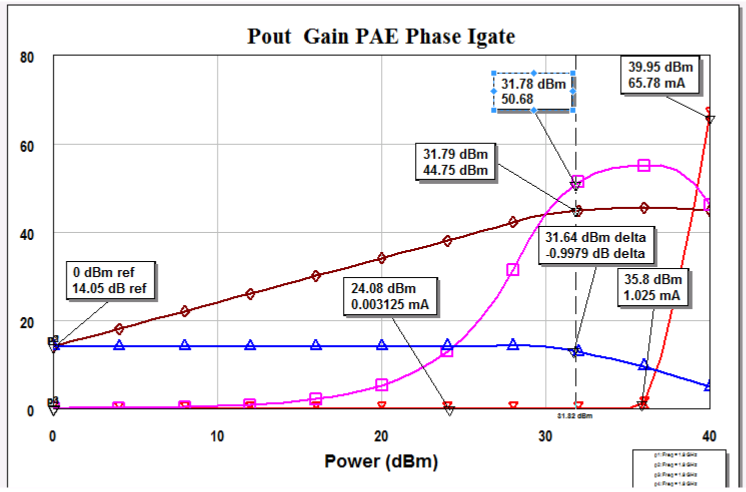
Example

- Rgate = 0 Ohms



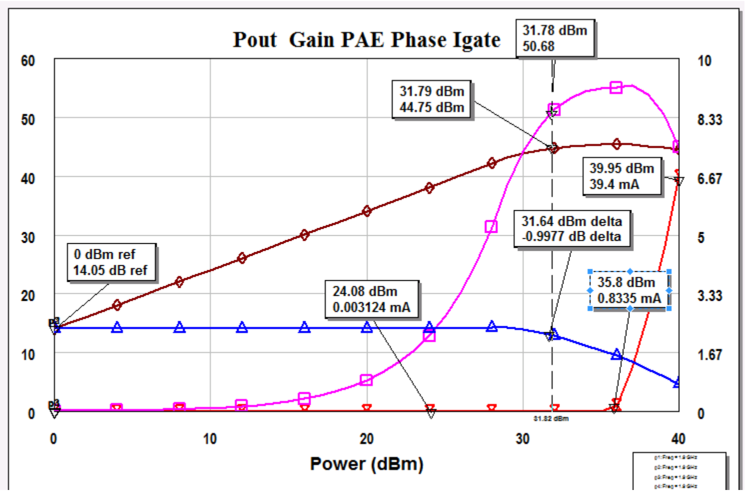
Example

- **Rgate = 50 Ohms**



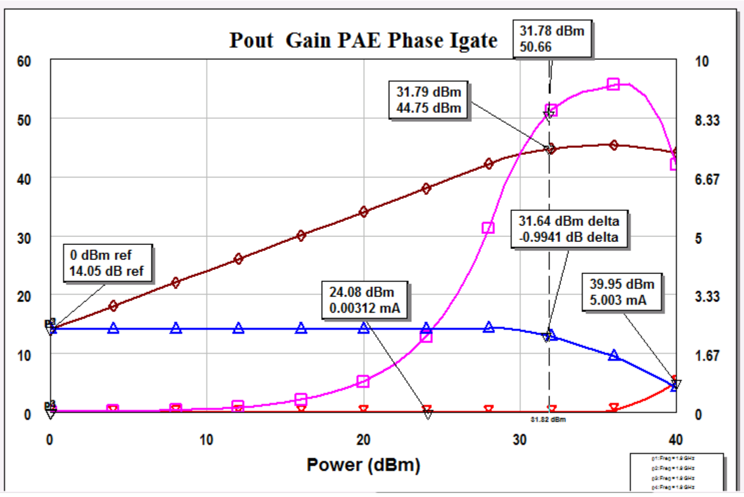
Example

- **Rgate = 100 Ohms**



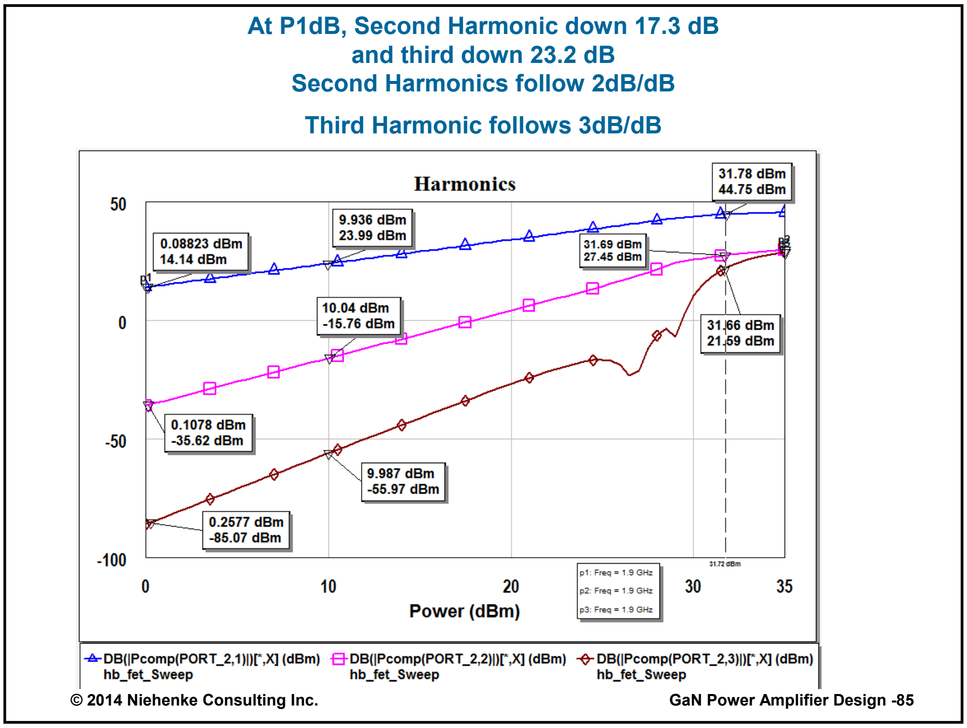
Example

- **Rgate = 1K**

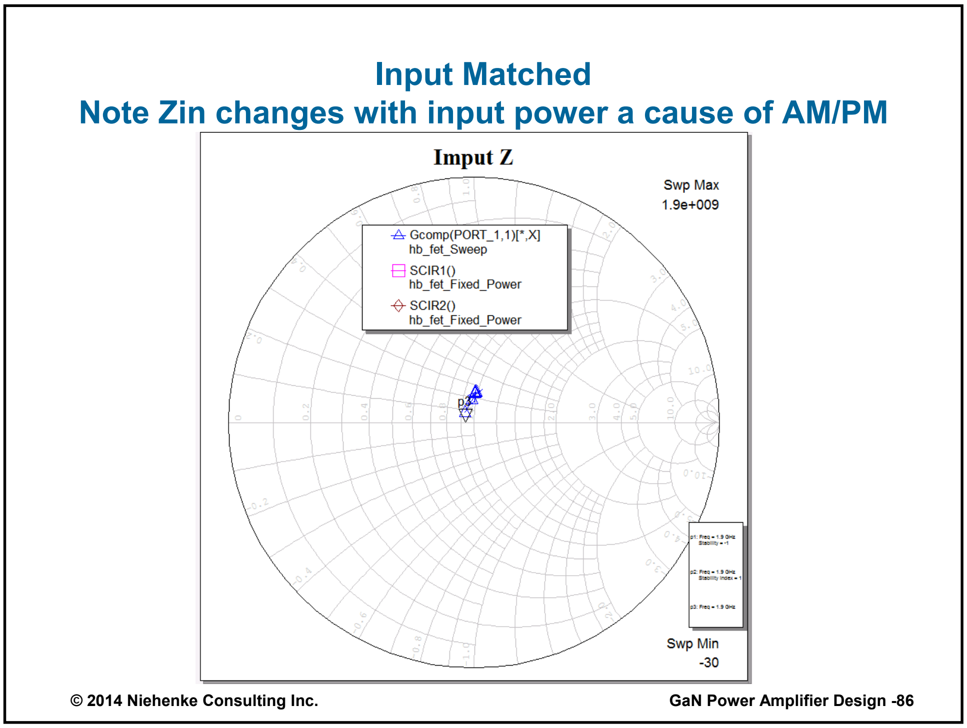


Conclusion

- For this transistor, the Pout at P1dB does not change for gate resistors 1 to 1000 Ohms
- The gate current starts at 4 dB above the P1dB point. So do not operate the transistor here
- Operating the transistor there does not make sense, because this is past the peak PAE point
- Adding 1K helps tremendously should one by accident overdrive the PA 4 dB or more above the P1dB point

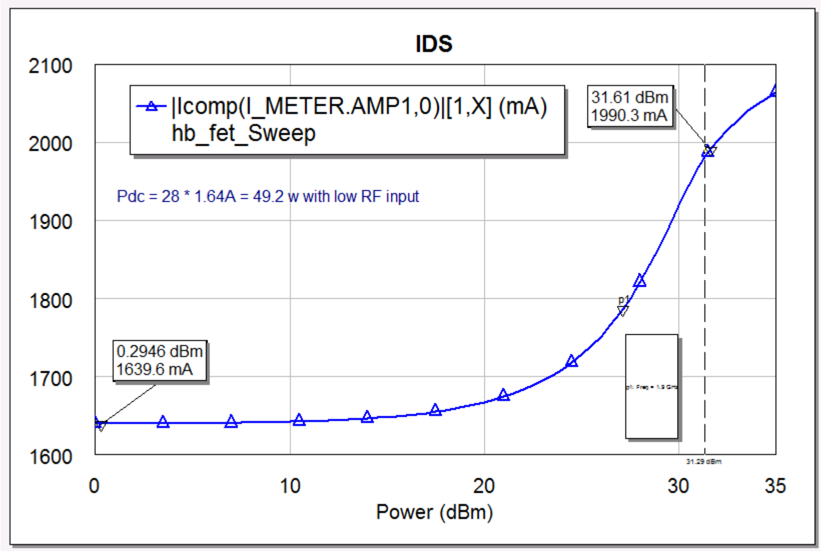


At P1dB, Second Harmonic down 17.3 dB and third down 23.2 dB
Second Harmonics follow 2dB/dB
Third Harmonic follows 3dB/dB

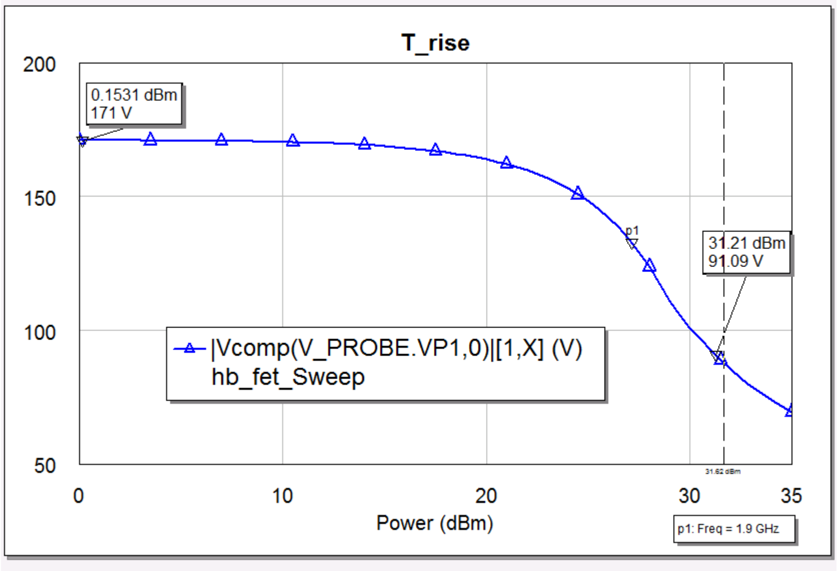


Input Matched
Note Zin changes with input power a cause of AM/PM

Pdc = 49.2 W for low RF Input Power



T = 25 + 171 = 196 ^{0}C for low RF input power



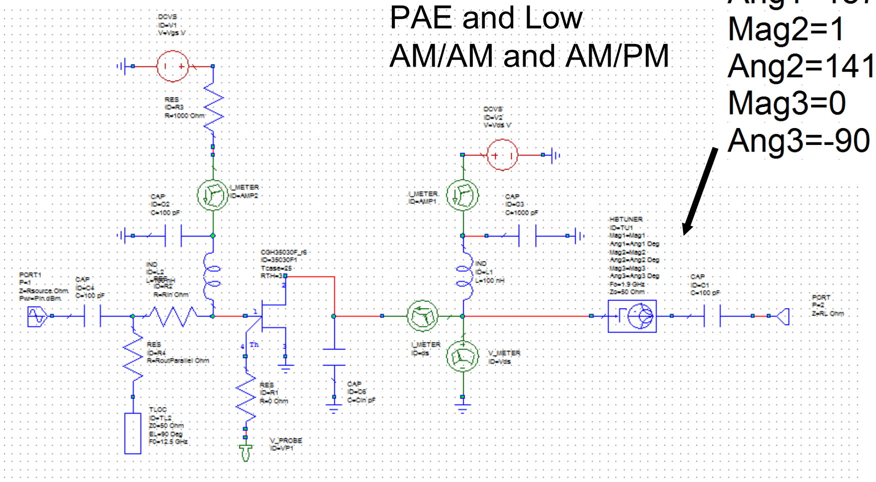
Investigate Working at Class B

- Better PAE
- Similar power
- Lower temperature for low input powers
- Better PAE at lower power compared to Class a
- However Class B has a gain and phase variation versus input power so design will sacrifice on Pout with digitally modulated signals with varying input amplitude envelop as experienced with modern digitally modulated signals like WCDMA, LTE, and WIMAX

Use Tuner for Optimization

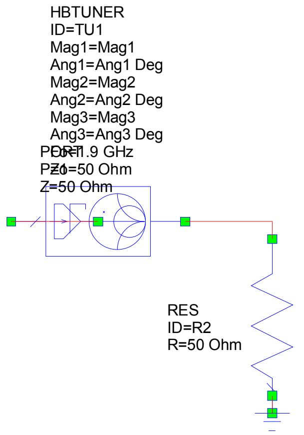
Optimum values for
Good Pout@P1dB
PAE and Low
AM/AM and AM/PM

Mag1=0.612
Ang1=157.4
Mag2=1
Ang2=141.8
Mag3=0
Ang3=-90

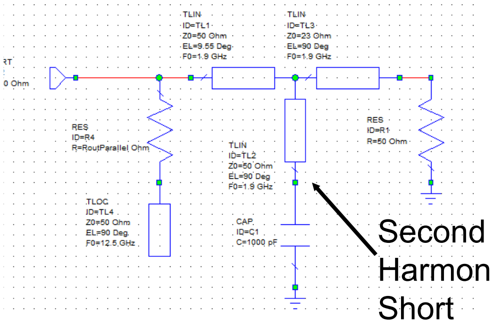


Translate the Impedances into a Circuit

Model



Circuit
Representation

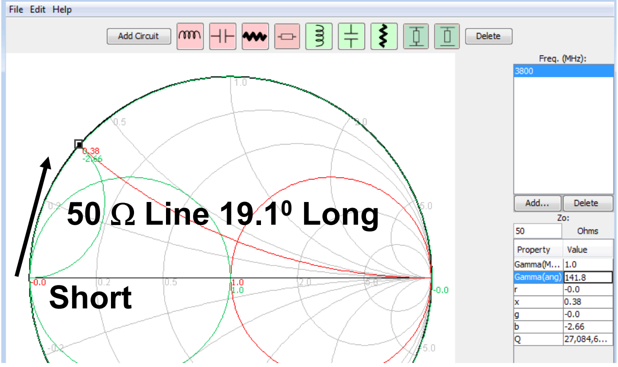


Second
Harmonic
Short

Matching at Second Harmonic

- **First we will design the second harmonic circuit close to the transistor**
- **It want to see a $\Gamma = 1@141.8^0$**

Mag2=1
Ang2=141.8



Freq. (MHz): 3800

Zo: 50 Ohms

Property	Value
Gamma(M...	1.0
Gamma(ang)	141.8
r	-0.0
x	0.38
g	-0.0
b	-2.66
Q	27,084,6...

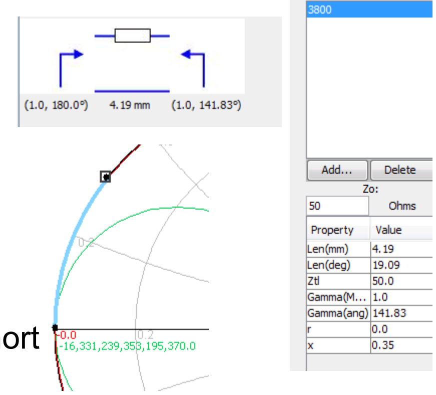
50 Ω Line 19.1^0 Long

Short

Matching at Second Harmonic

- **First we will design the second harmonic circuit close to the transistor**
- **It want to see a Γ = 1@141.8^0**
- **Add a 50 ohm line 19.1^0 long and terminate it with a short and you have the circuit as seen by the transistor This is 9.55^0 long at the fundamental**

Mag2=1
Ang2=141.8



Freq. (MHz): 3800

Zo: 50 Ohms

Property	Value
Len(mm)	4.19
Len(deg)	19.09
Ztl	50.0
Gamma(M...	1.0
Gamma(ang)	141.83
r	0.0
x	0.35

Short

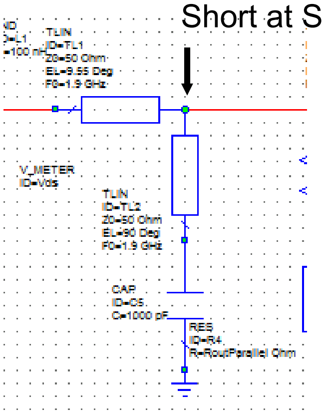
Matching at Second harmonic

- **First we will design the second harmonic circuit close to the transistor**

Short at Second harmonic

Transistor

Γ = 1@141.8^0



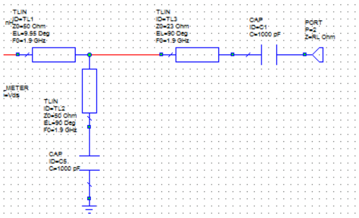
Matching at Fundamental

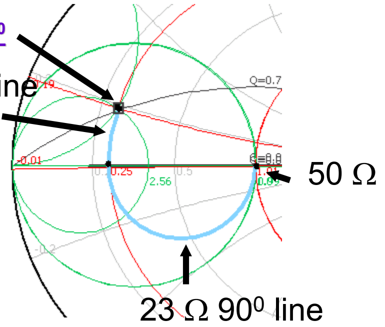
- **Now work at fundamental with the second harmonic circuit installed**

Mag1=0.612
Ang1=157.4

Transistor

Γ = **0.612@157.4^0**





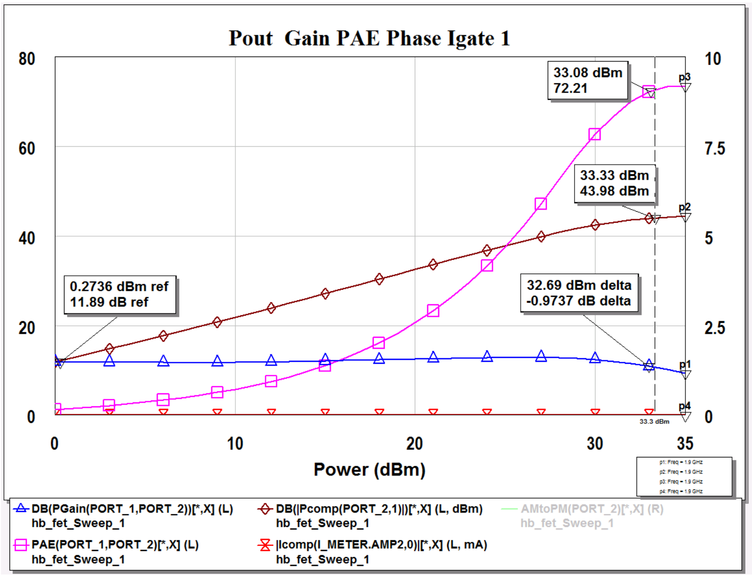
Γ = **0.612@157.4^0**

50 Ω 9.55^0 line

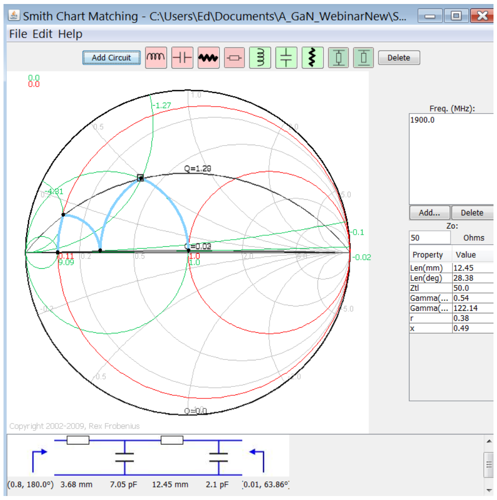
50 Ω

23 Ω 90^0 line

Results Pout = 20 W @P1dB, PAE = 72%, 11.9 dB SS Gain



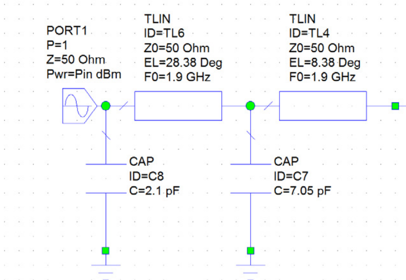
Match 5.5 Ohm Input

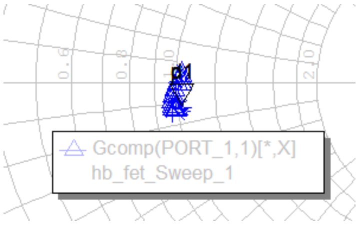


1900.0

50 Ohms

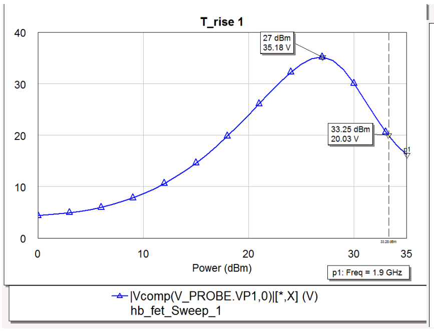
Property	Value
Len(mm)	12.45
Len(deg)	28.38
Ztl	50.0
Gamma(...	0.54
Gamma(...	122.14
r	0.38
x	0.49

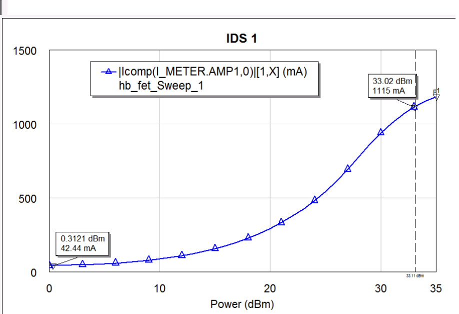




Results Pout = 20 W @P1dB, PAE = 72%, 11.9 dB SS Gain

Low temp rise 35^{0}C, DC current rises with Pin

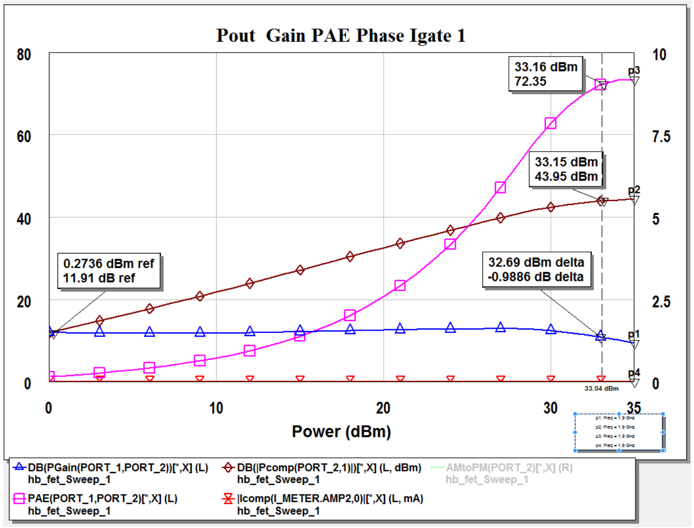




Results Pout = 20 W @P1dB, PAE = 72%, 11.9 dB SS Gain

Low temp rise 35^{0}C, DC current rises with Pin

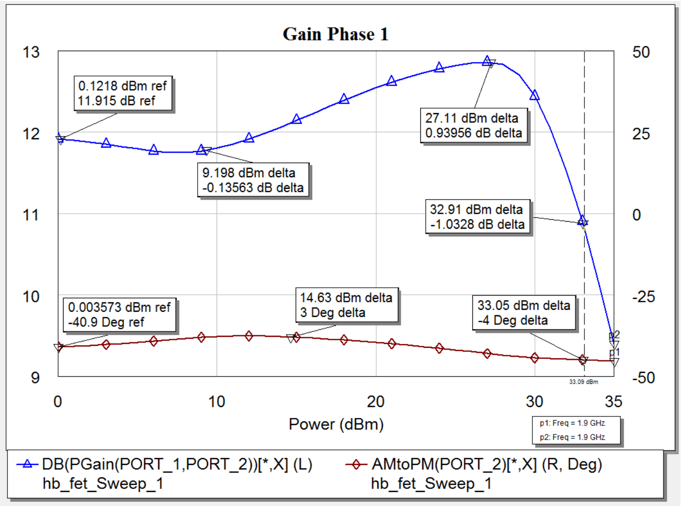
Unconditionally stable, Input Matched, however AM/AM & AM/PM variation



Results Pout = 20 W @P1dB, PAE = 72%, 11.9 dB SS Gain

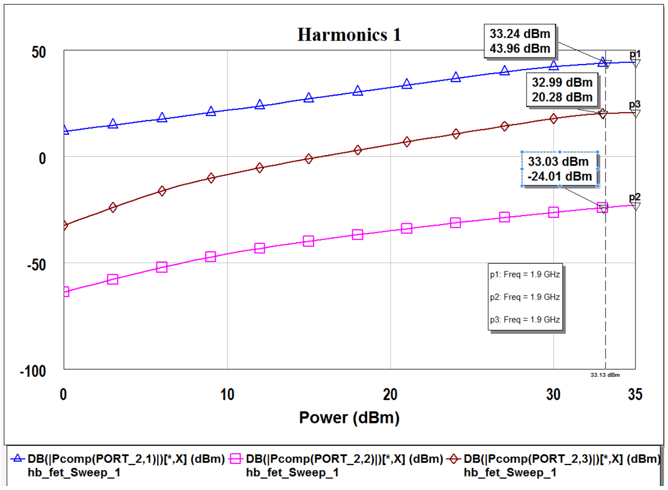
Low temp rise 35^{0}C, DC current rises with Pin

Unconditionally stable, Input Matched, however AM/AM & AM/PM variation



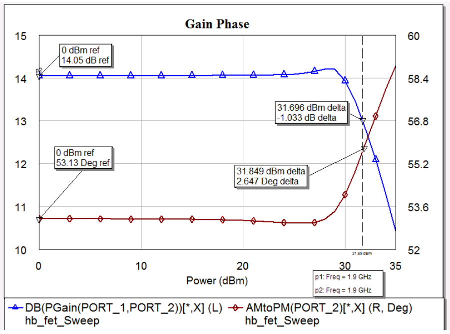
Results Pout = 20 W @P1dB, PAE = 72%, 11.9 dB SS Gain Low temp rise 35^0C, DC current rises with Pin Unconditionally stable, Input Matched, Low AM/AM & AM/PM,

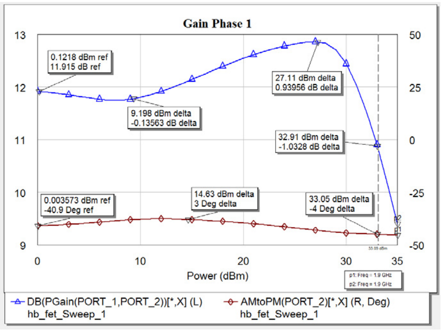
Low Harmonics



Summarization of AM/AM and AM/PM for Class A and B

Class A	Class B
Pout = 20 W @P1dB	Pout = 20 W @P1dB
PAE = 51%,	PAE = 72%,
14 dB SS Gain	11.9 dB SS Gain





Summarization of AM/AM and AM/PM for Class A and B

- Class A: Phase flat then phase increases rapidly with increasing power past around P1dB
- Class B: phase not flat with increasing power because dc average current constantly changing with increasing power. Phase increases slighly with increasing power then decreases slightly around P1dB.

Modeling GaN HEMT, GaN Nuances

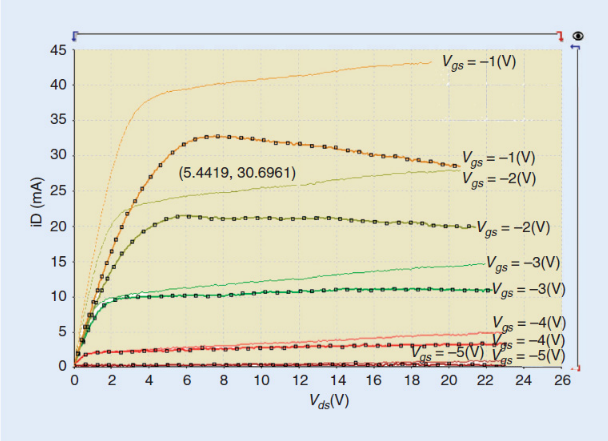
- Trapping effects and associated current-knee collapse: Increases knee voltage at which electron velocity occurs
- Bias dependencies:
  - Source resistance and drain to source resistance important
- Sub threshold valid modeling important for designers for Class B, C, D, E, and F high efficiency operating modes since not all models can fit behavior in this region. Curtice FET (CFET) model is well behaved in this region
- Models should be checked for gate voltages at or below threshold, if this is important
- Electrothermal modeling important for high voltage-current products
- Measurements must use pulsed IV characteristics

L. Dunleavy, C. Baylis, II, W. Curtice, and R. Connick, Modeling GaN: Powerful but Challenging," IEEE Microwave Magazine, pp82- 96, October 2010.

Modeling GaN HEMT

- **As GaN technology has developed, first in research laboratories and more recently in multiple commercial device manufacturers, the demand for improved nonlinear models has grown alongside the device process improvements.**
- **The need for improved models for GaN is twofold:**
  - **First, GaN devices have unique nuances in behavior to be addressed**
  - **Second, there is a desire for improved accuracy to take full advantage of the performance wins to be gained by GaN HEMT performance in the areas of high efficiency and high-power operation.**

Modeling GaN HEMT
Pulsed IV measurements are required



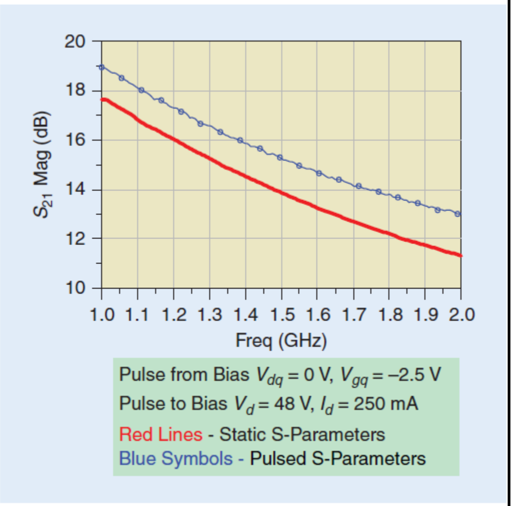
Comparison of pulsed I–V (solid lines without symbols) and static I–V for a GaN HEMT. Pulse conditions were 0.2 ms pulse width and 1-ms separation with quiescent bias set at Vdsq 5 0, Vgsq 5 0. Vgs is varied from 25 to 21 V in 1 V steps.

L. Dunleavy, C. Baylis, II, W. Curtice, and R. Connick, Modeling GaN: Powerful but Challenging," IEEE Microwave Magazine, pp82- 96, October 2010.

Modeling GaN HEMT

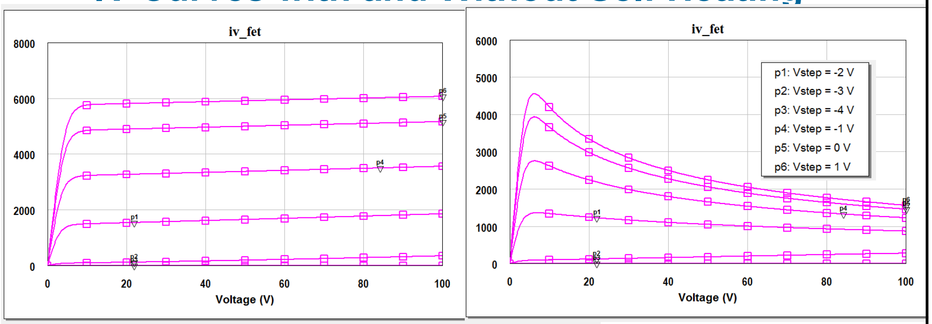
Pulsed IV Measurements Important for accurate modeling

Pulsed S-parameter and static S-parameter comparison for a 10 W GaN HEMT. Pulse conditions: 5 ms pulse width, 0.1% duty cycle (IF BW 5 1/pulse width 5 ,200 kHz).



L. Dunleavy, C. Baylis, II, W. Curtice, and R. Connick, Modeling GaN: Powerful but Challenging," IEEE Microwave Magazine, pp82- 96, October 2010.

Cree CGH3503F_r6 Device
IV Curves with and Without Self Heating



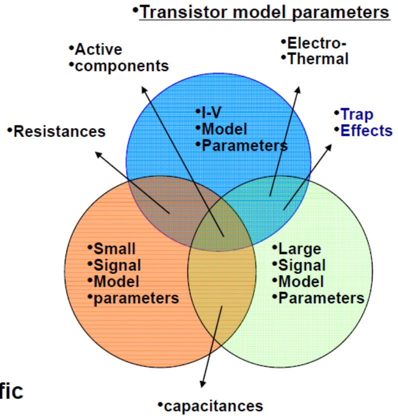
Self Heating Turned Off in Model **Self Heating Turned ON**

Electrothermal model feature essential for accurate design

Measurements for Modeling GaN HEMT

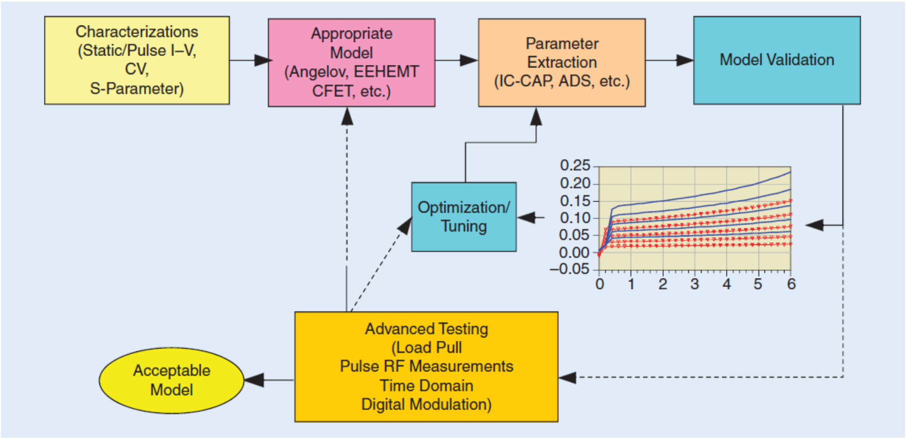
Main considerations for non-linear (NL) Empirical transistor models

- **Overall measurement accuracy**
  - Correct calibration
  - Repeatability
  - De-embedding model
  - Pulsed IV
- **Suitability of model**
  - equation set (model template) limitations/intent
  - physically meaningful parameters?
- **Model testing/validations**
  - Conventional - general
  - Advanced – application specific



IMS2011 WMJ Workshop: Modeling Considerations for GaN HEMT and Higher Level IC Devices, Dr. Larry Dunleavy, Dr. Jiang Liu, Modelithics, Inc.

Modeling GaN HEMT
Nonlinear transistor modeling process



L. Dunleavy, C. Baylis, II, W. Curtice, and R. Connick, Modeling GaN: Powerful but Challenging," IEEE Microwave Magazine, pp82- 96, October 2010.

Modeling GaN HEMT
Comparison of example FET models used for GaAs, silicon, and GaN FET/HEMT devices.

FET Models	Approx. Number of Parameters	Electrothermal (Rth-Cth) Model	Geometry Scalability Built-In	Original Device Context
Curtice3 [12]	59	No	No	GaAs MESFET
Motorola Electrothermal (MET) [25]	62	Yes	Yes	LD MOSFET
CMC (Curtice/ Modelithics/Cree) [26]	55	Yes	Yes	LD MOSFET
BSIMSOI3 [24]	191	Yes	Yes	SOI MOSFET
CFET [5]	48	Yes	Yes	HEMT
EEHEMT [13]	71	No	Yes	HEMT
Angelov [14]	80	Yes	No	HEMT/MESFET
Angelov GaN [11]	90	Yes	No	HEMT
Auriga [4]	100	Yes	Yes	HEMT
Cree (Modified Fager - Statz)	18+	Yes	Yes	HEMT

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Electrothermal Models

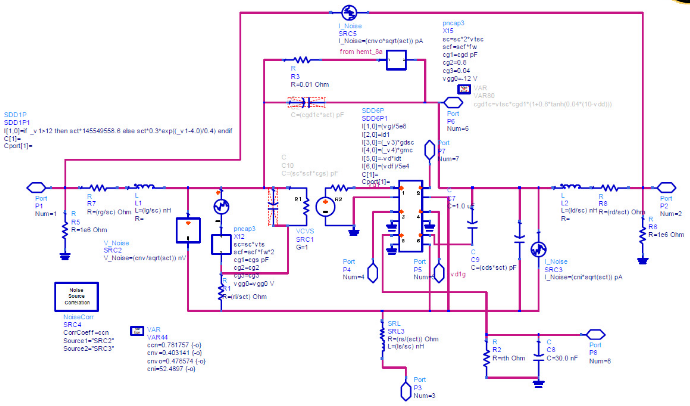
[4] Y. Tajima, "Introduction of new large signal model (LS7) for MESFET family of devices," presented at Workshop 38th European Microwave Conf.: WFR-15: Advances in Model-based HPA Design, Amsterdam, The Netherlands, Oct. 2008.

[5] W. R. Curtice, User's Guide for the C_FET Model for Agilent's Advanced Design Simulator. Washington Crossing, PA: W. R. Curtice Consulting, June 2004.

[11] I. Angelov, K. Andersson, D. Schreurs, D. Xiao, N. Rorsman1, V. Desmaris, M. Sudow, and H. Zirath, "Large-signal modelling and comparison of AlGaN/GaN HEMTs and SiC MESFETs," in Proc. Asia-Pacific Microwave Conf. 2006, Dec. 2006, pp. 279–282.

L. Dunleavy, C. Baylis, II, W. Curtice, and R. Connick, Modeling GaN: Powerful but Challenging," IEEE Microwave Magazine, pp82- 96, October 2010.

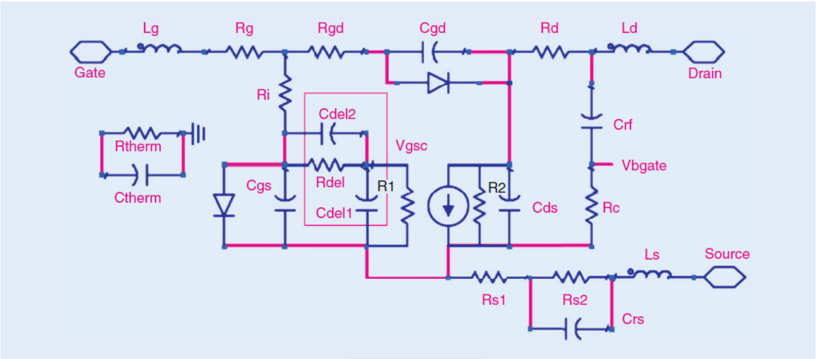
Non-linear Model Schematic



IMS2011 Baltimore WSA

"GaN MMIC Design and Modeling" Bill Pribble, Jim Milligan, Jeff Barner, Jeremy Fisher, Thomas Smith Cree, Inc. IMS2011 Workshop, "Introduction to GaN MMIC Design"

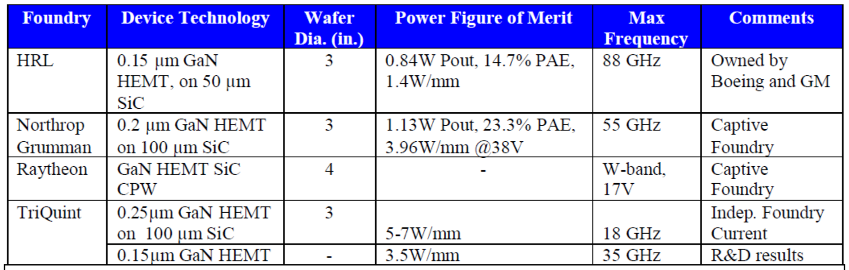
Modeling GaN HEMT
Topology for the Angelov GaN HEMT model



The electrothermal model elements Rtherm and Ctherm enable estimation of channel temperature rise due to power dissipation And varies model parameters to account for temperature rise.

Angelov, K. Andersson, D. Schreurs, D. Xiao, N. Rorsman1, V. Desmaris, M. Sudow, and H. Zirath, "Large-signal modelling and comparison of AlGaN/GaN HEMTs and SiC MESFETs," in Proc. Asia-Pacific Microwave Conf. 2006, Dec. 2006, pp. 279–282.

Millimeter Wave MMIC Foundries



Foundry	Device Technology	Wafer Dia. (in.)	Power Figure of Merit	Max Frequency	Comments
HRL	0.15 µm GaN HEMT, on 50 µm SiC	3	0.84W Pout, 14.7% PAE, 1.4W/mm	88 GHz	Owned by Boeing and GM
Northrop Grumman	0.2 µm GaN HEMT on 100 µm SiC	3	1.13W Pout, 23.3% PAE, 3.96W/mm @38V	55 GHz	Captive Foundry
Raytheon	GaN HEMT SiC CPW	4	-	W-band, 17V	Captive Foundry
TriQuint	0.25µm GaN HEMT on 100 µm SiC	3	5-7W/mm	18 GHz	Indep. Foundry Current
	0.15µm GaN HEMT	-	3.5W/mm	35 GHz	R&D results

BAE 0.2mm Non field Plate HEMT, ft = 50 GHz, fmax = 220 GHz, 5W/mm, 46% PAE at 30 GHz

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10W WIMAX PA Design

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10W WIMAX PA Design

- Transistor:
  - Eudyna 10W GaN HEMT amplifier, EGN010MK
  - Vds = 50V
  - Ids = 100 ma (no RF power) deep class b
- Frequency range: 3.4 to 3.8 GHz
- Design objectives: (at P1.5 dB)
  - Power > 41 dBm
  - PAE > 70%
  - η > 80%
  - G > 8.5 dB
  - Stable 0.1 to 10 GHz
  - Input return loss > 15 dB

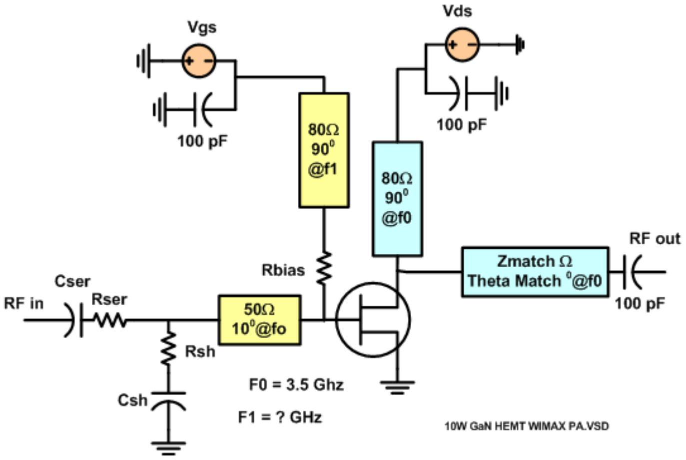
PA Design Steps

- Step 1:
  - Examine IV Curves and note knee voltage (one point on load line) and no current point at Vgs = 95 V
  - Note input dc voltage for no gate current
  - Determine Vgs for 100 ma of current
  - AWR circuit GaN HEMT WIMAX PA Step1
- Step 2:
  - Examine Load Pull data and determine optimum load for max power at Pin = 30 dBm
  - Determine circuit using transmission line. Hint try a length of line of length theta and impedance Zmatch
  - Examine Pout vs Pin and Pout vs freq at Pin = 30 dBm
  - Optimize circuit for operation over full frequency
  - AWR circuit GaN HEMT WIMAX PA Step2

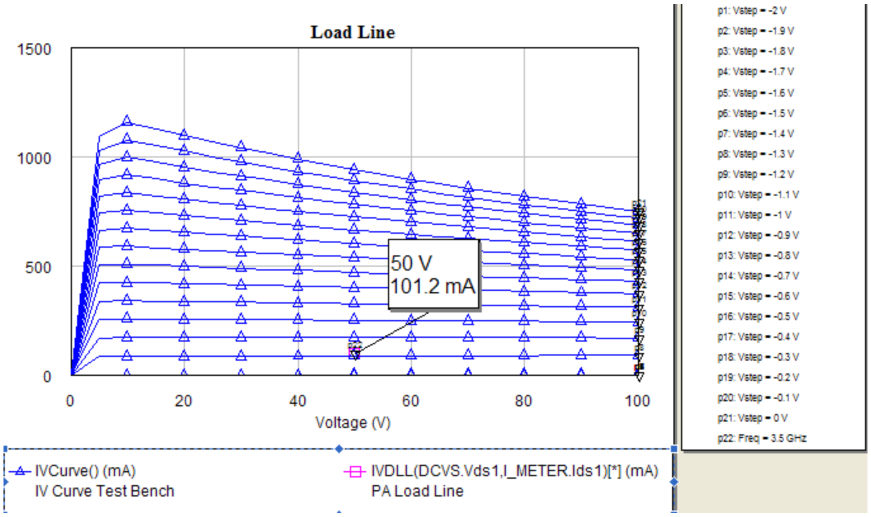
PA Design Steps

- Step 3:
  - Match input at Pin = 30 dBm over frequency. Need to use a 10 degree 50 Ω length of line on input in order to solder input transistor lead
  - Suggestion: try a shunt cap and series which will also serve as an input blocking cap
  - Examine circuit stability (k, MU2, input stability plane
  - AWR circuit GaN HEMT WIMAX PA Step3
- Step 4:
  - Now examine stability (k factor and MU2 as well as input stability plane) and completely stabilize circuit with minimal degradation of gain and rematch input circuit. This is the hardest step
  - AWR circuit GaN HEMT WIMAX PA Step5
  - Suggestion: See schematic next page
  - Try to keep Rsh equal to or greater than 200 Ω so that gain is not severely reduced
  - AWR circuit GaN HEMT WIMAX PA Step4

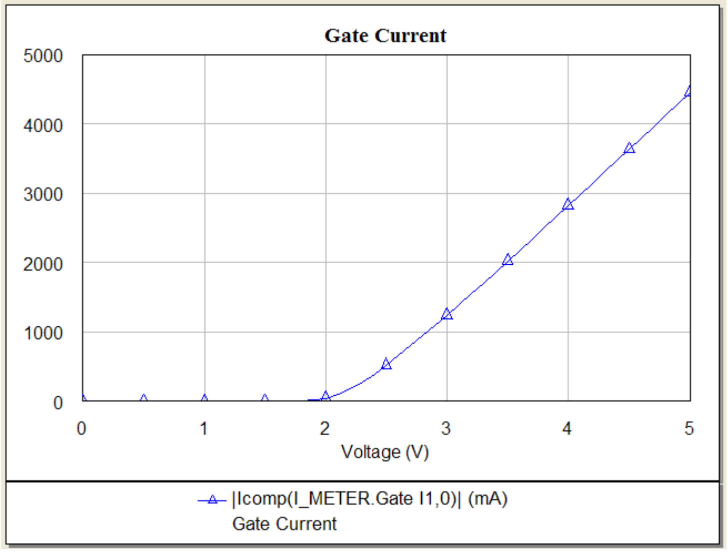
Suggested Circuit Schematic for Stability



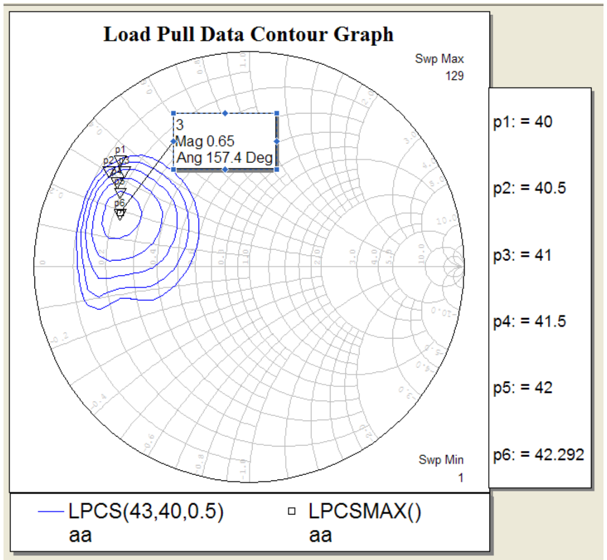
Results: Step 1



Results: Step 1

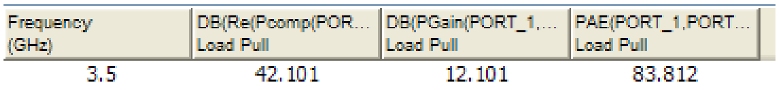


Results: Step 2



Results: Step 2

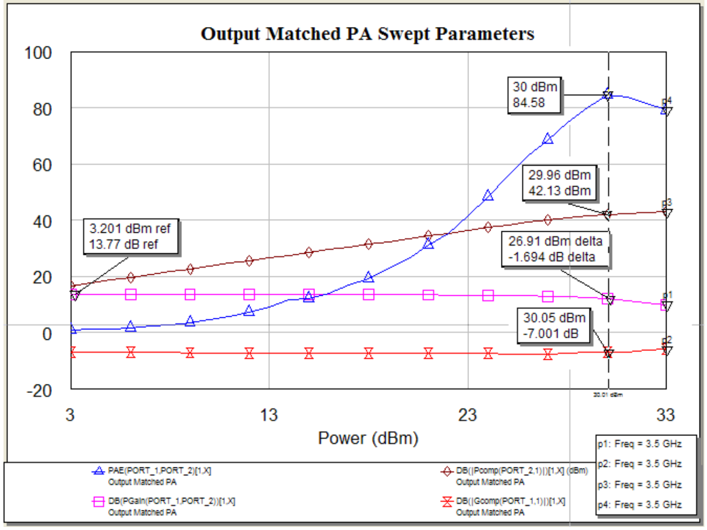
- **Optimize circuit for Pout > 43 dBm, PAE > 80% with Pin = 30 dBm and f = 3.5 GHz**



Frequency (GHz)	DB(Re(Pcomp(POR… Load Pull	DB(PGain(PORT_1,… Load Pull	PAE(PORT_1,PORT… Load Pull
3.5	42.101	12.101	83.812

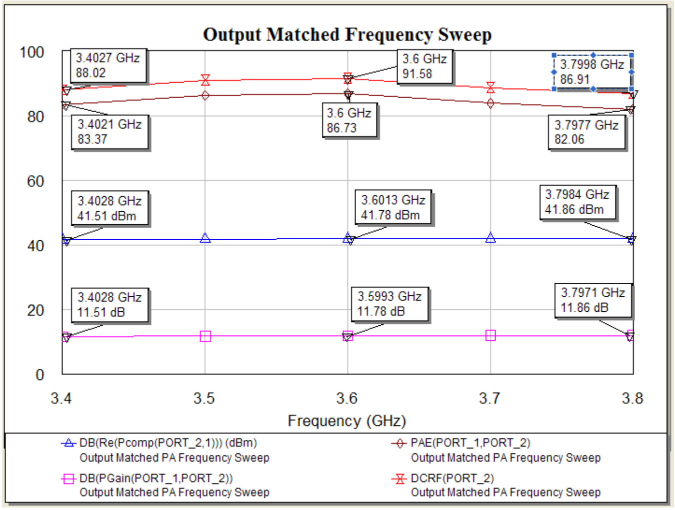
Results: Step 2

- **Review parameters versus Pin**



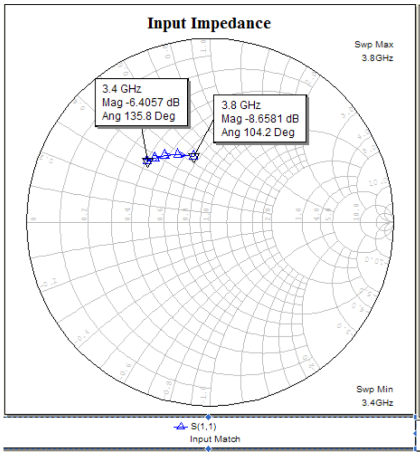
Results: Step 2

- **Optimize over frequency: 3.4 to 3.8 GHz**

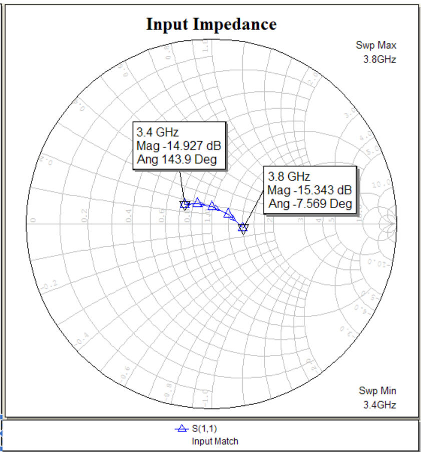


Results: Step 3 Input Match

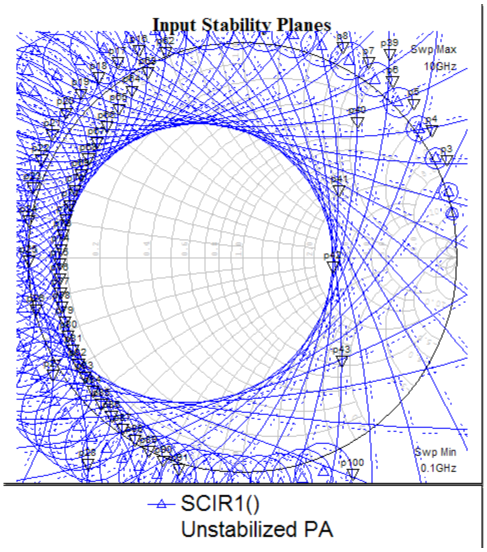
- **Unmatched**



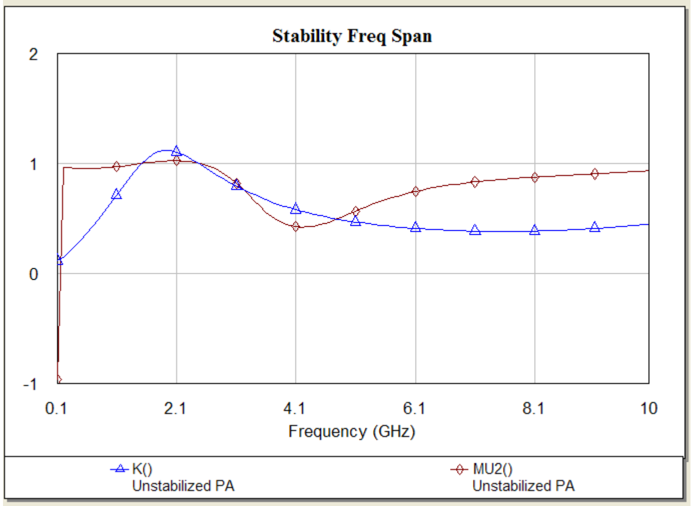
- **Matched**



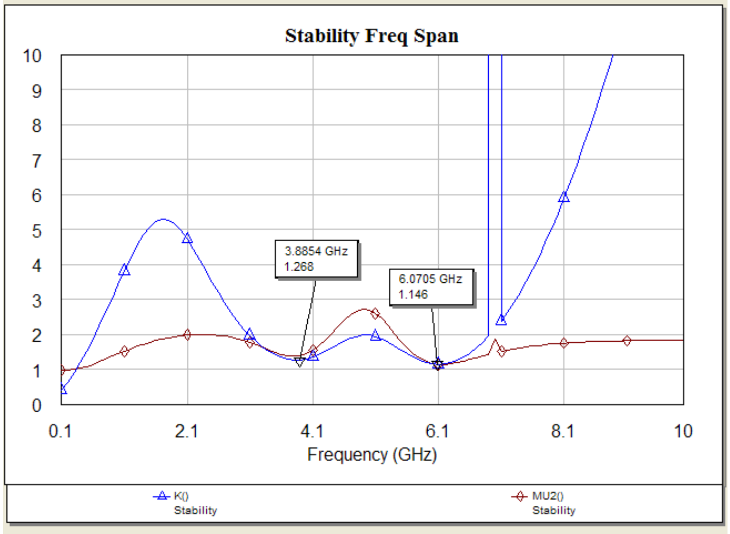
Results: Step 3 Unstabilized Stability



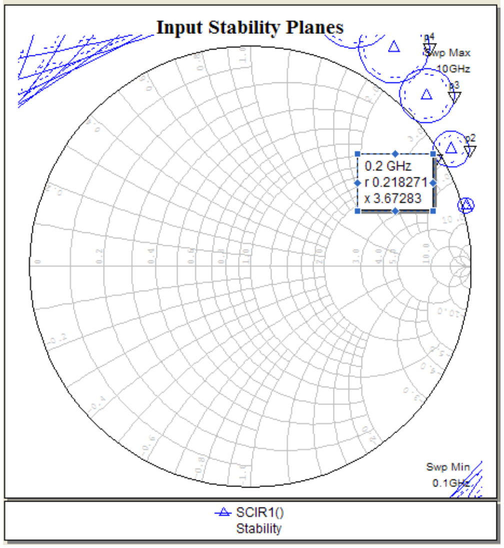
Results: Step 3 Unstabilized Stability



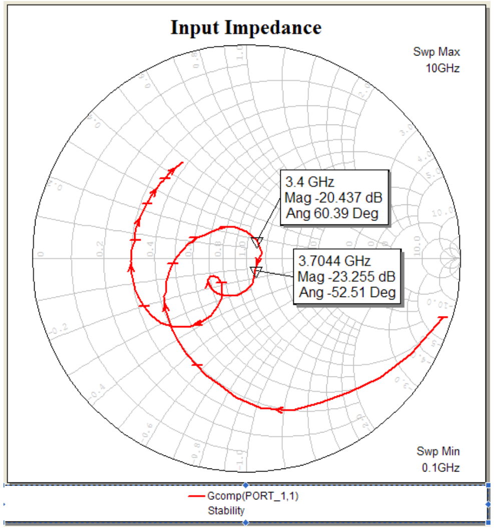
Results: Step 4 Stabilized Stability



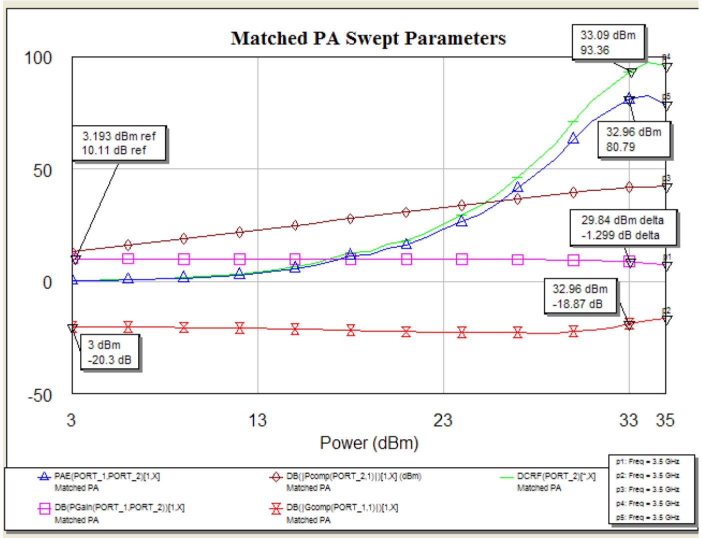
Results: Step 4 Stabilized Stability



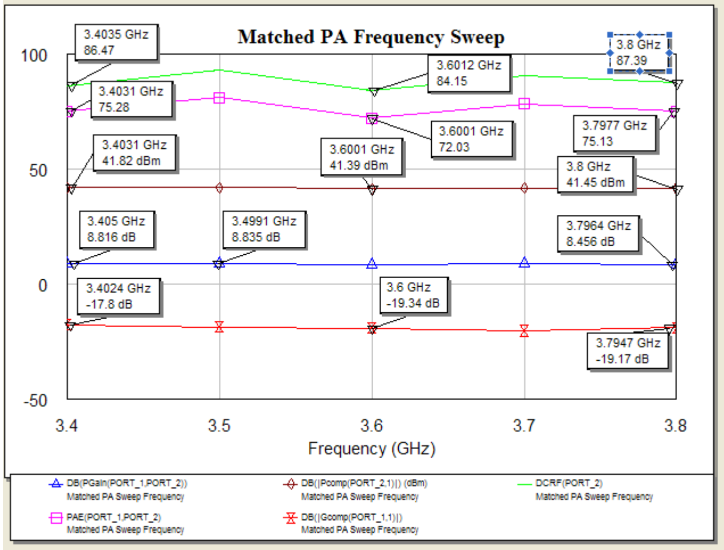
Results: Step 4 : Input Match



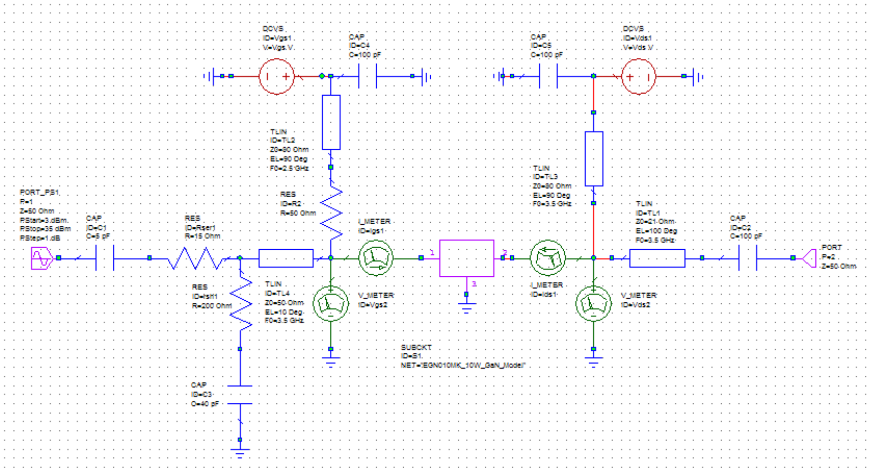
Results: Step 4 : Power Sweep

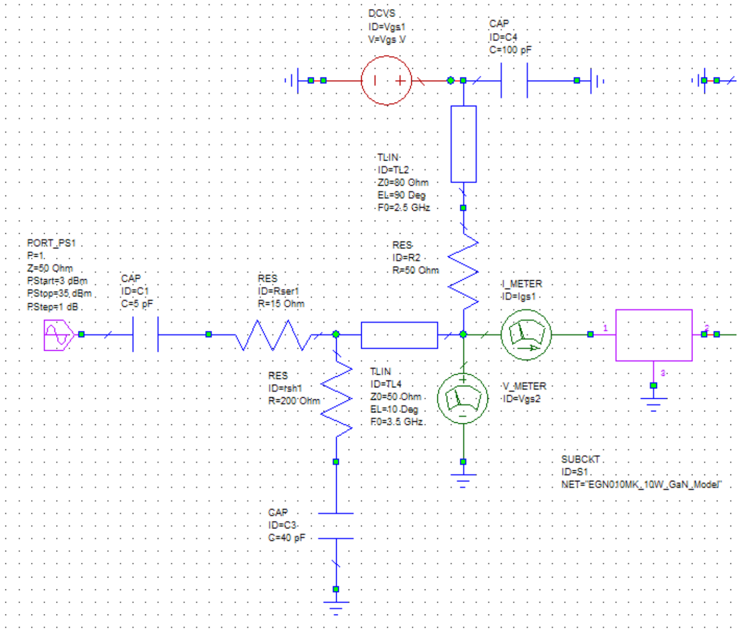


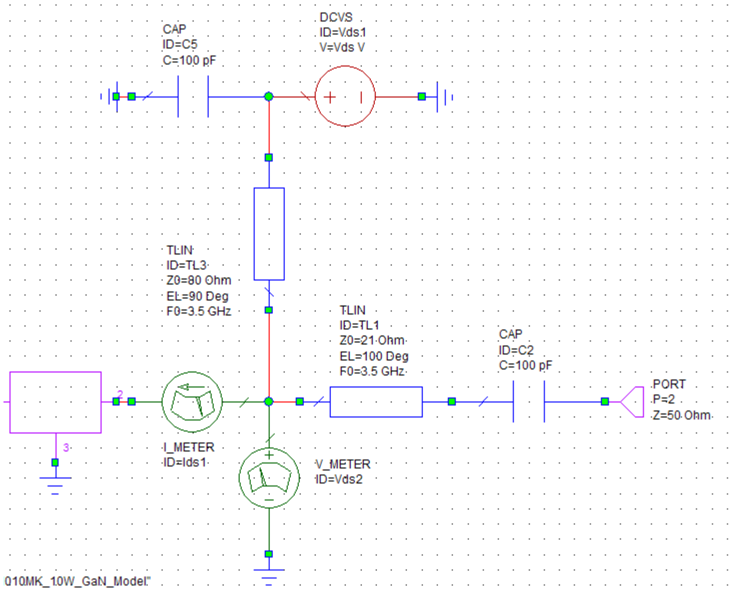
Results: Step 4 : Frequency Sweep Pin = 33 dBm



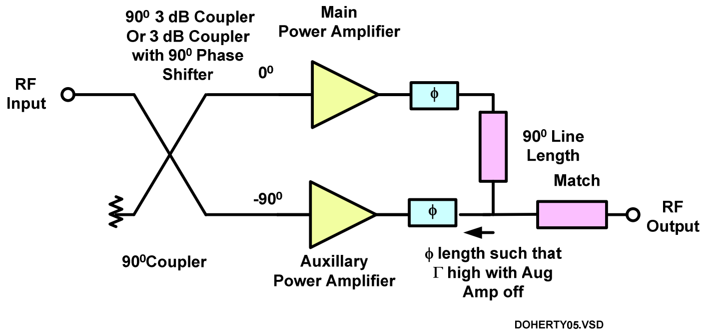
Final Schematic







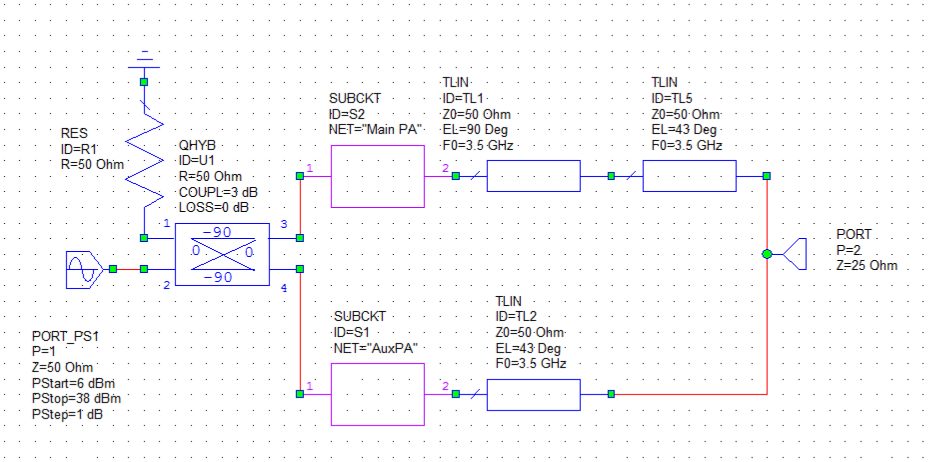
Doherty Amplifier Design



- Main Amp Class AB, Aux amp Class C
- At -6dB for high power, aux amp turned off
- Each amp changes load that each sees resulting in better efficiency and linear power

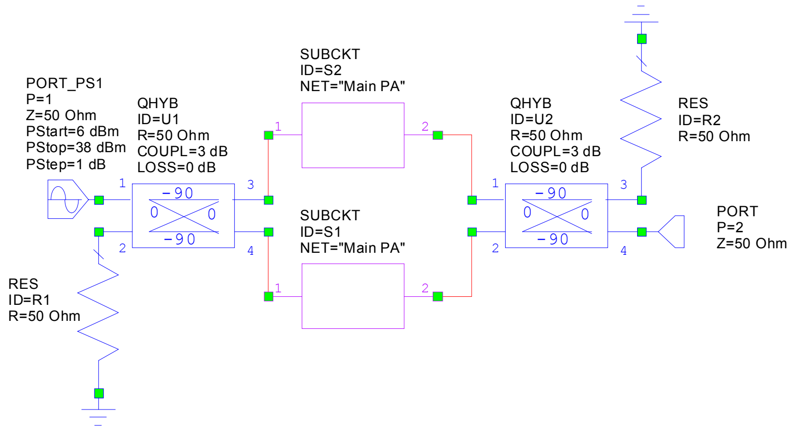
Design Doherty PA Using 10W WIMAX PA

- **AWR Balanced PA for Comparison**



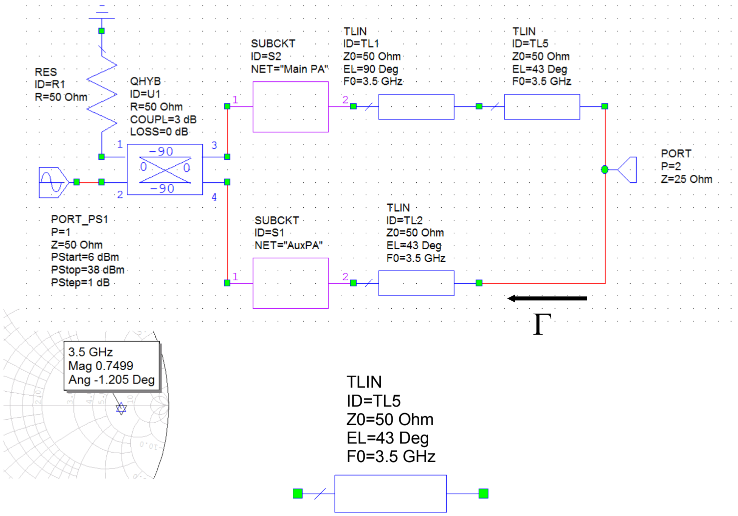
Design Doherty PA Using 10W WIMAX PA

- **AWR Balanced PA for Comparison**



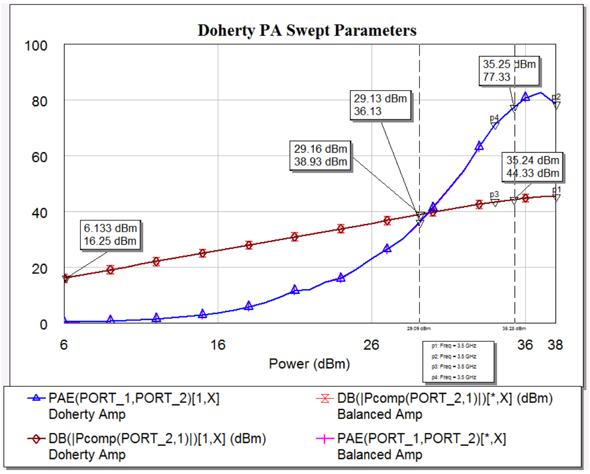
Design Doherty PA Using 10W WIMAX PA

- **ϕ length set to 43^0 for high output Reflection Coefficient (Γ) Aux PA when turned off**



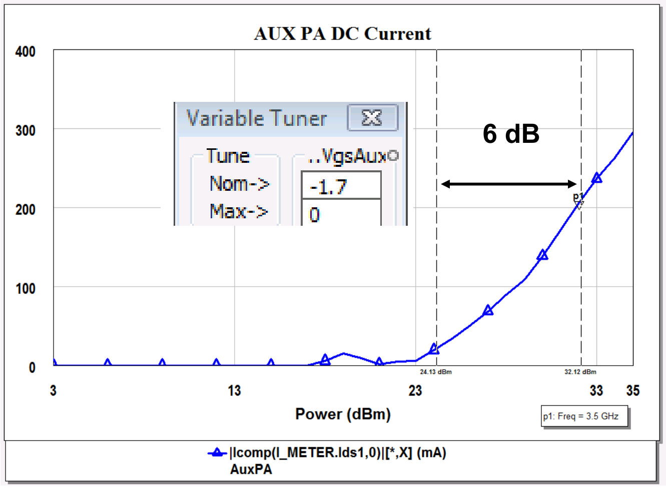
Design Doherty PA Using 10W WIMAX PA

- **Performance the same for both circuits with equal gate biases for each PA**



Design Doherty PA Using 10W WIMAX PA

- Examine DC Current of Aux PA and adjust so that at 6 dB down the Transistor DC current is zero so the aux PA should be turned off



Tune ..VgsAux
Nom-> -1.7
Max-> 0

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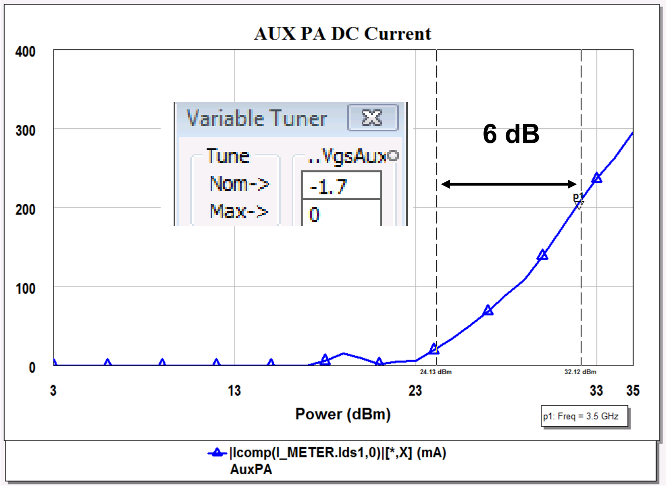
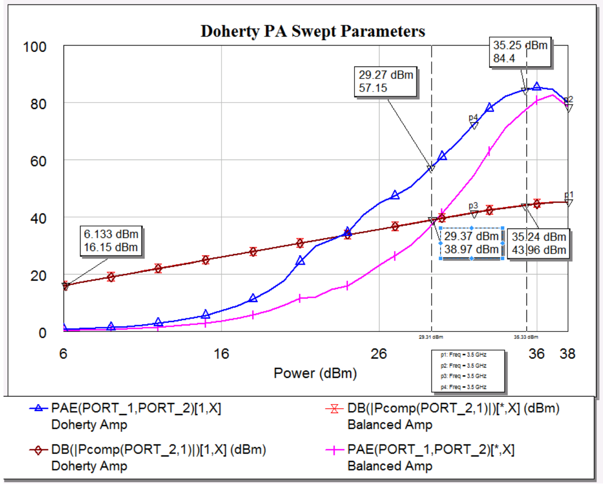


Tune ..VgsAux
Nom-> -1.7
Max-> 0

Design Doherty PA Using 10W WIMAX PA

- Performance enhanced with similar PA output with significant enhancement of PAE
- Suspect there is a problem with nonlinear model operating in deep class C
- The exercise does show technique and better performance but not that of theoretical performance (Same PAE at 6 dB backoff)



Conclusions

- GaN HEMT for power amplifiers
  - High breakdown voltages with Vds dc operation at 28 to 50 V depending on manufacturer
  - How power in a small footprint requiring care to get the heat out
  - High reliability operation MTBF 10^6 to 10^8
  - More easily matched due to high voltage operation and small equivalent capacitances and high bandwidth operation
  - Design techniques shown for class a and class b operation
  - Design techniques shown for digitally modulated signals as well as Dougherty PA operation