DO-254 CTS

Meeting Agenda

- Aldec's Positioning in DO-254
- FPGA Level Verification with DO-254 CTS
  - ✓ Main Features, Components, Deliverables and Methodology
  - ✓ Challenges with Traditional Methods
  - ✓ Compliance with Chapter 6.2 Verification Process
  - ✓ Customer Design Examples

Aldec's Positioning in DO-254

- ✓ Help applicants comply with chapter 6.2 Verification Process (Level A/B)
- ✓ Provide a fully customized hardware/software to verify the design at-speed in the target device
- ✓ FPGA Level Functional Verification
- ✓ Automated and single testing environment to verify all FPGA requirements
- ✓ Decrease verification cycle

FPGA Level Verification

"The verification process may be applied at any level of the design hierarchy as defined in the hardware verification plan."

Chapter 6.2 RTCA DO-254 Spec

". . . It is not intended that requirements should be verified at every hierarchical level . . . "

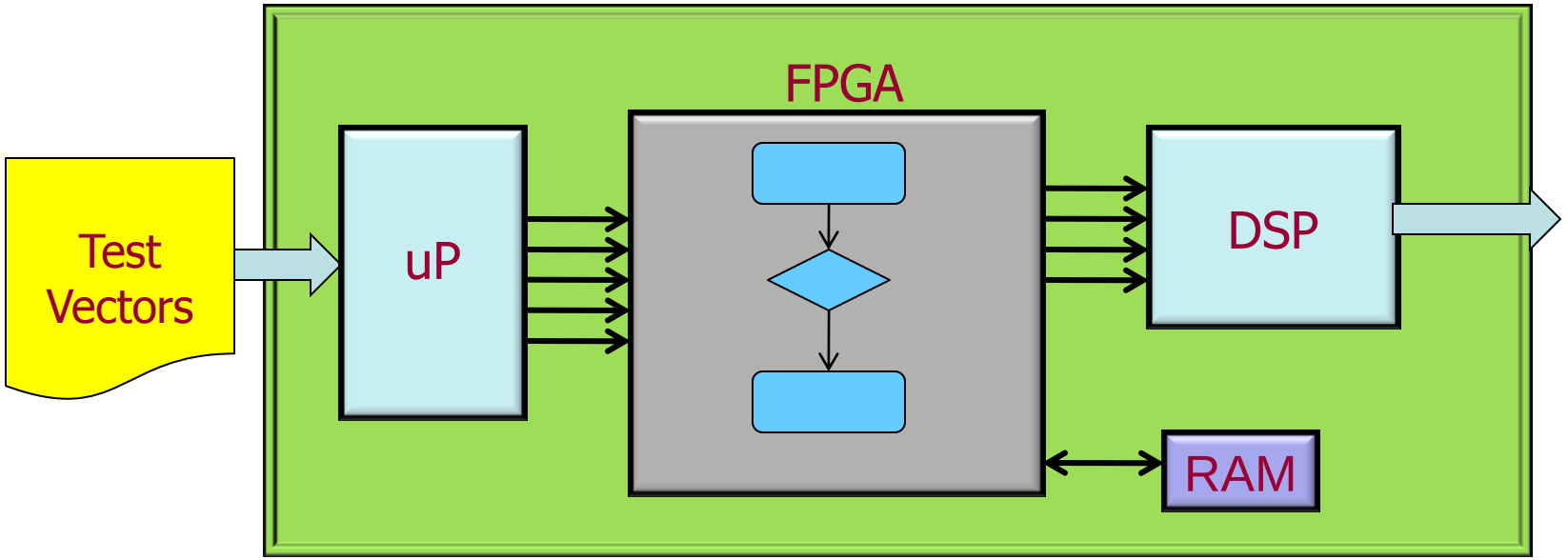
Chapter 6.2.2 RTCA DO-254 Spec

"When it is not feasible to verify specific requirements by exercising the hardware item in its intended operational environment, other verification means should be provided, and justified."

Chapter 6.3.1 RTCA DO-254 Spec

Traditional Hardware Verification

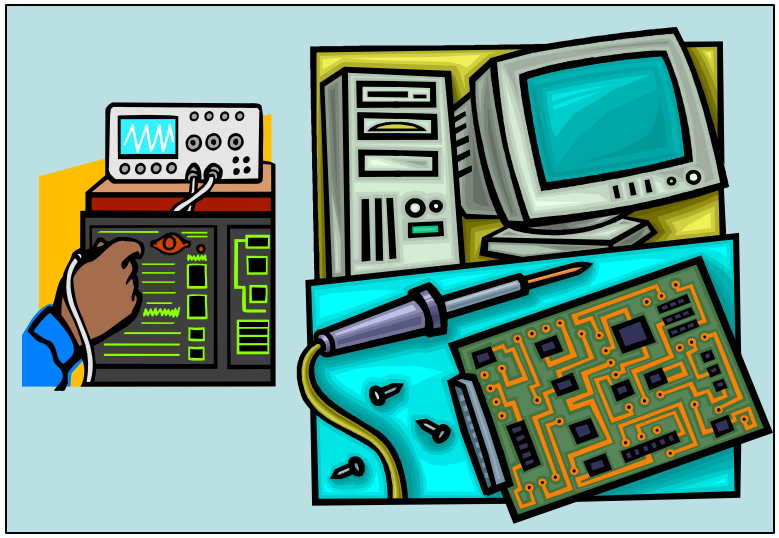
- Real-time data is streaming through the design inputs
- Design outputs (FPGA) are connected to other components on the board
- No test headers on the FPGA I/Os



Board Under Test

Traditional Hardware Verification Challenges

- Ensuring RTL and Hardware simulation results match
- Development of input data to cover all the design requirements (time!)
- Limited visibility and controllability on the FPGA I/Os
- Preserving documentation of results
- How to automate the testing environment for many test cases?



Traditional Hardware Testing Methods vs. DO-254 CTS

	Traditional Hardware Verification	Aldec's DO-254 CTS Approach
Input Type	Data	RTL Test Vectors
Verification Type	At Speed	At Speed
Target Device	Yes	Yes
Test Data Generation	Manual engineering time required	Automatic, no additional development required
Test Environment Setup	Manual connections of wires and cables	PCIe based Hardware Boards
FPGA I/O Access	Limited controllability	Complete controllability and visibility
Output Format	From Logic Analyzer, Oscilloscope	RTL Simulator Waveform Format
RTL and Hardware Results Comparison	Limited	Easy and automated
Result Documentation	Manual documentation	Automatically generated waveform and PDF export
FPGA Device Verification Time	Manual Process and takes months to complete, thus development cost is very high	Automated process and only takes weeks to complete, thus development cost is reduced substantially

FPGA Level Verification with DO-254 CTS

- At-speed verification in the target device
- Reusing testbench as test vectors for in-hardware testing
- No changes in the design and testbench
- Easy results capturing, analysis and documentation
- Supports Chapter 6.2 Verification Process
- Supports Chapter 11.4 Tool Assessment and Qualification Process

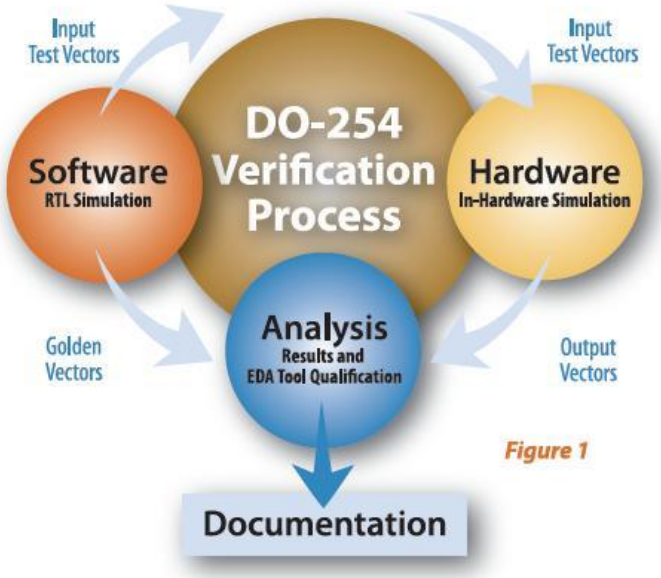


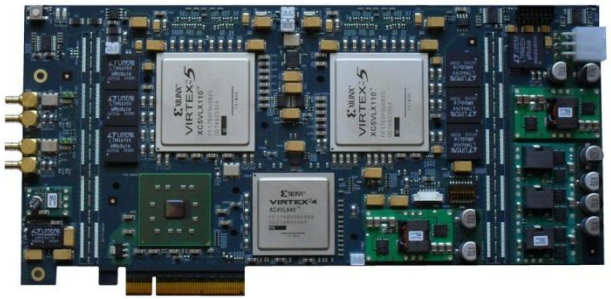
Figure 1

DO-254 CTS Components

DO-254 CTS CVT (Software)

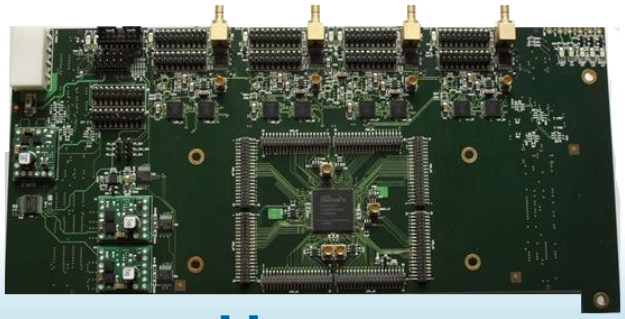
- Converts final testbench into test vectors
- Controls In-Hardware Verification
- Writes hardware results to a waveform file

COTS Mother Board



- Provides test vectors into daughter board "at speed"
- 1-environment to test all FPGA requirements
- Samples FPGA outputs "at speed"
- PCI/e interface to PC

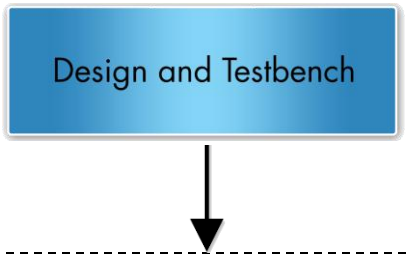
Customized Daughter Board

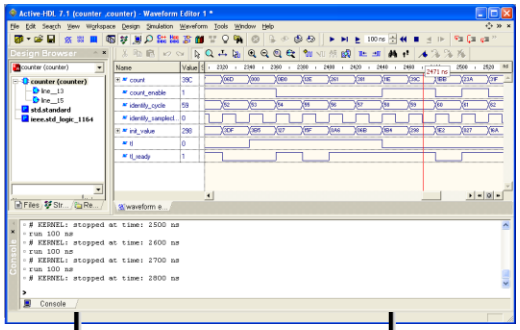


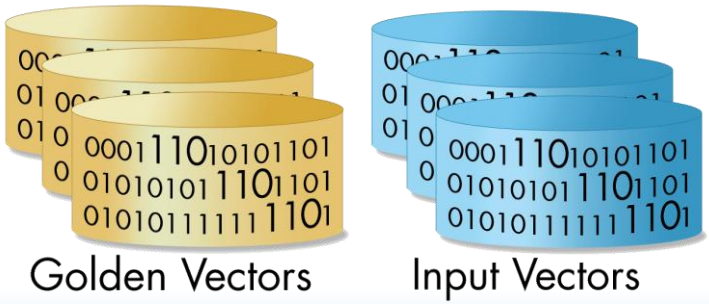
- FPGA level verification
- Customized to target FPGA and DUT
- Contains target FPGA and DUT

DO-254 CTS Methodology (Part 1)

Test Vectors Generation







INPUT

- Design under test – from customer, no changes required
- Testbench for DUT – from customer, no changes required

TOOLS

- HDL Simulator – Aldec or third party
- CVT plugin – Test Vectors Conversion (TVD)

ACTIONS

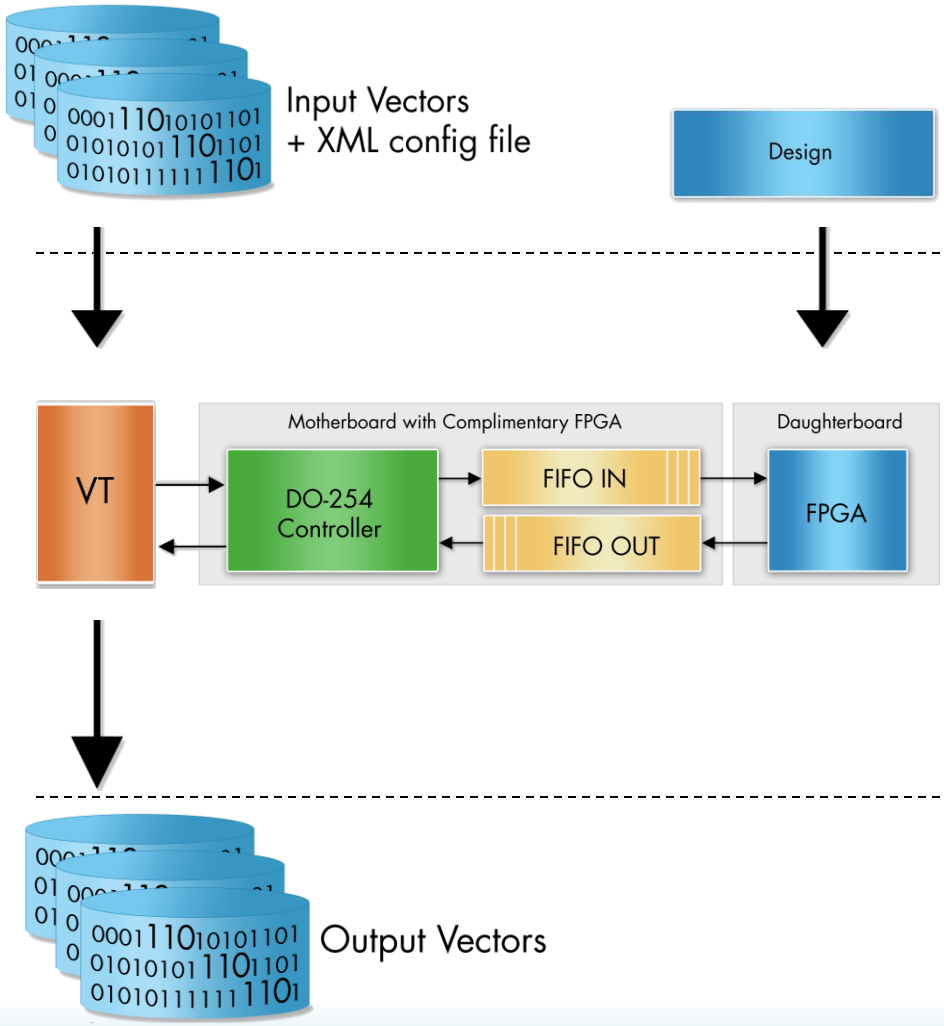
- Running RTL simulation
- Test vectors generation

OUTPUT

- Golden Vectors – RTL simulation results
- Input Vectors – RTL input vectors to be used for in-hardware simulation

DO-254 CTS Methodology (Part 2)

In-Hardware Simulation At Speed



INPUT

- Design under test (binary post implementation) – provided by customer, no changes required
- Input Vectors – the same for RTL simulation
- CVT config file – XML format

TOOLS

- Verification Tool (VT) – controls in-hw simulation
- Mother Board – contains DO-254 controller
- Daughter Board with a target device

ACTIONS

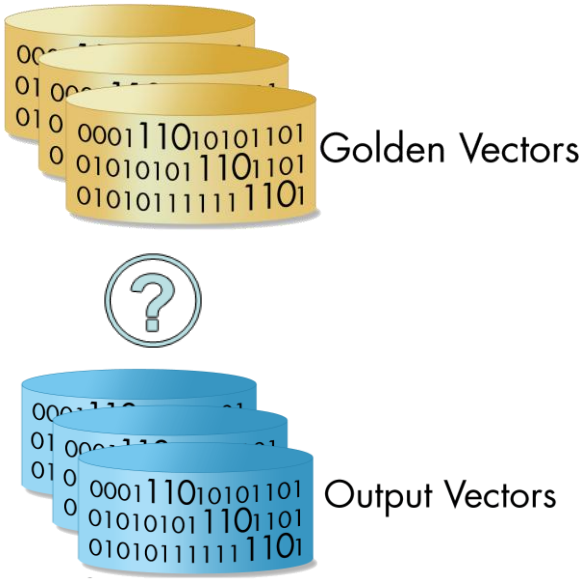
- Programming target FPGA
- In-hardware testing - at-speed (MHz)
- In-hardware test results generation

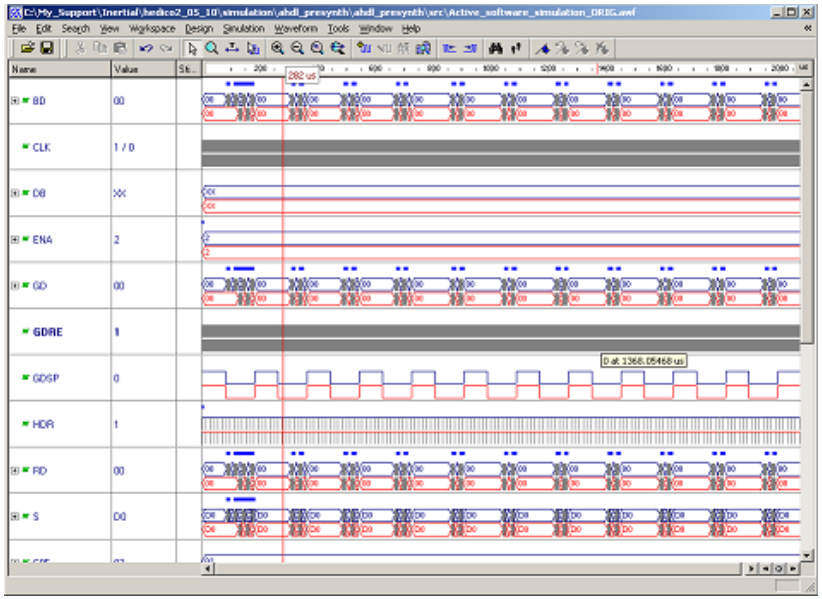
OUTPUT

- Output Vectors – in-hardware simulation results

Hardware Output Validation

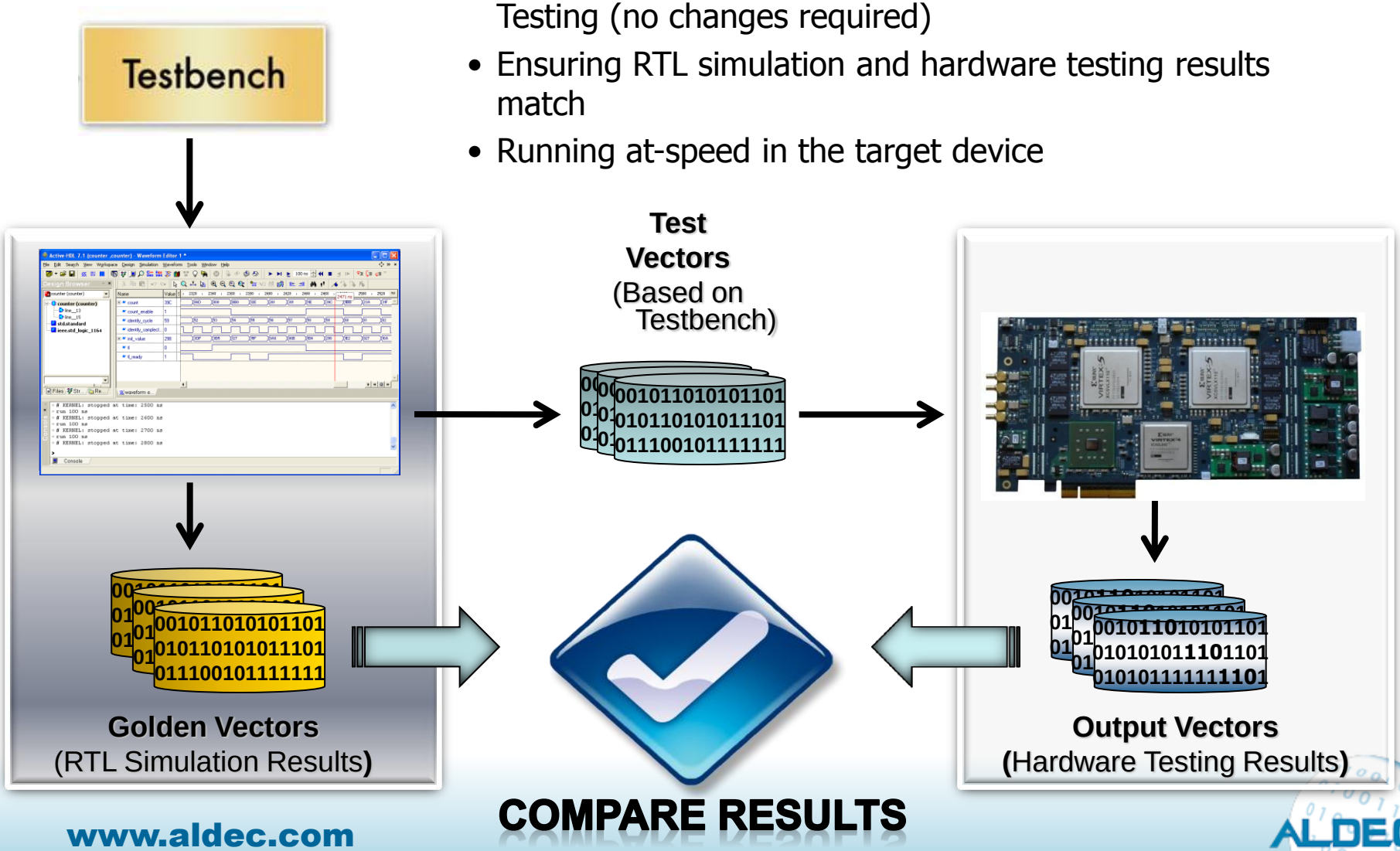
- Visual analysis of generated waveforms
- Golden vectors are generated during RTL simulation
- Output vectors from in-hardware simulation are compared
  - graphically as waveform files
  - as two binary files





Compliance with Chapter 6.2 Verification Process

- The simulation is driven by the same Testbench
- The same design is used for RTL Simulation and Hardware Testing (no changes required)
- Ensuring RTL simulation and hardware testing results match
- Running at-speed in the target device



Our Customer's Design Example - #1

Design Parameters	
Target device	Altera Cyclone II EP2C8-I8 BGA 256
Design clocks	4 clocks: @256 MHz @128MHz, @128MHz, @32MHz
Total I/O	84
Verification time	50 ms
Verification type	Test vectors based verification
Verification Tool Requirements	
At-speed testing in target device – High Speed and Low Speed modes	
Reuse of RTL test vectors	
Results capturing and documenting	
Automated verification environment	

Our Customer's Design Example - #2

Design Parameters	
Target device	Altera Cyclone III EP3C40F780C8
Design clocks	3 clocks: @65MHz, @13MHz, @66MHz
Clock modules	**PLL to drive all clocks**
Total I/O	**370 I/Os: IN:167 – include LVDS and SER-DES, OUT:116, INOUT:87**
Verification time	**300 ms**
Verification type	Test vectors based verification
Verification Tool Requirements	
At-speed testing in target device – High Speed	
Reuse of RTL test vectors	
Results capturing and documenting	
Automated verification environment	
Variable voltage testing - +/- 10%	

Our Customer's Design Example - #3

Design Parameters	
Target device	**Xilinx SPARTAN 3A** XC3S700A-FG400I
Design clocks	2 clocks: @48 MHz, @40MHz, **50MHz (reserve), @80MHz (internal)**
Clock modules	**DCM** for internal operation only
Total I/O	212 I/Os: **IN:135 , OUT:61, INOUT:16**
Verification time	200 ms
Verification type	Test vectors based verification
Verification Tool Requirements	
At-speed testing in target device – High Speed	
Reuse of RTL test vectors	
Results capturing and documenting	
Automated verification environment	
Spare I/Os and clocks for future DB reuse, All I/O available on gold-pins	

Open discussion questions

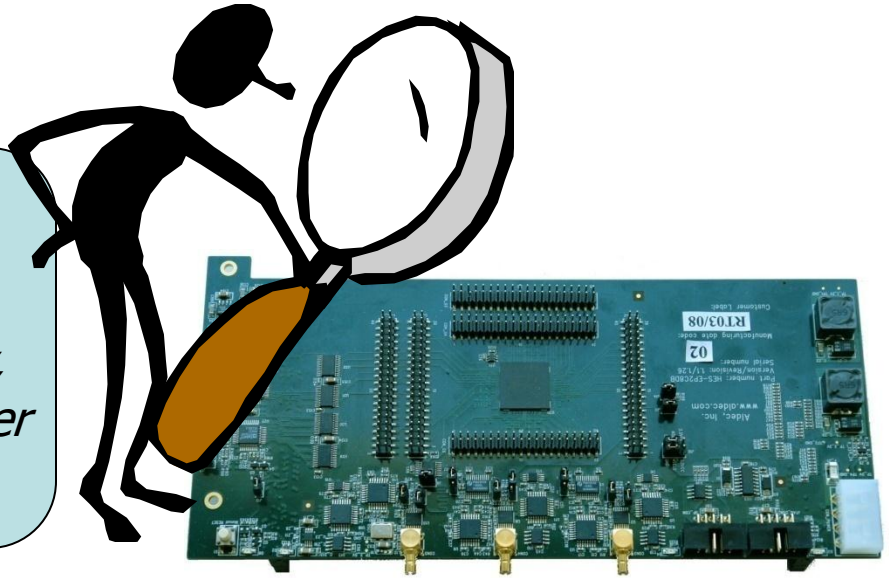
FPGA Testing with a Daughter Board

- Allows testing of the DUT in the target device

… DO-254 requires testing of Level A/B designs on the target device

- Testing "at speed"
- Provides 1 testing environment to test all FPGA requirements, and fully customized to specified requirements
- A wrapper is not required to drive the design in real hardware

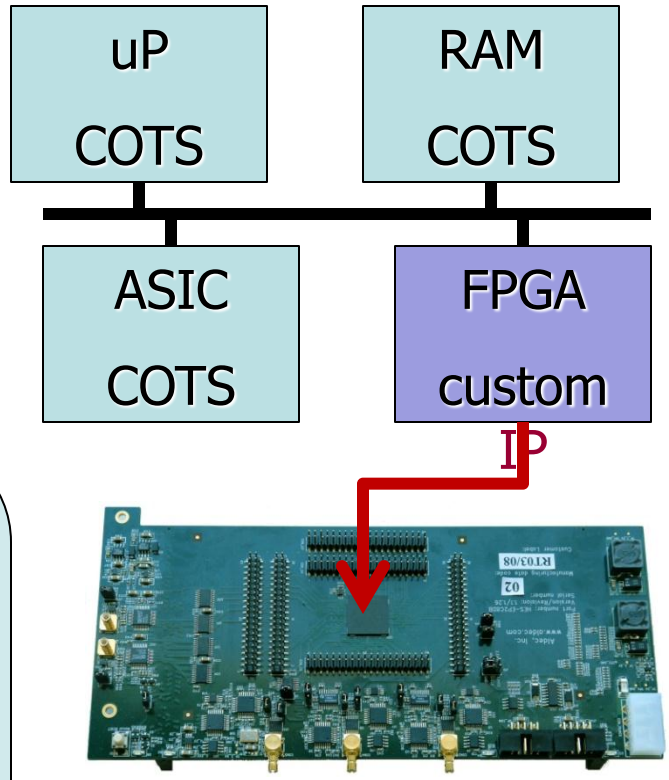
… A wrapper adds code that no longer represents what the FPGA requirements indicate
… A wrapper adds a level of uncertainty, so that if a bug is found, is it the wrapper or is it the hardware?



FPGA Level Testing with DO-254 CTS

Board Level Testing

- **For final PCB with all board components**
- Confirms correct operation of complete board
  - Board level functions
  - Physical parameters and characteristics
  - Board components interfaces
- Environmental testing



FPGA Level Testing

- For reconfigurable components like FPGA

BENEFITS

- FPGA is fully debugged and stable
- Leveraging simulation testbench ensures requirements are met
- Automated simulation, driven by simulator
- Visibility/Controllability into FPGA I/Os

Component testing is much easier in separation from the system.

Target FPGA used

All I/O hooks available.

Independent Assessment Path with DO-254 CTS

"Independent assessment of a design tool's output may include a manual review of the tool outputs or may include a comparison against the outputs of a separate tool capable of performing the same verification activity as the tool being assessed.

Chapter 11.4.1.3, DO-254 Specification, Apr 19, 2000

1. Manual Review of the in-hardware simulation results
    - User Design, Diagnostic Design or Loopback tests can be used to analyze results if they are the same as expected
2. Comparison of RTL simulation results and In-Hardware simulation results.
    - User Design, Diagnostic Design or Loopback tests
    - The Waveform Viewer of the HDL simulator with its waveform comparison feature
    - The CTS built-in script-driven waveform comparison feature

Basic Tool Qualification Path with DO-254 CTS

"Establish and execute a plan to confirm that the tool produces correct outputs for its intended application using analysis or testing. The tool's user guide or other description of the tool's function and its use may be used to generate requirements."

Chapter 11.4.1.7, DO-254 Specification, Apr 19, 2000

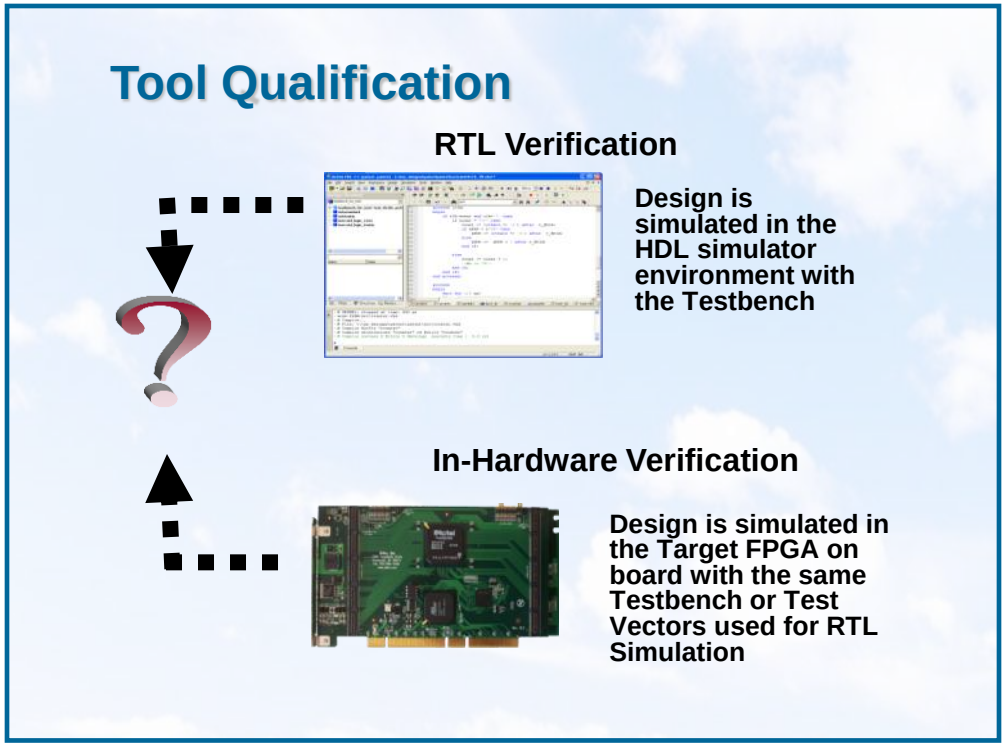
Necessary Documents for Basic Tool Qualification Path

- Tool Operational Requirements
- Tool Qualification Plan
- Tool Qualification Accomplishment Summary

HDL Simulator
Tool Assessment Qualification

Comparing Outputs of RTL and Hardware Simulation

- Validates RTL simulation results
- Validates Hardware simulation results



Code Coverage
Tool Assessment and Qualification

Full Documentation Package

- Tool Operational Requirements
- Tool Qualification Plan
- Tool Qualification Accomplishment Summary
- 56 Test Analysis Documents for VHDL constructs such as Sequential Statements, Concurrent Statements, Functions and Procedures