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Why should you care about
JTAG / Boundary Scan / IEEE 1149.x

GOEPEL Boundary Scan Seminar

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Why do we need DFT ?

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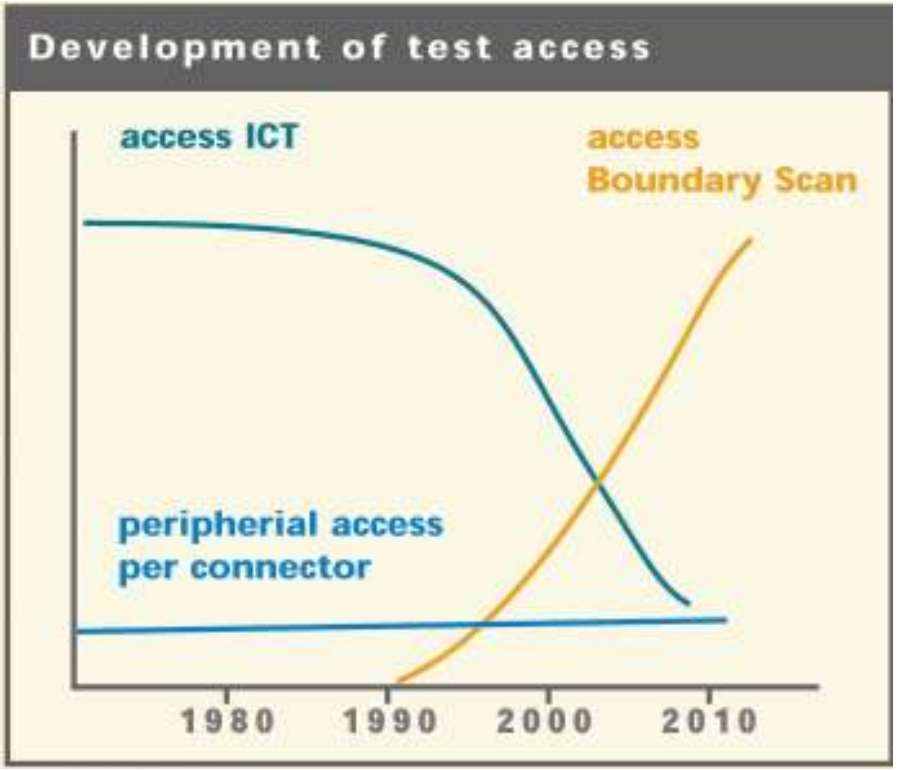
- Shrinking device geometries, device pitch
- New packaging technologies
- Diminishing test access
- Rising UUT complexity
- Rising test time



Test obstacles

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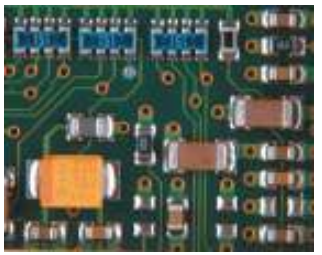
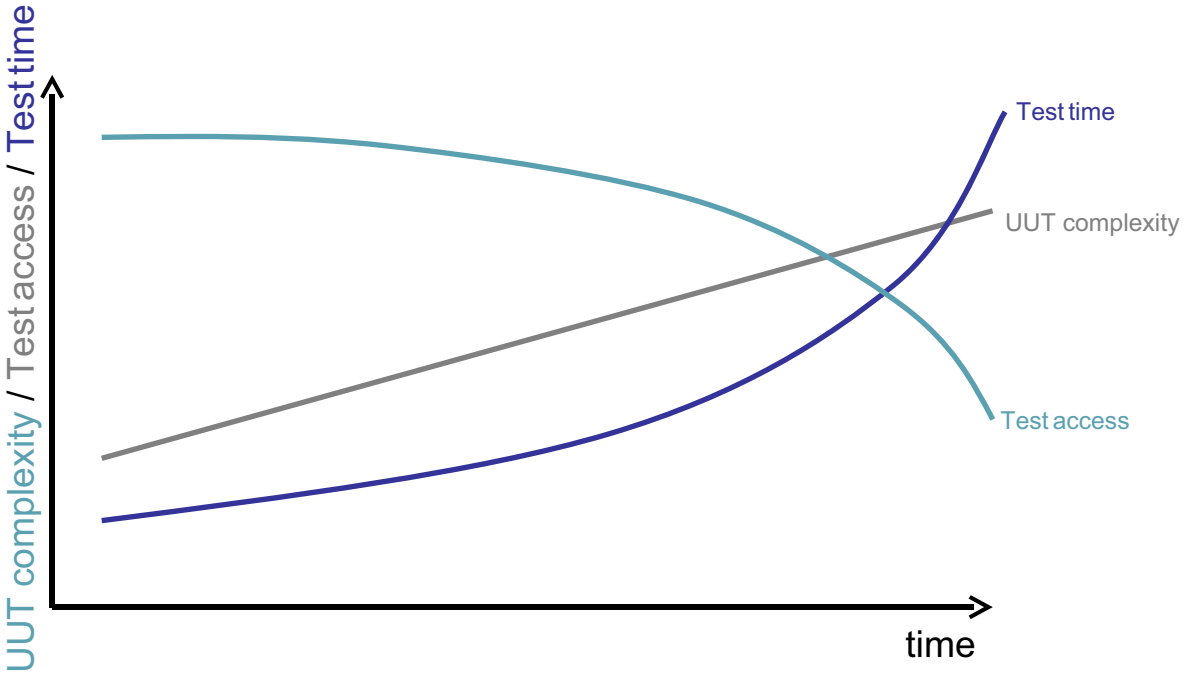
- UUT complexity
- Test access
- Test time





UUT complexity

- Highly integrated components
- More functionality on one board
- Reduced testability

And at the same time …

- Shorter NPI and PLC
- High product mix

Reduced test access

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- New device packaging *(µBGA, CSP, COP, …)*
- Passive components embedded in PCB
- Denser board layouts
- Fewer, smaller test points

Diminishing test access
with probe based test systems

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Cost of Test

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- Requirement to lower cost because of
  - Inflation
  - Shorter PLC
  - Smaller profit margins

- Test DOES “add value” by
  - Catching defects
  - Helping control the manufacturing process
  - Reducing field returns and warranty issues

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How do we test?

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Automated Optical / X-Ray Inspection (AOI/AXI)

Manufacturing Defect Analyser (MDA)

Flying Probe Test (FPT)

Functional Test (FT)

Manual Inspection

In-Circuit Test (ICT)

most likely: *a combination of those methods*

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Common test solutions

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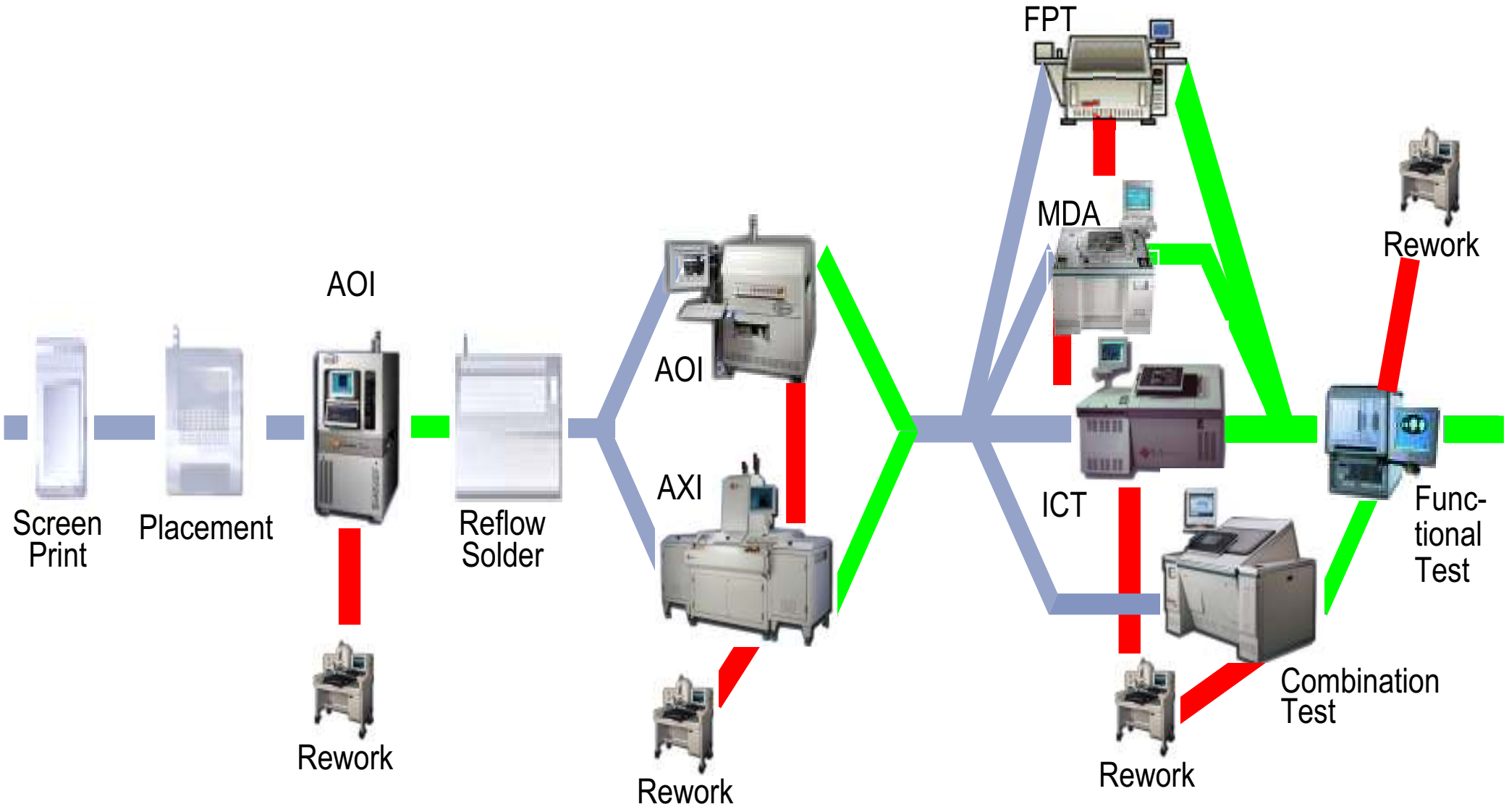

Frequent problems

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- High density, small footprint components
  (BGA, microBGA, Chip On Board, Chip Scale Packages)
- Loss of test access
- Ballooning Fixture Costs
- Long test development time
- Reduced diagnostic resolution

Is there a way out?

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Can Boundary Scan help?

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- Regain test access
- Improve time to market
- Use Boundary Scan throughout the whole product life cycle (reuse test applications)
- Supports chip, board, and system level test
- Reduce fixture cost
- Improve diagnostic resolution
- Shorten debug time

Reduce cost of test

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Case Study A

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Type 1: single PCB, predominantly digital circuits

- components with relatively small pin count, no BGA's;
- Some components with Boundary Scan capabilities;
- well suited for In-Circuit-Test;
- cost saving potential in combination of Boundary Scan with ICT

- ***Example:***
  - ~ 1200 component leads
  - 200 nets
  - 3 BScan compliant components
  - 54 BScan accessible nets (27%)
  - Bed-Of-Nail adapter with 200 nails: about $5,000 (80% of the total account for nails, or $4,000)
  - reducing the number of nails by 54 (27% of all 200 nets) ⇒ achievable savings: 27% of $4,000, or $1,080
  - 50 different kinds of such PCB's: save ~ $54,000 annually

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Case Study B

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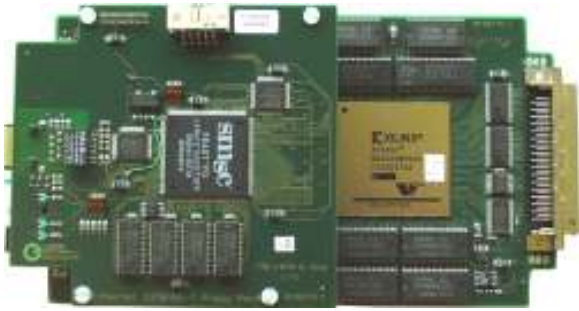
Type 2: single PCB, predominantly digital circuits

- components with high pin count, few BGA's;
- Some components provide Boundary Scan capabilities;
- High product mix, low volume ⇒ Flying Prober most useful



- ***Example (average unit):***
  - 560 nets, 3200 pins,
  - 2 BScan compliant BGA's (total of 688 Pins),
  - other high-pin components, total of 956 pins,
  - 230 low pin count components;
  - total of 5114 Flying Probe test steps,
    13 test steps per second ⇒ test time of 6.5 minutes;
  - BScan can eliminate 1937 Flying Probe test steps
    (38% of all 5114 steps) ⇒ cost saving of $2.74 per assembly
  - 50,000 PCBs per year ⇒ savings potential is $137.000 annually

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Case Study C

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Type 3: single PCB, predominantly digital circuits

- components with high pin count, many BGA's,
- Most components provide Boundary Scan capabilities.

⇒ BScan testing is a "no-brainer"

- ***Example:***
  only alternative: X-ray inspection, however:
  - average investment (in-line AXI): $300,000
  - test execution time: AXI >> BScan test;
    430mm x 380mm PCB with 50 BGA's:
    - Inspection by AXI: 75 seconds
    - ~ 10 seconds via BScan
  - average costs per test minute calculated as $1
  - production volume of 50,000 PCB's per year,
    reduction in test execution time: > $50,000 savings annually

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Is BScan right for you?

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What can BScan potentially do for you?

- Simplify your test
- Lower your cost of test
- Improve your test strategy

Let's find out for sure by doing a
Design For Testability analysis
... free of charge *[contact info@goepelusa.com]*

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In-Circuit Test

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+ Short test execution
+ Relatively fast test program development
- Expensive test fixtures, maintenance, storage
- New fixtures needed when layout changes
- Typically not available during prototyping
- Test fixtures take weeks to design and build
- Test access limited on modern PCB's

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Flying Probe Test

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+ No bed-of-nail fixture required
+ Relatively fast test program development
- Very long test execution time
- Modifications of test programs required when layout changes
- Typically not usable in production test
- Test access limited on modern PCB's

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Functional Test

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+ Very good at-speed test to verify UUT functionality
- Very long test development times (cost!)
- Poor diagnostic capabilities
- Difficult fault isolation
- Test of all functions (to cover all faults) practically impossible

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MDA

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+ Short test execution
+ Fast test program development
- Expensive test fixtures, maintenance, storage
- New fixtures needed when layout changes
- Typically not available during prototyping
- Test fixtures take weeks to design and build
- Test access limited on modern PCB's

AOI / AXI

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+ No bed-of-nail fixture required
+ Relatively fast test program development
+ Test of non-electrical properties, such as alignment
- Long test execution time
- No test of electrical properties
- Only visible features can be verified (AOI)
- Very expensive test equipment (AXI)

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Boundary Scan / JTAG

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- Potential to enhance time to market;
- Available throughout product life cycle;
- Early, easy and fast test development;
- Test for connectivity problems
  (stuck-at 1/0, open pins, shorted nets);
- Value-adding:
  - In-System Programming,
  - BIST and Debug access,
  - System Test;

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ICT vs. Boundary Scan

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	In Circuit Test		Boundary Scan
	bed of nails	Flying Probe	
speed	+	– –	o
analog devices (power)	+	++	(–) (IEEE 1149.4)
digital devices	o	(–)	+ (functional description not necessary)
net contacting	– (mechanically)	– (mechanically)	+ (via test bus)
flexibility	– –	+	++
costs per new UUT	– – (nail adapter)	o (test creation)	o (test creation)
costs fortest equipment	–	o	++

BScan in Product Life Cycle

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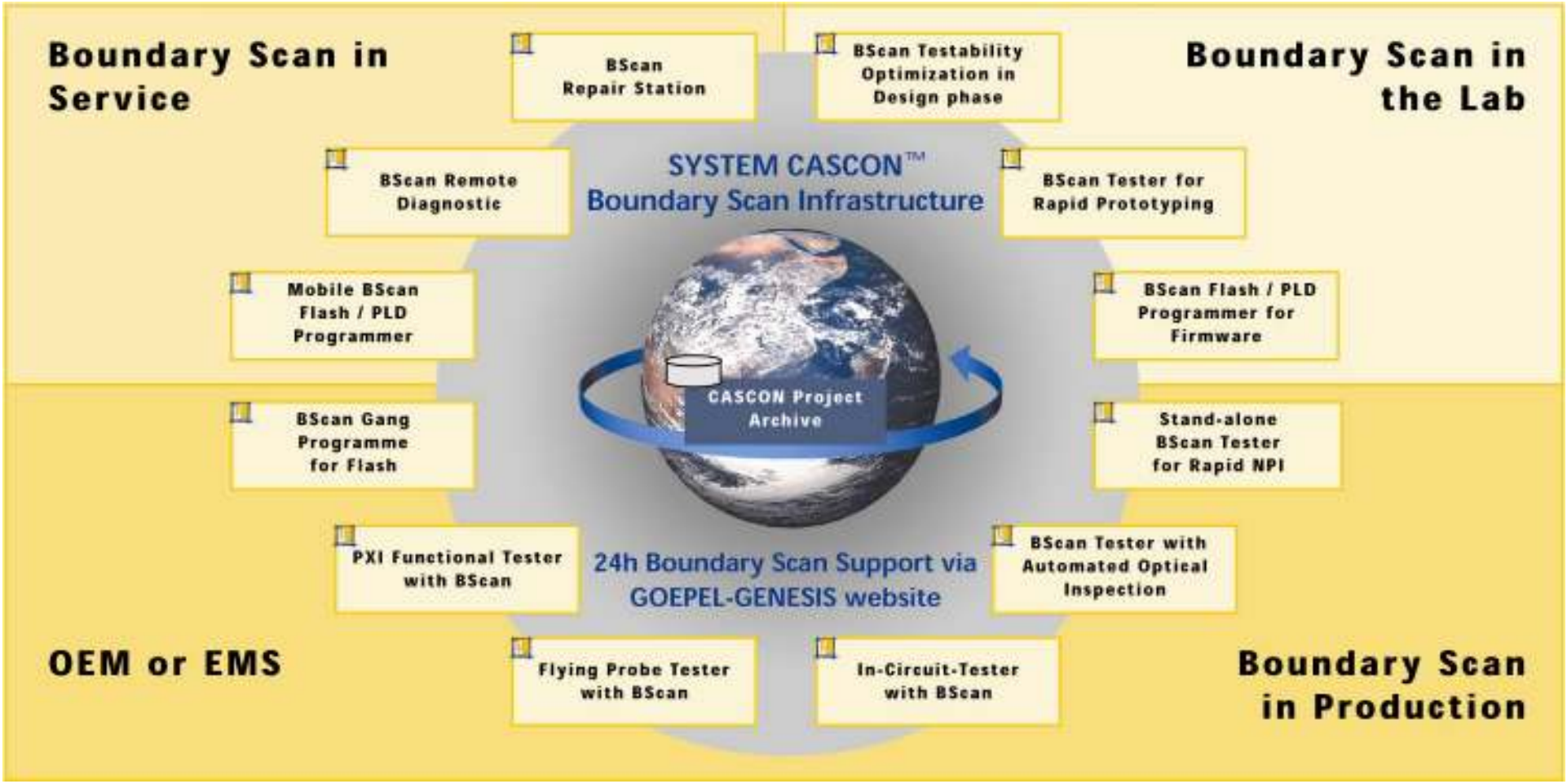

Boundary Scan / JTAG

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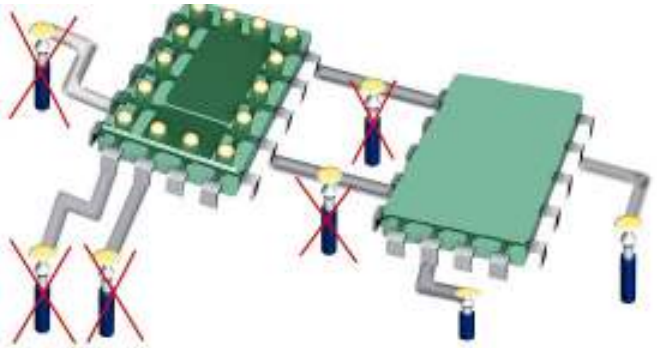
- Regain test access (BGA, CSP, etc.)
- Quick test execution;
- Inexpensive test equipment;
- No or very simple test fixture;



JTAG Boundary Scan IEEE 1149.x

Boundary Scan applications

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- Providing test access for ...
  - Checking interconnections
  - Debugging / emulating circuitry
  - Supporting functional test
  - Enabling remote test / verification
- Programming devices
- ...

JTAG Boundary Scan IEEE 1149.x

Extended Boundary Scan

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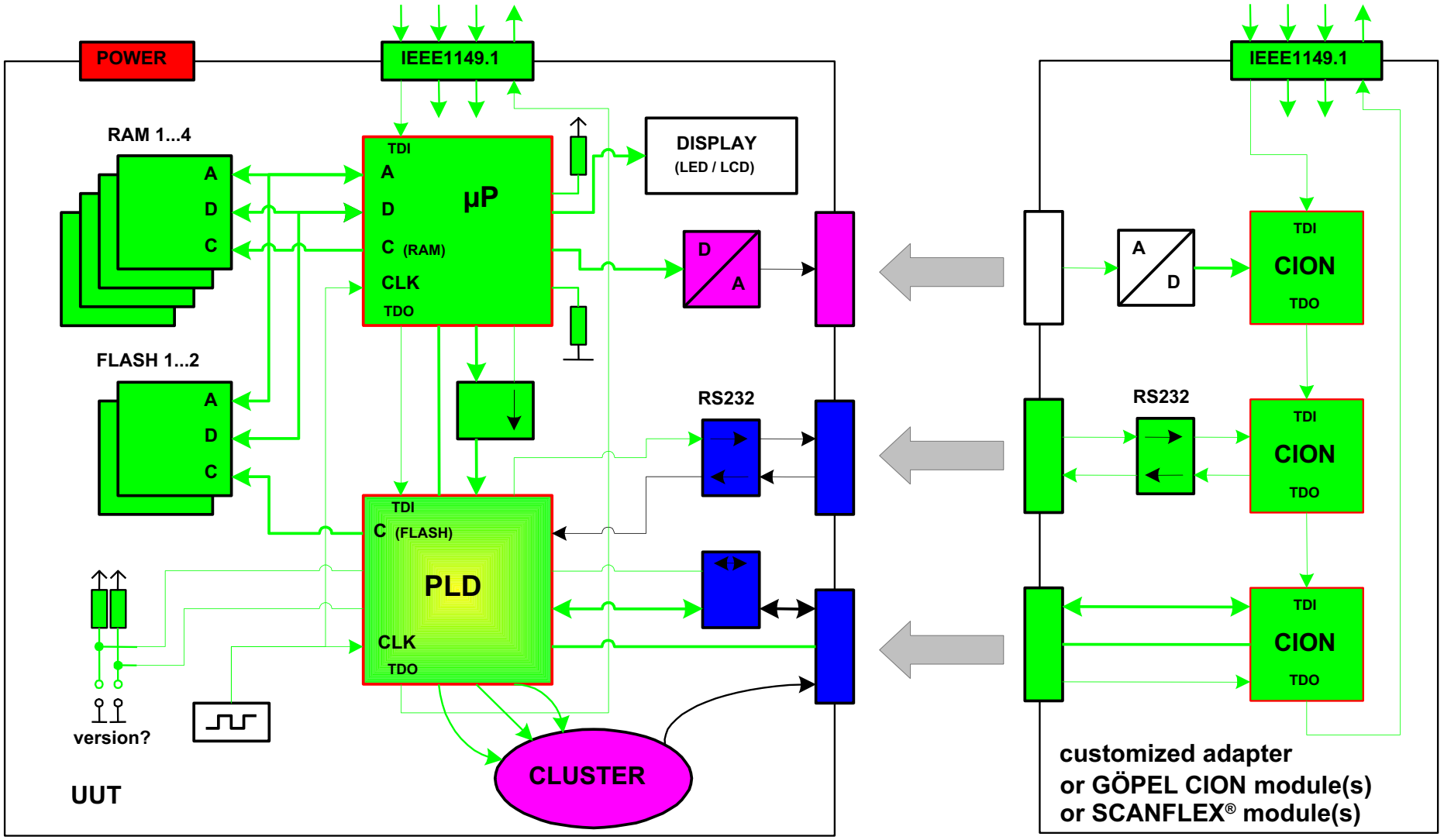

Testable device

Boundary Scan compliant device

Limits of Boundary Scan

- IEEE 1149.1 limited to digital interconnect test
- No at-speed test (exception: BIST)

→ New standards (dot4, dot6, ...)

→ Combination of Boundary Scan and other Test Methodologies

Fault spectrum

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Discussion topics:

What kind of faults do you see most in your production ?

When and how to you test ?

What is your yield ?

What is your slip-through rate ?

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Fault spectrum

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Test Coverage models for structural defects:

- **MPS** - Philips Research
  (Material, Placement, Solder)
- **PPVS** - ASTER Ingénierie
  (Presence, Polarity, Value, Solder)
- **PCOLA/SOQ** - Agilent Technologies
  (Presence, Correctness, Orientation, Live, Alignment, Short, Open, Quality)

Of concern for functional test coverage:

- Design defects
- Functional defects

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What is Boundary Scan ?

JTAG Boundary Scan IEEE 1149.x

What is Boundary Scan ?

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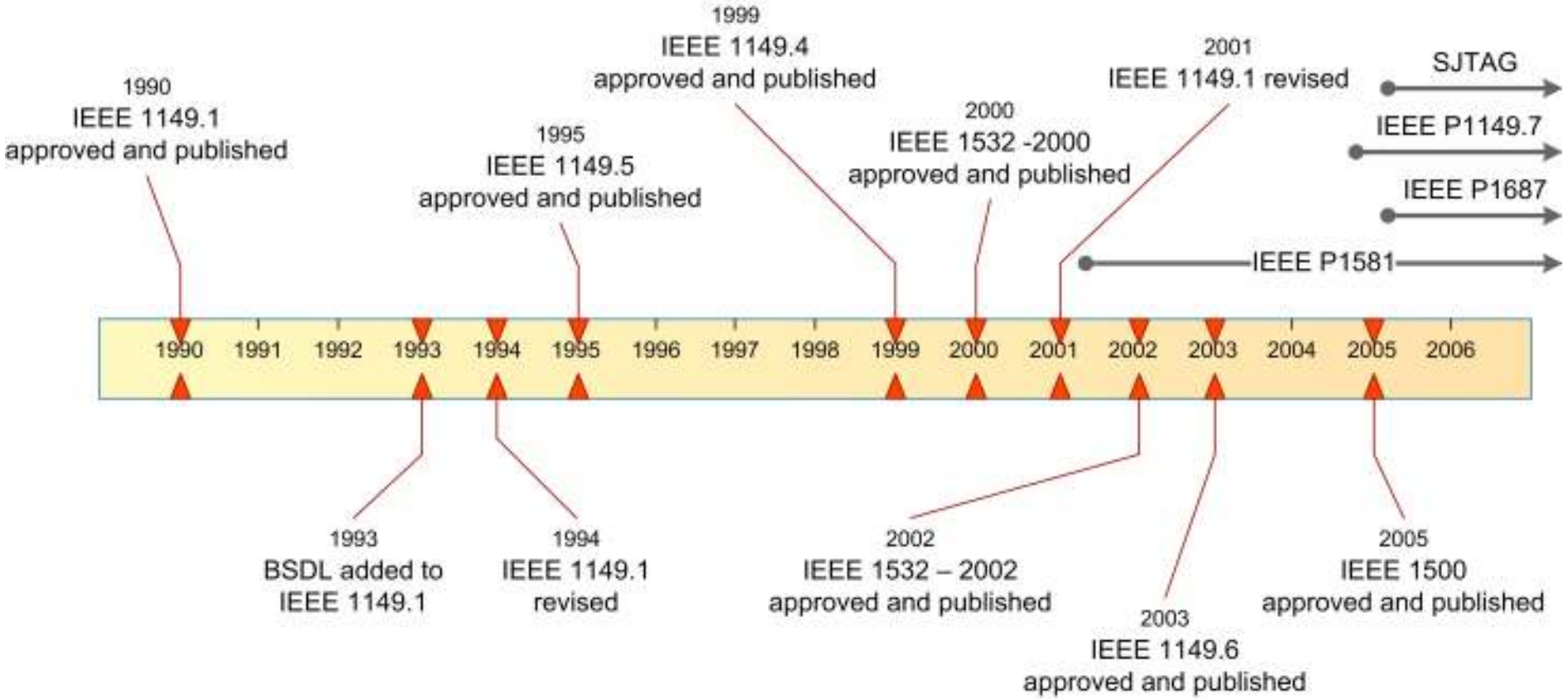
A little bit of history (and outlook) ...



BScan – PCOLA/SQL

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Component properties:

- ✔ Presence
- ✔ Correctness *(correct device)*
- ✔ Orientation
- ✔ Live *(the device is basically alive)*
- • Alignment *(device is centered, no skews or small rotations)*

Connections:

- ✔ Shorts
- ✔ Opens
- • Quality

JTAG Boundary Scan IEEE 1149.x

Basics of IEEE 1149.1

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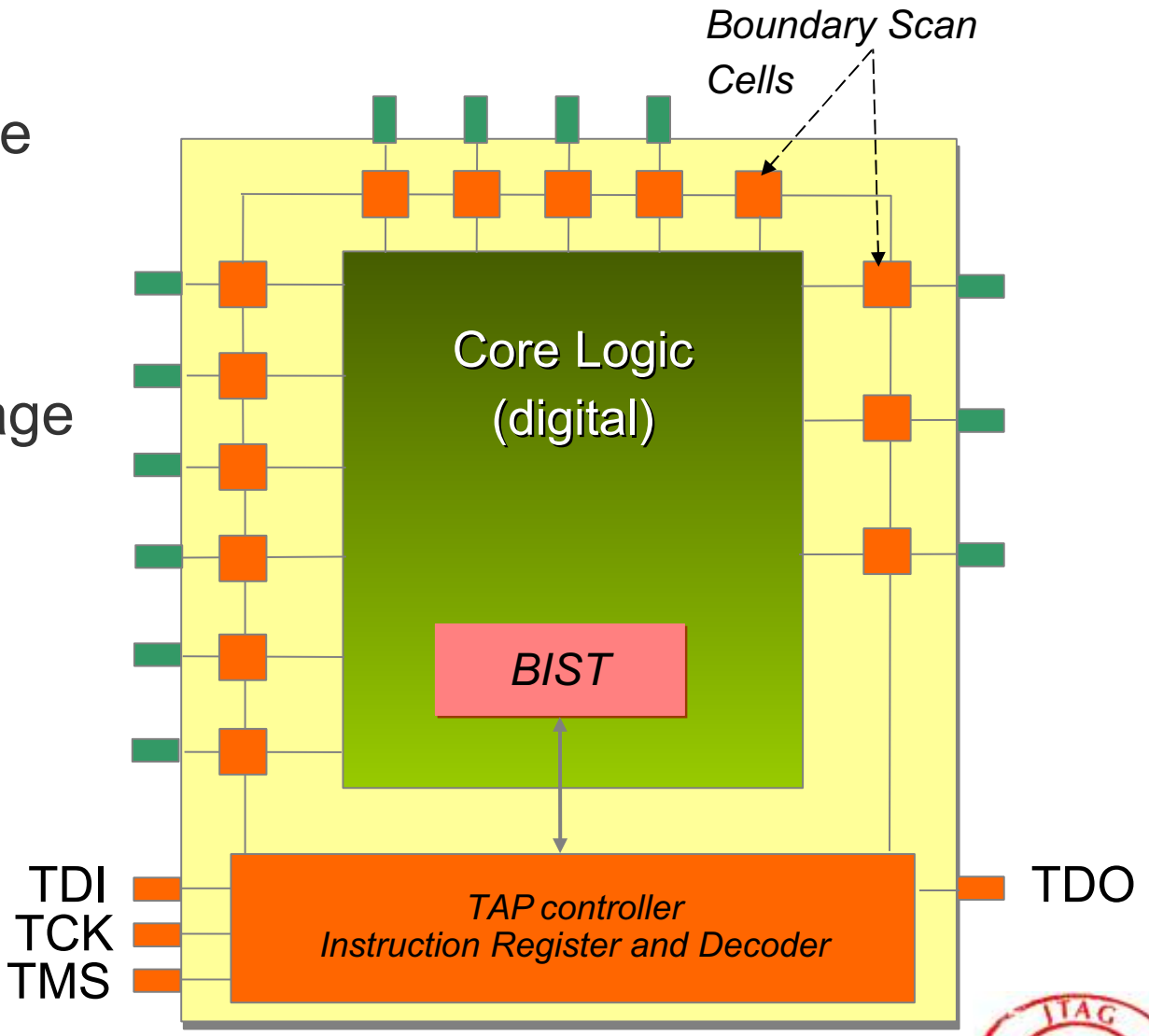
IEEE 1149.1 specifies ...

- Test resources to be implemented in devices
- Boundary Scan Description Language (BSDL)



Basics of IEEE 1149.1

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Mandatory features:

- Test Access Port (TAP):
  TCK, TMS, TDI, and TDO
- TAP Controller
- Instruction Register (2 bit or more)
- Bypass Register (1 bit)
- Boundary Scan Register (1 bit or more)

Basics of IEEE 1149.1

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Optional features:

- Fifth Test Access Port (TAP) signal:
  /TRST
- IDCode Register (32 bit)
- UserCode Register (32 bit)
- Other via TAP accessible resources
  (such as BIST circuitry,
  in-circuit programming controller,
  etc.)

JTAG Boundary Scan IEEE 1149.x

IEEE 1149.1 in practice

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Typical applications *(only a few examples)*:

- Check for shorts between BScan accessible nets
- Check for opens on a BScan pin
- Check for stuck-at-0/1 faults at a net level
- Check for missing resistors
- Check connections to memory devices
- Detect faults in non-BScan circuit clusters
- Control optical indicators (e.g. LED's)
- Provide easy test access for mixed-signal and functional tests
- Use SAMPLE mode to capture signal pattern

JTAG Boundary Scan IEEE 1149.x

IEEE 1149.1 in practice

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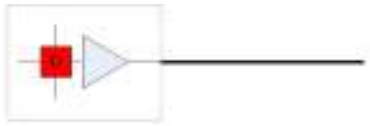
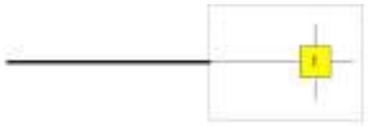
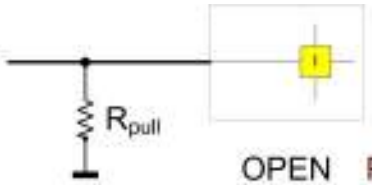


OPEN No / No
SA-0/1 No / No
SHORT No / No



OPEN No / No
SA-0/1 Yes / Yes
SHORT Yes / Partial



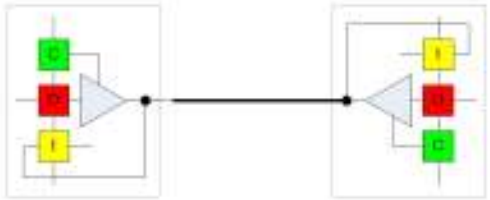
OPEN Partial / Partial
SA-0/1 Partial / Partial
SHORT Partial / Partial

OPEN Yes / No
SA-0/1 Yes / Partial
SHORT Yes / Yes

OPEN Yes / No
SA-0/1 Yes / Partial
SHORT Yes / Yes

Detection / Diagnostics

OPEN Yes / No
SA-0/1 Yes / Partial
SHORT Yes / Yes



OPEN Yes / No
SA-0/1 Yes / Yes
SHORT Yes / Yes

IEEE 1149.1 in practice

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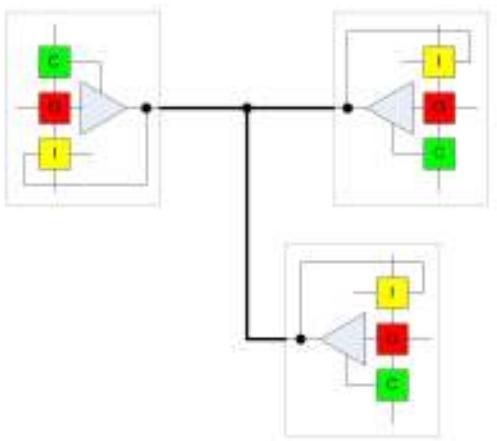
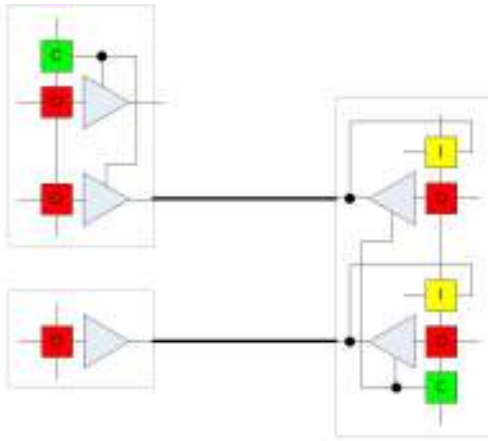
Fault detection, diagnostics depend on BScan resources connected to a particular net:





Detection / Diagnostics

OPEN	Yes / Yes	Yes / Partial
SA-0/1	Yes / Yes	Yes / Partial
SHORT	Yes / Yes	Yes / Yes

IEEE 1149.1 in practice

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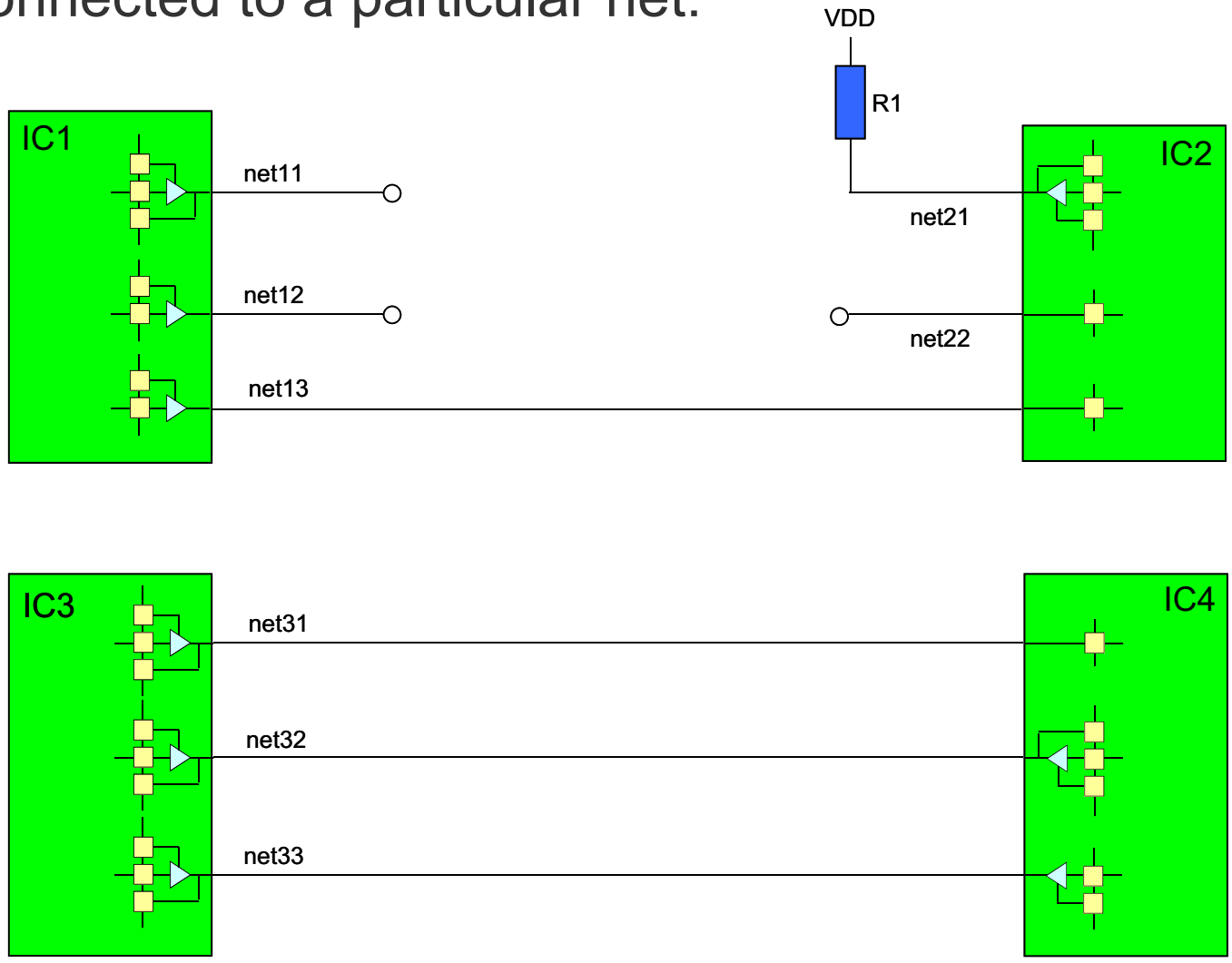
Fault detection, diagnostics depend on BScan resources connected to a particular net:



IEEE 1149.1 in practice

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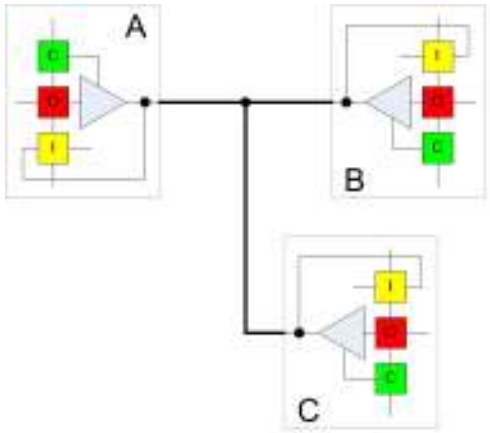
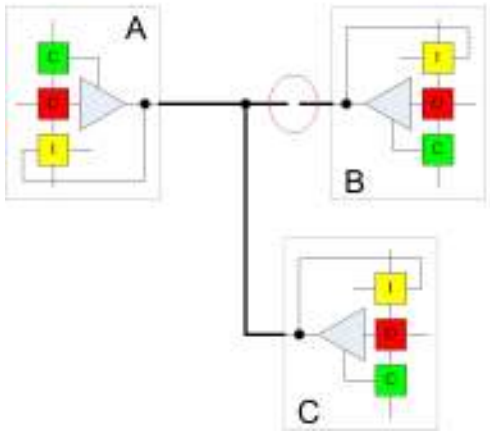
Test pattern without and with fault (open pin):



PASS

	A			B			C		
	C	O	I	C	O	I	C	O	I
Preload pattern	L	Z	H	L	Z	H	L	Z	H
A drives, B and C measure	H	L	L	L	Z	L	L	Z	L
A drives, B and C measure	H	H	H	L	Z	H	L	Z	H
B drives, A and C measure	L	Z	L	H	L	L	L	Z	L
B drives, A and C measure	L	Z	H	H	H	H	L	Z	H
C drives, A and B measure	L	Z	L	L	Z	L	H	L	L
C drives, A and B measure	L	Z	H	L	Z	H	H	H	H



FAIL

	A			B			C		
	C	O	I	C	O	I	C	O	I
Preload pattern	L	Z	H	L	Z	H	L	Z	H
A drives, B and C measure	H	L	L	L	Z	H	L	Z	L
A drives, B and C measure	H	H	H	L	Z	H	L	Z	H
B drives, A and C measure	L	Z	H	H	L	L	L	Z	H
B drives, A and C measure	L	Z	H	H	H	H	L	Z	H
C drives, A and B measure	L	Z	L	L	Z	H	H	L	L
C drives, A and B measure	L	Z	H	L	Z	H	H	H	H

IEEE 1149.1 in practice

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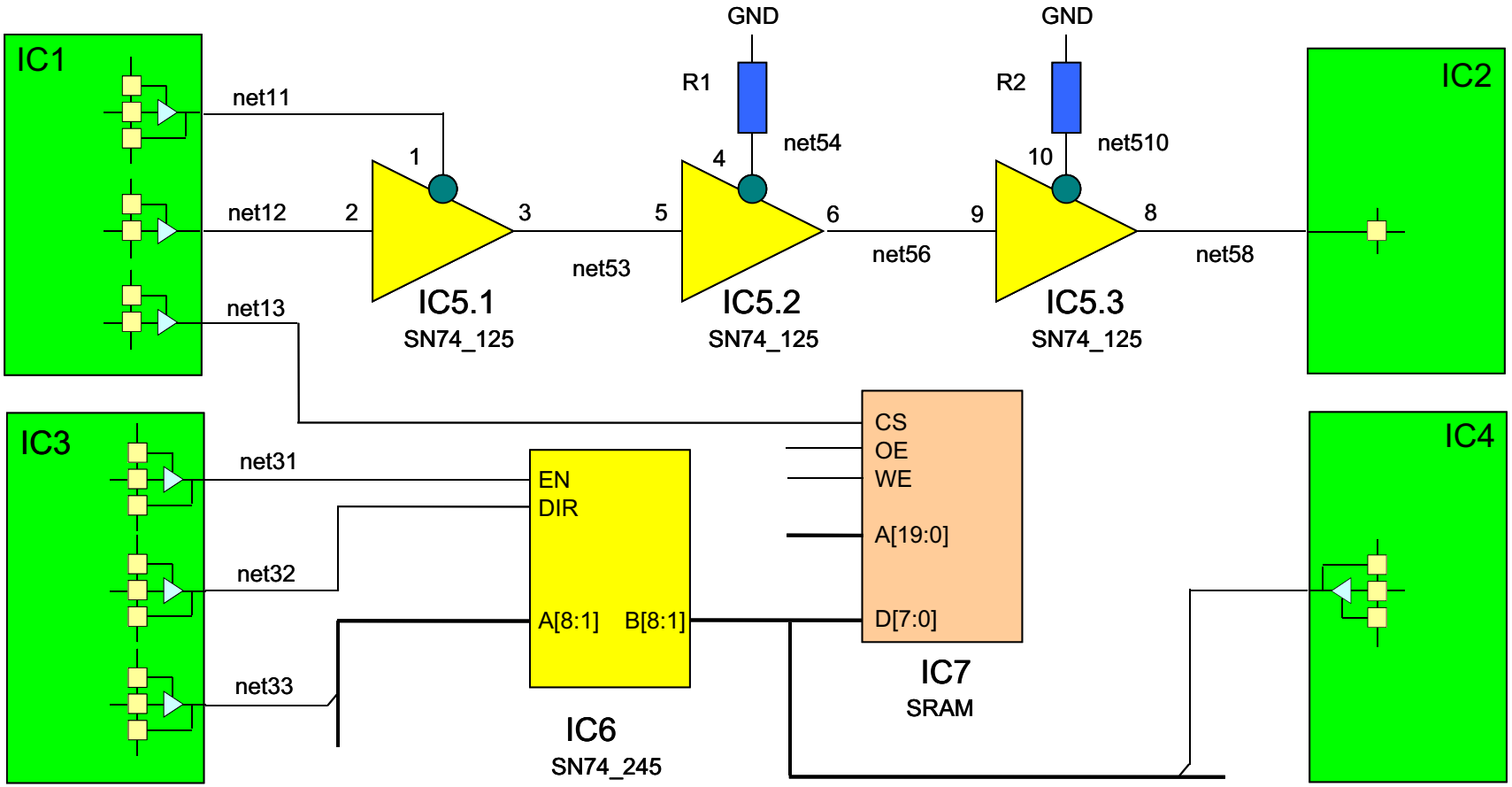
How about non-BScan devices?



Board Level applications

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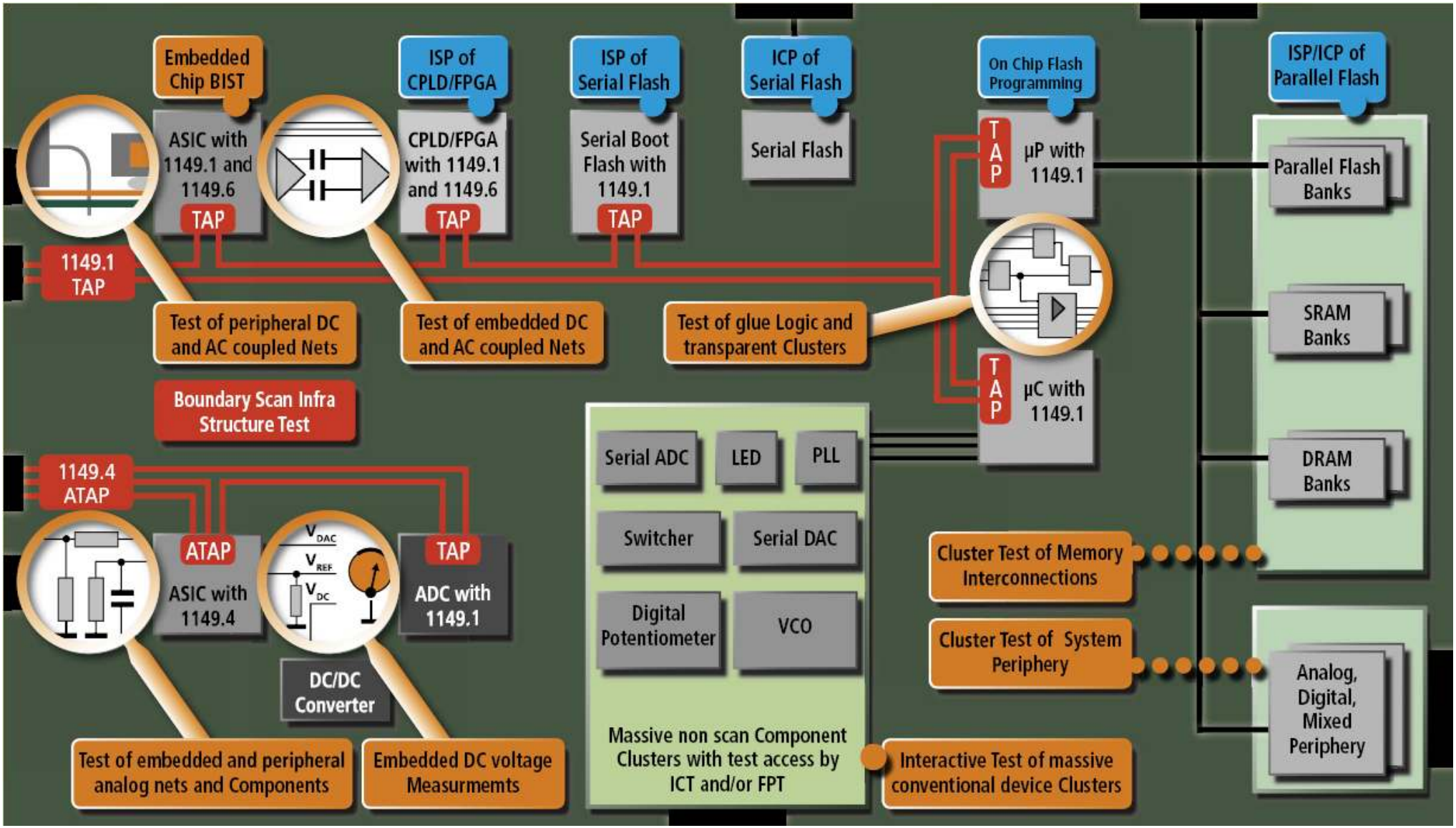

ISP = In-System Programming

ICP = In-Circuit Programming

BIST = Built-In Self Test

JTAG Boundary Scan IEEE 1149.x

Board Level applications

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- Infrastructure Test
- Interconnection Test
- Memory Cluster Test
- Logic Cluster Test
- Other Cluster Tests
- ISP for FLASH
- ISP for serial EEPROM
- ISP for PLD/FPGA
- BIST
- Emulation, Debugging, Fault Insertion, ...

JTAG Boundary Scan IEEE 1149.x

BScan / Functional Test

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- Low cost, flexible, powerful
- Very good test coverage, diagnostics:
  - Boundary Scan for structural test
  - Functional Test for parametric and at-speed test
  - BScan for simplified access in functional tests
- Integrated, highly automated test flow
- Combination through API's; off-the-shelf or ad-hoc software

JTAG Boundary Scan IEEE 1149.x

Basics of IEEE 1149.4

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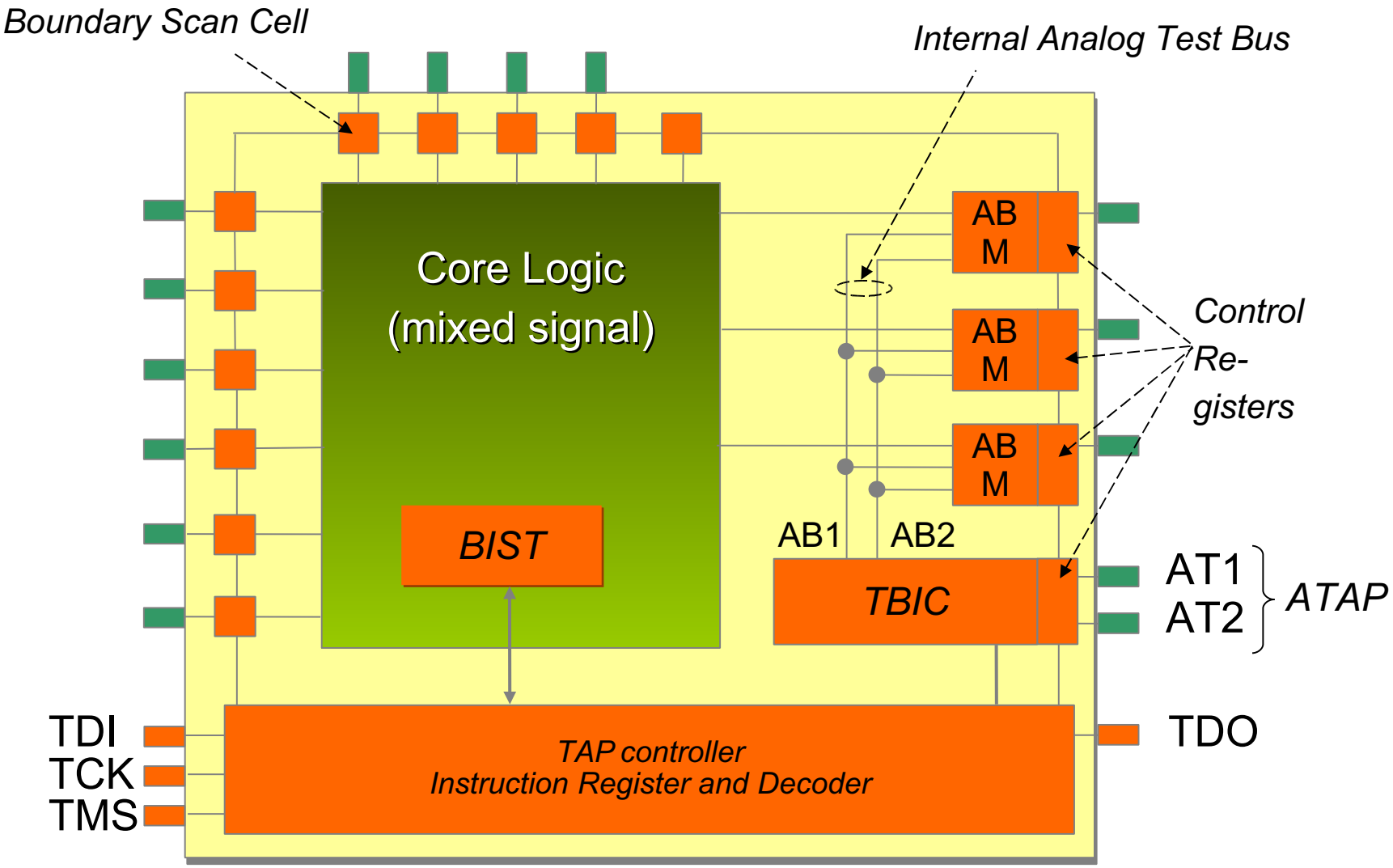

Basics of IEEE 1149.4

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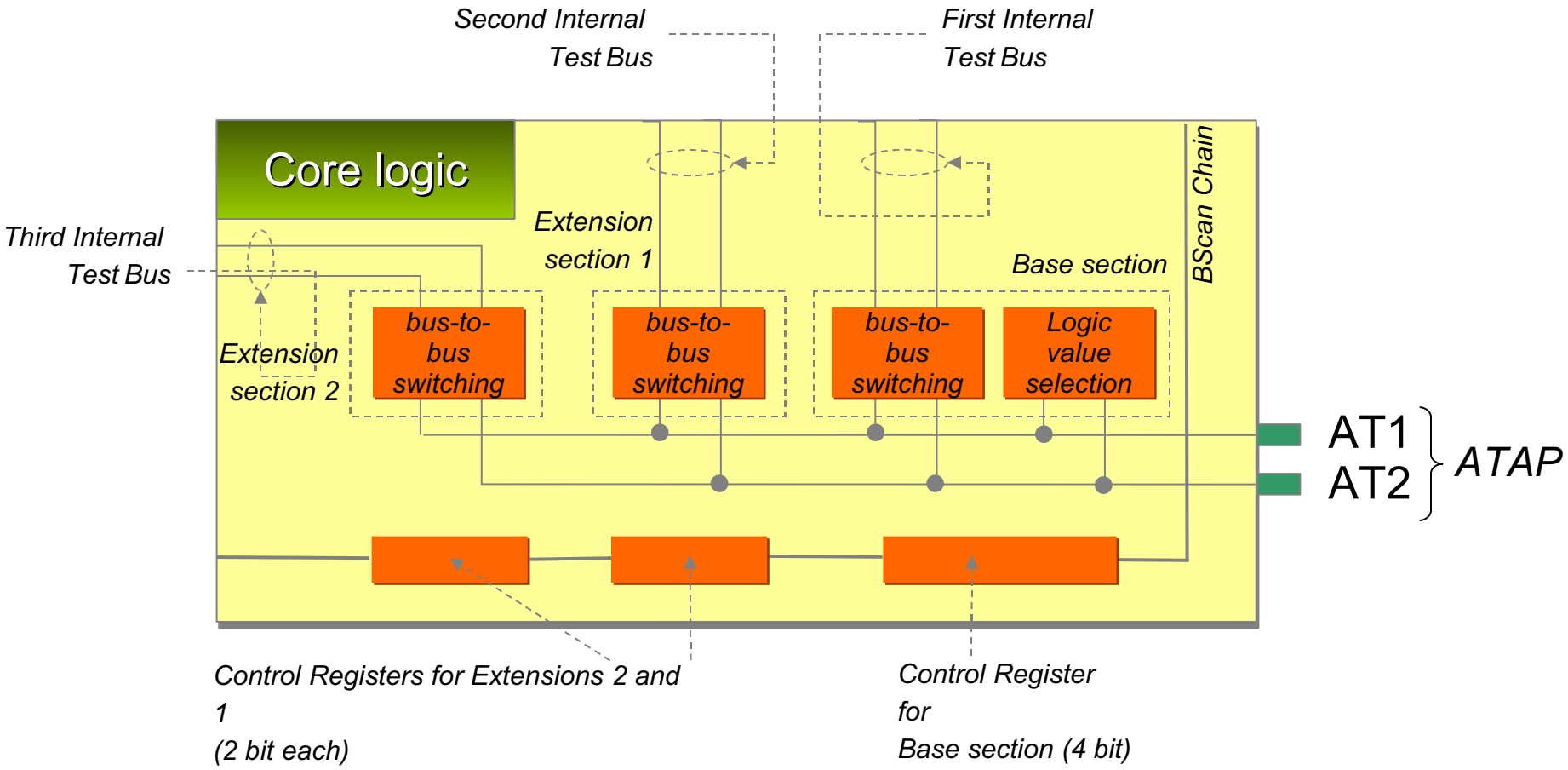
- Parametric Test for
  - *Passive components (resistors, capacitors, inductors, etc.) and/or passive elements intrinsic to the interconnect*
  - *Pull- or termination resistors*
  - *Active components (diodes, transistors, sensors, etc.)*
  - *Impedance networks*
- Extended Interconnect Test
- Limited number of devices available
- Emerging tool support

JTAG Boundary Scan IEEE 1149.x

Basics of IEEE 1149.4



Basics of IEEE 1149.4

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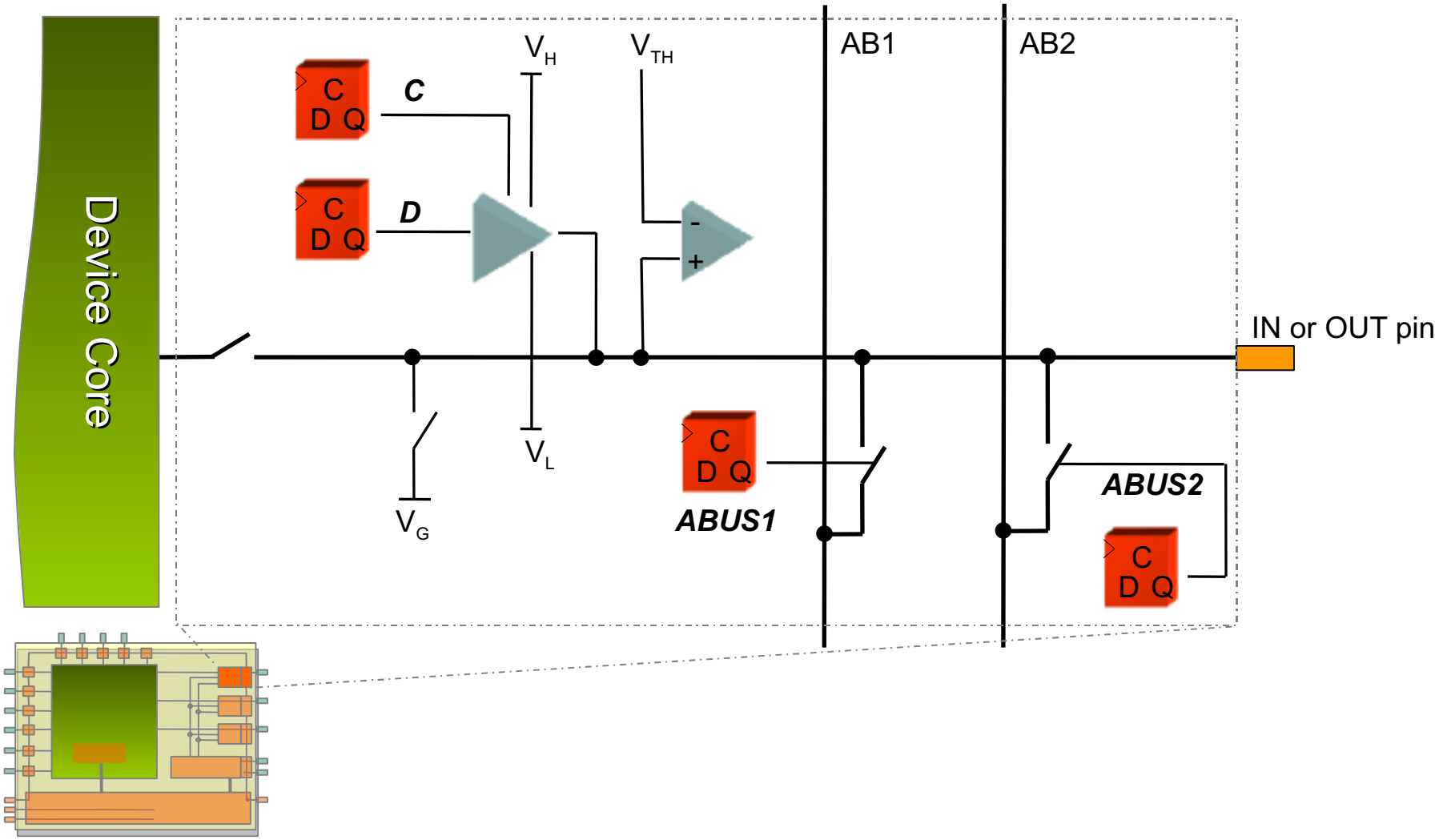

Basics of IEEE 1149.6

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- Extending Interconnect Test to AC-coupled networks
- Standard approved in 2003
- Devices are emerging
- Tool support is available

Purpose of IEEE 1149.6

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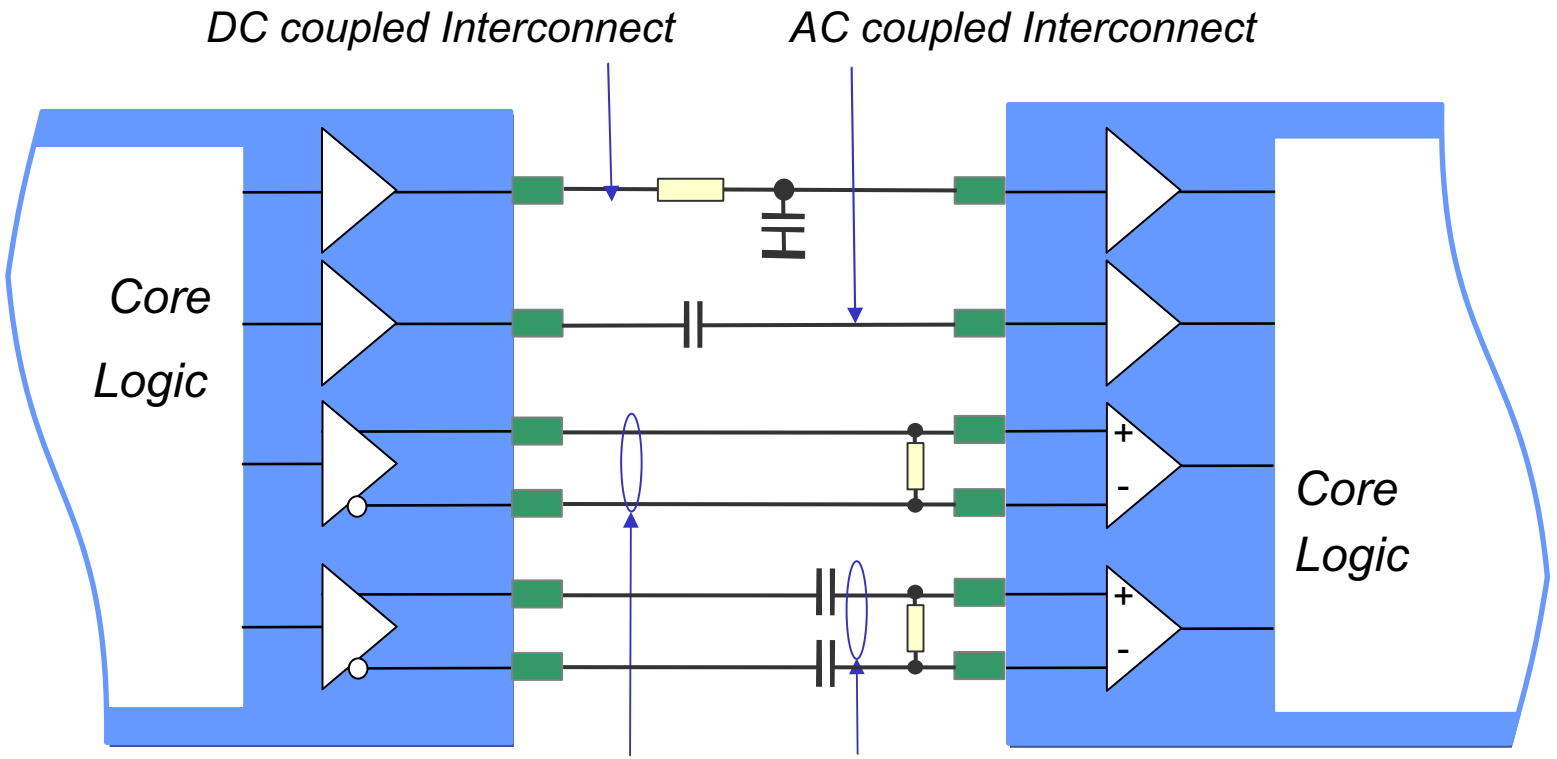
- Extending IEEE-Std. 1149.1 capabilities by providing test methodology for
  - Differential interconnections
  - AC coupled networks
- Defines hardware structure and two new instructions

JTAG Boundary Scan IEEE 1149.x

Principle of IEEE 1149.6

- Operates in parallel with 1149.1 and 1149.4
- Proposes a way of testing AC coupled networks by providing AC Test Signal on output and recovering signal on inputs
- Access to test resources through IEEE-1149.1 TAP

Signal coupling



Shown above are just a few sample coupling schemes
Coupling capacities could also be implemented inside the IC

1149.6 Main Features

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- A IEEE-1149.6 compliant device is also 1149.1 compliant
- New AC-Test instructions defined in 1149.6:
  - EXTEST_PULSE (mandatory)
  - EXTEST_TRAIN (mandatory)
- AC-pins receiving data have test receiver:
  - Single ended AC-pin: one test receiver
  - Differential channel: two test receiver
- AC outputs use mission driver

JTAG Boundary Scan IEEE 1149.x

Basics of IEEE 1532

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- Standardized in-system programming (ISP) method
- Formal extension to IEEE-1149.1b-1994
- Access to on-chip programming resources via TAP
- Unified programming approach for devices from different vendors
- Concurrent programming of multiple devices from different vendors, reducing cost related to ISP
- Data and programming algorithm in separate files

Basics of IEEE 1532

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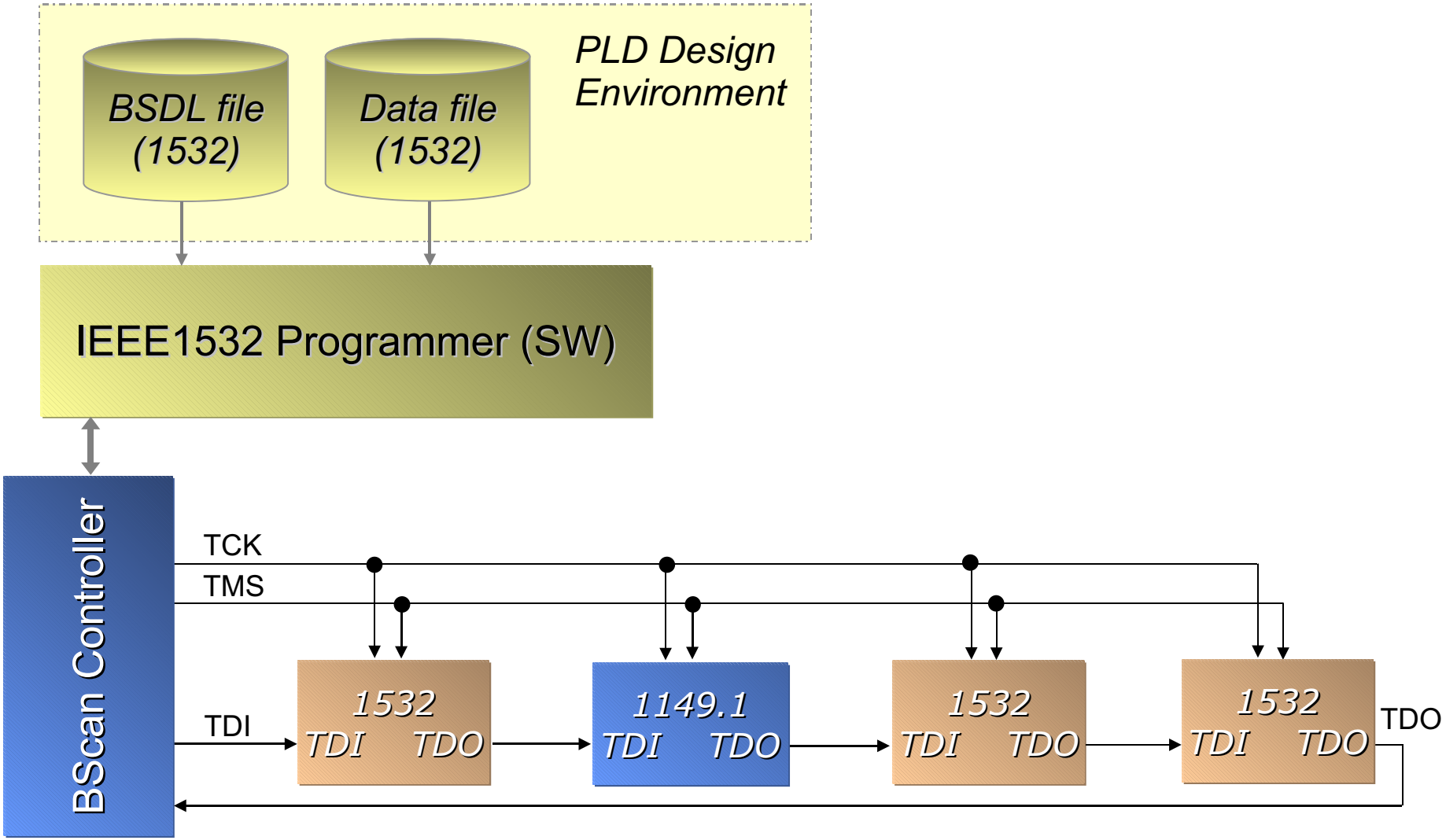

New standards / initiatives

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- IEEE P1581
- IEEE P1149.7 (cJTAG)
- SJTAG
- IEEE P1687 (IJTAG)
- other

Basics of IEEE P1581

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- To test connectivity to non-BScan devices easily
- Solve test problems for devices such as DDR-SDRAM, DDR2-SDRAM, FLASH, etc.
  - 1149.1 not built in !
  - Controllability, complexity
  - Test time
  - Test conditions
    (use of untested resources to test the DUT)
- Simple, quasi-static interconnect test
  (no need for at-speed access or initialization)
- Multiple P1581 devices in bus structure

Basics of IEEE P1581

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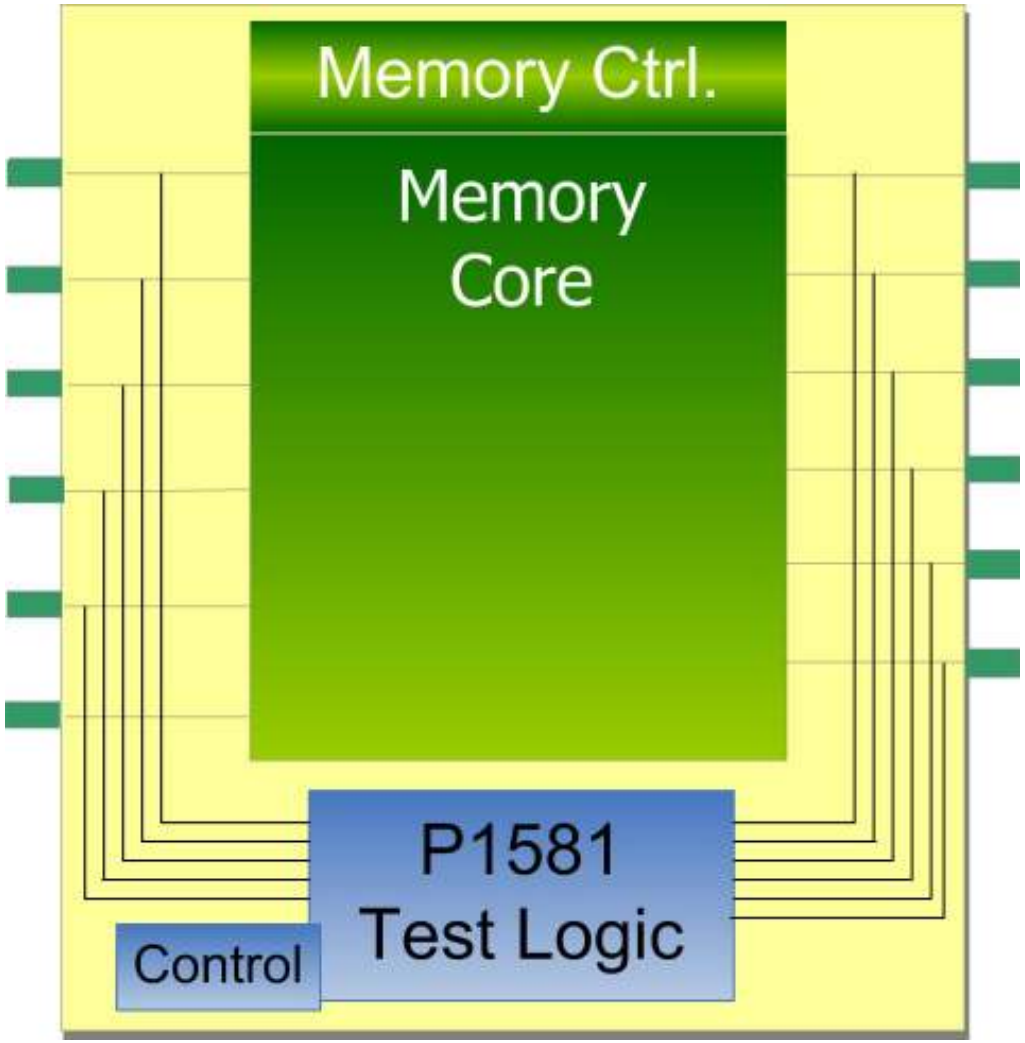
Device is a "slave"

Test Control:

- Optional Test Pin

Or

- Test Control Circuitry (various proposals)



P1581 test logic circuitry

- XOR/XNOR, or Inverters/AND
- Only combinational, non-sequential logic
- Easy to implement, simple test vectors
- Faults on pins don't inhibit test of other pins
- Fault detection guaranteed
- Fault diagnostics depends on implementation, test vectors
- Patented vs. public domain

Basics of IEEE P1149.7

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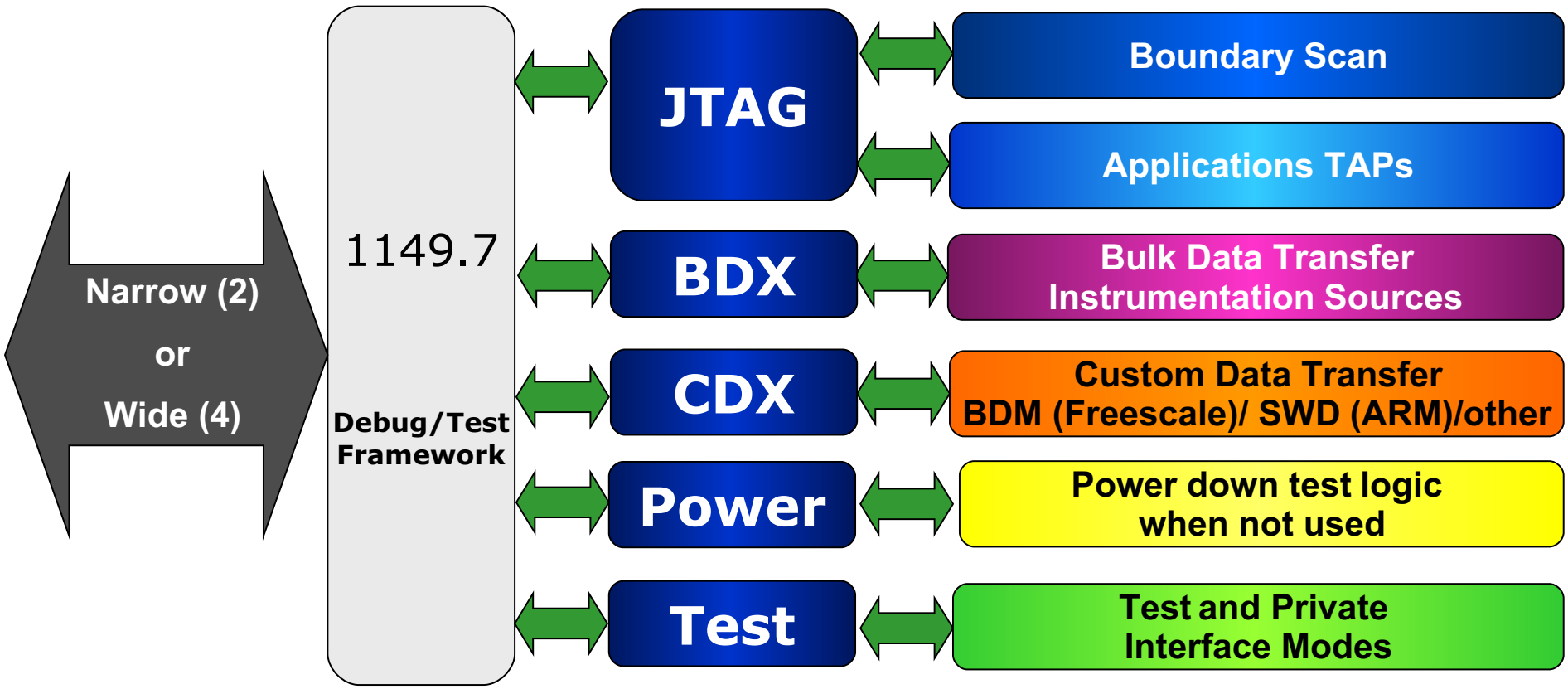

- IEEE 1149.1 signaling used at start-up
- SW directed mode switches between JTAG modes and advanced modes
- SW directed mode switches between JTAG modes and advanced modes. Software drivers always use IEEE state sequences.
- Framework for multiple debug and other technologies

Basics of IEEE P1687

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Focus on

- Documentation: architectural descriptions
  - Identify accessible embedded instruments,
  - Specify characteristics of the instrument;
- Access protocols: procedure descriptions
  - How to communicate with an instrument,
  - Facilitate re-use through portability;
- "Enhanced", secondary access/interface:
  - Access instruments not easily handled solely by the TAP (i.e. use high bandwidth I/O)
  - Simplify hierarchical test architectures

Basics of IEEE P1687

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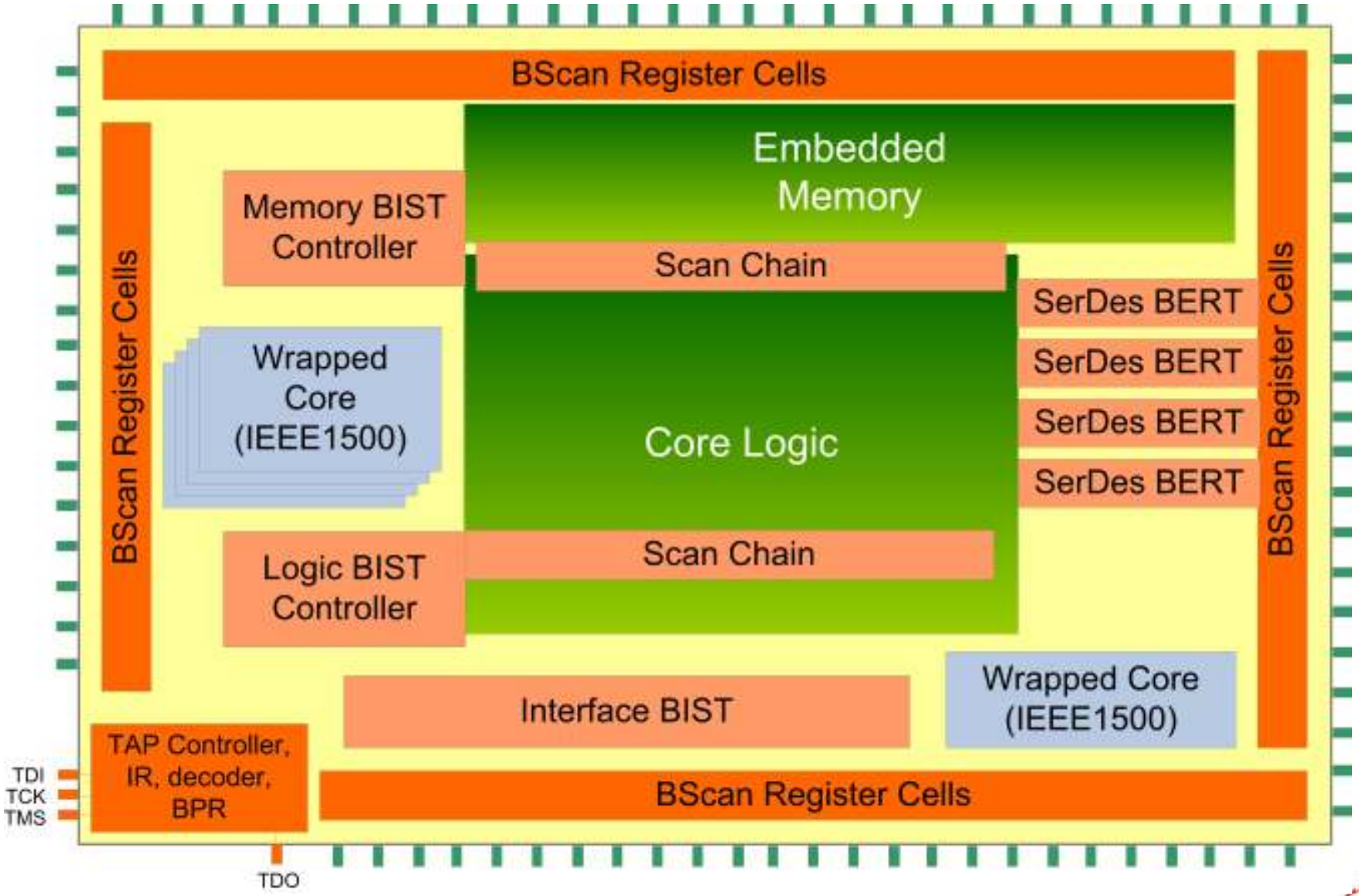

Basics of SJTAG

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Goal:

to standardize data contents and formats for communication:

between external Test Manager platforms and internal Embedded Test Controllers,

and

between Embedded Test Controllers and the UUTs they serve

for all variants of XBST and EBST

XBST - external Boundary Scan Test
EBST - embedded Boundary Scan Test

References

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Books:

- Boundary Scan Handbook, 3rd Edition, Ken P. Parker, Kluwer Academic Publishers, ISBN 1-4020-7496-4
- Analog and Mixed-Signal Boundary-Scan, Adam Osseiran, Kluwer Academic Publishers, ISBN 0-7923-8686-8
- Digital Systems Testing and Testable Design, Miron Abramovici et.al., IEEE Press, Wiley Interscience, ISBN 0-7803-1093-4

Websites:

- www.goepelusa.com
- www.freeDFT.info
- www.DFTdigest.com

Other publications:

- ITC Proceedings (papers on the topic; there are plenty ...)
- Testability Guidelines, SMTA TP-101C (2002), www.smta.org

JTAG Boundary Scan IEEE 1149.x

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For further information, please:

- Visit our website at www.goepelusa.com
- Contact your local sales representative
- Call us at 1-888-4GOEPEL
- Email us at sales@goepelusa.com

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