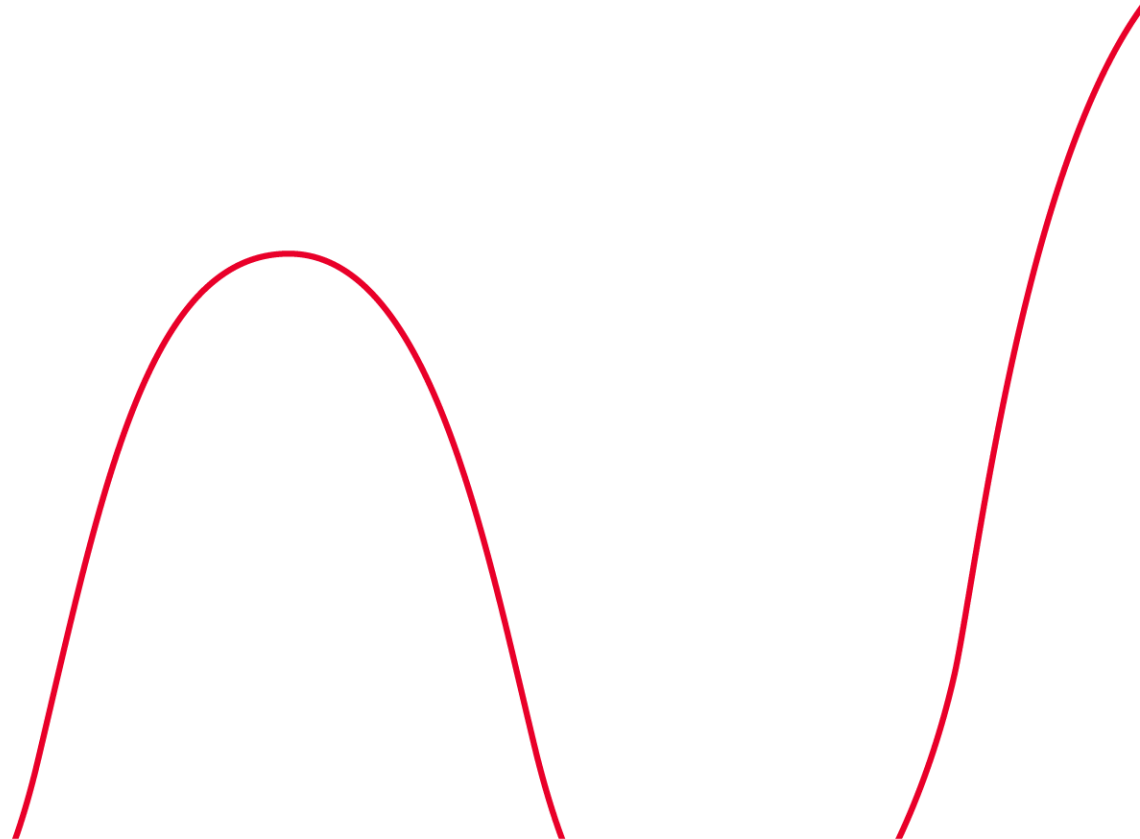


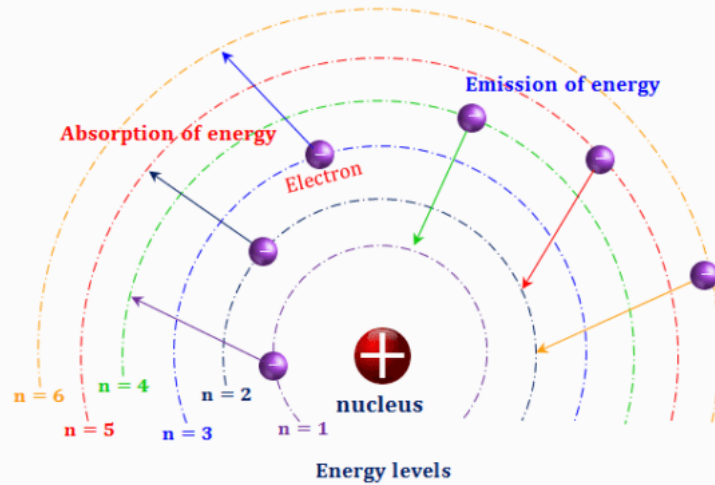
# Power Semiconductor Considerations for Inverter Design

**Ervin Mile, PhD**  
**Power Specialist, Keysight Technologies**

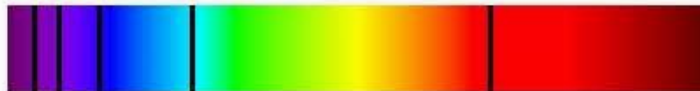
# What is Bandgap?



# Hydrogen Atom Electron Energy Levels



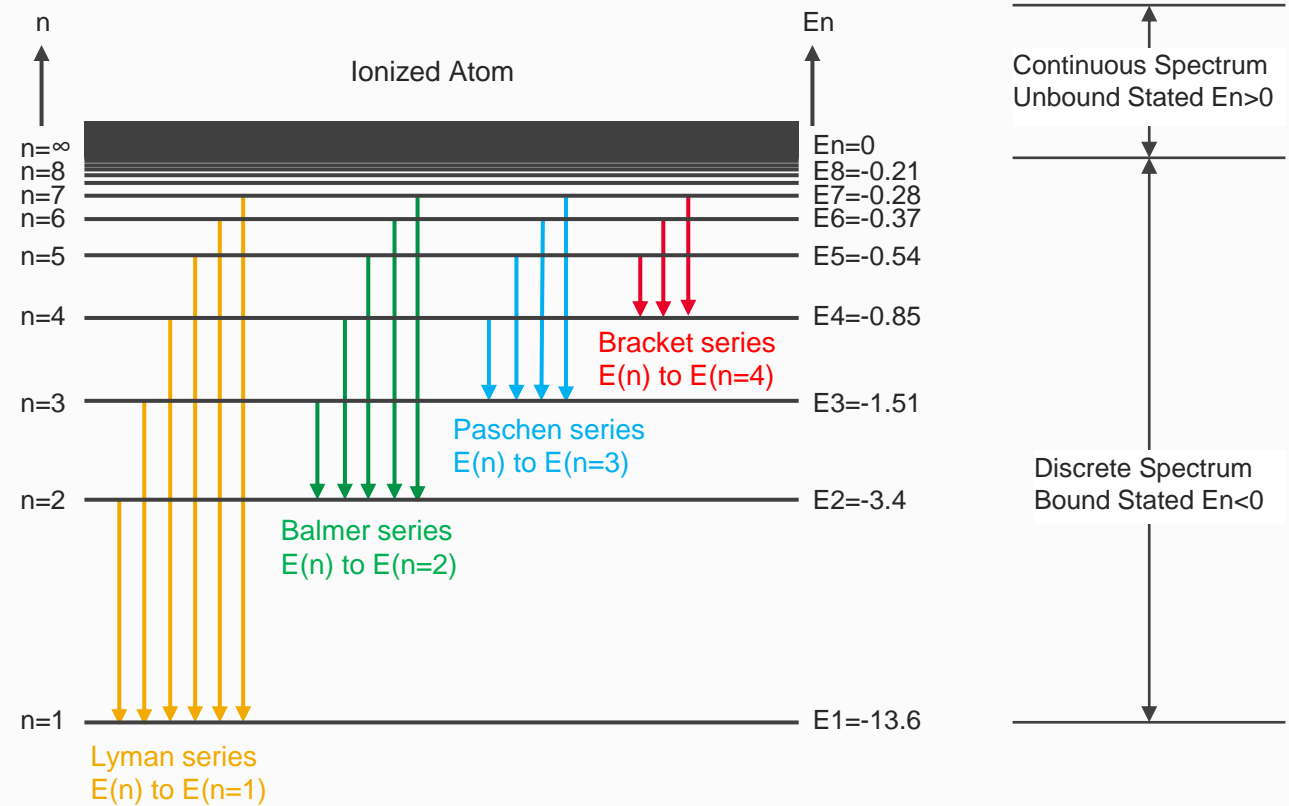
Hydrogen Absorption Spectrum



Hydrogen Emission Spectrum



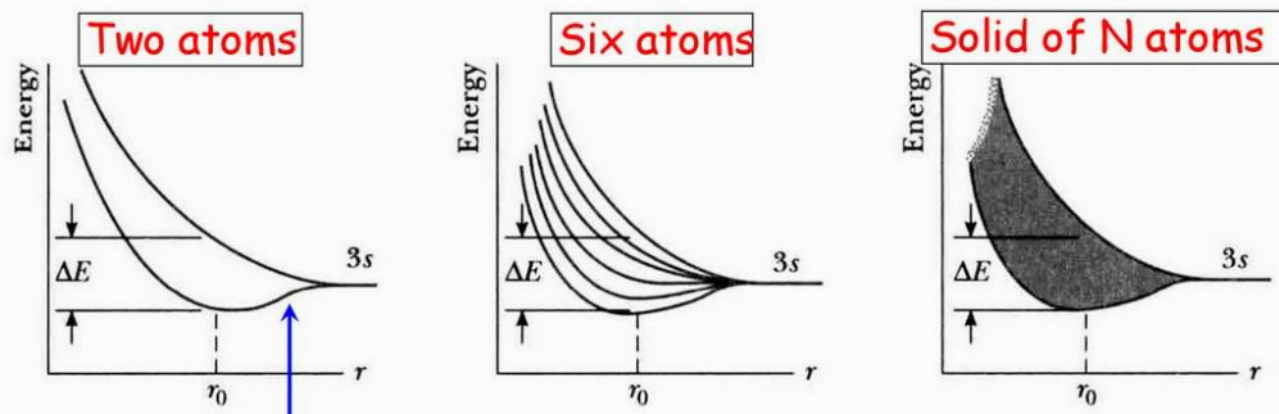
$$E_n = \frac{-Z^2 m_o q^4}{8 \epsilon_o^2 h^2 n^2}$$



Energy levels and transitions between them for the Hydrogen Atom

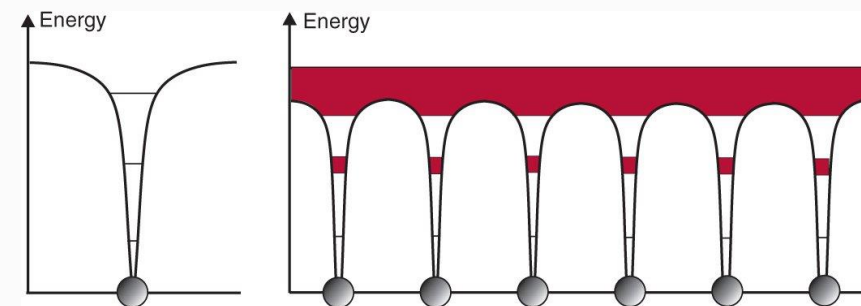
# Electrons in an Atom Have Fixed Allowed Energy Levels

Bringing multiple atoms together in a lattice forces the electron energies to split

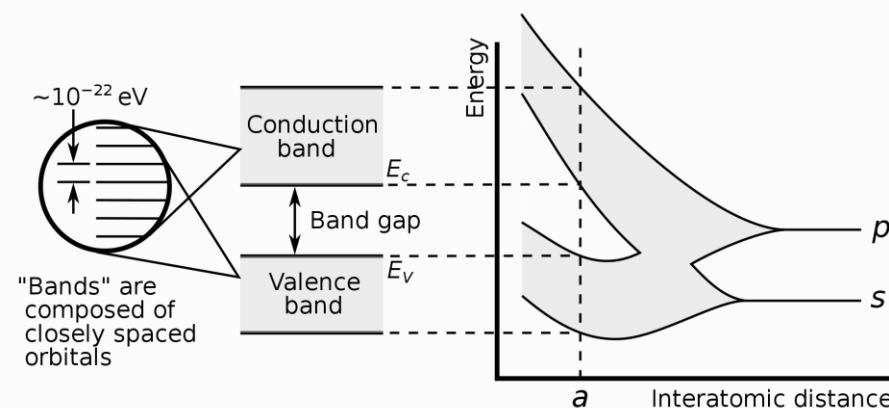


Electrons must occupy different energies due to Pauli's exclusion principle

- Bringing **two atoms** together splits the energy levels of the atoms' electrons into **two slightly separated energy levels**
- Bringing **N atoms** together causes the original electron energy level,  $E_n$ , to split into **N different allowed energy levels** which form an energy band.
- An energy band with N levels can contain up to  $2N$  electrons because two electrons of opposite spin can inhabit one energy state

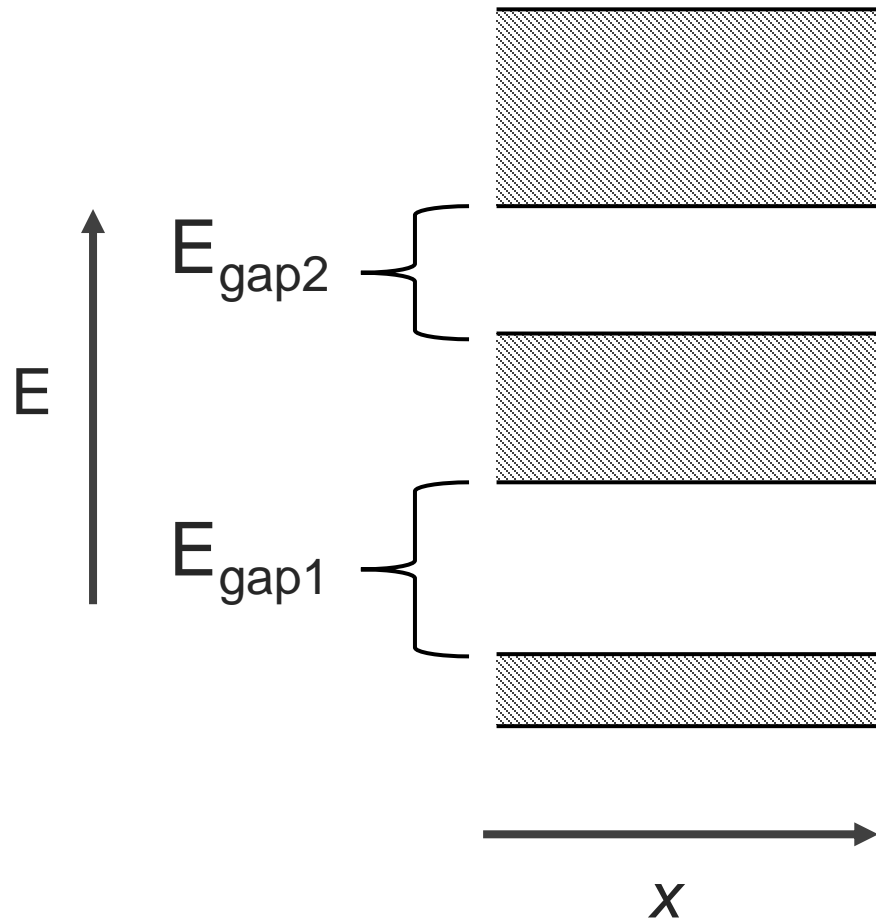


Potential energy of a 1-dimensional material



# The Broadening of Allowed Energy Levels into Bands and Gaps

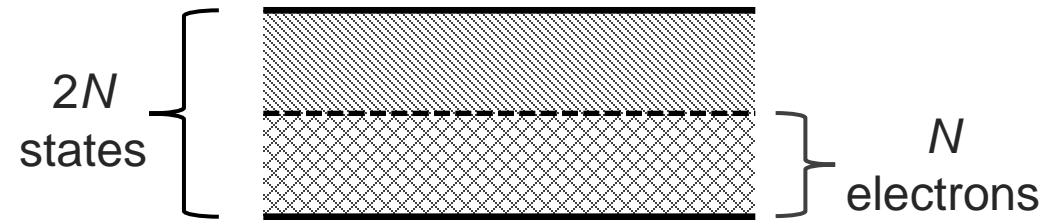
Plotted as energy versus distance in one dimension



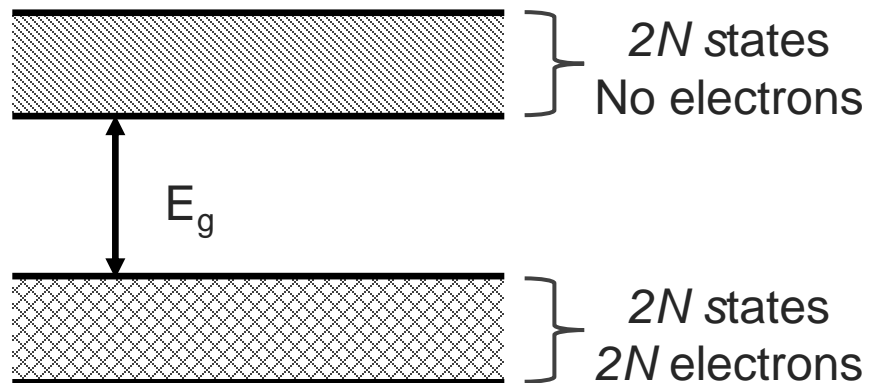
- The separation between the N energy levels within a band is much less than the average thermal energy of an electron at room temperature
- Electrons are therefore free to move between different levels within a band
- However, bands are bounded by minimum and maximum energy levels, and they are separated by *forbidden energy gaps*
- The detailed behavior of the bands is what determines the electronic properties of a given material

# Band Models for Conductors and Insulators

Entirely filled or entirely empty states cannot conduct electricity



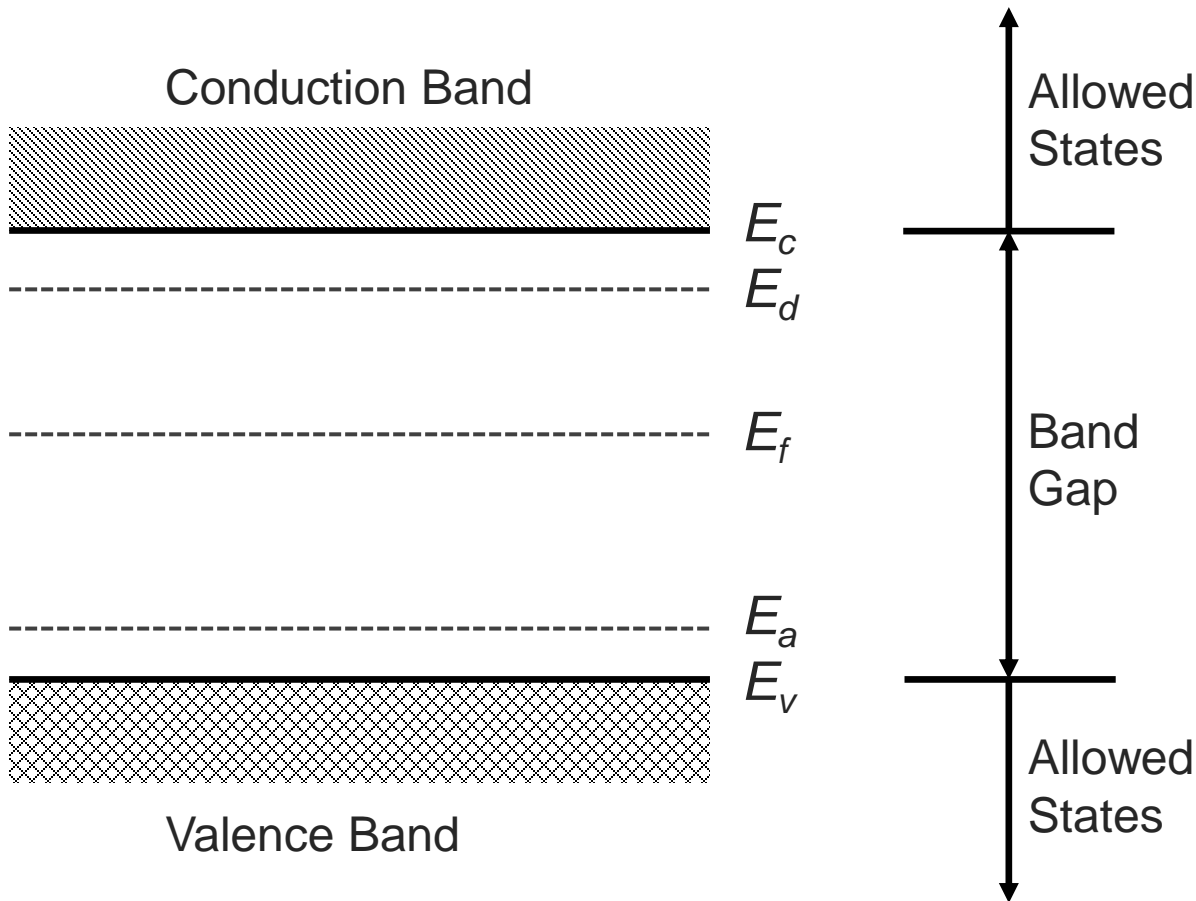
Band model for a conductor



Band model for an insulator

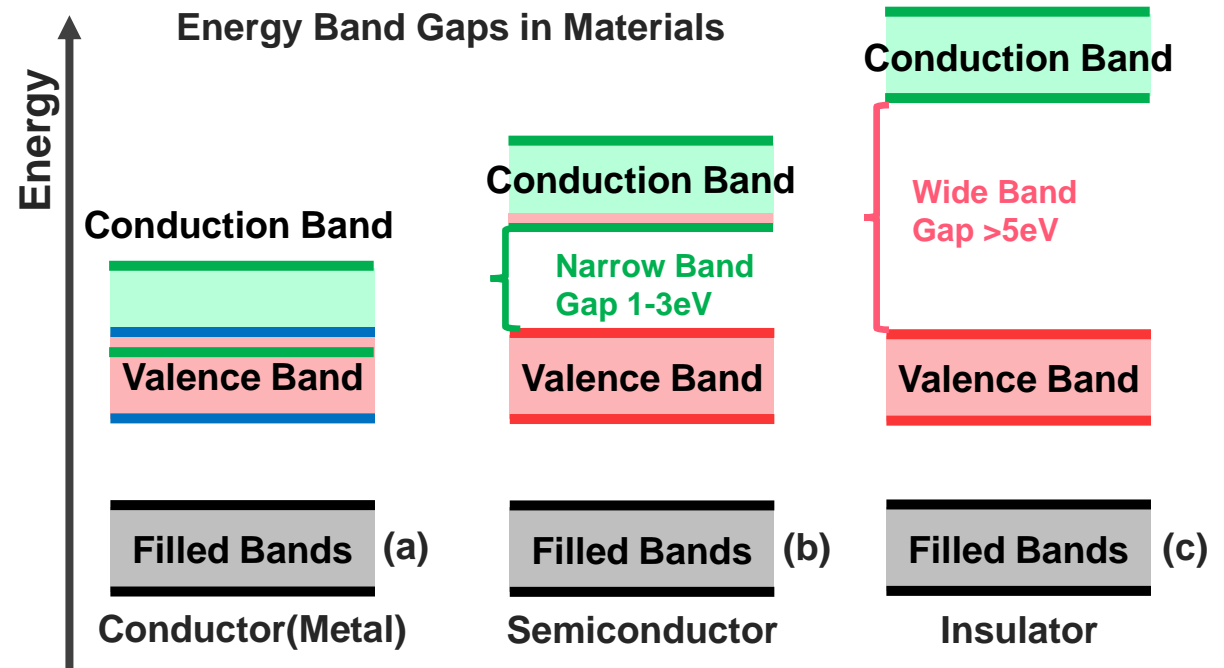
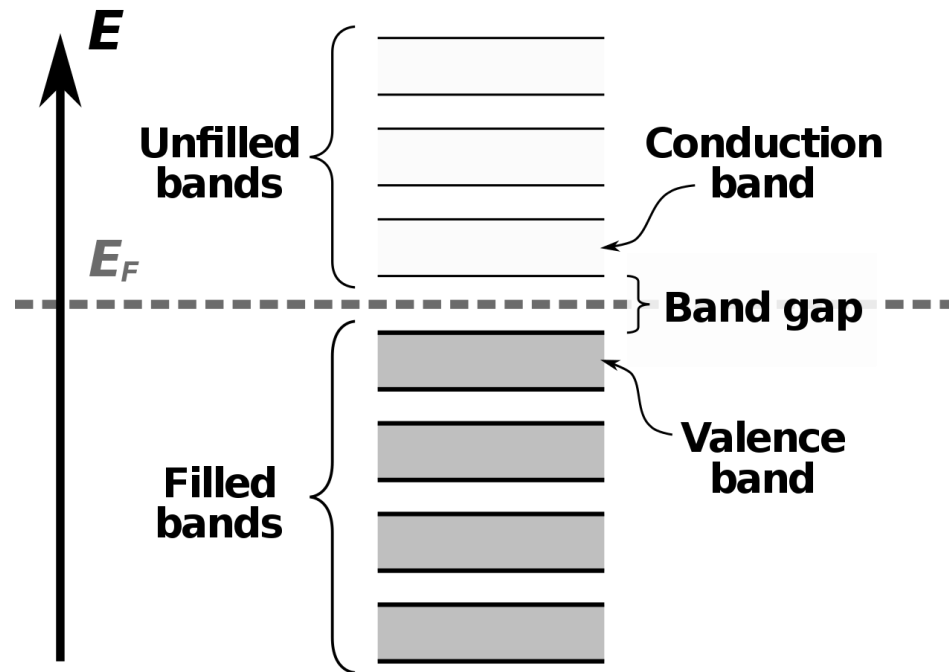
# Band Model for a Semiconductor

Doping a semiconductor creates electron donors and acceptors



- Doping the semiconductor with electron donors ( $E_d$ ) adds electrons to the conduction band, creating excess electrons (an “n” type semiconductor)
- Doping the semiconductor with electron acceptors ( $E_a$ ) removes electrons from the valence band, creating electron holes (a “p” type semiconductor)
- The Fermi energy level ( $E_f$ ) is analogous to the “average” energy of the system, and it is always constant across different material interfaces

# Energy Band Gaps In Materials

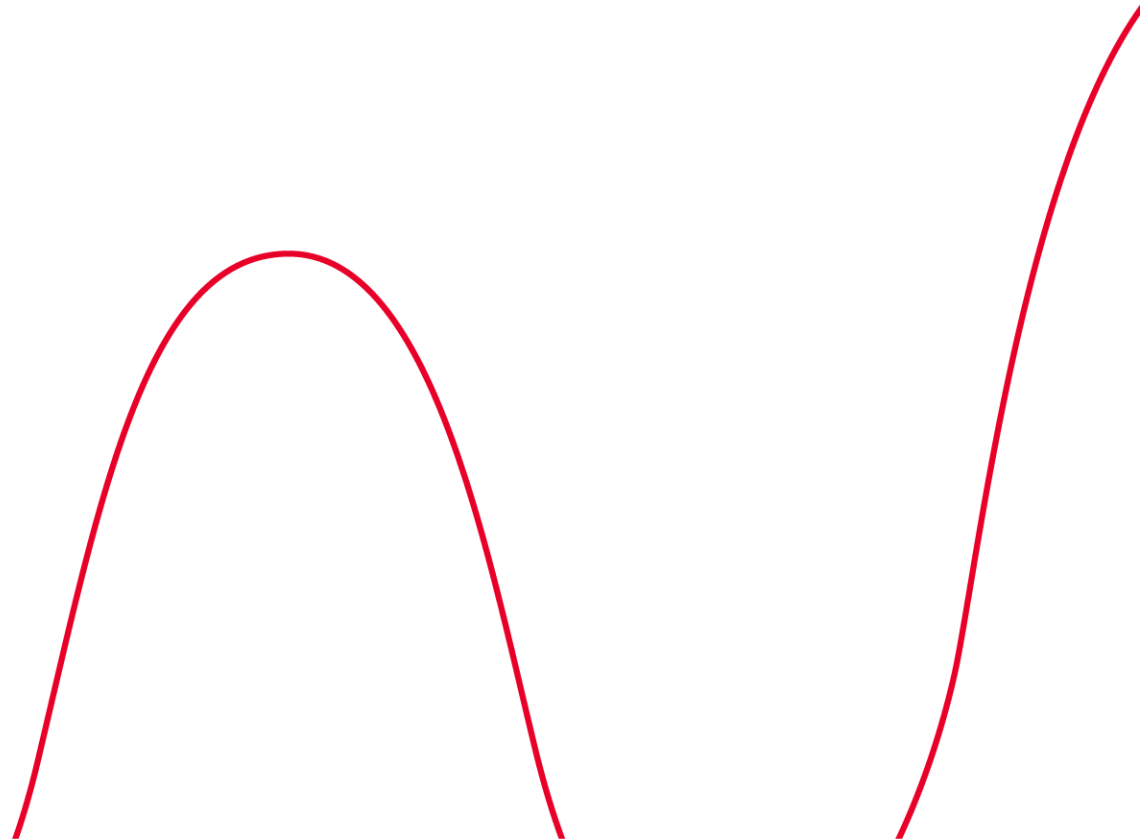


Material	Resistivity Carrier Type ( $\Omega\cdot\text{m}$ )	Density (cm-3 )	Type
Cu	$2 \times 10^{-8}$	$10^{23}$	Conductor
Si	$3 \times 10^3$	$10^{10}$	Semiconductor
Diamond	$2 \times 10^{16}$	small	Insulator

# Common Semiconductor Materials

Semiconductor materials		
Material	Chemical Symbol	Bandgap Energy (eV)
Germanium	Ge	0.7
Silicon	Si	1.1
Gallium Arsenide	GaAs	1.4
Silicon Carbide	SiC	3.3
Zinc Oxide	ZnO	3.4
Gallium Nitride	GaN	3.4
Diamond	C	5.5

# Why Use Wide Bandgap Semiconductors?



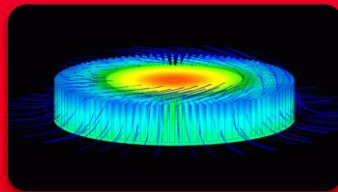
# Why Transition to Wide Band Gap Semiconductors?

Many improved performance parameters over silicon



## Improved Conversion Efficiency

- Reduced losses (switching and conduction)
- Higher voltages & currents
- Faster switching frequencies



## Smaller Cooling Systems

- Higher operating temperatures

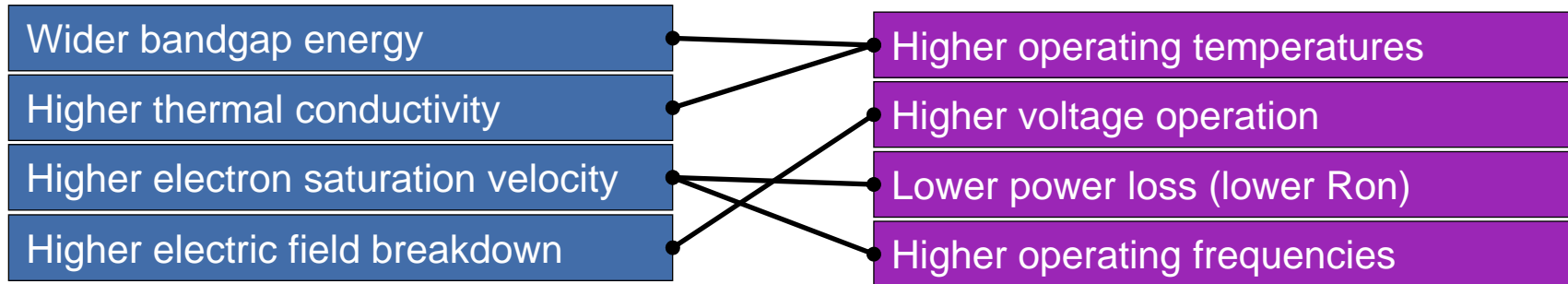


## Reduced Volume and Weight

- Smaller & lighter system components

## Benefits of WBG Power Devices

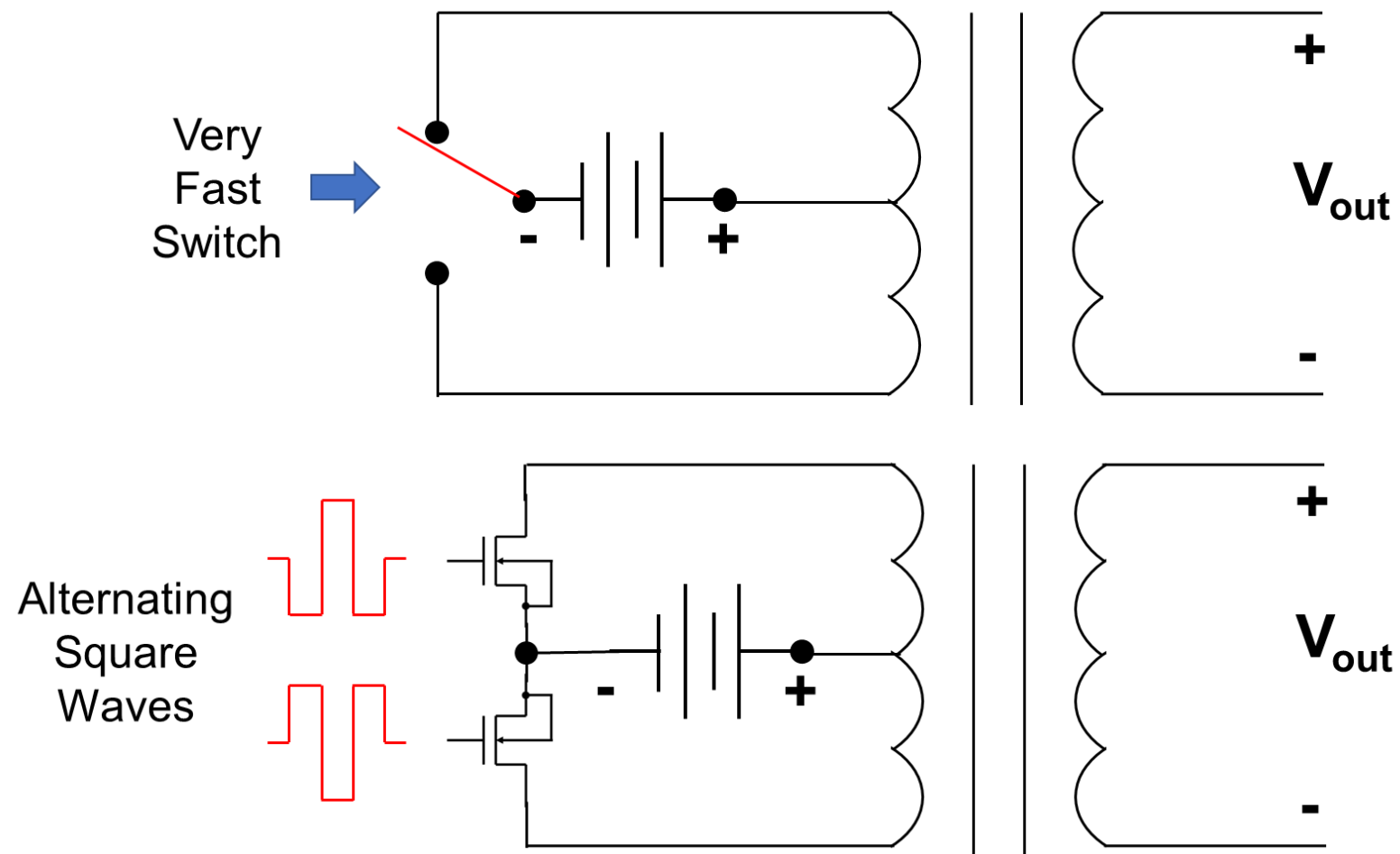
	Band gap energy $E_g$ (eV)	Thermal conductivity $\lambda$ (W/cm-°K)	Electron saturation velocity $V_{sat}$ ( $\times 10^7$ cm/s)	Electric field break- down $E_c$ (kV/cm)
Si	1.12	1.5	1	300
GaN	3.39	1.3	2.2	3300
4H-SiC	3.26	4.9	2	2200
Ga <sub>2</sub> O <sub>3</sub>	4.5 ~ 4.9	0.1 ~ 0.3	1.8 ~ 2.0	~ 8000
Diamond	5.45	22	2.7	5600



- The superior electrical properties of WBG power devices offers significant performance improvements over conventional silicon-based devices
- SiC has become quite commonplace
- GaN devices are gaining popularity, but still have some issues to resolve

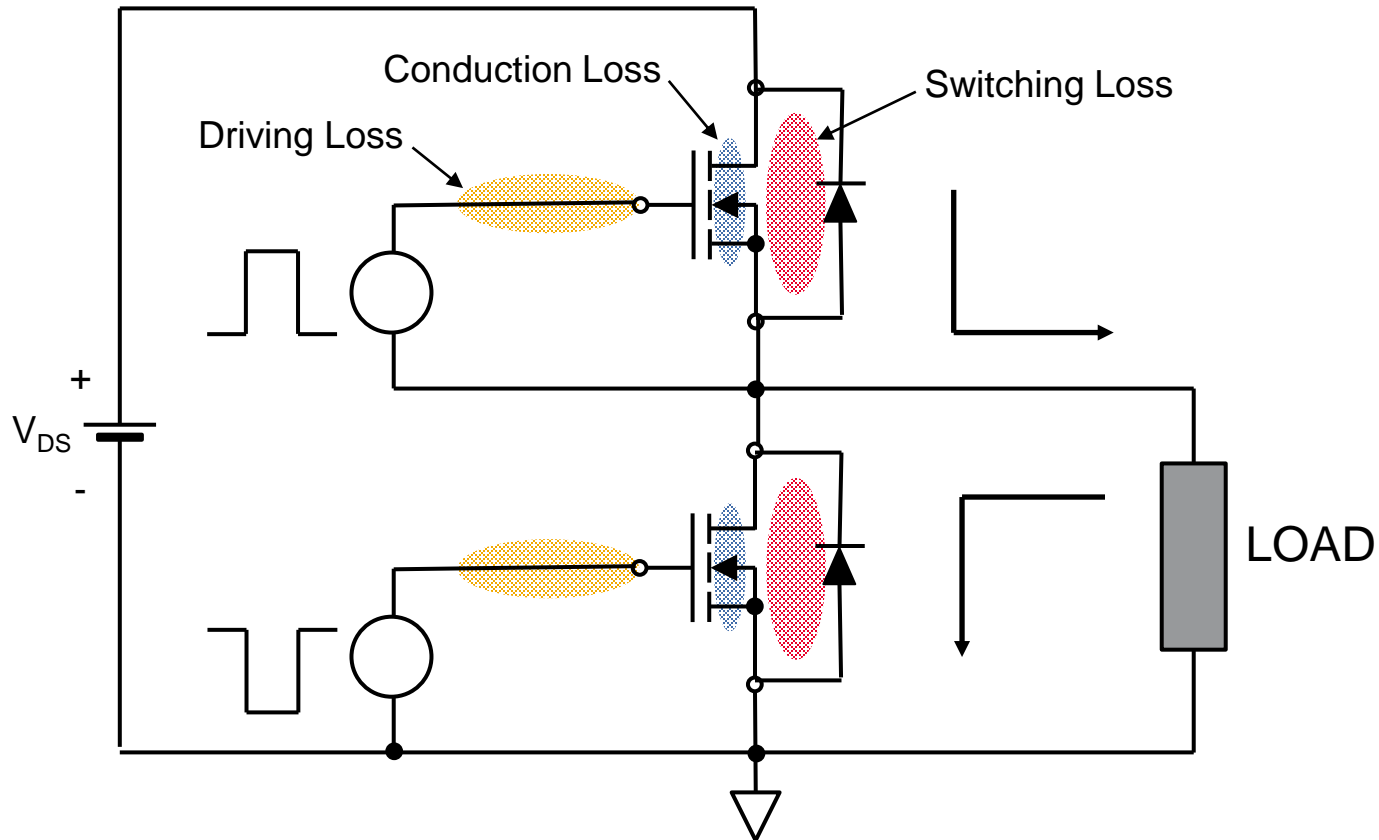
# DC to AC Conversion

## Power Inverters



# The Components of Semiconductor Power Loss

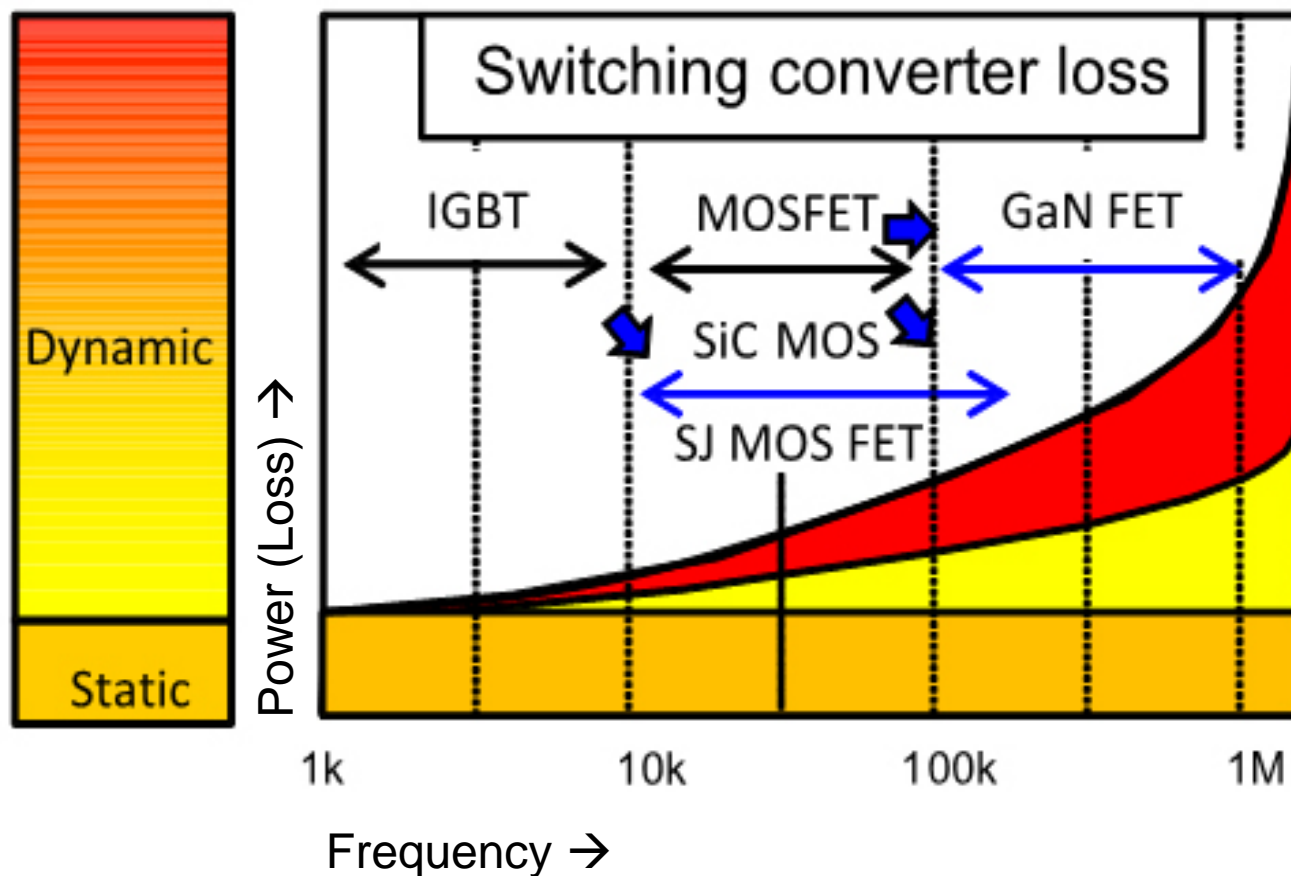
Total Loss	=	Conduction Loss	+	Switching Loss	+	Driving Loss
Key Parameters:		$R_{on}$		$R_g, C_{rss}, C_{oss}$		$Q_g$



- Conduction loss is due to the on-resistance of the transistor (very small for WBG devices).
- Switching loss is due to the transistor capacitances and gate resistance.
- Driving loss is due to the gate charge requirements of the transistor.

# Converter Power Loss Increases with Frequency

Switching and driving loss components dominate for WBG devices



## Drive Loss

$$= f * Q_g * V_{gs}$$

## Switching Loss

$$\propto f * (V * I * \Delta T) \propto R_g, C$$

## Conduction Loss

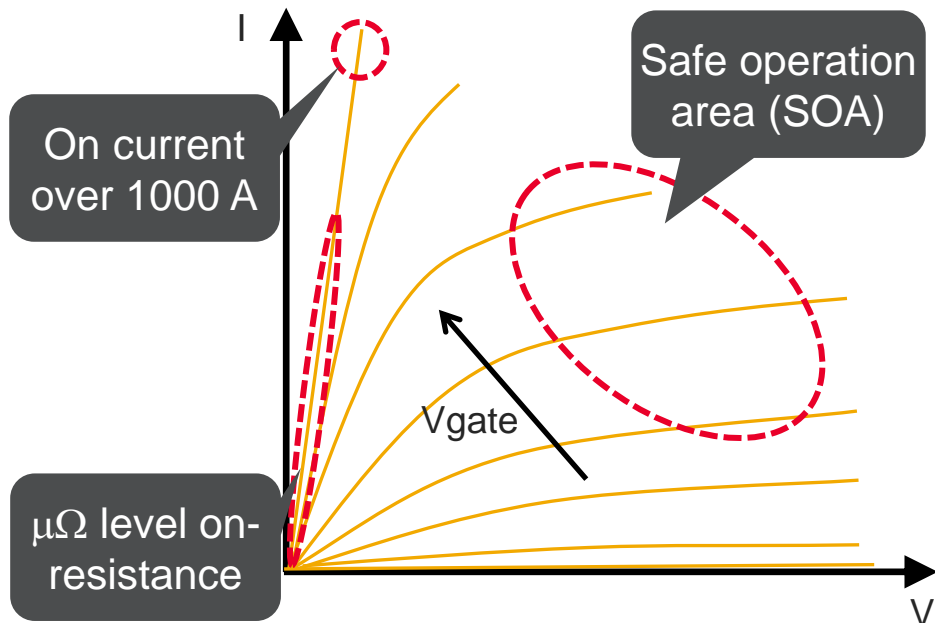
$$= R_{on} * (I_{RMS})^2$$

Device parasitic capacitances: Input capacitance ( $C_{iss}$ ), output capacitance ( $C_{oss}$ ) and reverse transfer capacitance ( $C_{rss}$ ). Gate charge  $Q_g$  is defined as the total amount of charge that is required to fully turn on a power device.

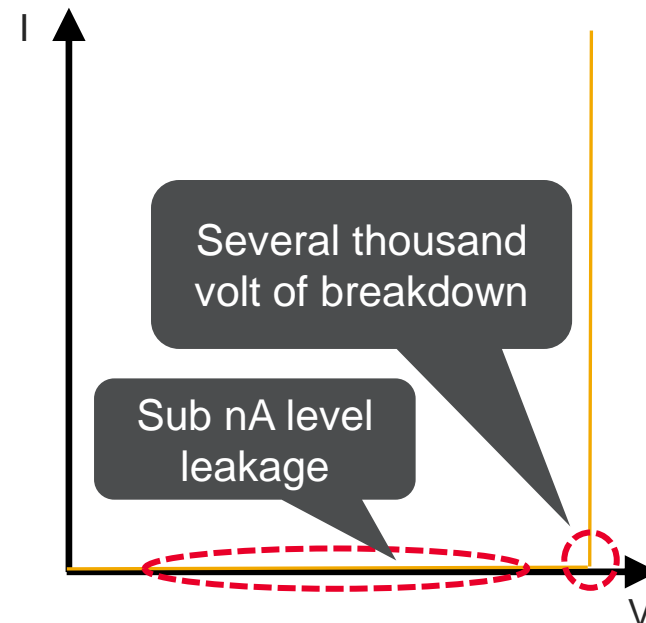
# WBG Power Device Characterization Test Requirements

- Measure resistance at high current levels in the ON-state
- Measure low current (leakage) characteristics at high voltages in the OFF-state
- Measure power loss as the device switches between its ON and OFF-states

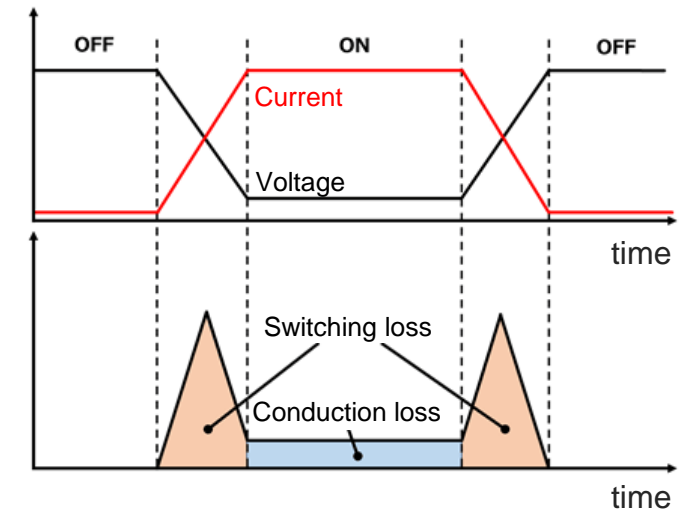
## ON Characteristics



## OFF Characteristics



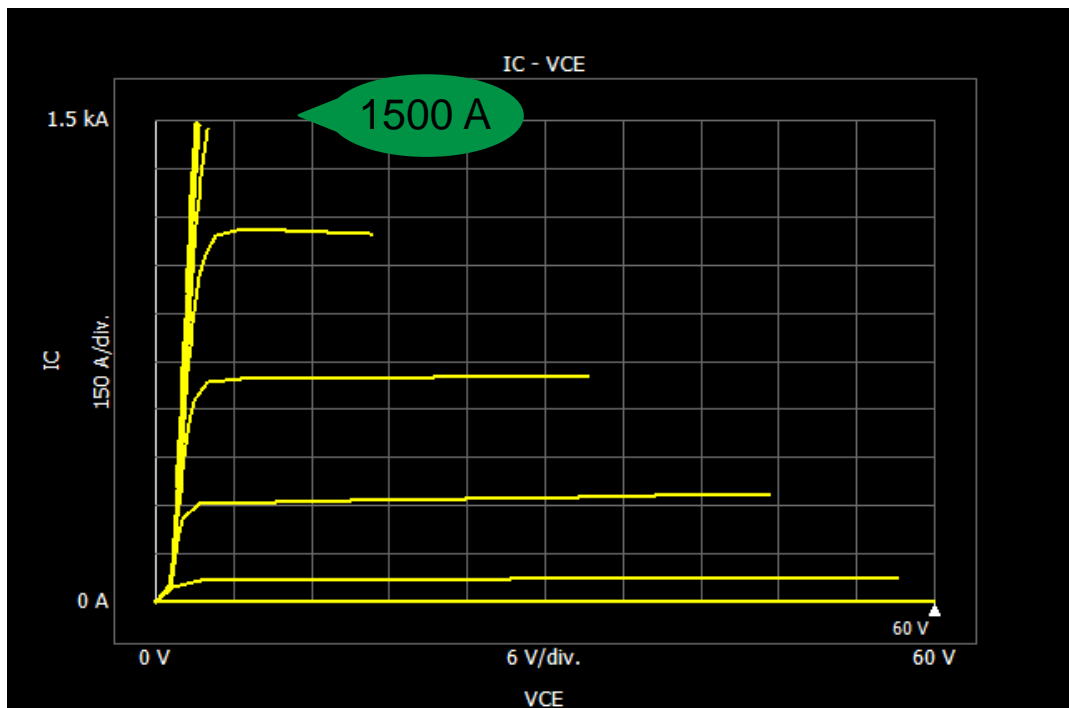
## Efficiency Characteristics



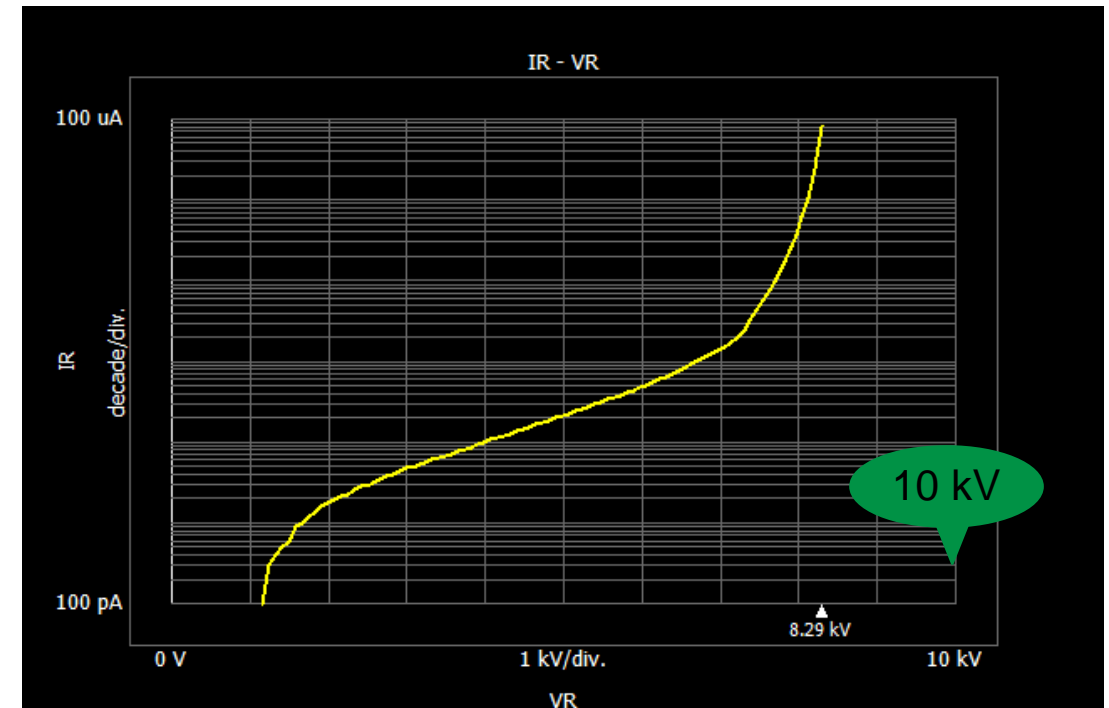
# WBG Power Devices Span Large Current/Voltage Ranges

ID-VD measurements at 1500 A and breakdown measurements at 10 kV are not uncommon

WBG devices often require much broader ranges of current and voltage than do silicon power devices



Ic-Vce family of curves created for an IGBT module

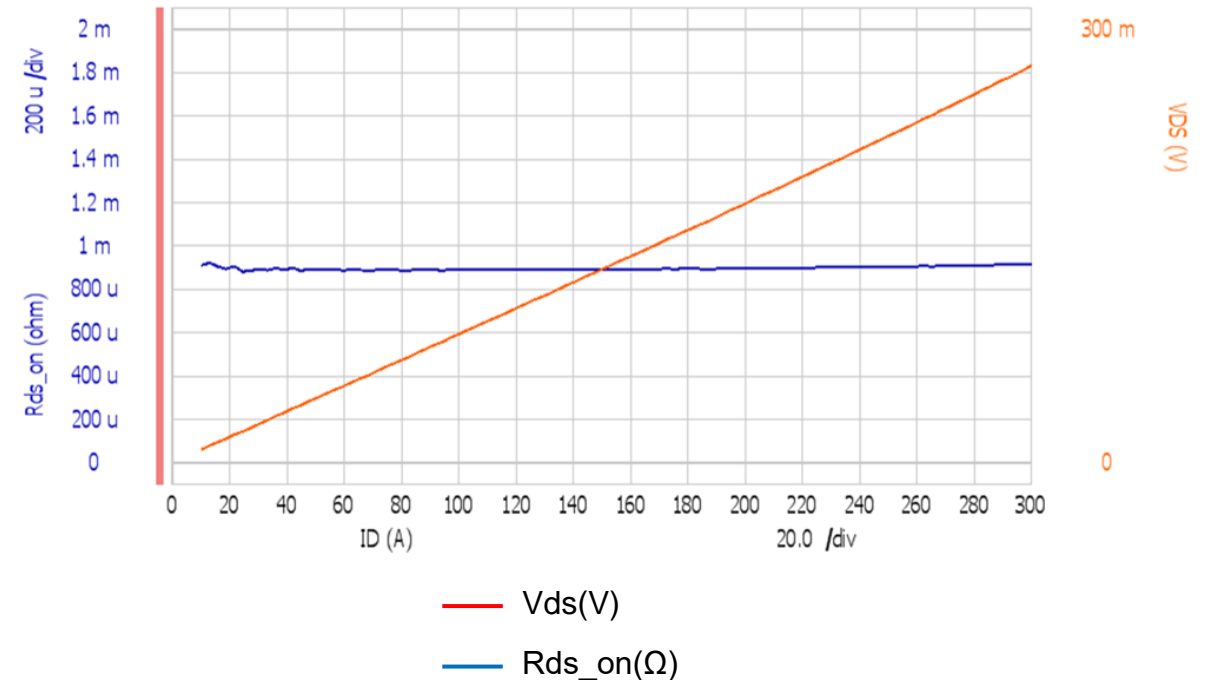
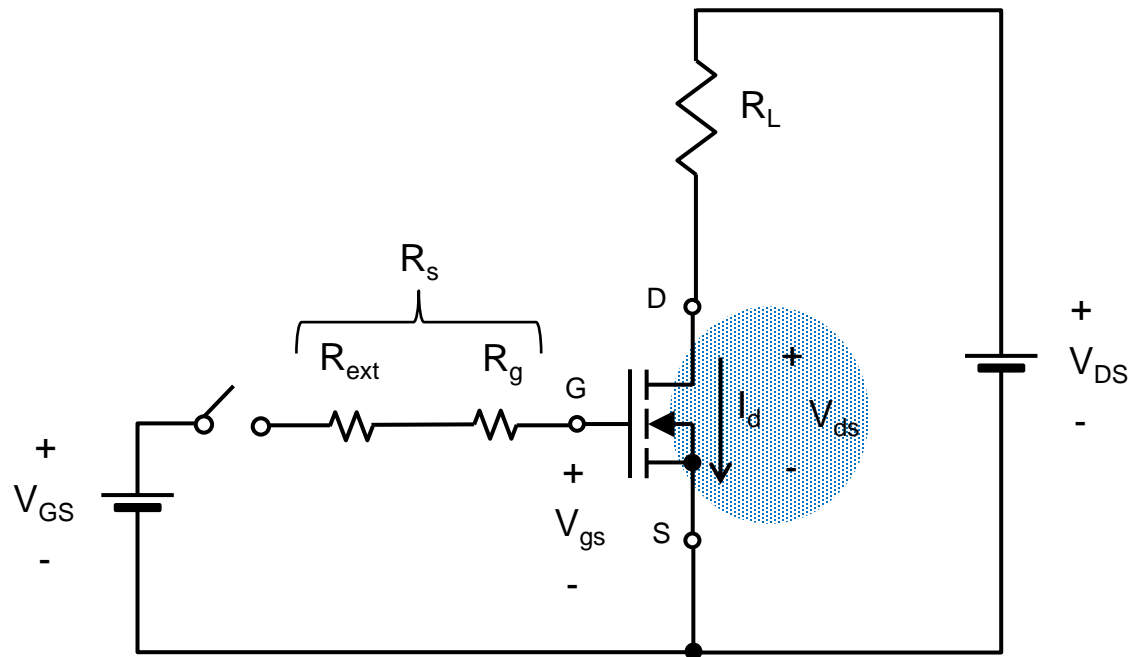


Breakdown measurement of an IGBT 8.3kV

# Conduction Loss is Always Present for Power Devices

Determining On resistance is not necessarily trivial

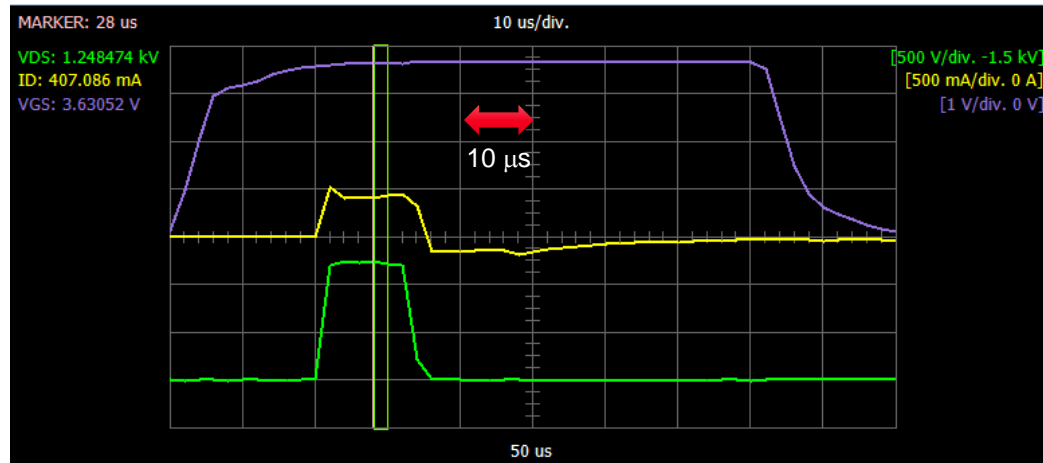
**Challenge** : Source hundreds of amps of current and at the same time accurately measure voltage in the microvolt range with extremely short pulses



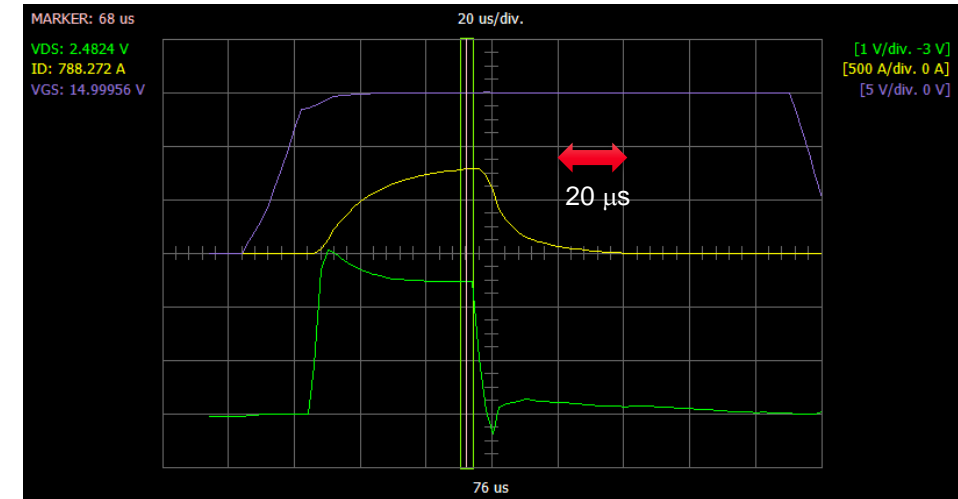
Accurate sub  $m\Omega$  measurements need to be made at hundreds of amps of current!

# Power Semiconductor IV Measurement Must be Pulsed

Needed to prevent device self-heating



10 µs high-voltage pulsed measurement

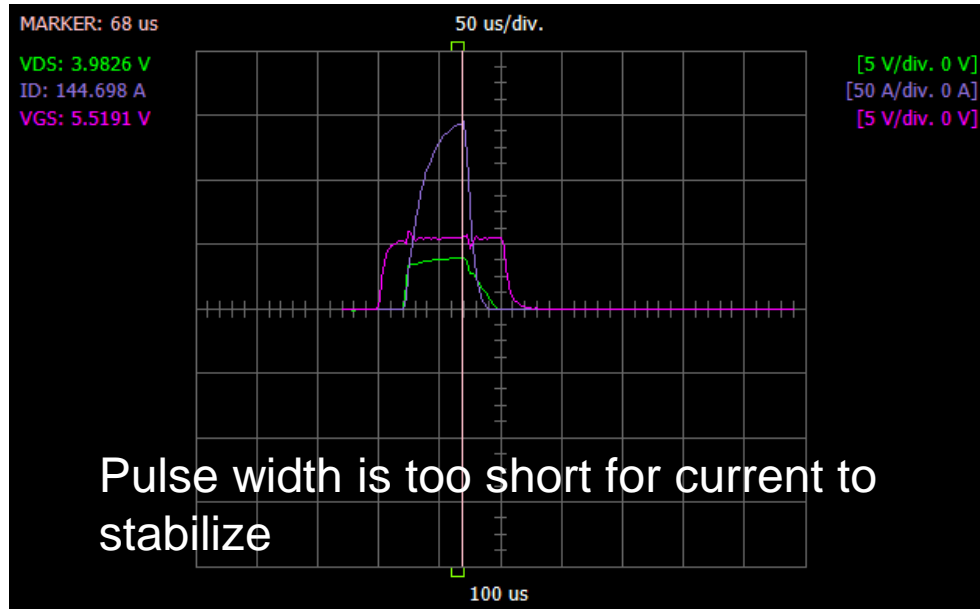


50 µs high-current pulsed measurement

Verifying device waveforms is often difficult or impossible using an oscilloscope or other conventional measurement instruments, so having this capability built-in to the power device analyzer is highly useful to maintain measurement integrity.

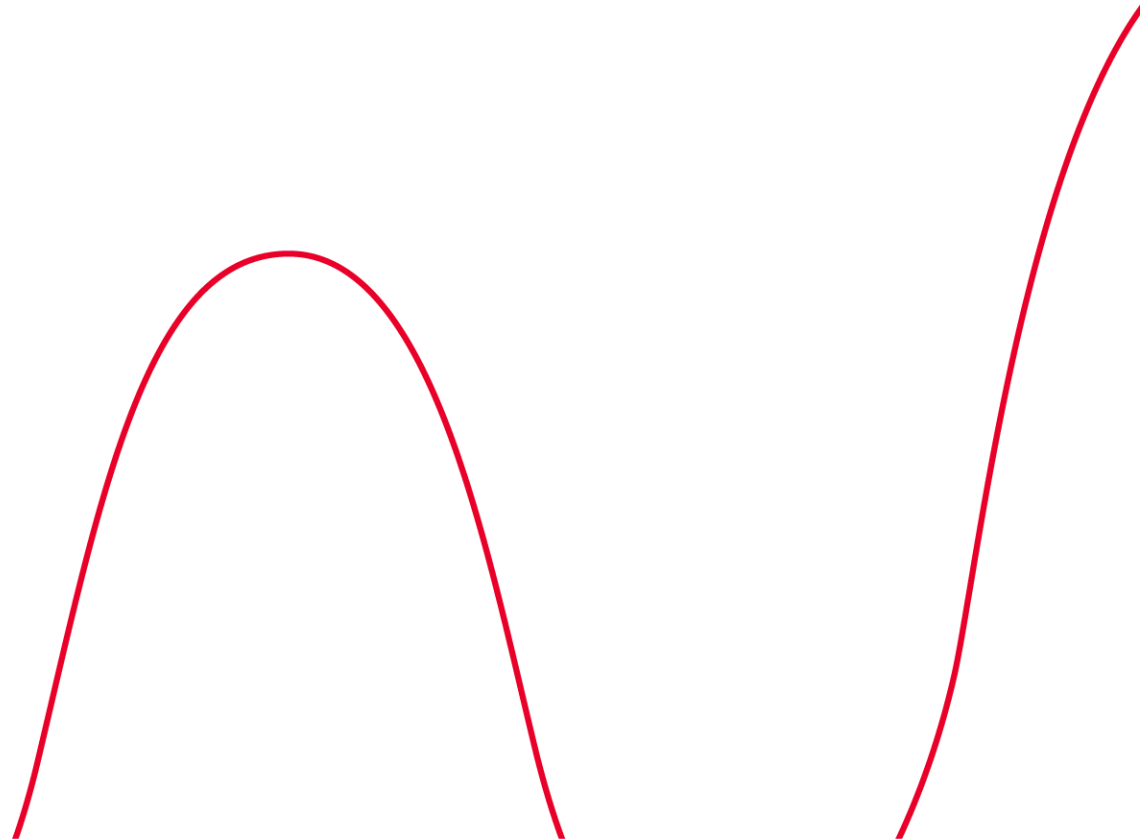
# Visually Verifying Pulsed Waveforms is Essential

Need to make sure pulses reach final value and no oscillations are occurring

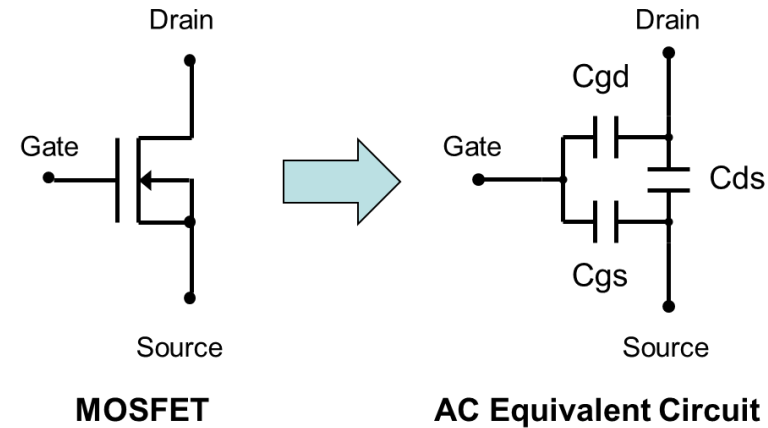
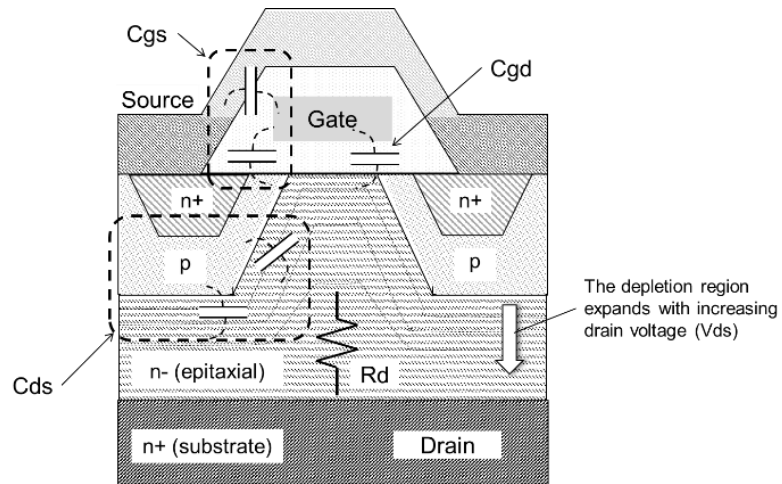


As you can see from this example, being able to visually verify the pulsed IV waveforms is important to obtain valid measurement results.

# Measuring Power Semiconductor Device Capacitance



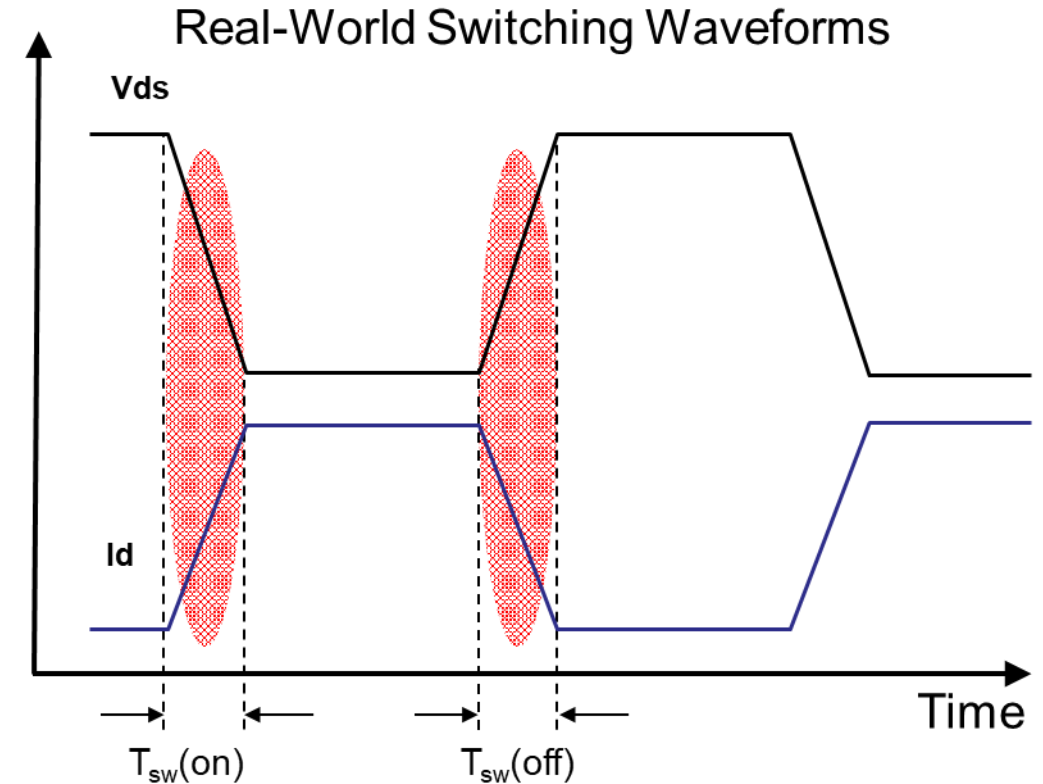
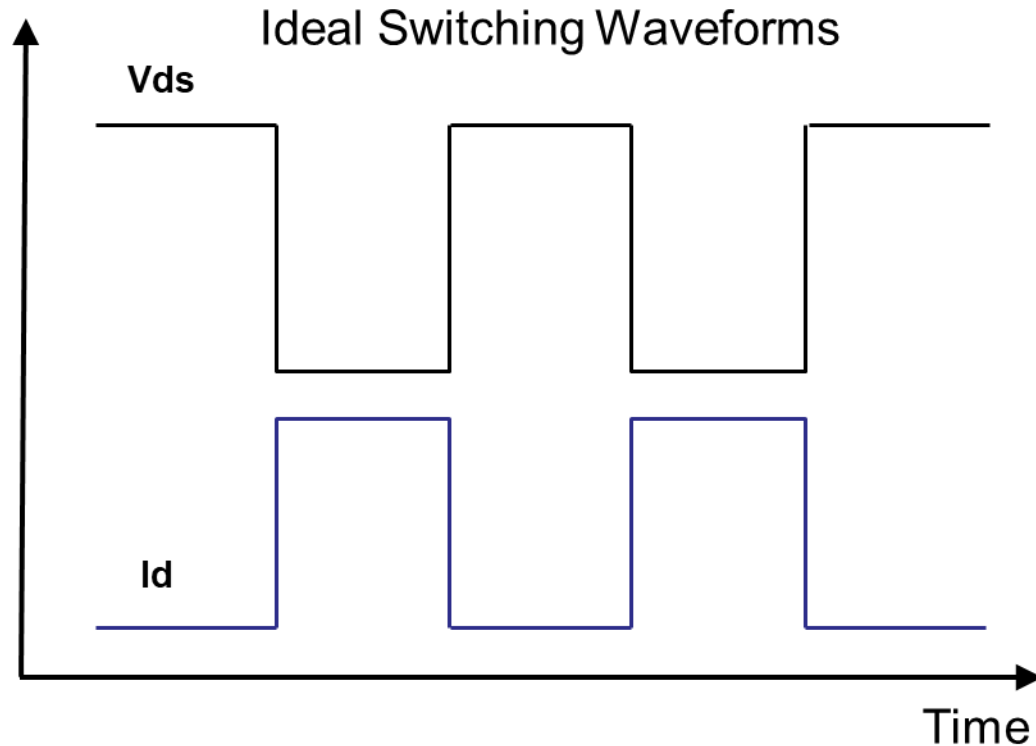
# Typical Dynamic Transistor Parameters



- Input capacitance  $C_{iss} = C_{gd} + C_{gs}$  ➡ Affects turn-on time
- Output capacitance  $C_{oss} = C_{gs} + C_{ds}$  ➡ Affects circuit resonance and dynamic behavior
- Reverse transfer capacitance  $C_{rss} = C_{gd}$  ➡ Affects turn-off times

# Switching Loss Increases with Frequency

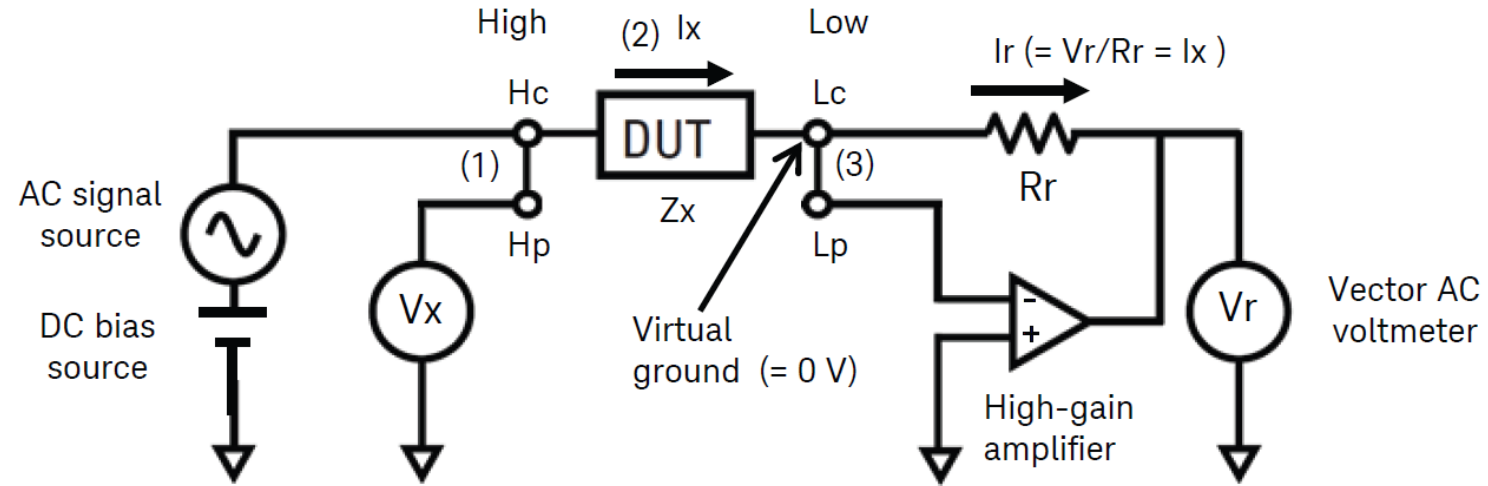
Dependent on the device capacitances



**Challenge:** Measuring capacitances on power devices is not simple. Capacitances must be measured under their operating conditions, potentially thousands of volts across the device drain-to-source (or collector-to-emitter).

# CV Measurement Bridge Technique

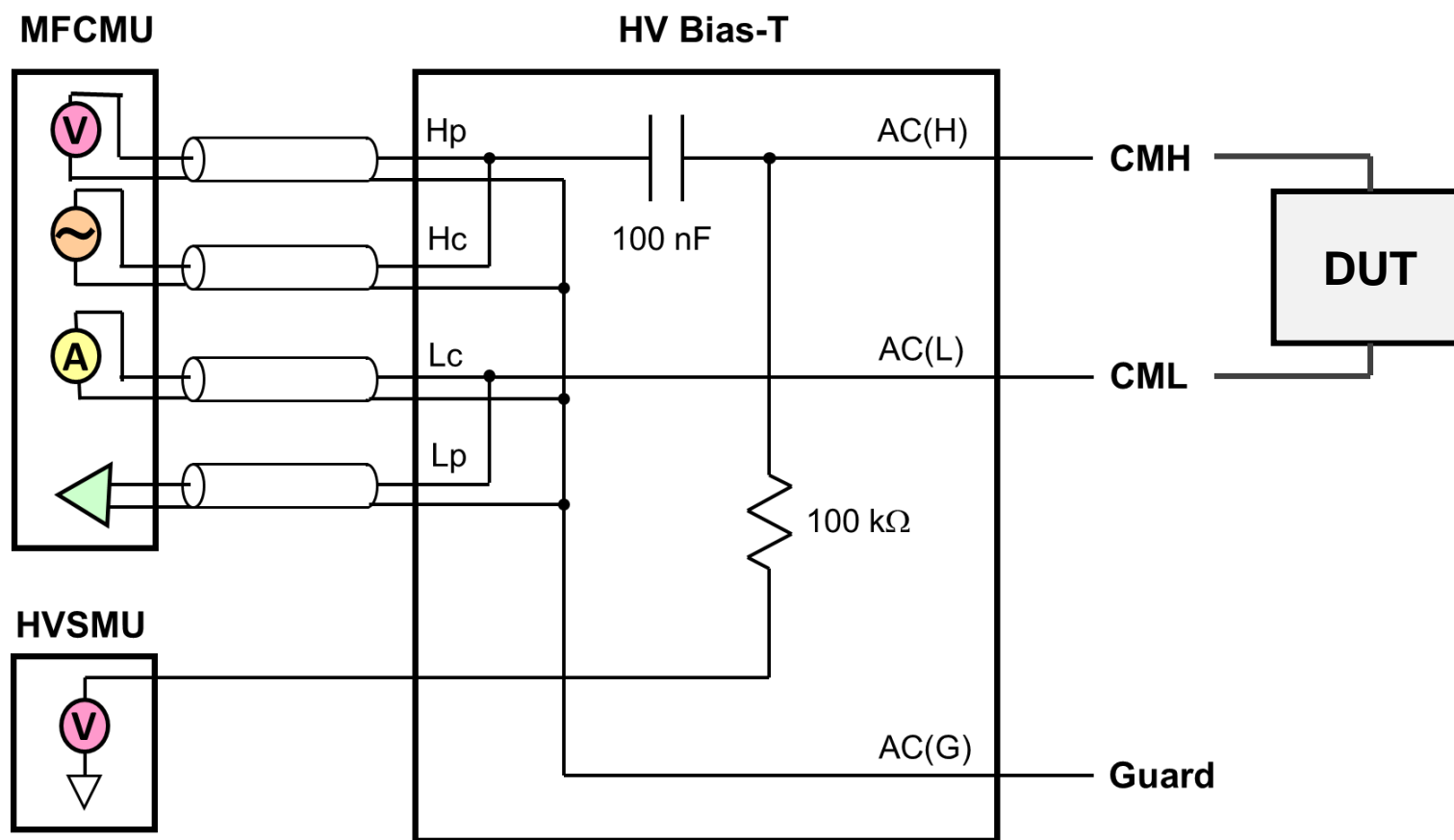
## Auto Balancing Bridge



Equation for DUT impedance:  $Z_x = \frac{V_x}{I_x} = R_r \frac{V_x}{V_r}$

### Simplified auto balancing bridge type CV meter block diagram

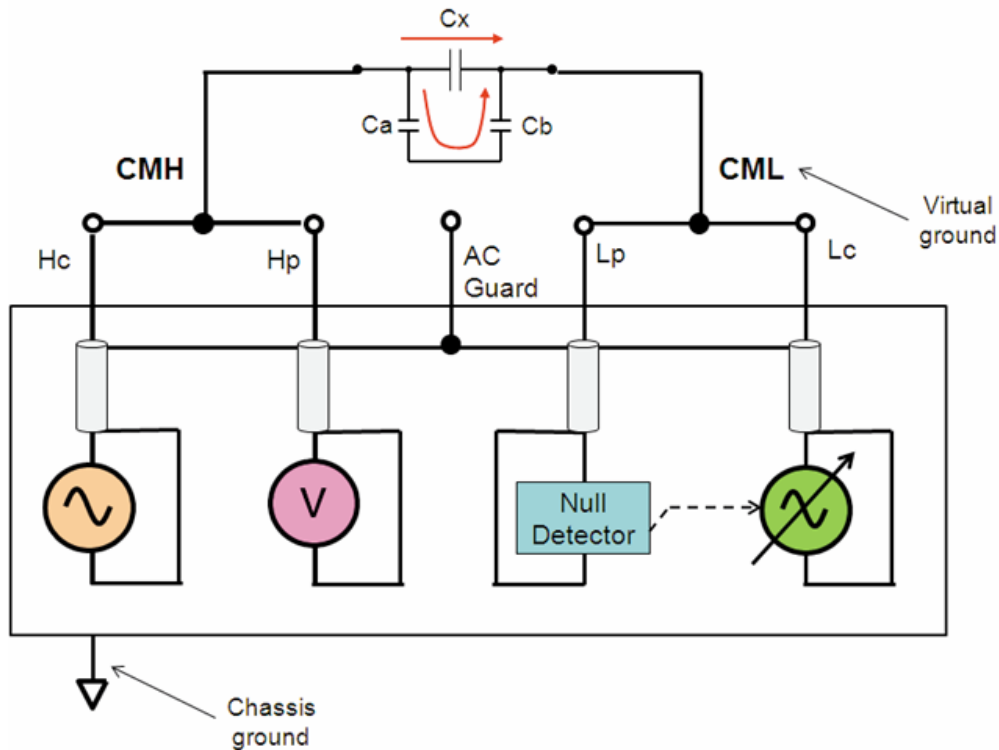
# Capacitance Measurement is Tricky for Power Devices



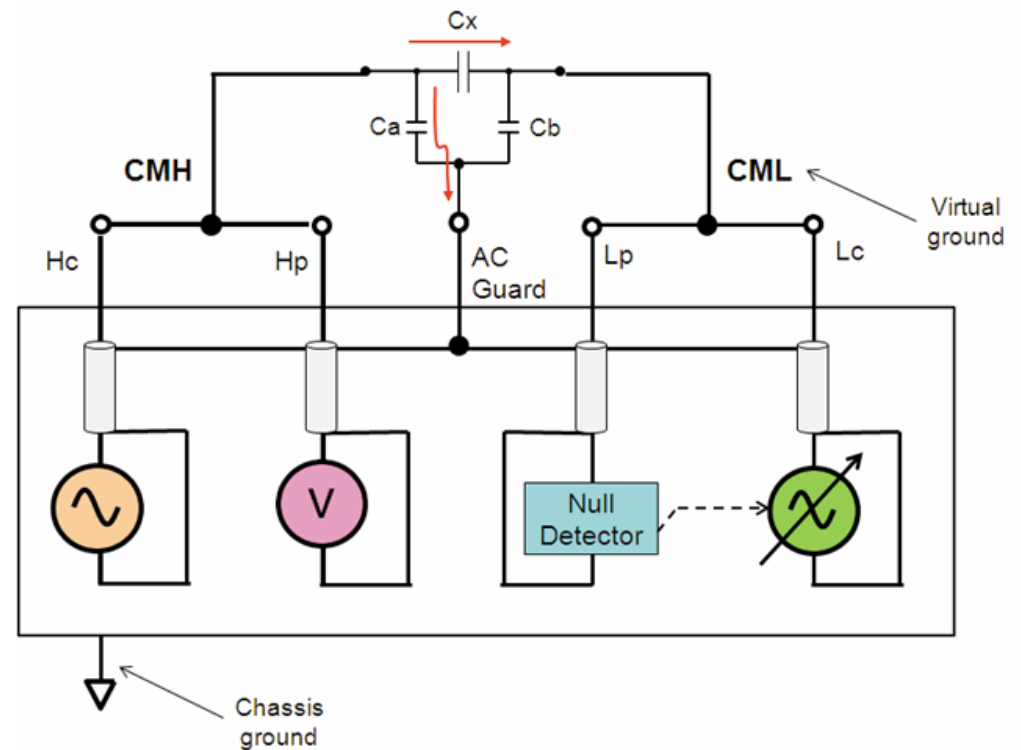
High-voltage bias-T: Combine a MFCMU with a high-voltage SMU

DC bias can be at thousands of volts while the AC signal is in the tens of millivolts.

## Why Do You Need a Separate Output for the AC Guard?



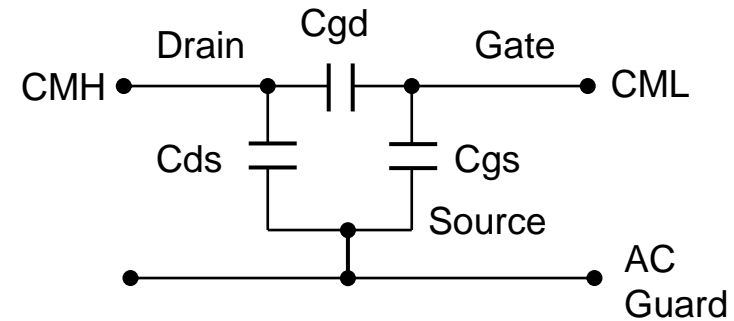
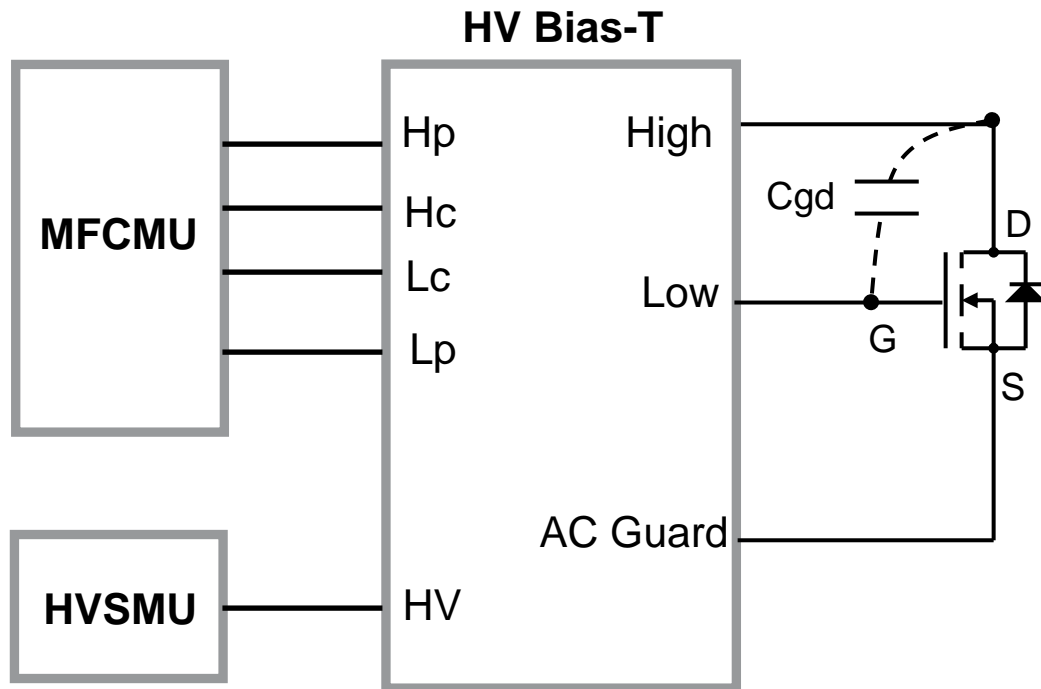
**Problem:** Some of the measured current passes through a parasitic path, which degrades measurement accuracy.



**Solution:** Use the AC guard to provide an alternative current path that keeps the parasitic current from going into the measurement node.

# Measuring $C_{rss}$ ( $=C_{gd}$ ) Using a HV Bias-T

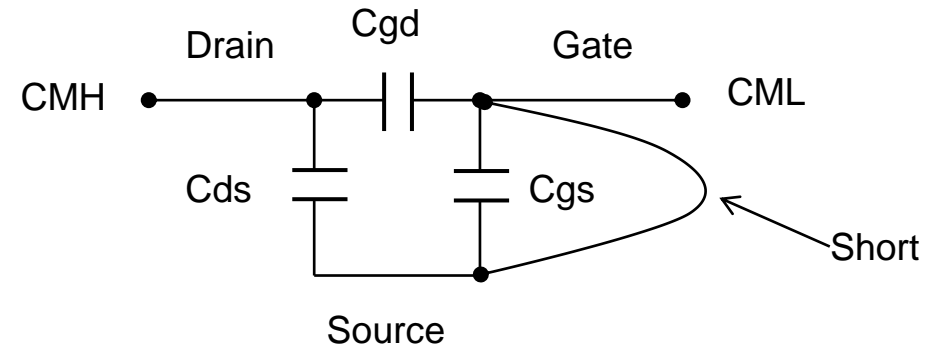
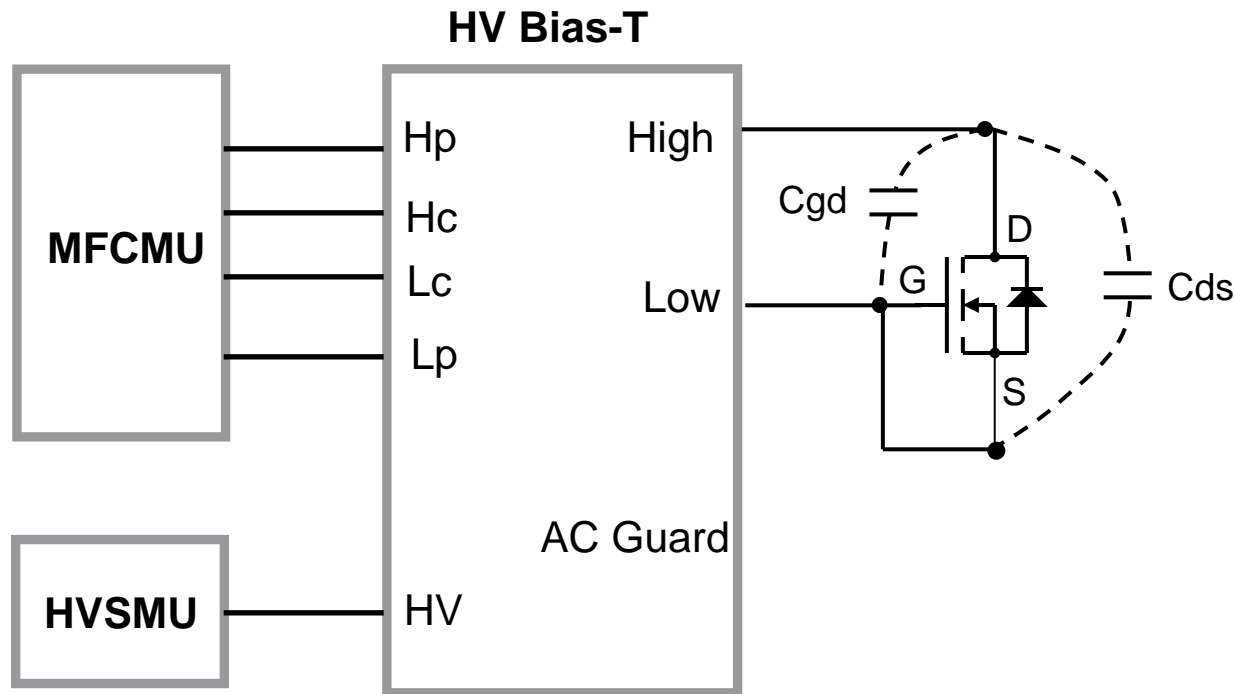
Normally OFF device



Connecting the AC Guard to the transistor source removes the  $C_{ds}$  and  $C_{gs}$  capacitances from the measurement.

# Measuring $C_{oss}$ ( $=C_{gd} + C_{ds}$ ) Using a HV Bias-T

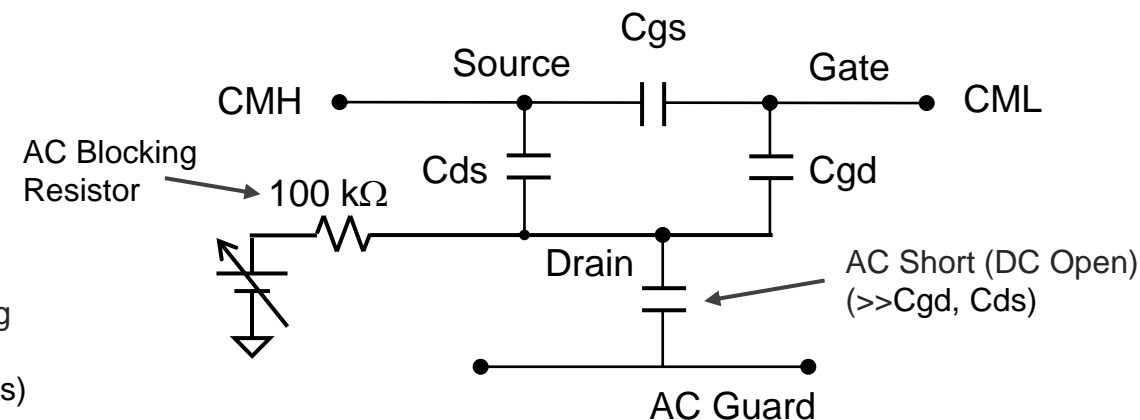
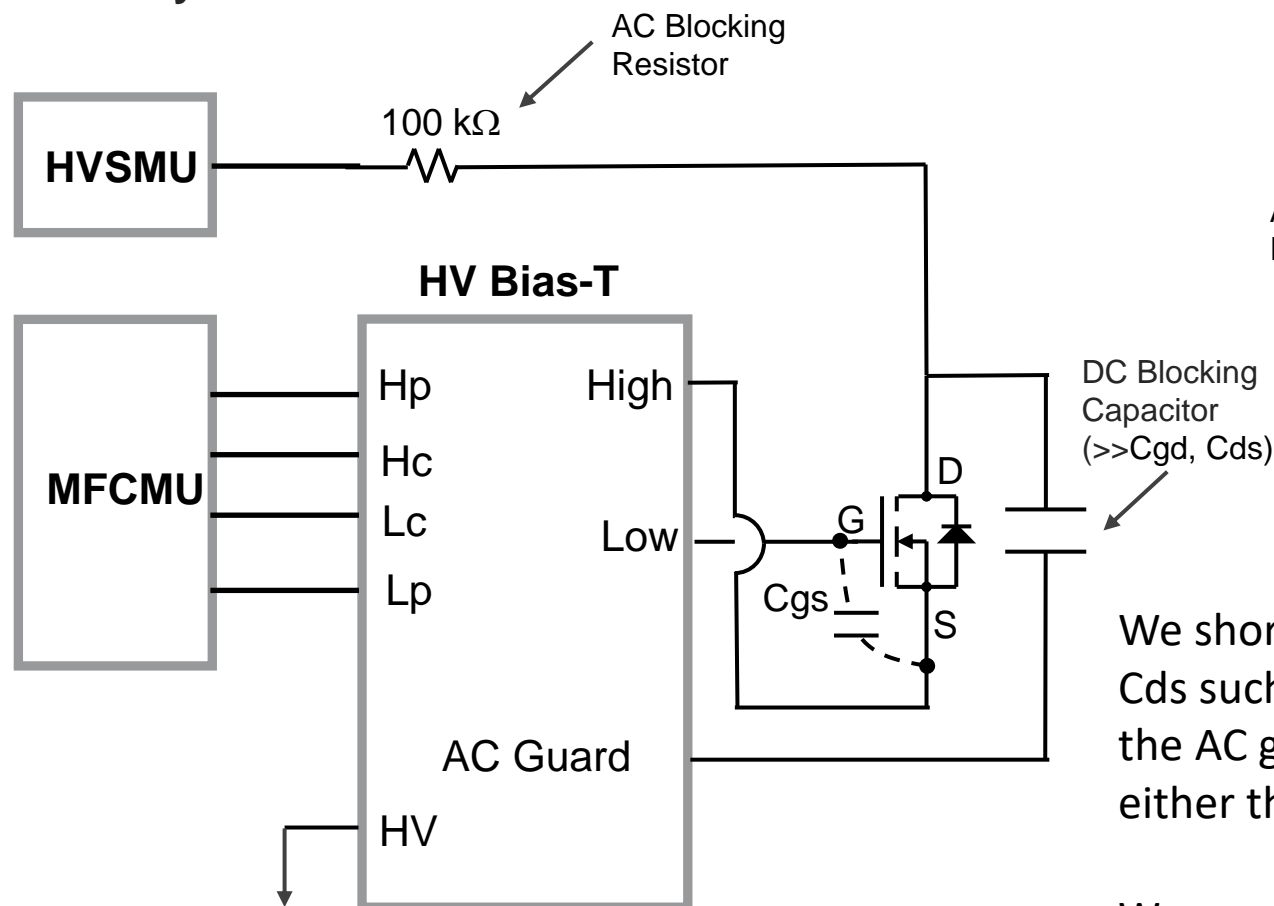
Normally OFF device



In this case we do not need the AC Guard since we are shorting out  $C_{gs}$  and we want to measure  $C_{gd}$  and  $C_{ds}$  in parallel.

# Measuring $C_{gs}$

Normally OFF device

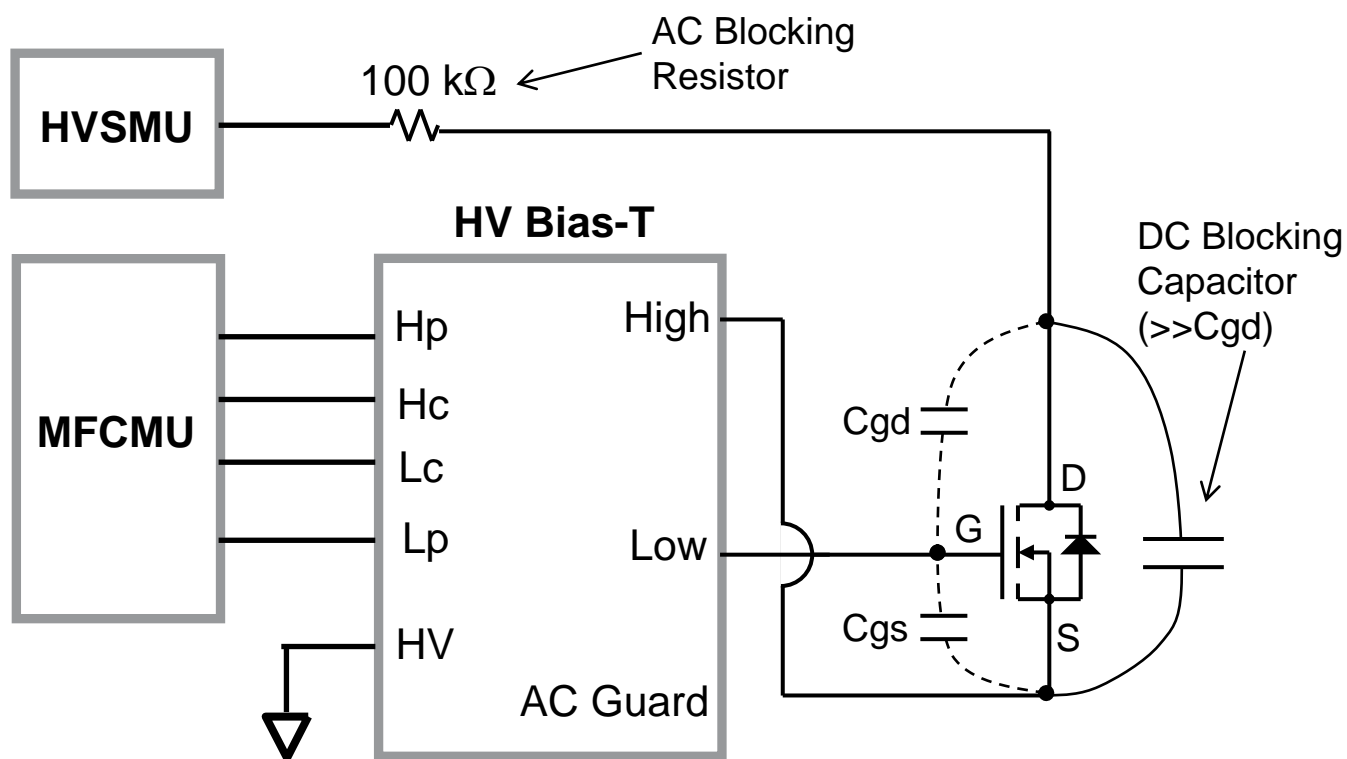


We short the AC guard to the drain via a large capacitor  $\gg C_{gd}$  or  $C_{ds}$  such that the impedance seen by the drain with respect to the AC guard is much smaller than the impedance that it sees to either the source or to the gate

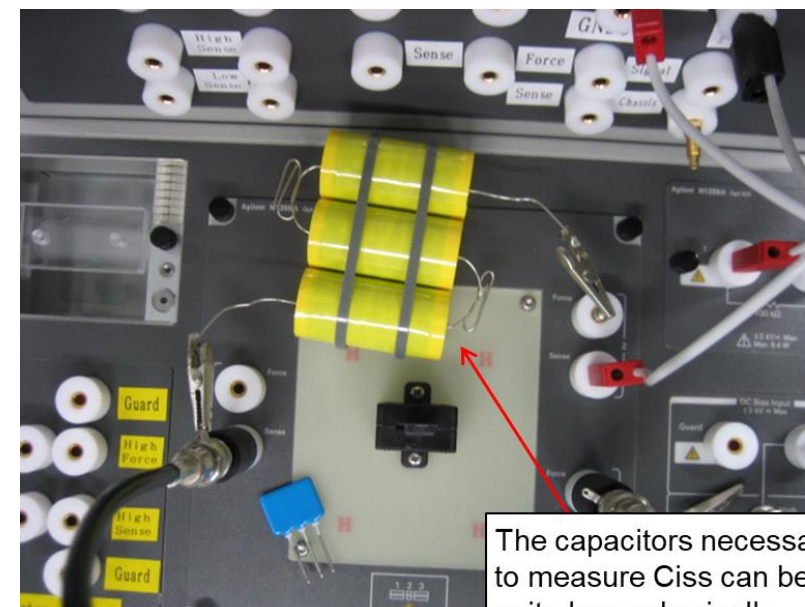
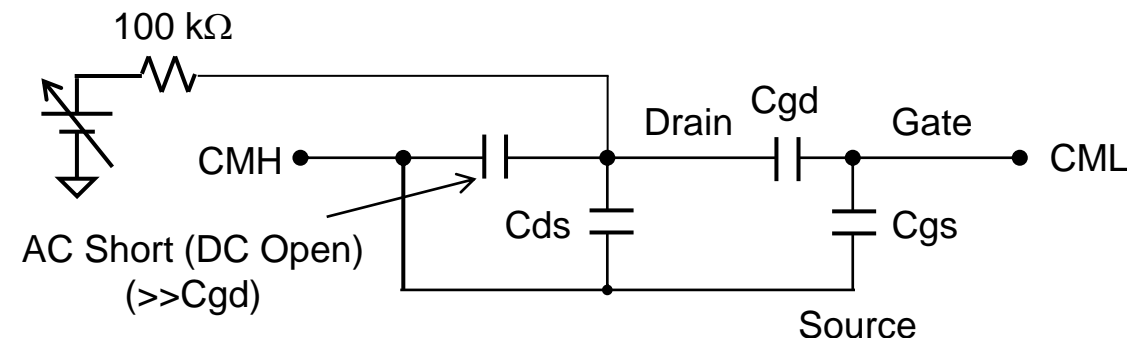
We also need to connect the HVSMU up to the drain through a relatively large resistor to prevent the HVSMU from interfering with the AC signal coming from the MFCMU

# Measuring Ciss (=Cgs + Cgd) Using a HV Bias-T

Normally OFF device



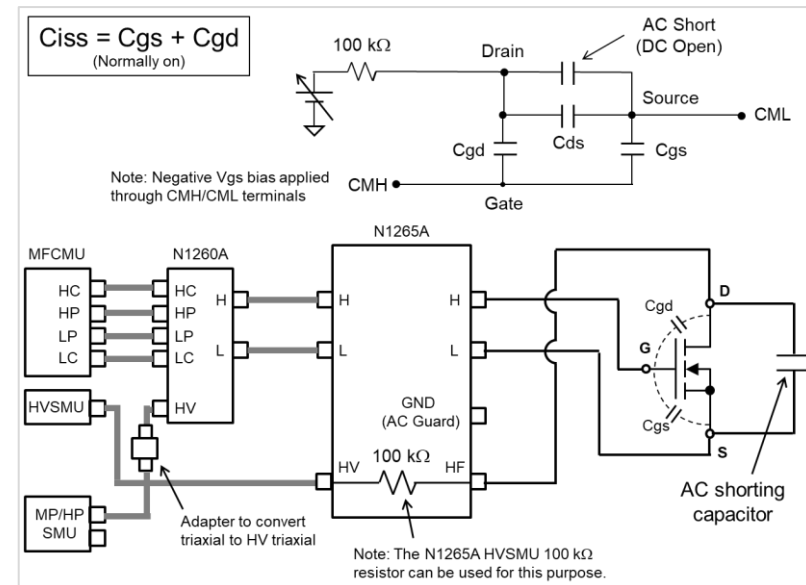
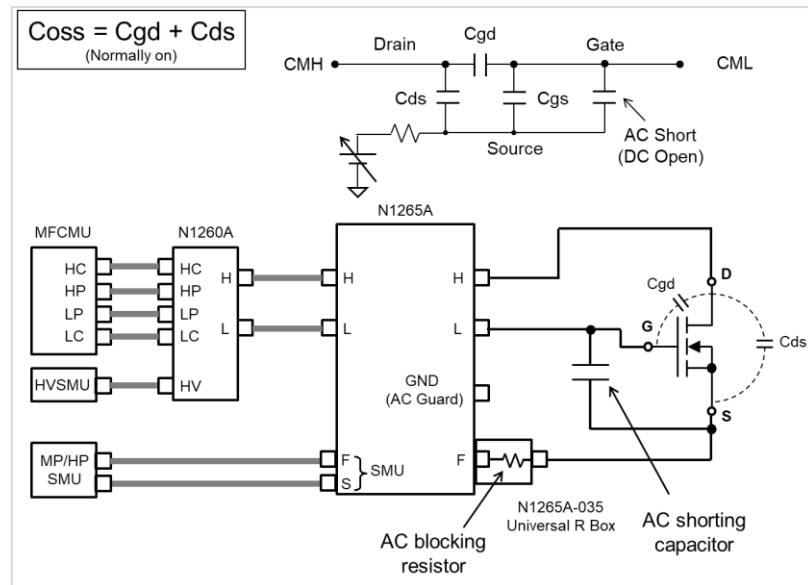
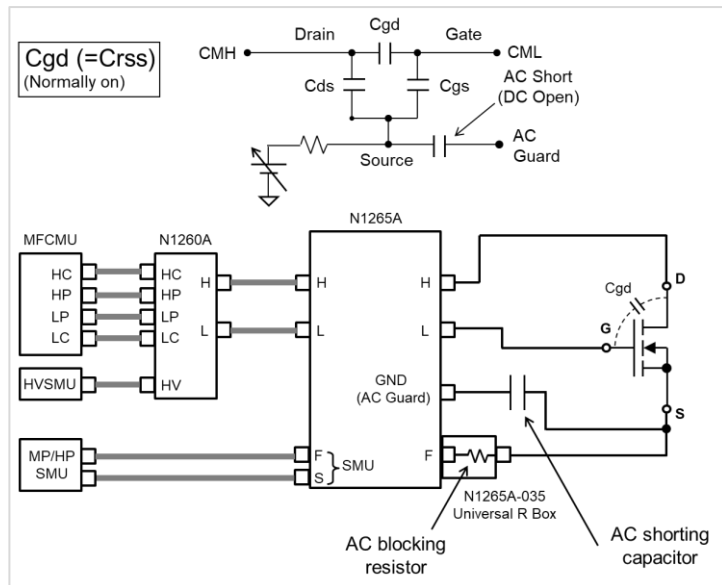
Here we are using a large capacitor to short out the drain-to-source in the AC, while still allowing a large DC voltage across these terminals.



The capacitors necessary to measure Ciss can be quite large physically.

# Measuring Capacitances Using a HV Bias-T

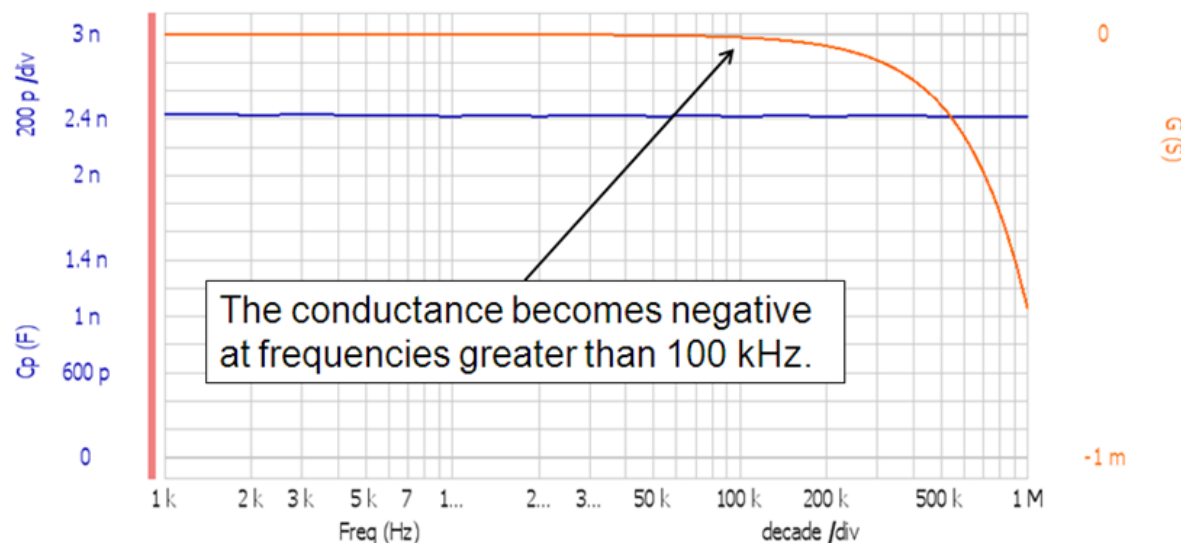
## Normally ON device



## Key Points:

- Need to follow all previous procedures while also keeping source biased positive to maintain a negative Vgs.
- Complexity (and chance for error) goes up significantly.

# Calibration Issues and Measurement Frequency



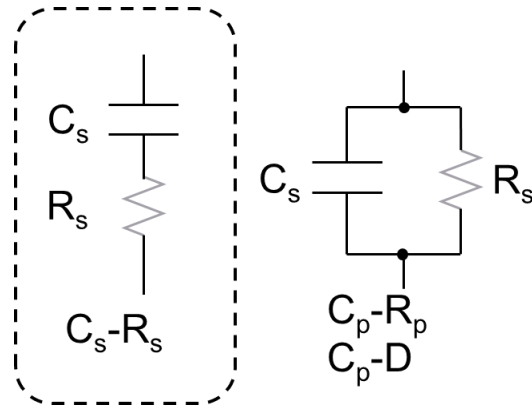
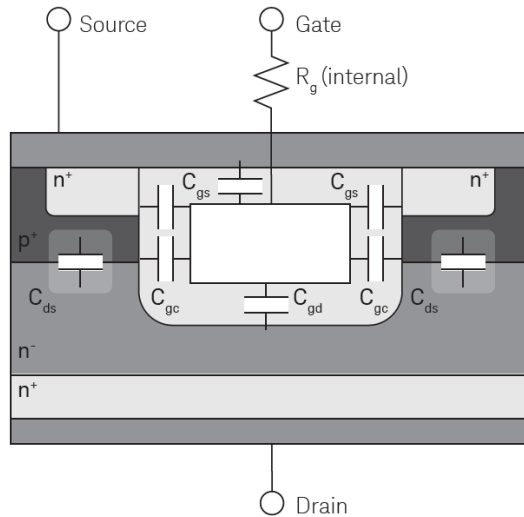
A plot of gate to source (Cgs) capacitance (Cp-G) versus frequency using a high-voltage Bias-T after performing open/short capacitance compensation. Note that the measured conductance becomes negative as the frequency increases beyond 100 kHz.

	100 kHz		1 MHz	
	Cp	G	Cp	G
<b>Open</b>	Small error (1%)	OK	Large error	Large error
<b>Open/Short</b>	OK	OK	OK	Large error
<b>Open/Short/Load</b>	OK	OK	OK	OK

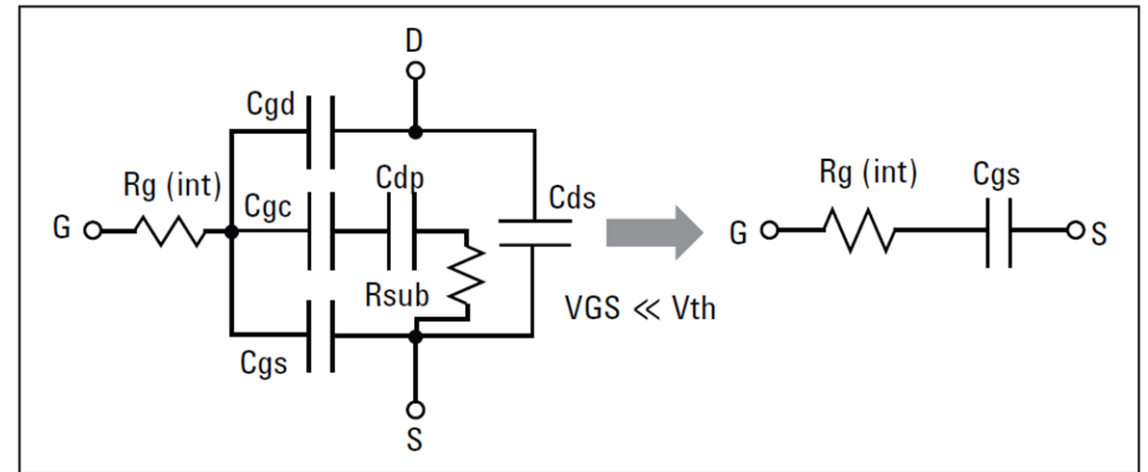
To measure at frequencies above 100 kHz you need to perform a load calibration, which is not always practical or possible.

# Measuring Gate Resistance

It is best to use an LCR meter to measure gate resistance

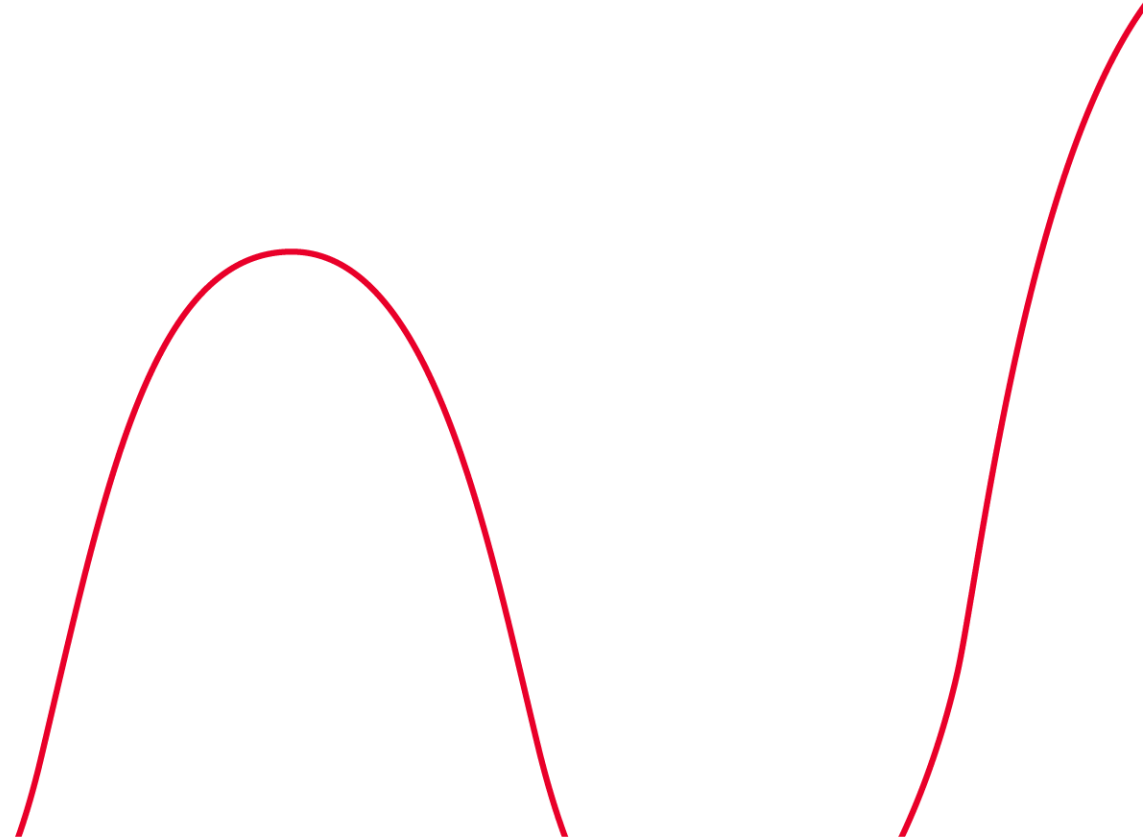


To determine  $R_g$ , we use the  $C_s$ - $R_s$  model built-in to the LCR meter.



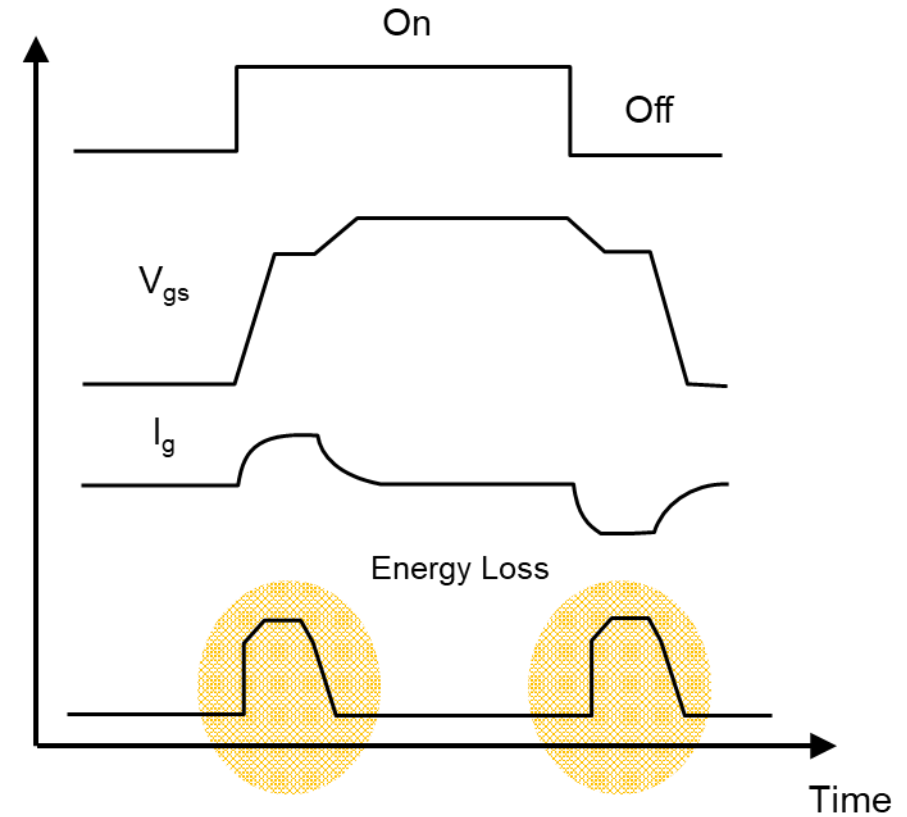
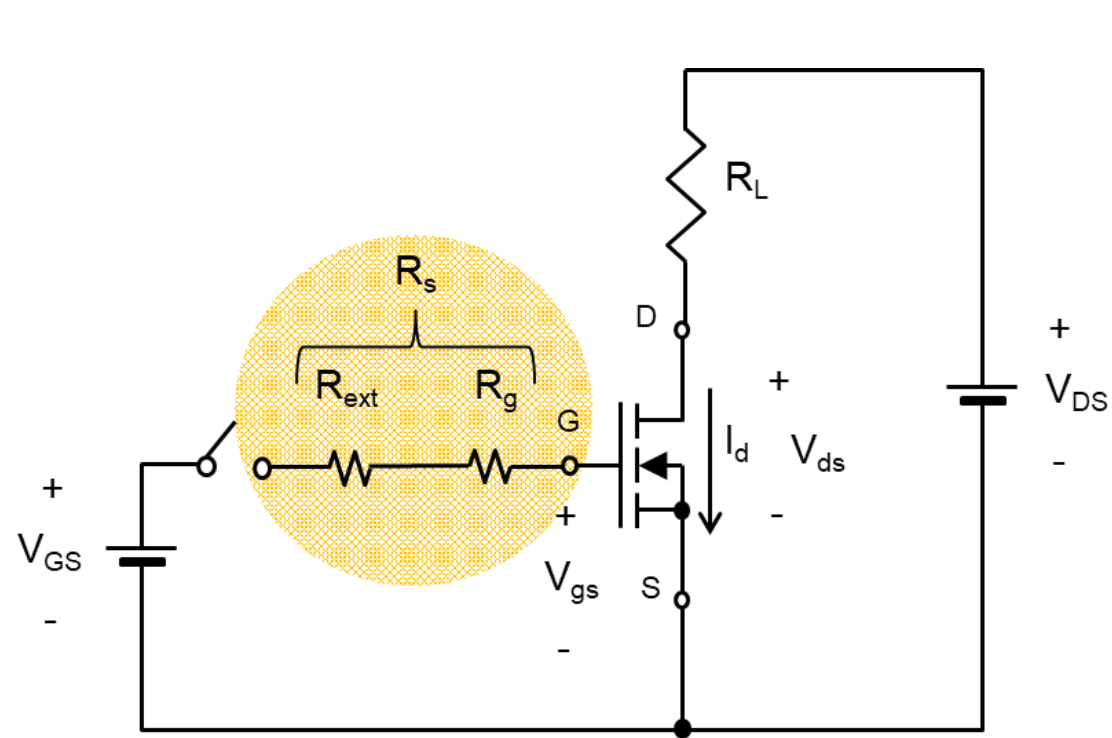
When the transistor is off, the gate-to-source capacitance is the dominant factor in the series capacitance.

# Characterizing Gate Charge in Semiconductor Devices



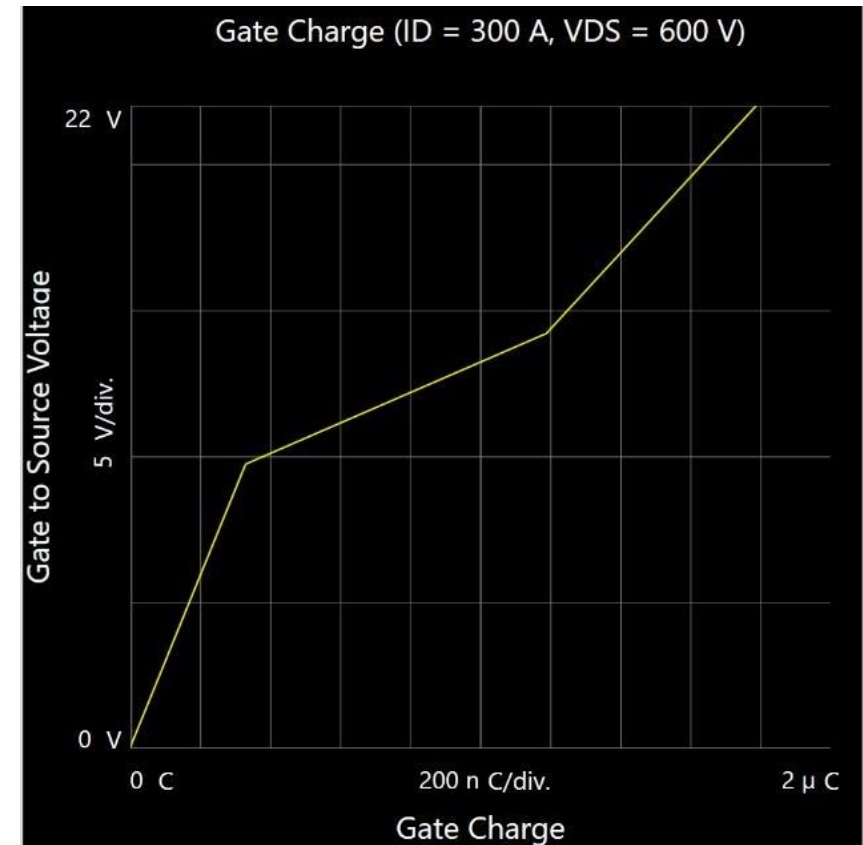
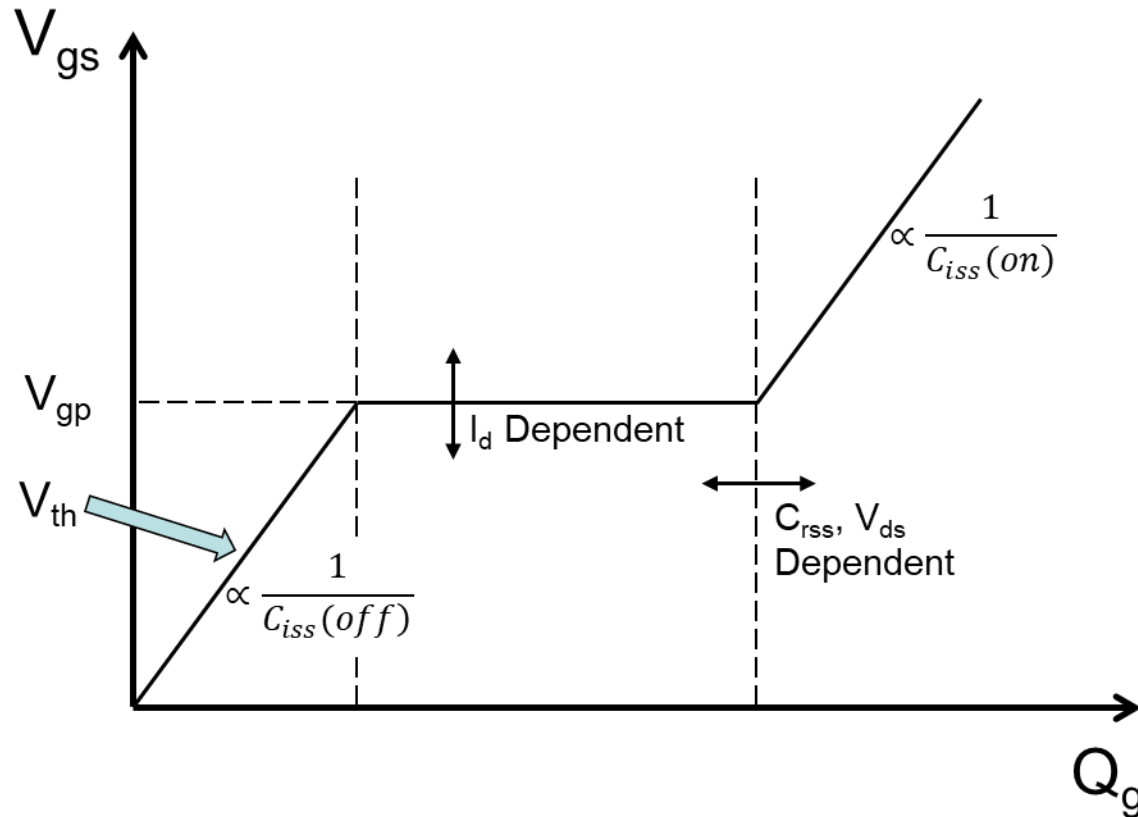
# Driving Loss in a Power Device

Becomes more pronounced at high switching frequencies



# What is Gate Charge?

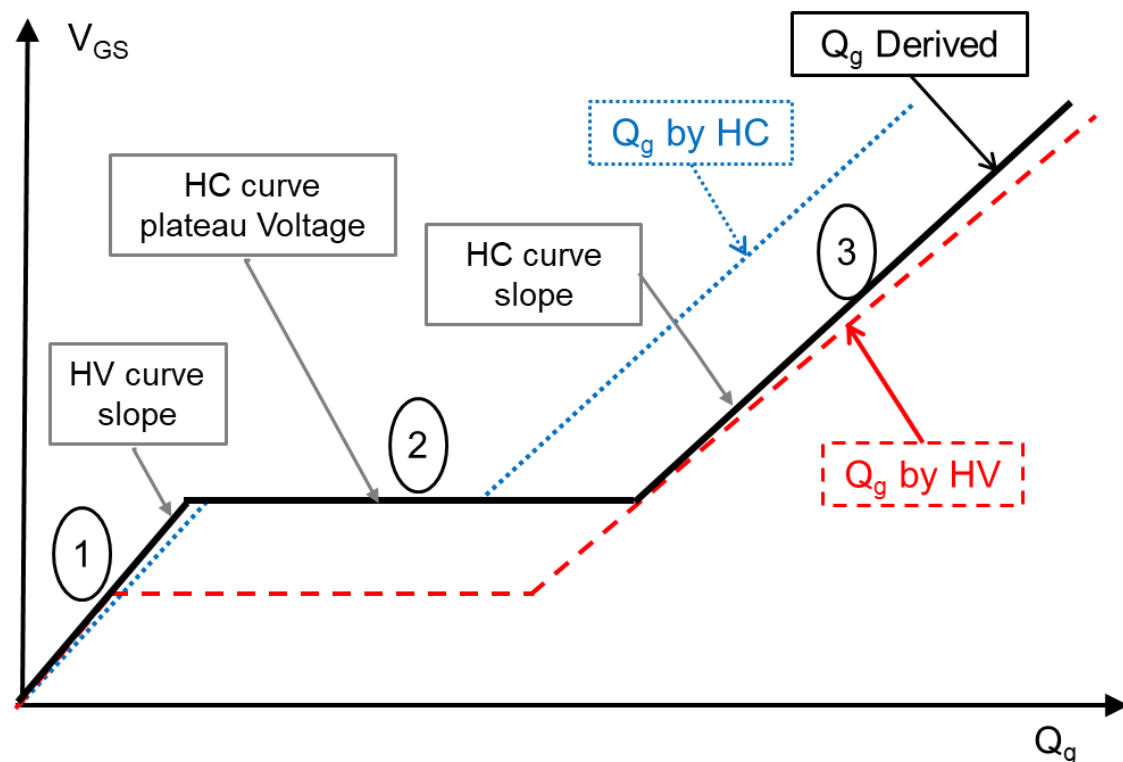
Charge needed to turn transistor on/off



Typical WBG device gate charge characteristic

# Challenge: Measure Gate Charge at High V and I

Solution: Two pass gate charge method

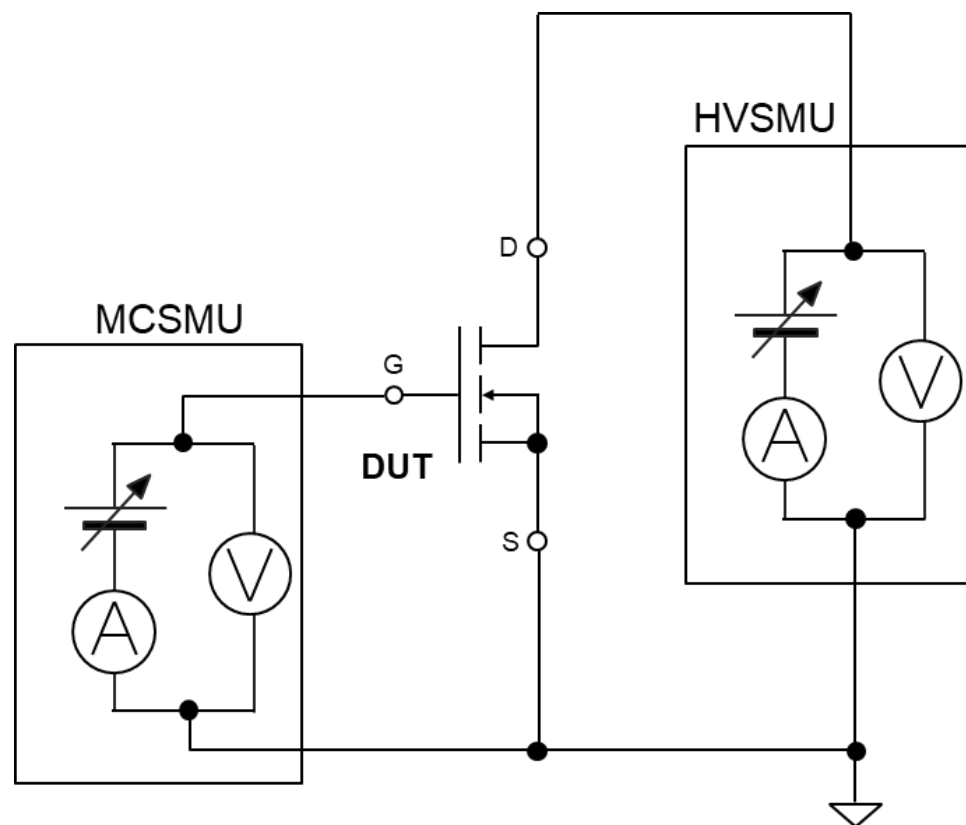


- Gate charge is measured twice: once at high voltage and once at high current
- Curves are combined to create the complete gate charge curve
- Can make gate charge measurements up to 3 kV and over 1,000 A

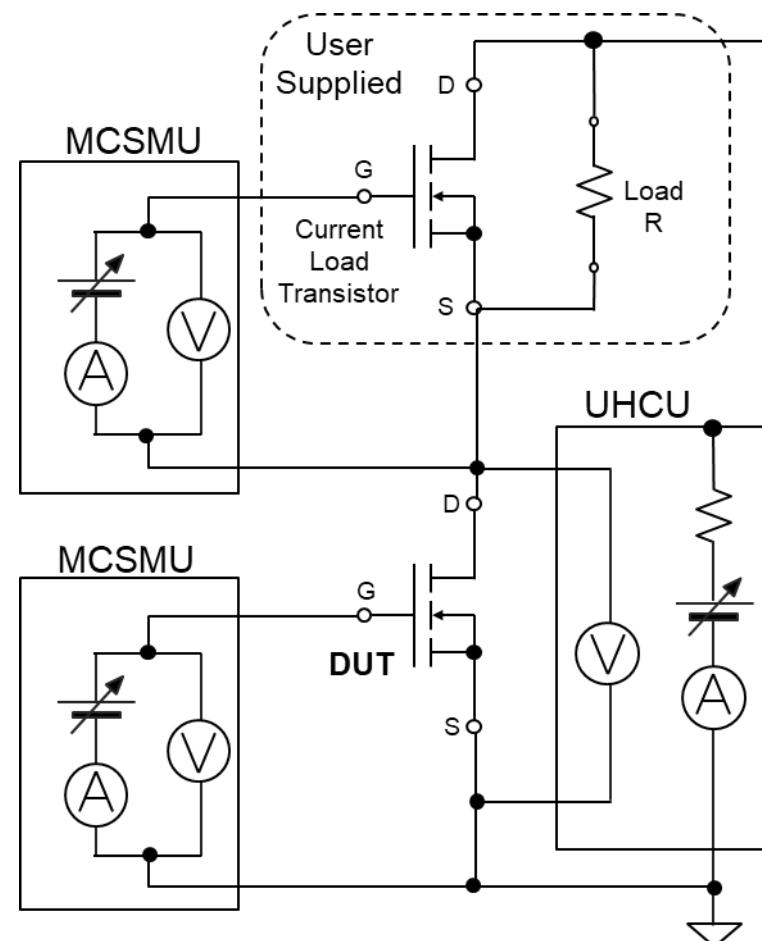
1. The values of  $C_{gs}(off)$  and  $C_{iss}(off)$  are almost the same at high-current and high-voltage.
2. The value of  $V_{ds}(on)$  is virtually the same for high-current and high-voltage operation.

# How is the Two-Pass Gate Charge Measurement Done?

Two pass gate charge method implementation



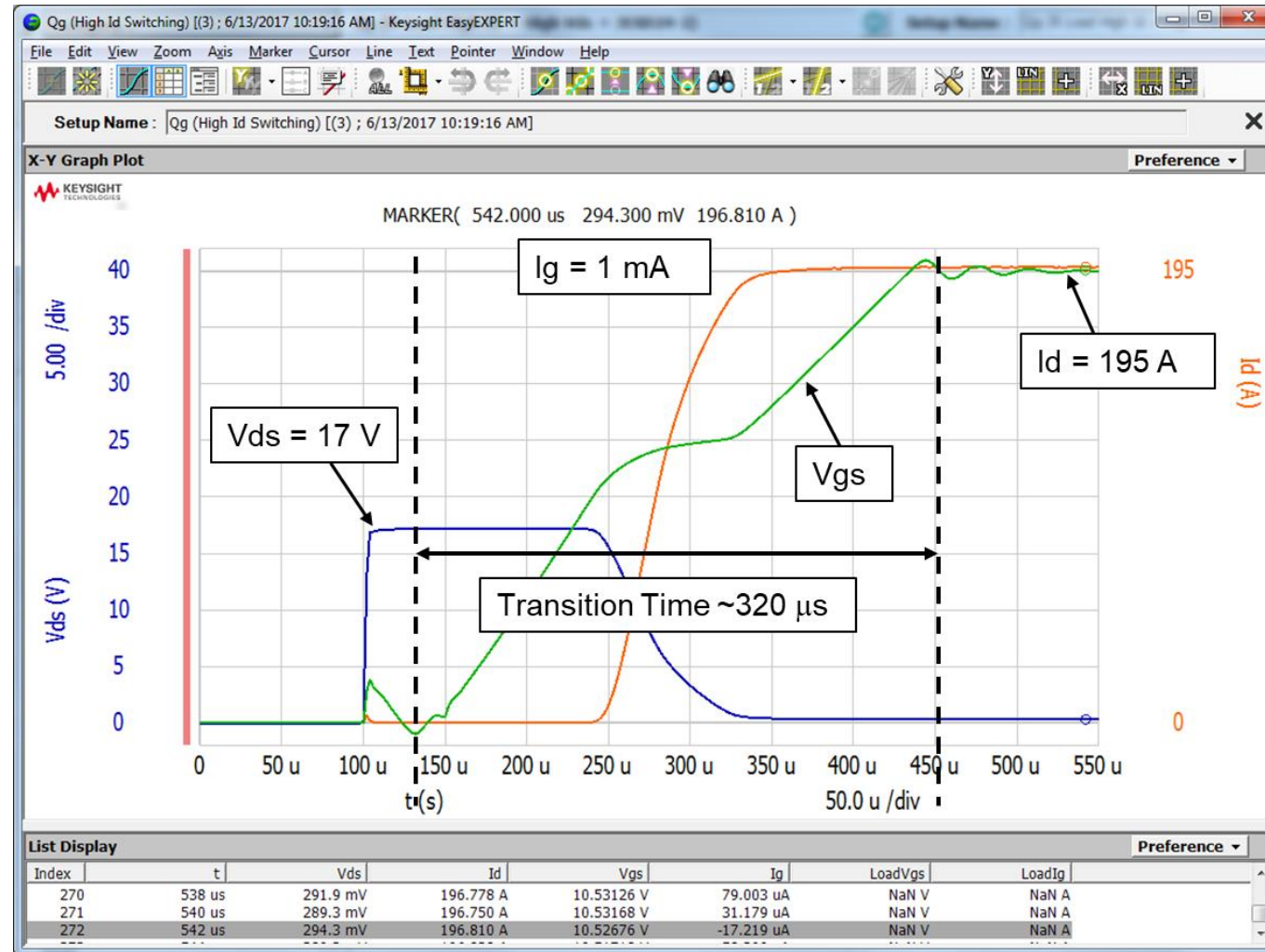
High-voltage (HV) gate charge measurement connection scheme



High-current (HC) gate charge measurement connection scheme showing both supported load options.

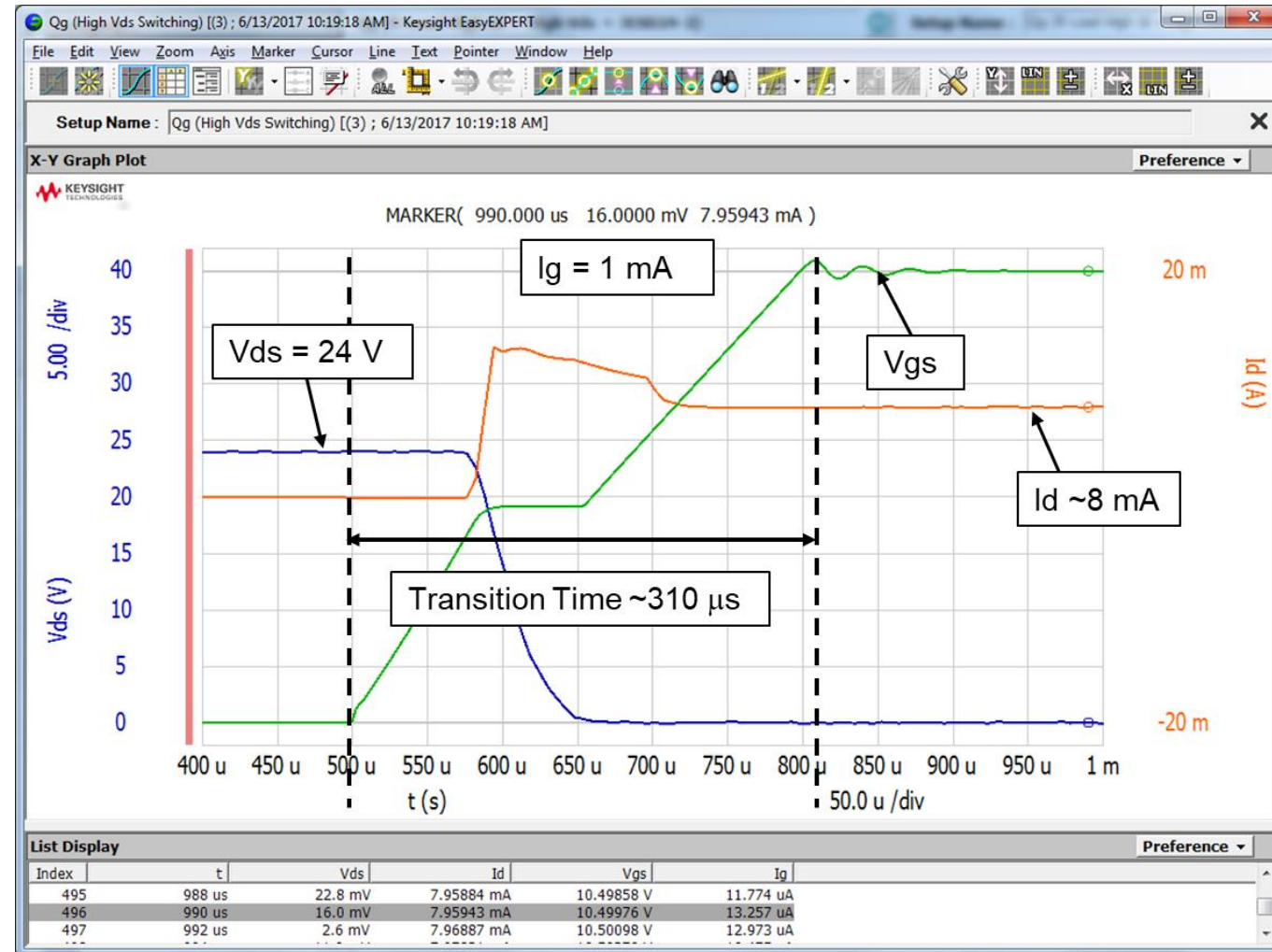
# High-Current Switching Waveforms

It is important to verify the switching waveforms when making gate charge measurements



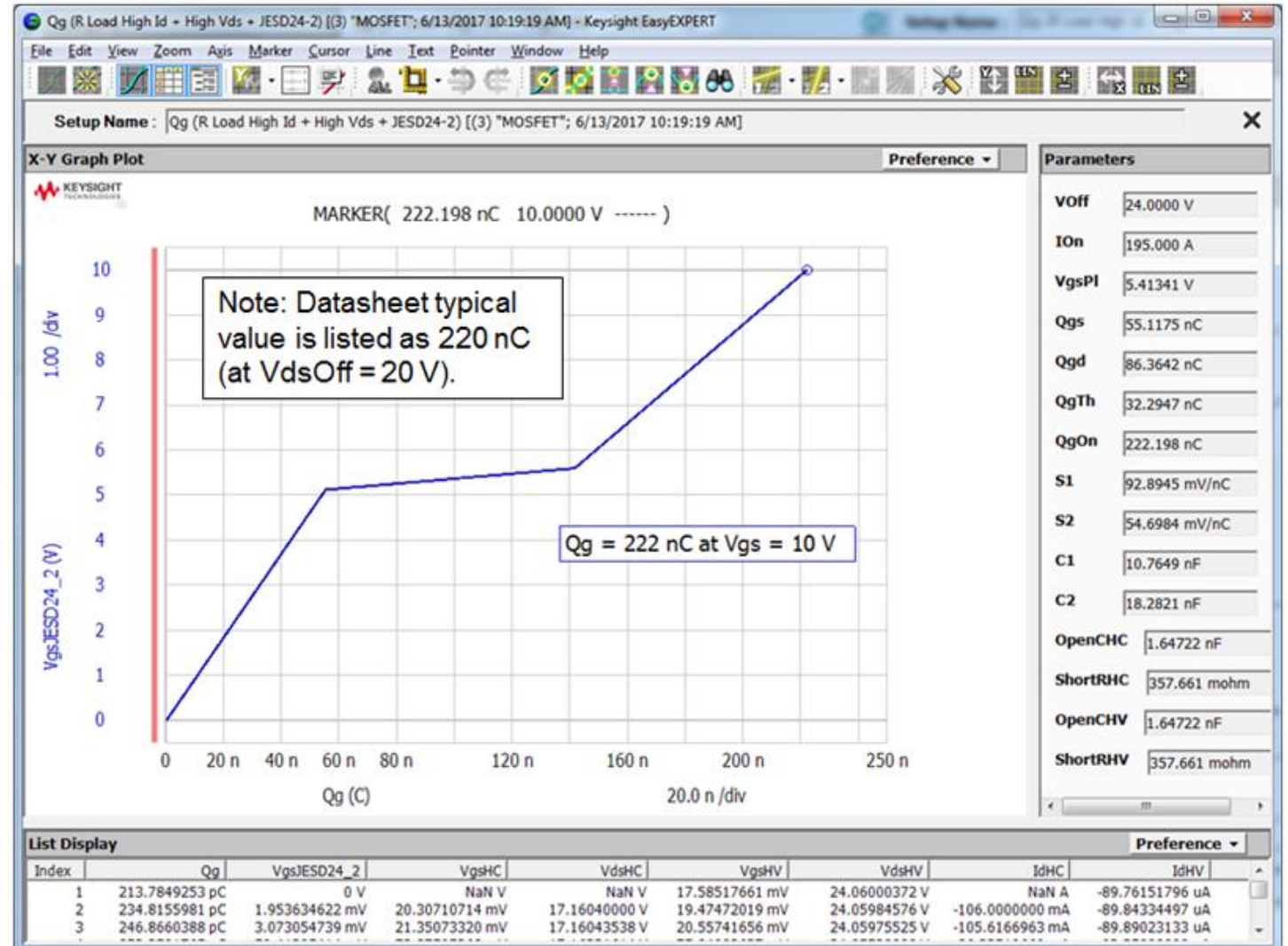
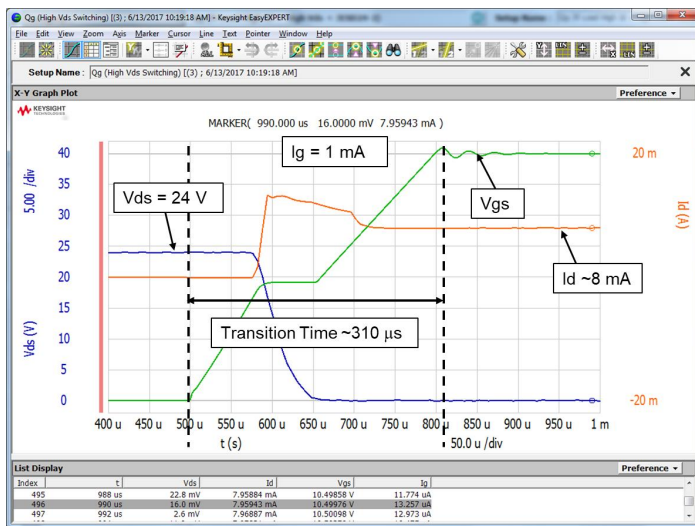
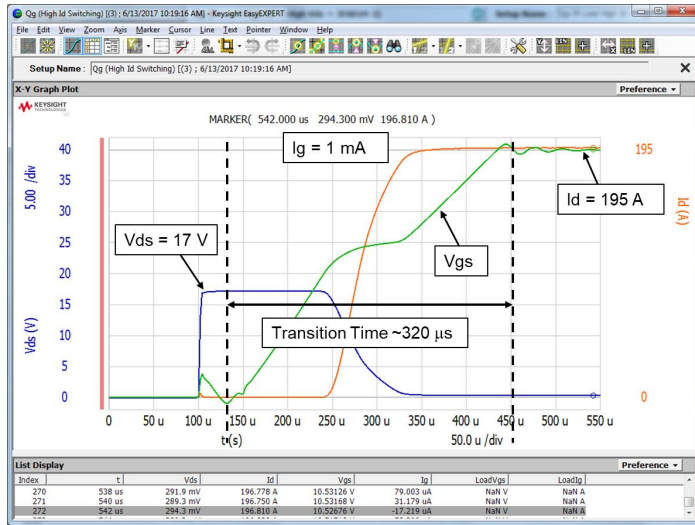
# High-Voltage Switching Waveforms

This device has a drain to source breakdown of around 44 V, so 24 V is “high voltage” for it



# Excellent Agreement with Datasheet Parameters

## Power MOSFET Example

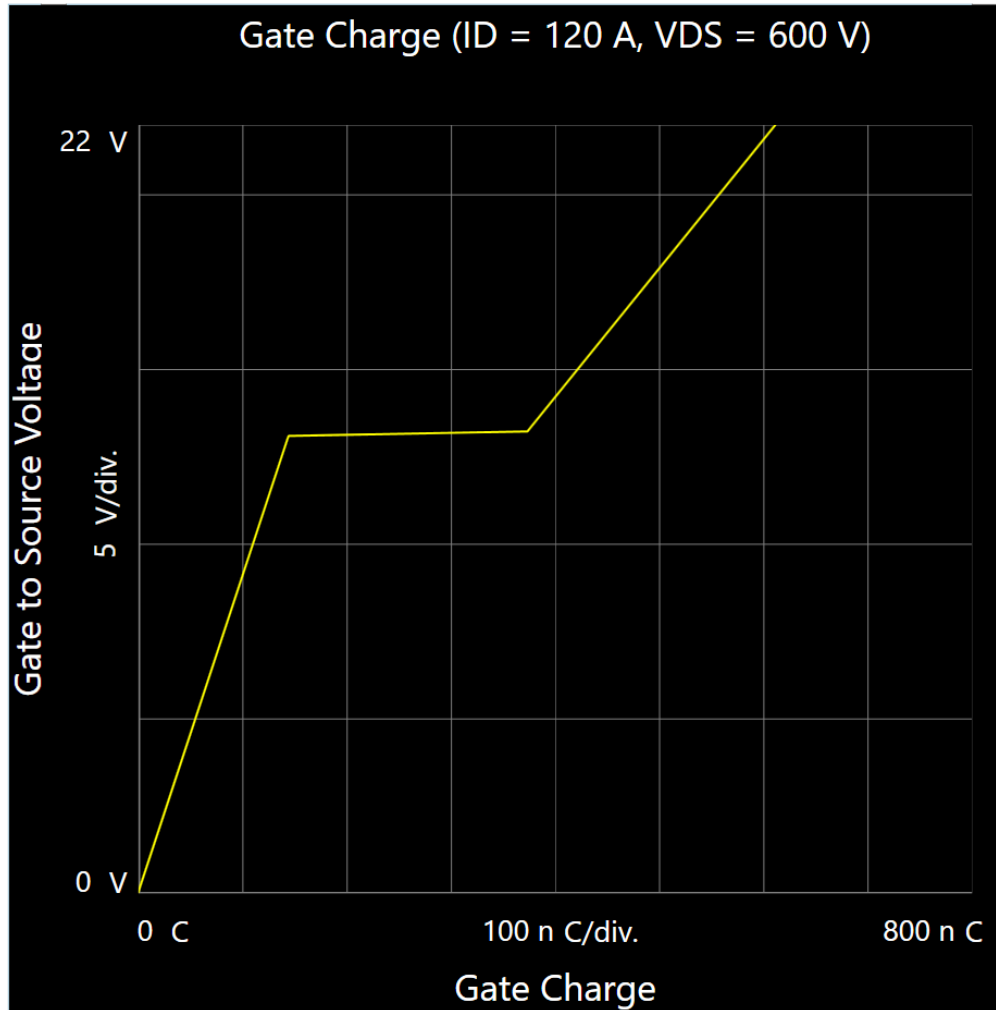


## Key Considerations When Testing WBG Devices for Inverters

- While the basic IV tests are the same as for silicon devices, WBG devices typically require testing at higher voltage and currents
- When measuring junction capacitances using a bias-T, you need to pay careful consideration to the connections. You also need to use external resistors and capacitors
- The two-pass method for measuring gate charge works well for Si and SiC devices but can show oscillation issues with GaN devices. For GaN devices the double-pulse method works better.

# SiC Module Gate Charge Measurement Example

Here is an example of both high current and high voltage

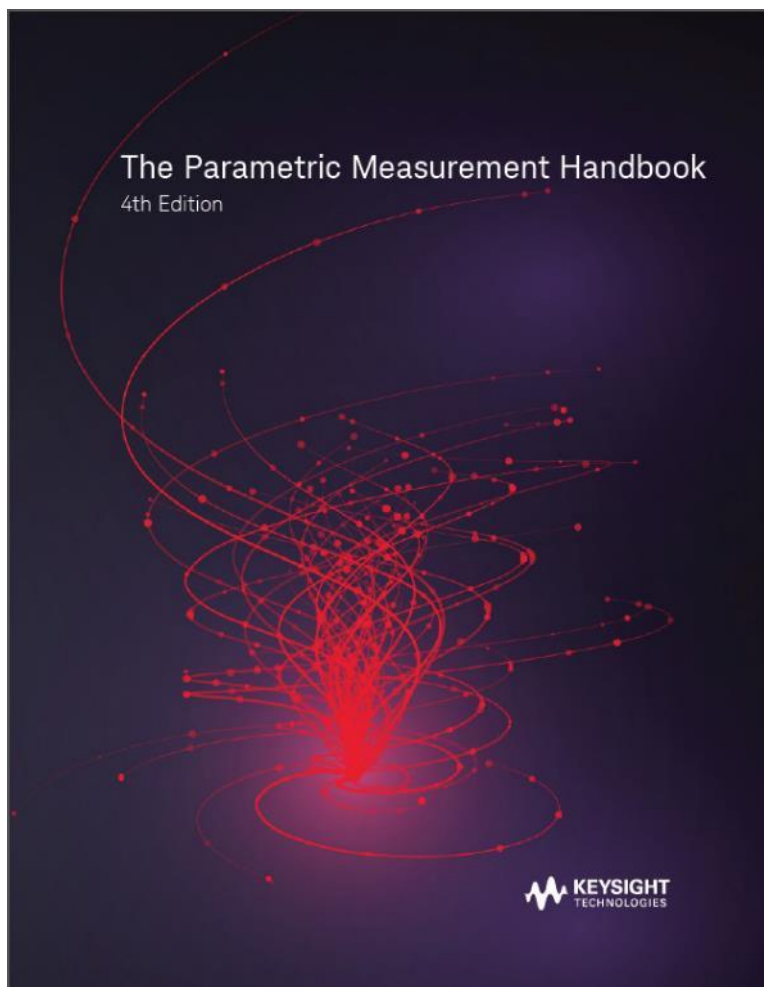


$I_D = 120\text{ Amps}$

$V_{ds} = 600\text{ V}$

# Want More Power Device Measurement Information?

Download our Parametric Measurement Handbook

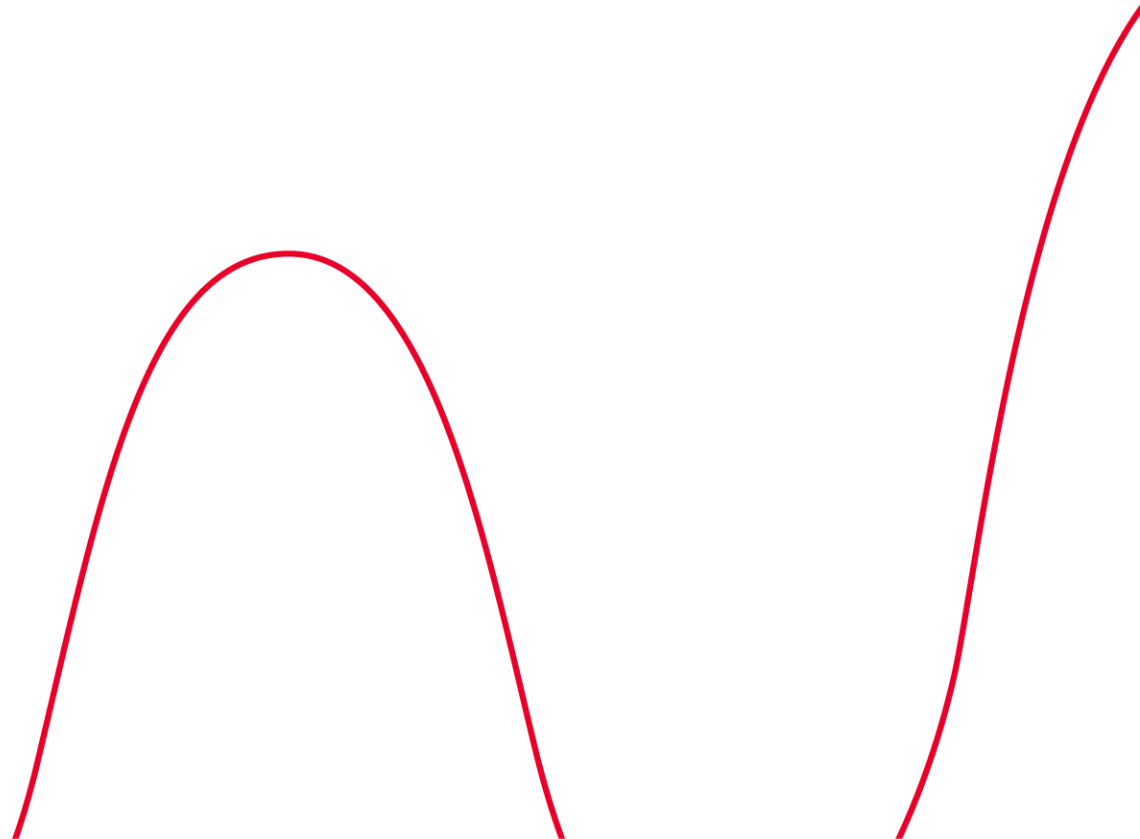


- Now in its 4<sup>th</sup> edition
- Over 276 pages of information on parametric test
- A new chapter (Ch 9) devoted to power device test issues

[www.keysight.com/find/parametrichandbook](http://www.keysight.com/find/parametrichandbook)

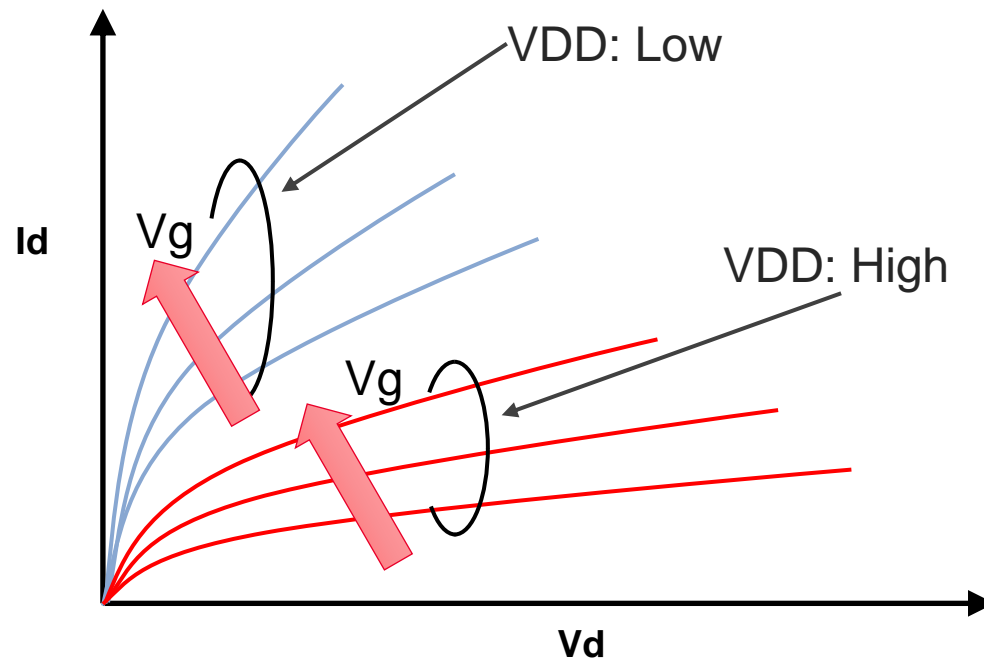
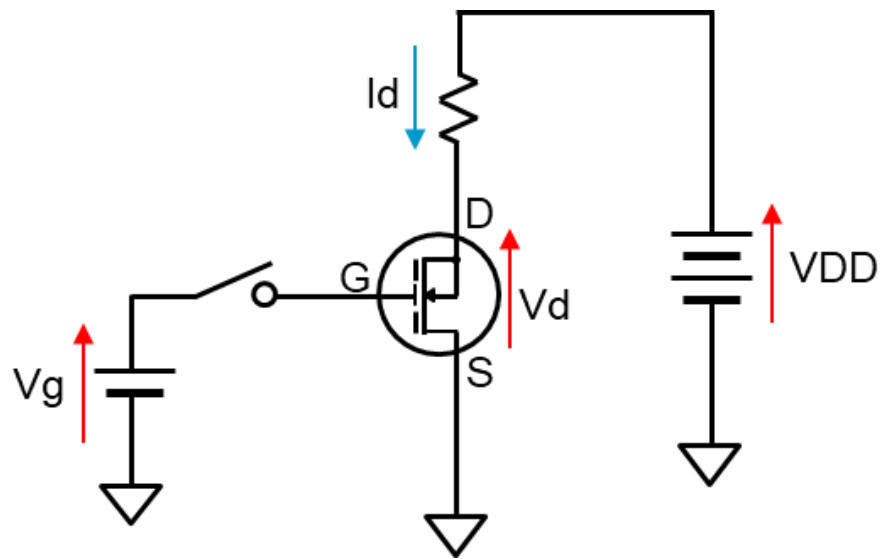
# Thank you

# What is GaN Current Collapse?



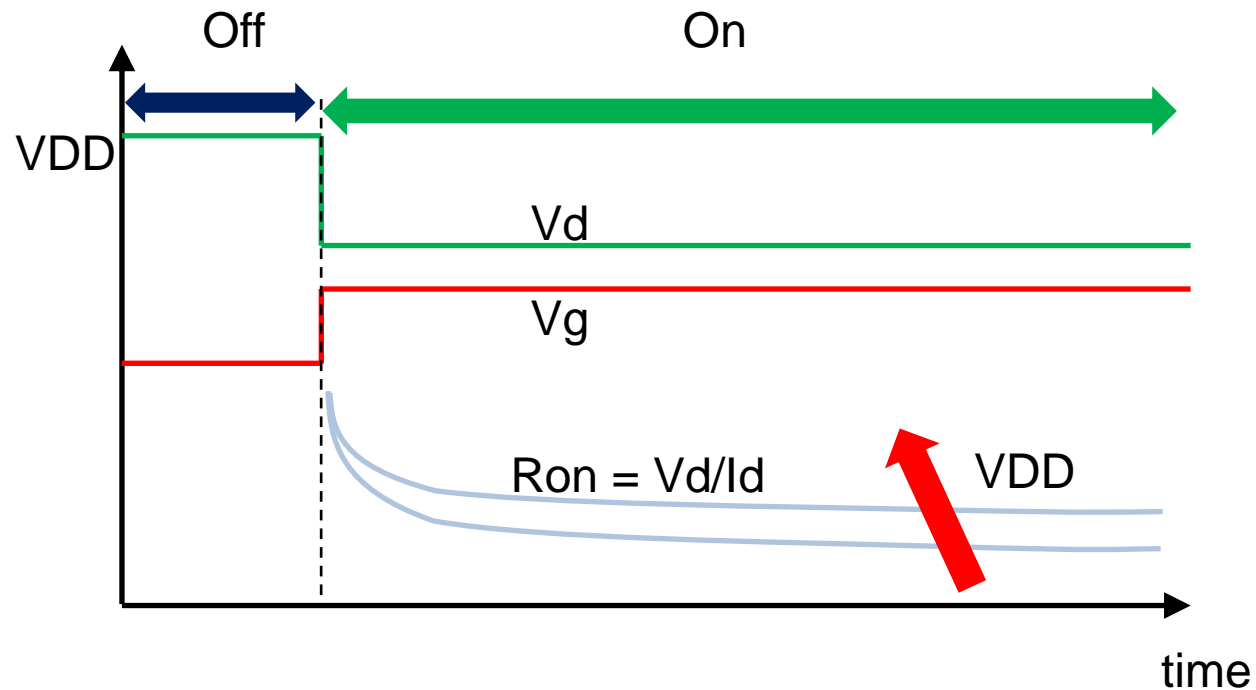
# What is Current Collapse (on GaN Transistors)?

The drain current at higher VDD is less than at lower VDD?



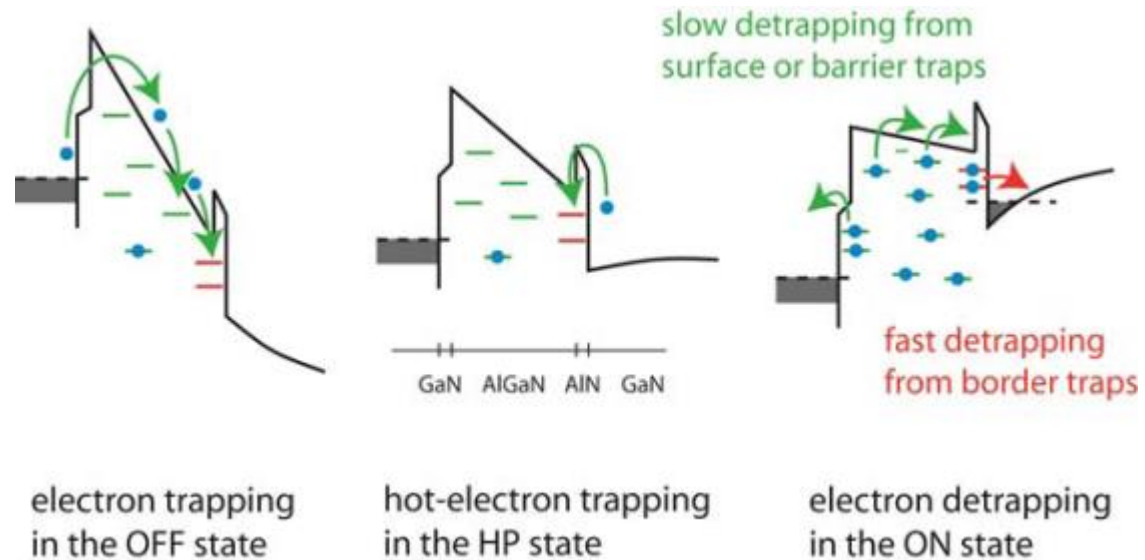
# What is Dynamic ON Resistance (on GaN Transistors)?

This phenomena is caused by the same mechanism as the current collapse behavior



- The On-resistance changes dynamically after changing from OFF-state to ON-state.
- The On-resistance depends on both the applied  $V_{DD}$  and the duration of the OFF-state

# Physics of Current Collapse



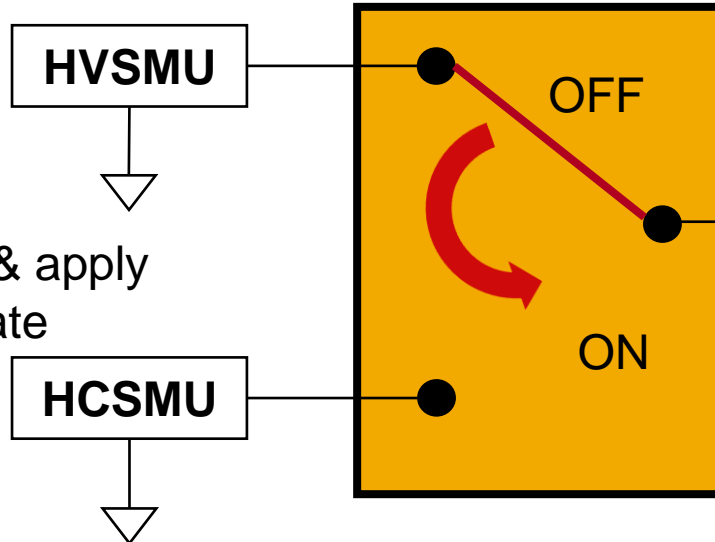
Donghyun Jin, et. al. "Mechanisms responsible for dynamic ON-resistance in GaN high-voltage HEMTs", Proc the 2012 24th ISPSD, pp 333-336

- Numerous traps with various time constant exist
- Fast response and slow response must be measured
- Various technique to reduce current collapse are ongoing

# How to Measure Current Collapse?

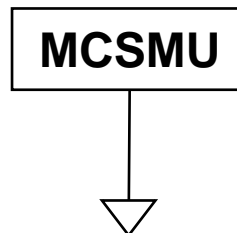
Need to coordinate switching between high-voltage and high-current with device turn on

Apply high-voltage bias in the  
OFF-state



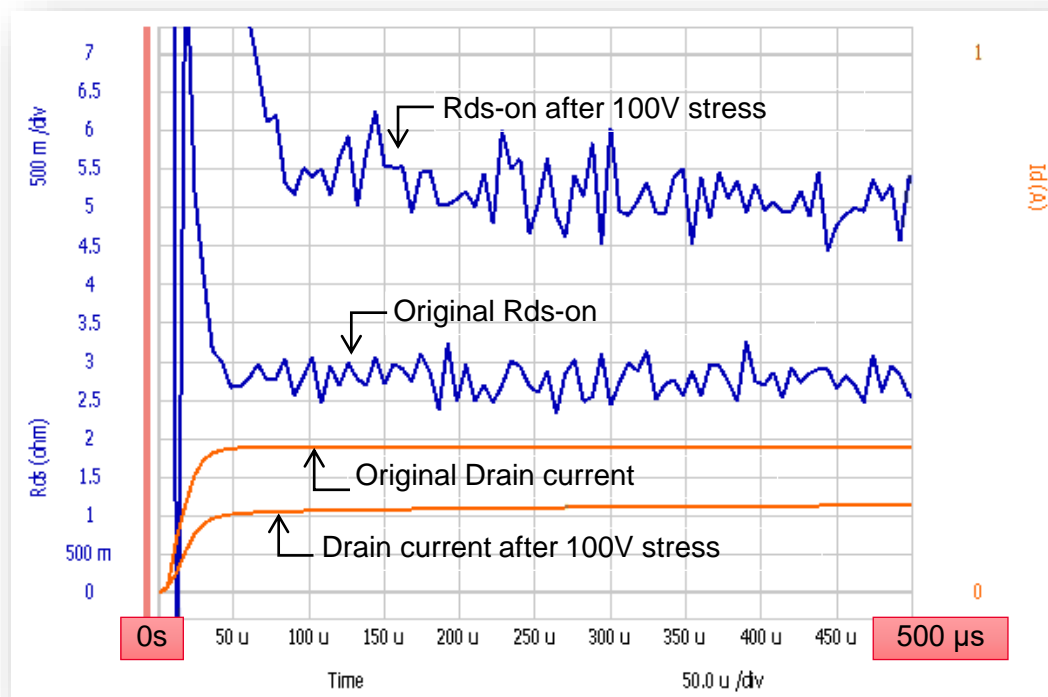
Measure on-current & apply  
voltage in the ON-state

Gate control synchronized  
with switching

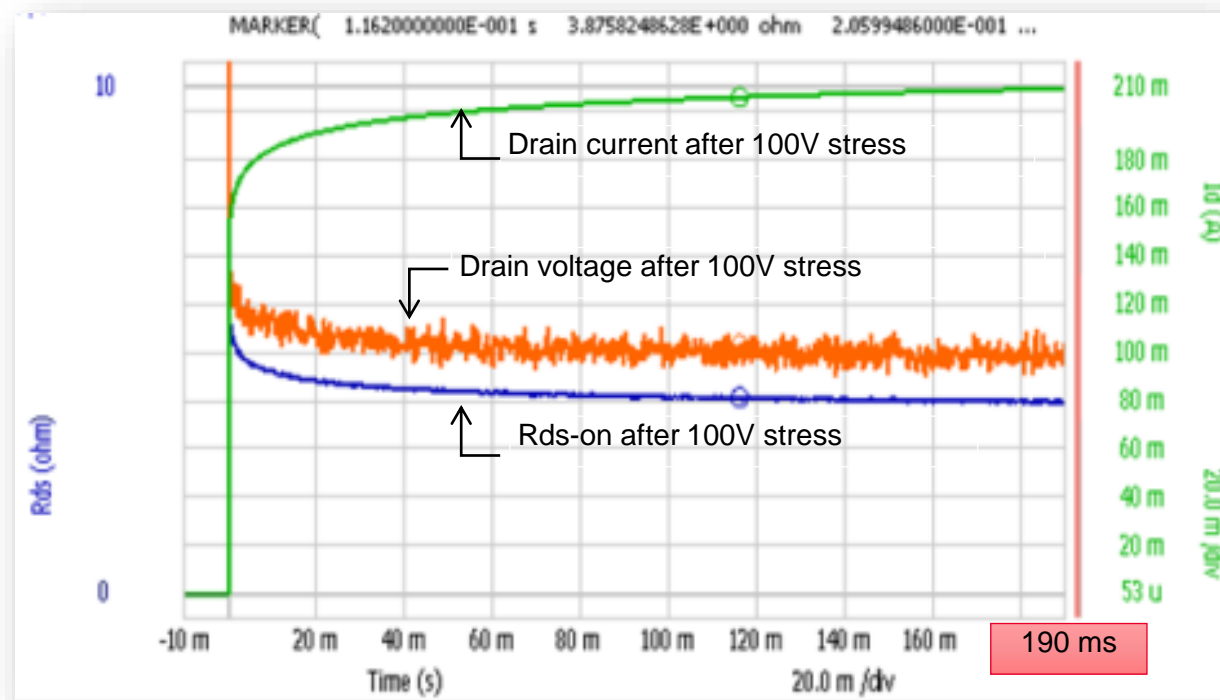


# Dynamic ON Resistance Measurement Examples

Note that behavior changes depending on the length of the stress time



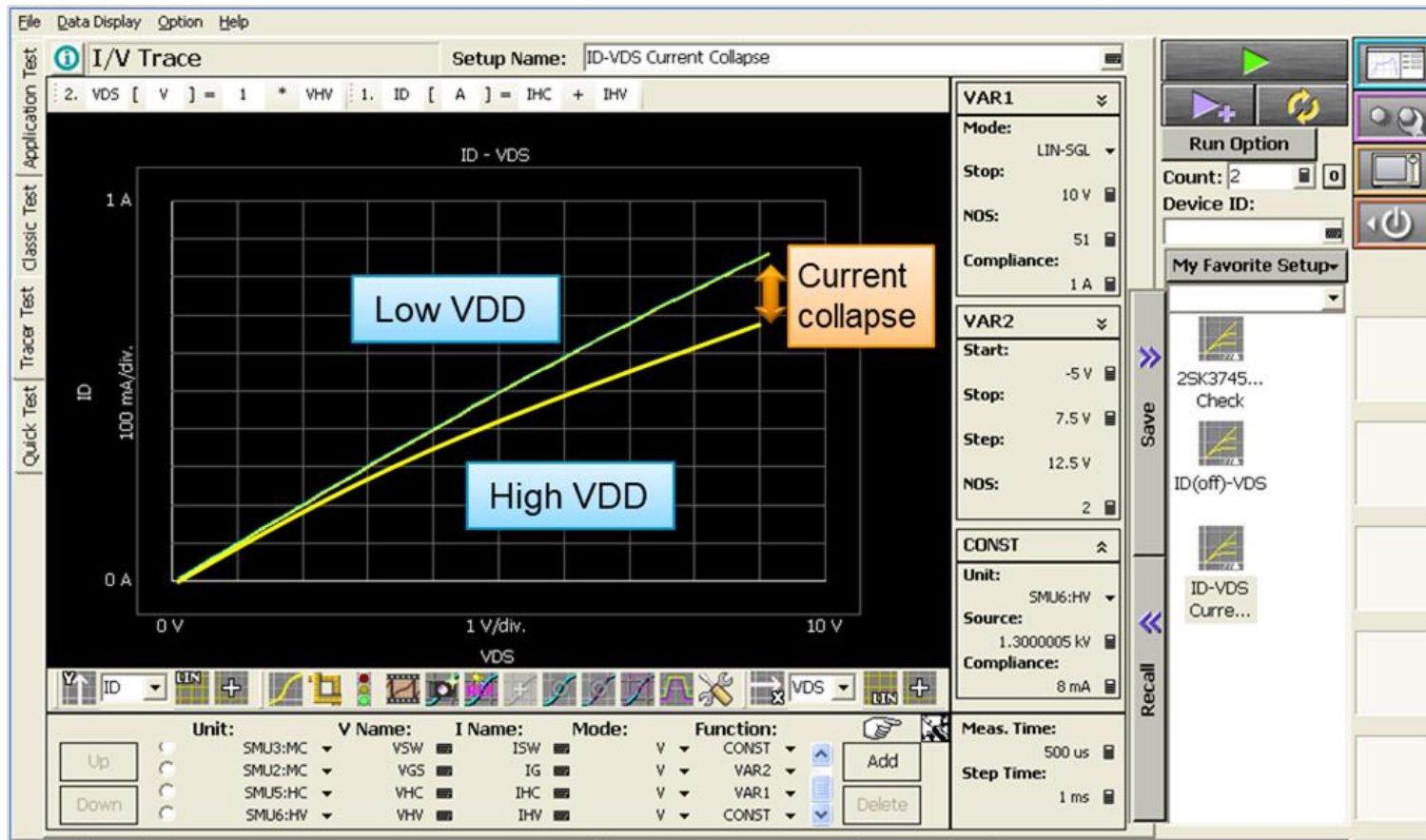
Short Term (<1 ms)



Long Term (>1 ms)

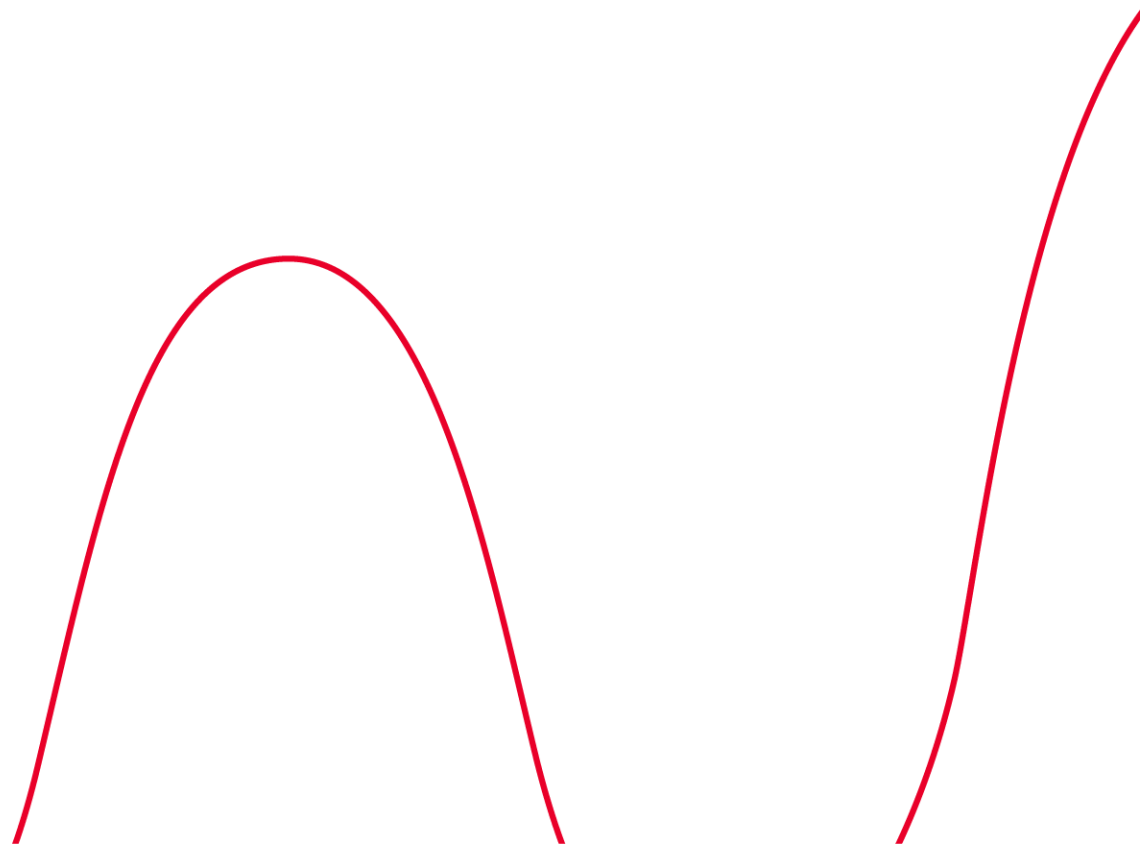
# Example of a current collapse measurement

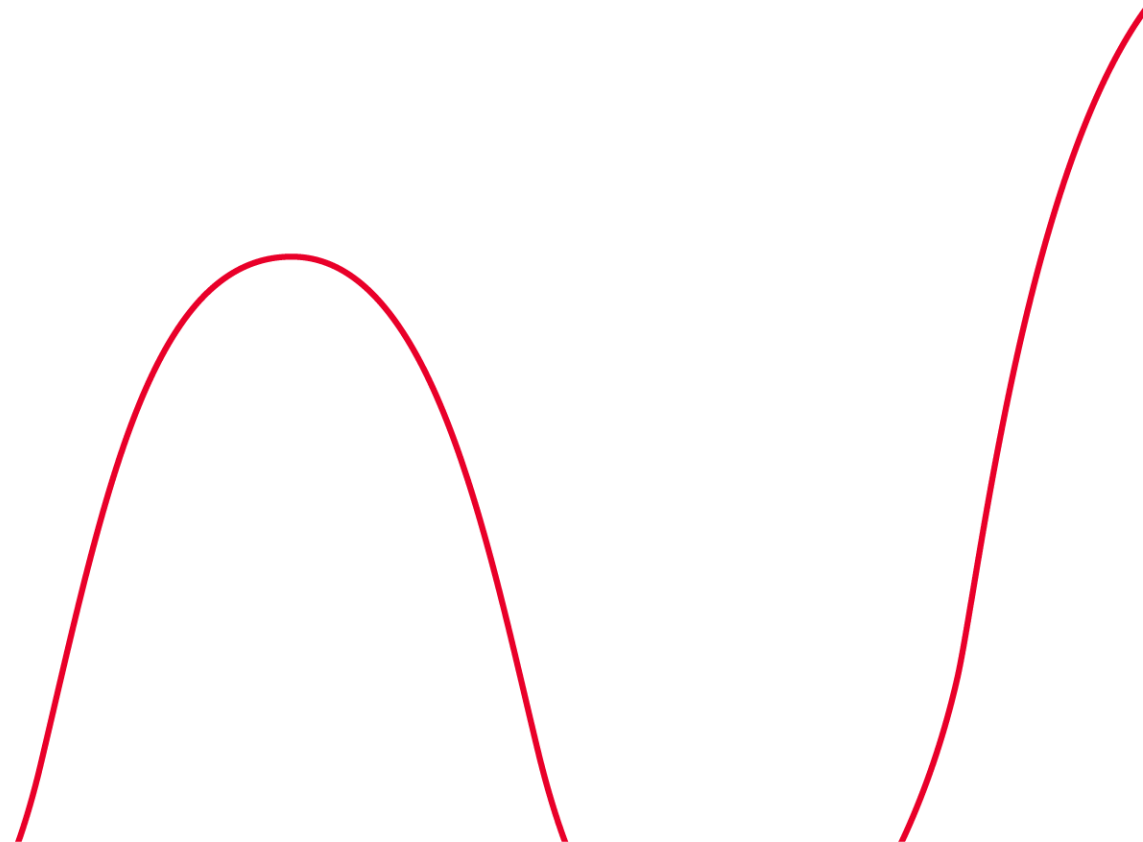
Using a curve tracer emulation mode



In this example, it is easy to see the difference between applying a low VDD and a high VDD when the device is in its off state.

# Summary





# Please Come by Our Booth to Learn More About Keysight

We have many solutions for testing high-power, WBG devices



**B1505A Power Device Analyzer/Curve Tracer**



**B1506A Power Device Analyzer for Circuit Design**



**PD1500A Double-Pulse Test Solution**