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Power Supply Case Histories

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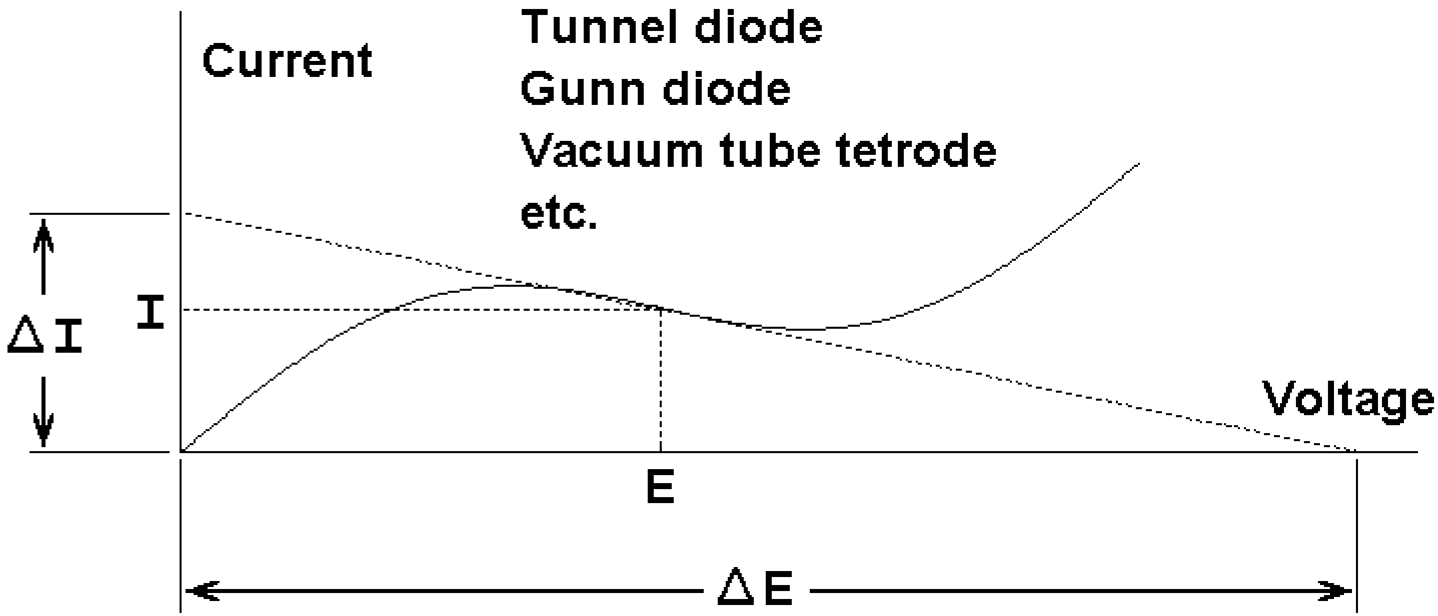
A Negative Resistance Device



Static resistance = $\frac{E}{I}$ Dynamic resistance = $\frac{\Delta E}{\Delta I}$

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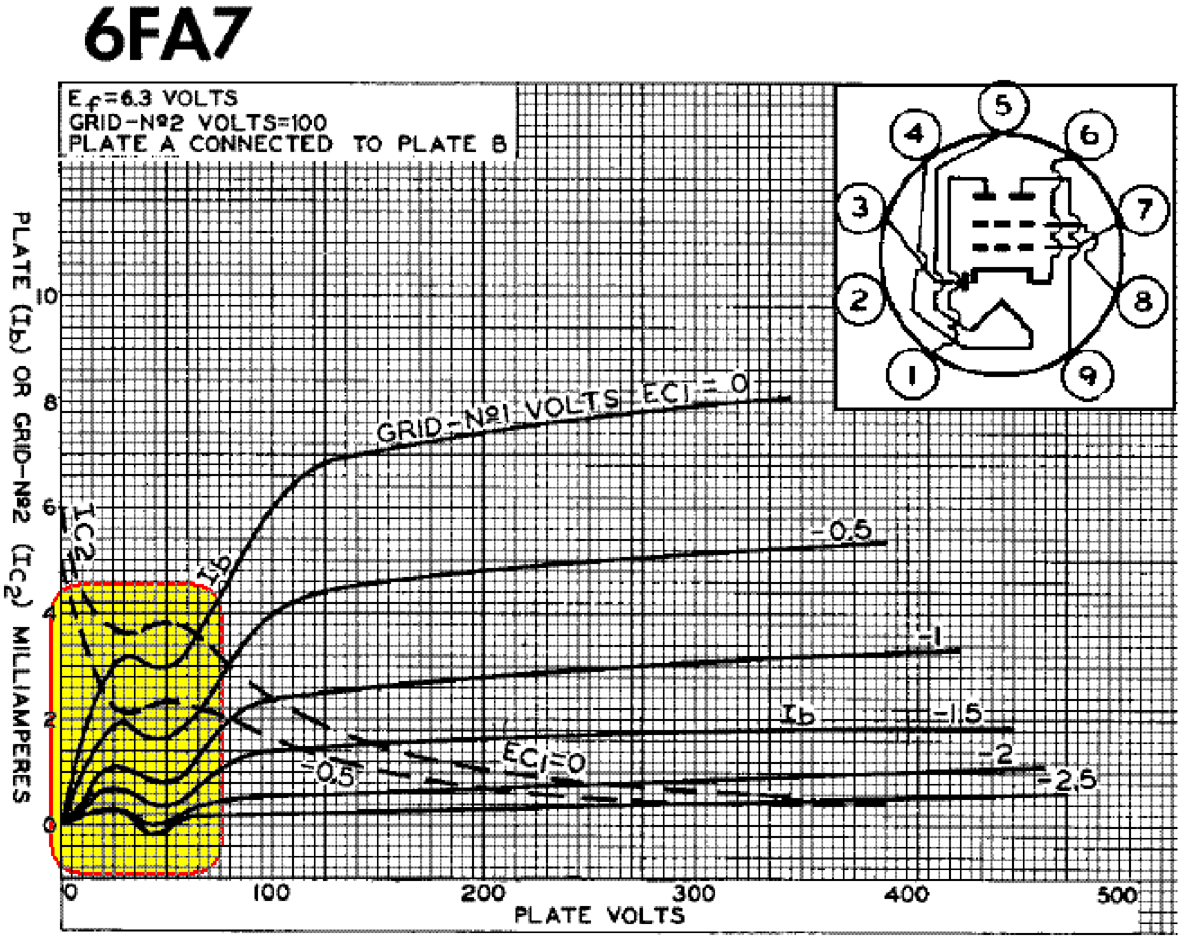
Negative resistance where???



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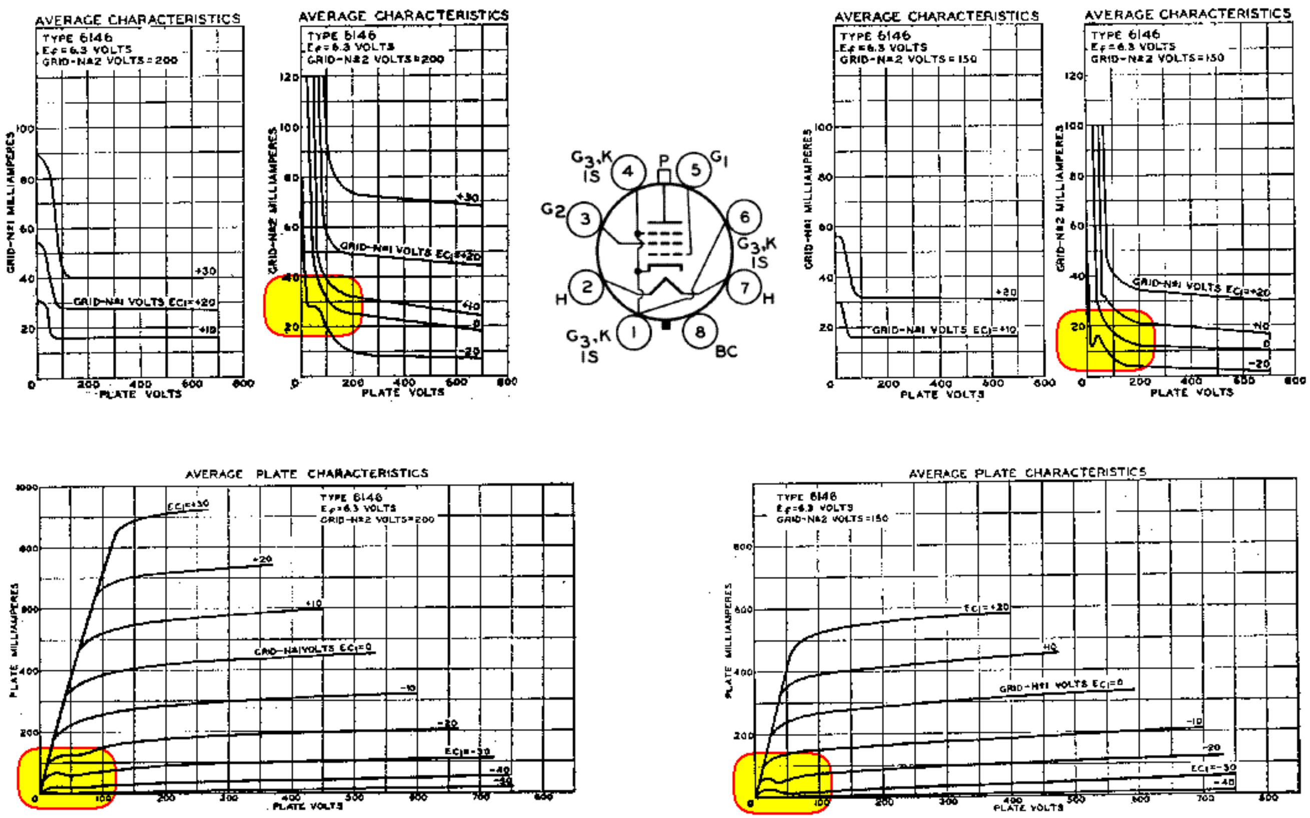
Negative resistance where???



Regions of negative resistance, type 6146 beam power tetrode.

Negative resistance where???

http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=4051846

Proceedings of the IRE ...> Volume: 44 Issue: 1

Negative Resistance Regions in the Collector Characteristics of the Point-Contact Transistor

Miller, L.E.;
Bell Tel. Labs., Inc., Allentown, Pa.

This paper appears in: Proceedings of the IRE
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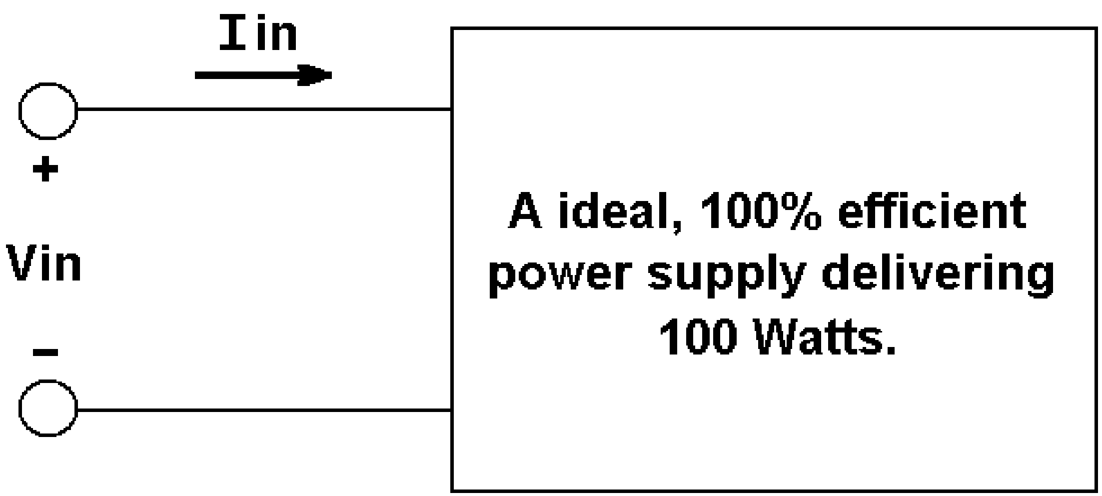
ABSTRACT

The negative resistance regions in the active portion of the point-contact collector characteristics are characterized in terms of three unique types of anomalies in the current multiplication properties of the device. While the interaction of the Â¿ anomalies and the associated circuitry result in a measuring circuit instability, the negative resistances are true device properties which are attributable to variations in the collection efficiency of the reverse biased collector junction.

A change of terminology

Now let the word "resistance" be replaced by the more generalized term "impedance".

A Perfect 100 W Power Supply



Let the power in be 100 Watts as 100 Volts and 1 Ampere.

The static input impedance is the 100 Volts / 1 Ampere or 100 Ohms.

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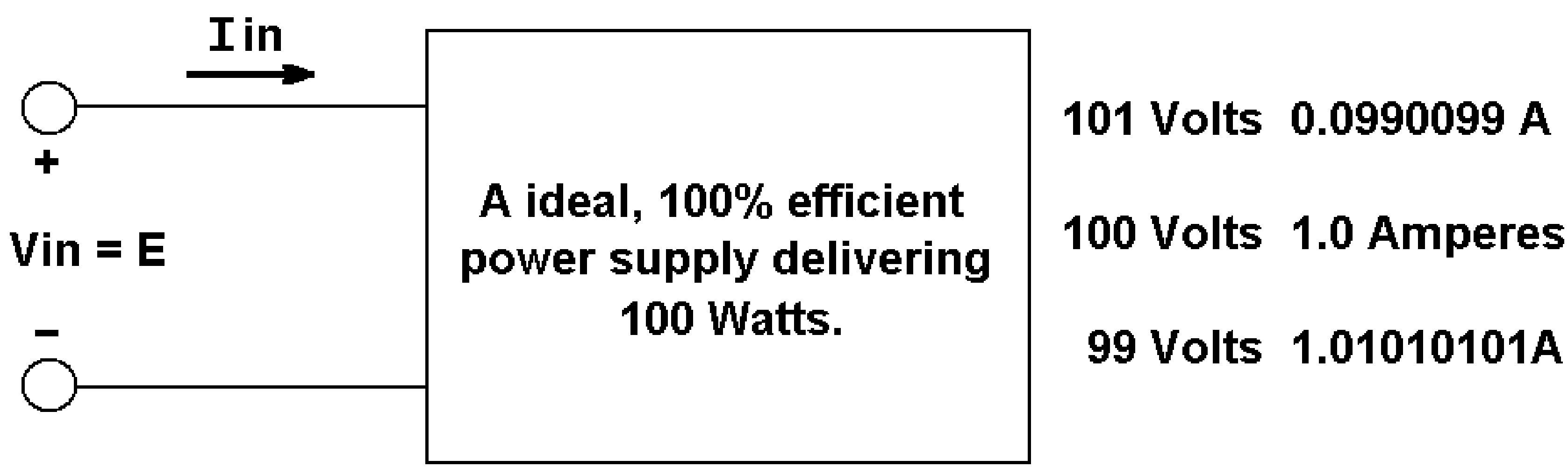
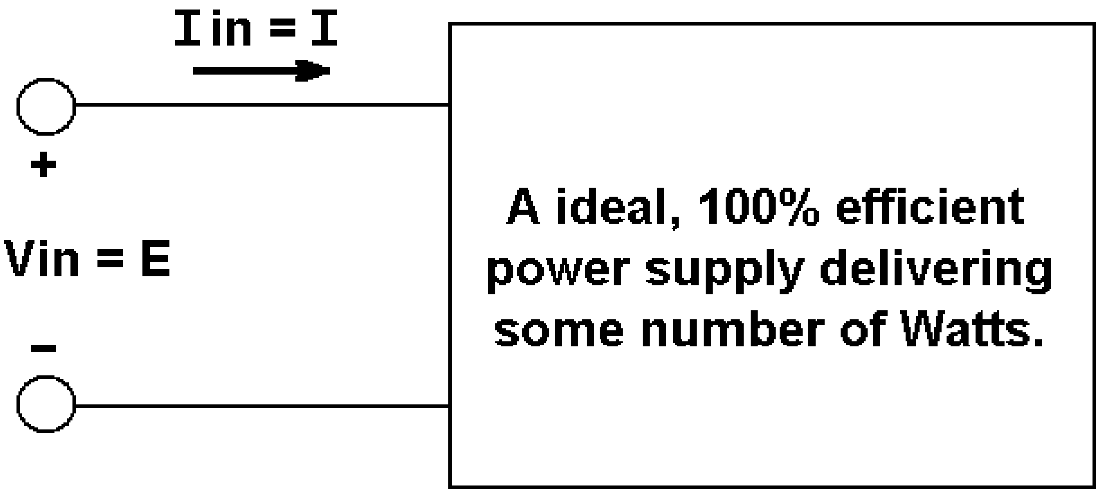
The Same 100 W Power Supply



Any Perfect Power Supply



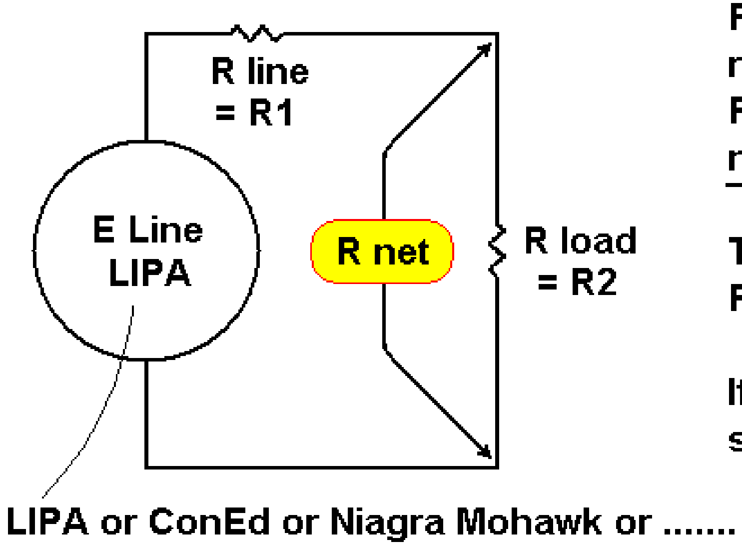
$$P = E * I \;\; ; \;\; E = P / I$$

$$\frac{\partial E}{\partial I} = \frac{I * Zero - P * 1}{I^2}$$

$$\frac{\partial E}{\partial I} = \frac{-E * I}{I^2} = \frac{-E}{I}$$

The dynamic input impedance is the negative of the static input impedance.

High Line Impedance Issue

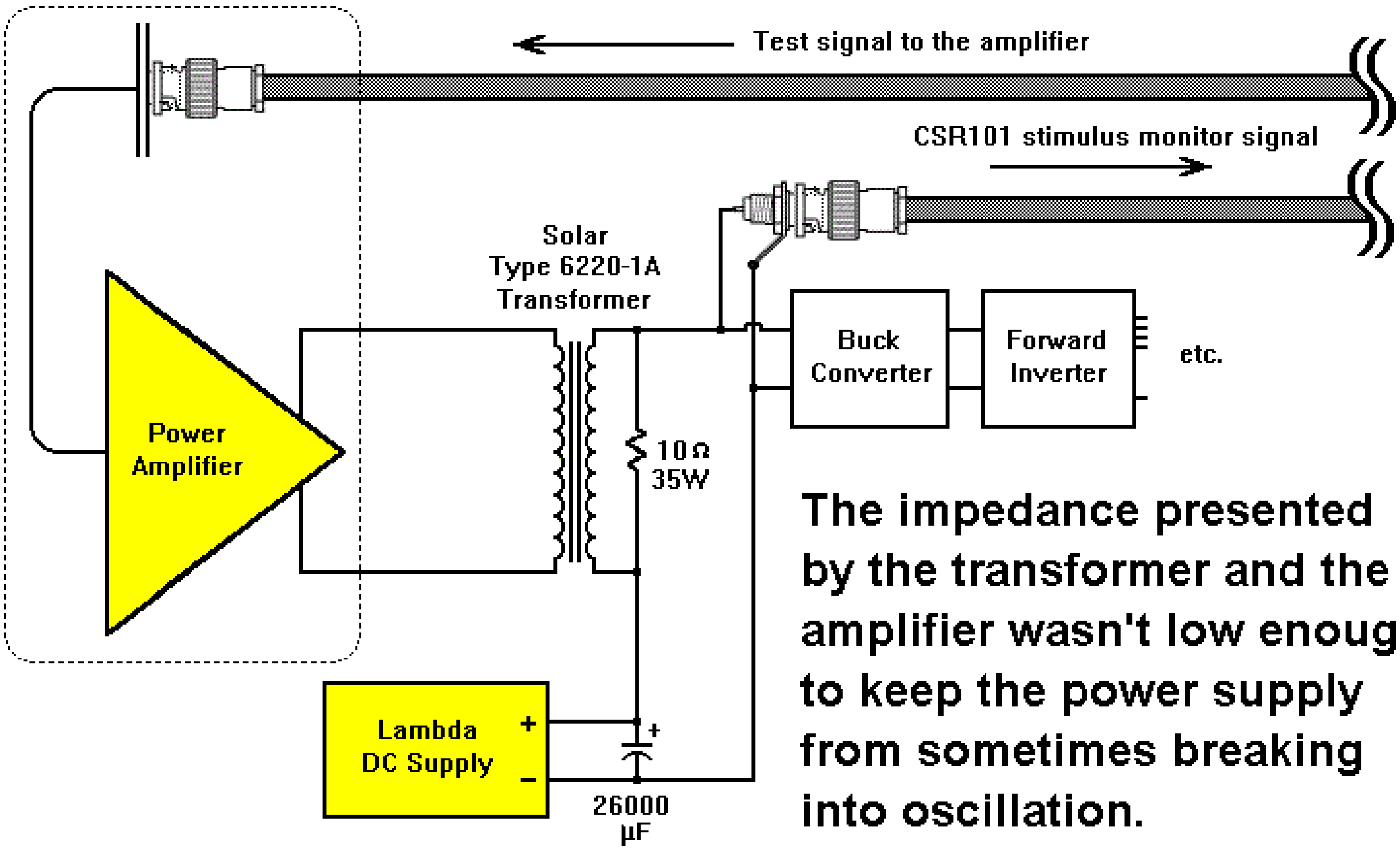


Remembering that these are dynamic impedances re. our 100% efficient, ideal switchmode power supply, R1 is a postive number of Ohms while R2 is a negative number of Ohms.

The net resistance (impedance) of this system is R net = R1 || R2 = R1 x R2 / (R1 + R2).

If R1 > abs (R2), then R net <0 and the combined system becomes a negative resistance oscillator.

A Line Impedance Issue, CS101



The impedance presented by the transformer and the amplifier wasn't low enough to keep the power supply from sometimes breaking into oscillation.

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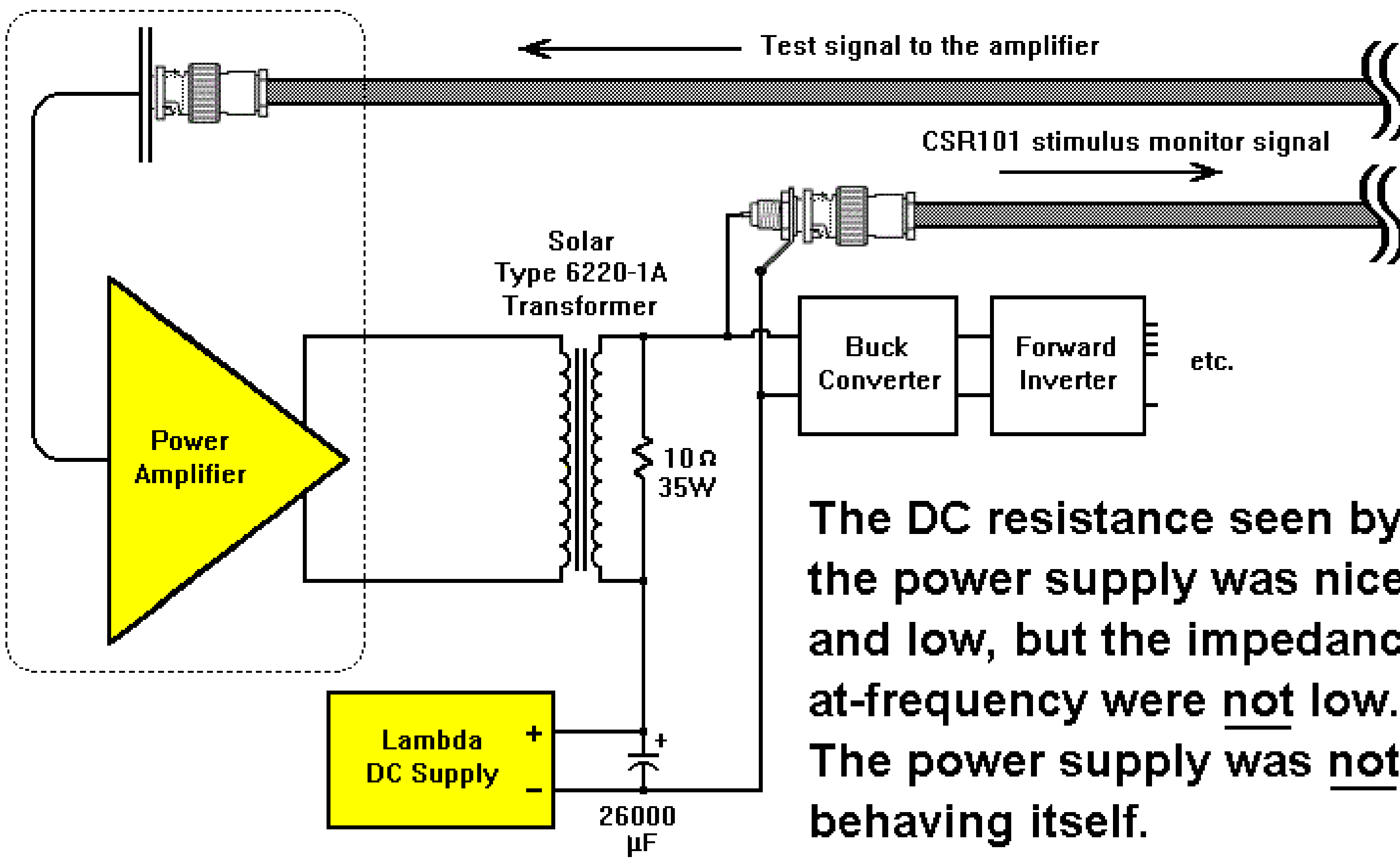
A Line Impedance Issue, CS101



The DC resistance seen by the power supply was nice and low, but the impedances at-frequency were not low. The power supply was not behaving itself.

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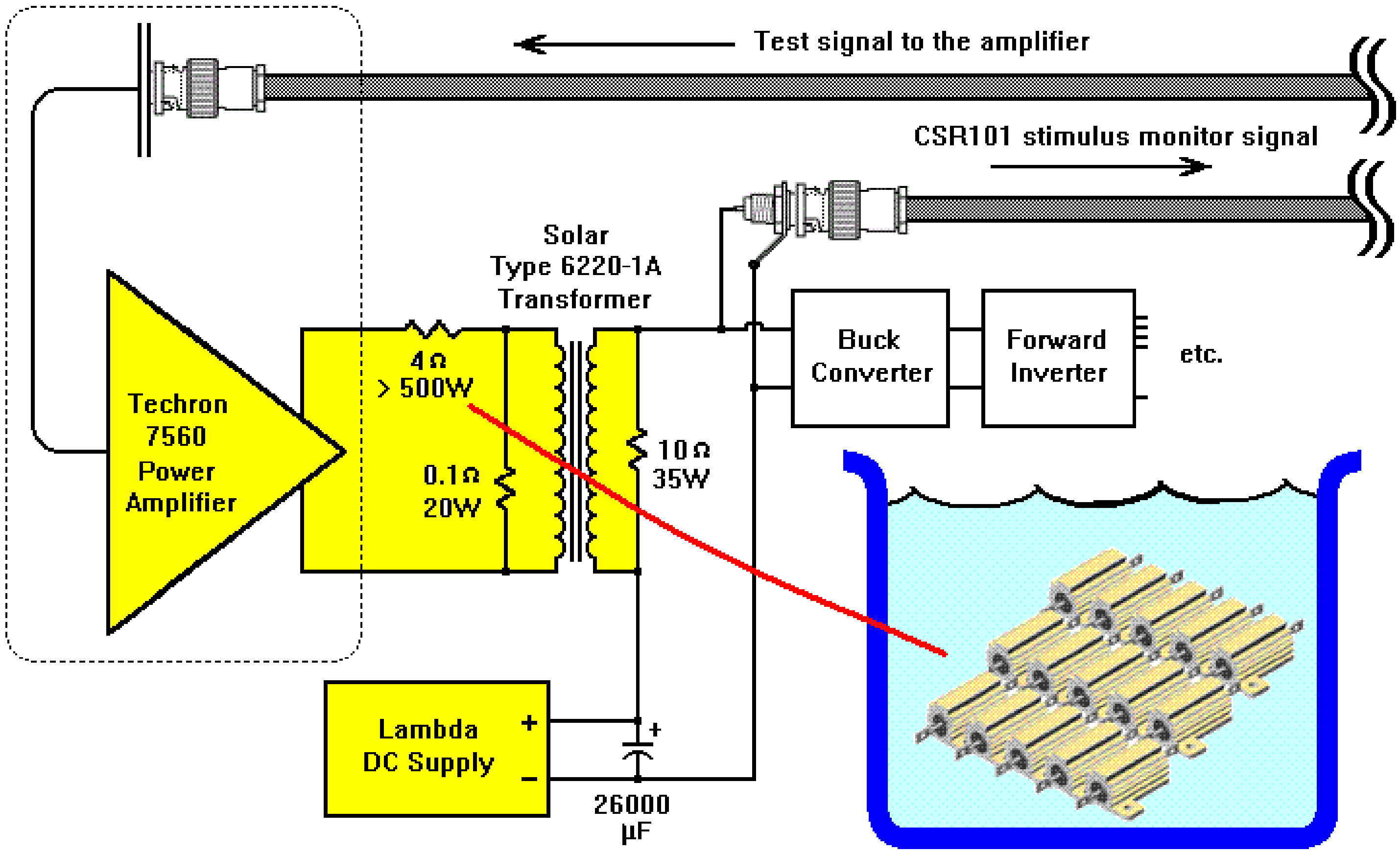
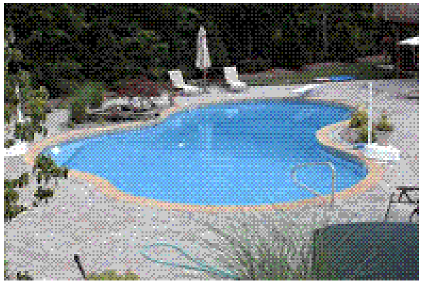
Stabilized Line Impedance



You might think you're failing ….

You might think that your equipment is failing its conducted susceptibility test, but you might simply be falling prey to the AC source impedance of your signal injection test fixture.

The CS101 performance of the unit shown before was markedly better with the big tub of water.



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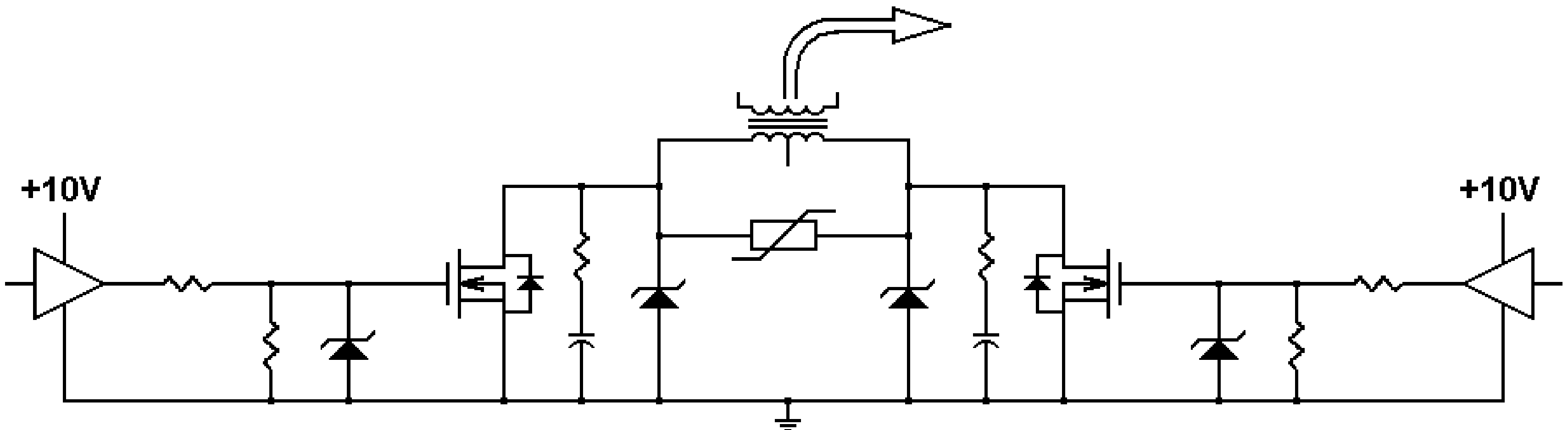
A Seemingly Good Inverter



This push-pull driver was designed with considerable attention devoted to protection of the two power MOSFETs. Notice the four transient catching zener diodes, the varistor connected between the two drains and the pair of RC snubbers, one across each power MOSFET's drain-to-source.

For all of that, these inverters were blowing out their power MOSFETs with considerable regularity for a reason that the designer seemed not to grasp.

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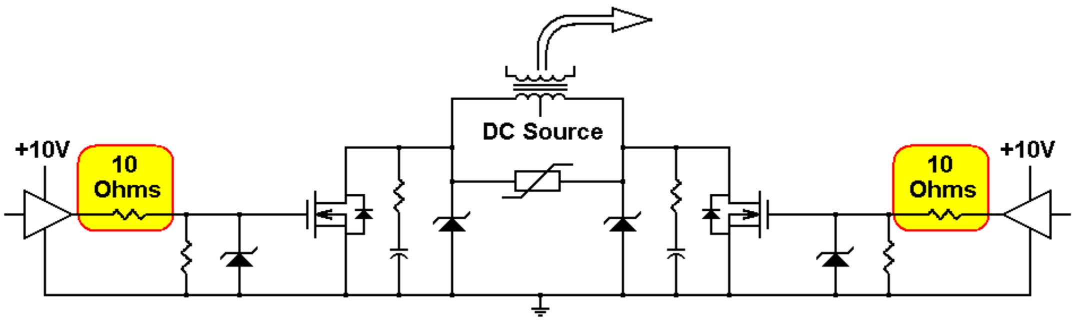
Overlap Effects (Bad!!!)



Simplifying assumptions:

1) We neglect the source impedances of the two drivers.

2) We assume that the two drivers are delivering zero to +10V square waves at 50% duty cycle and at negligibly small rise and fall times of their own.

3) The two MOSFETs are assumed to have the same threshold voltages, Vth.

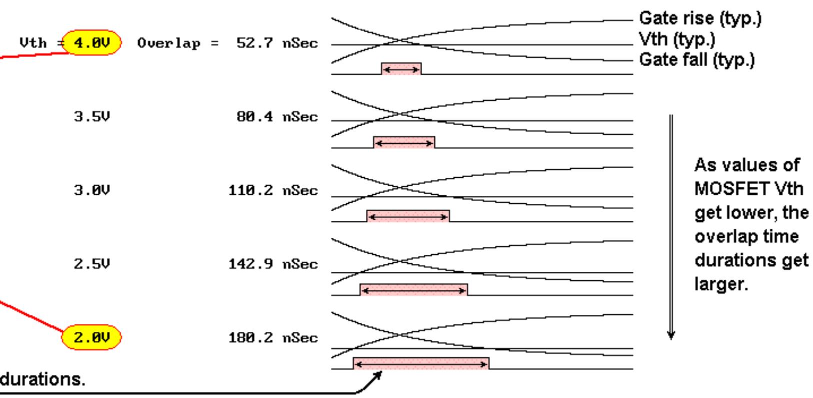
International
IOR Rectifier

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}$, I_D = 250µA
Q_g	Total Gate Charge	—	—	130		I_D = 28A
Q_{gs}	Gate-to-Source Charge	—	—	26	nC	V_{DS} = 80V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	43		V_{GS} = 10V, See Fig. 6 and 13

Cgate ~ 130 nC / 10V = 13000 pF
Let Rgate = 10 Ohms

Gate voltage rises and falls are taken as exponential. They will result in simultanteous MOSFET turn-ons of 52.7 nSec to 108.2 nSec (nominal) overlaps.



During these overlaps, the two MOSFETs effectively short circuit their DC power source and can draw current pulses of virtually unlimited amperage. Such pulses can lead to device failures.

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Don’t do it. Really!

Failing to provide for dead-time in that push-pull inverter was like putting the top-cap on backwards on this bottle of OJ. The inverter can work, but FETs frequently get burned out. You can pour juice from this bottle, but spills are quite likely.

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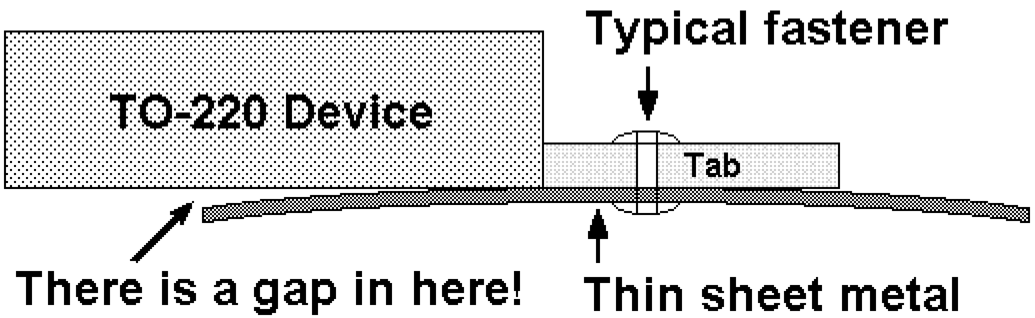
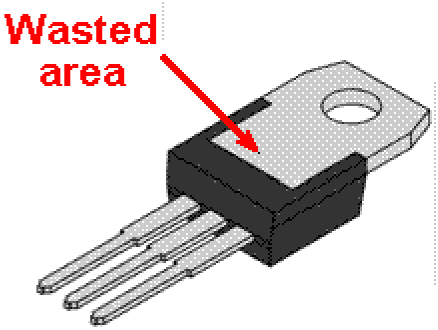
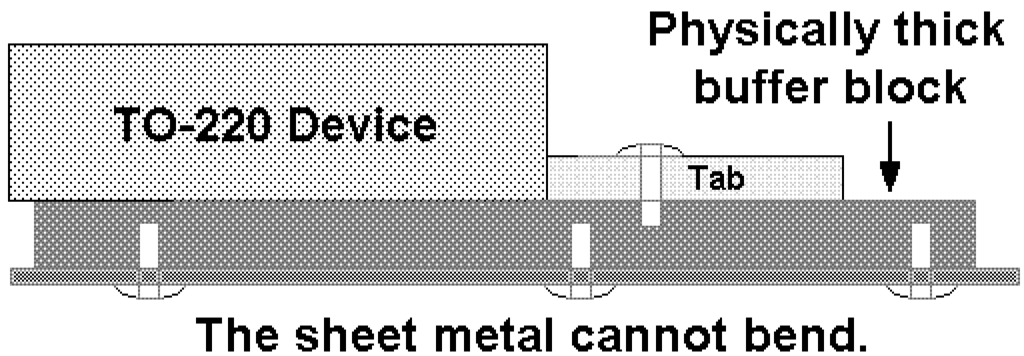
How much heat can a heat sink sink when the metal gets bent?





Adding a thick block underneath the TO-220 closes up the gap.

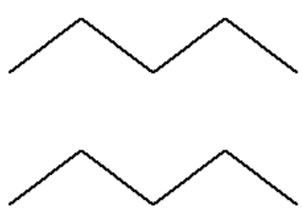


Power Factor

Power factor is the ratio of real power to apparent power. For a resistor, power factor is unity (1) for whatever the waveshape of the applied voltage may be because the waveshape of the resultant current will exactly match the waveshape of that applied voltage.

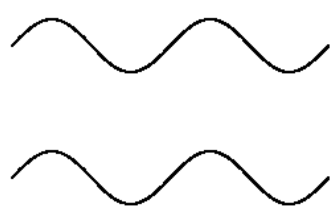
However, we in the power-supply world look at power factor for cases where the applied voltage is sinusoidal and where the resultant current may or may not be an exact match to that sinusoidal shape.

A non-sinusoidal applied voltage to a resistor yields a matching current waveshape:



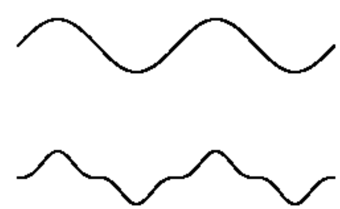
Power factor = 1

A sinusoidal applied voltage to a resistor yields a matching current waveshape:



Power factor = 1

A sinusoidal applied voltage to a who-knows-what-it-is yields a non-matching current waveshape:



Power factor < 1

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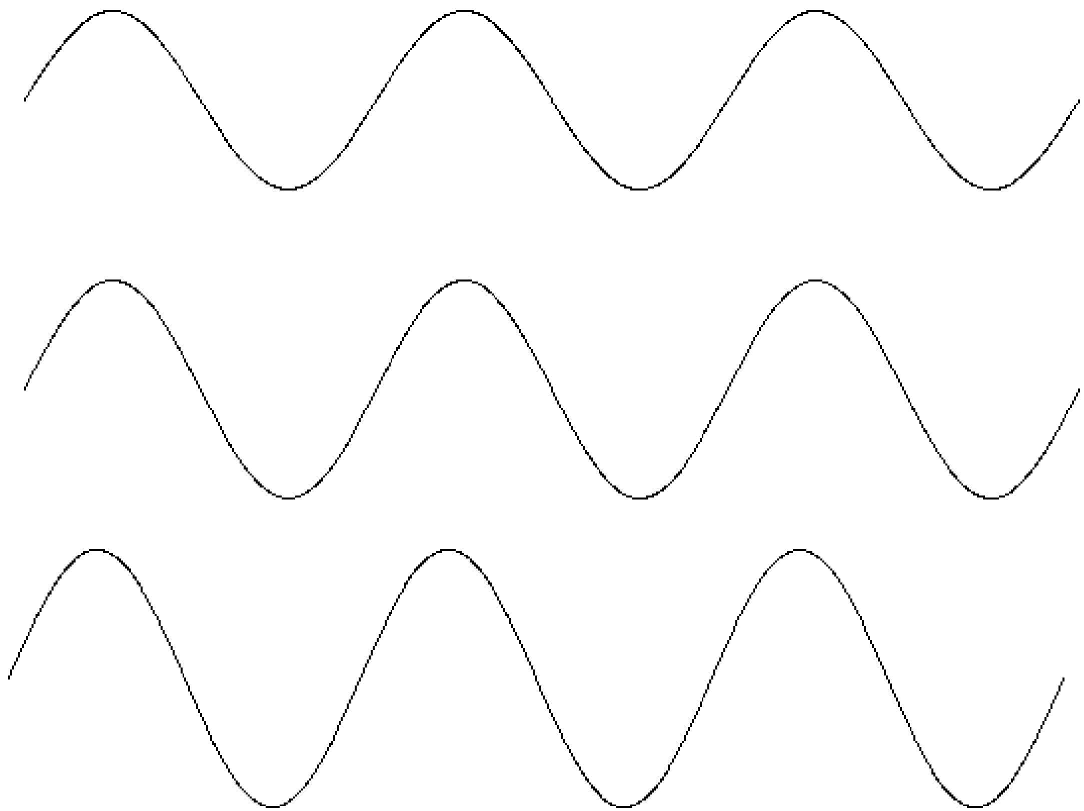
Variable Amplitude AC Power Line



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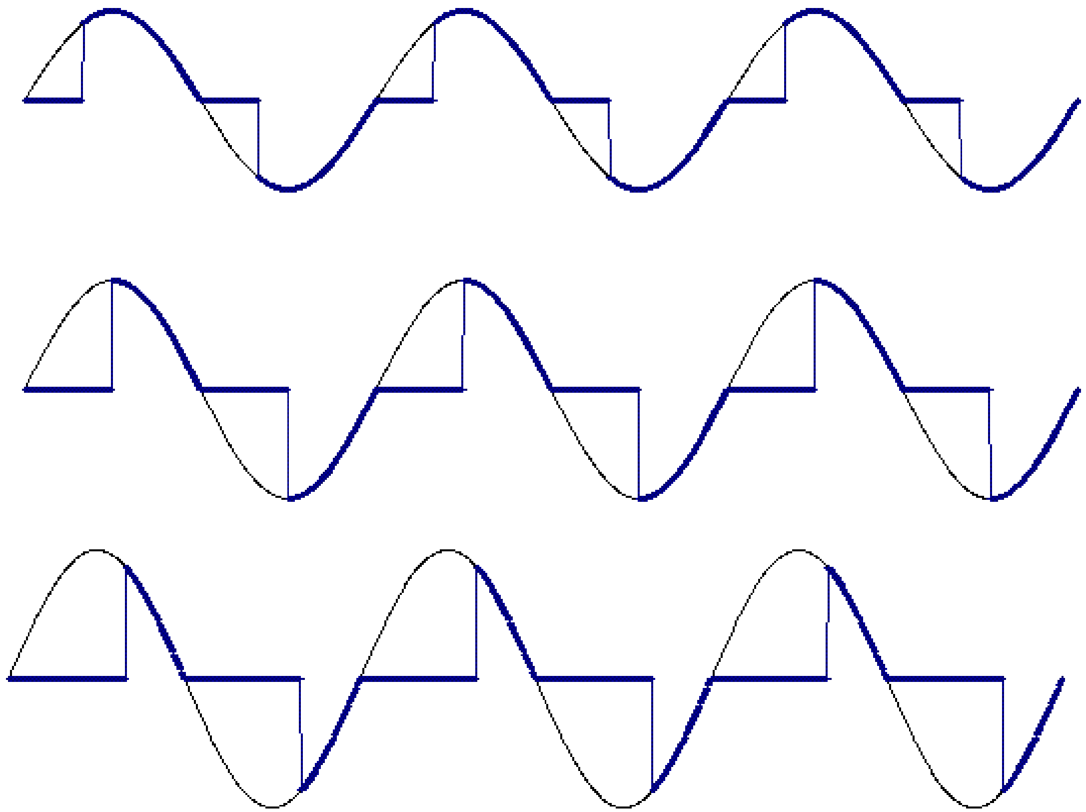
Triac or 2x SCR Waveforms



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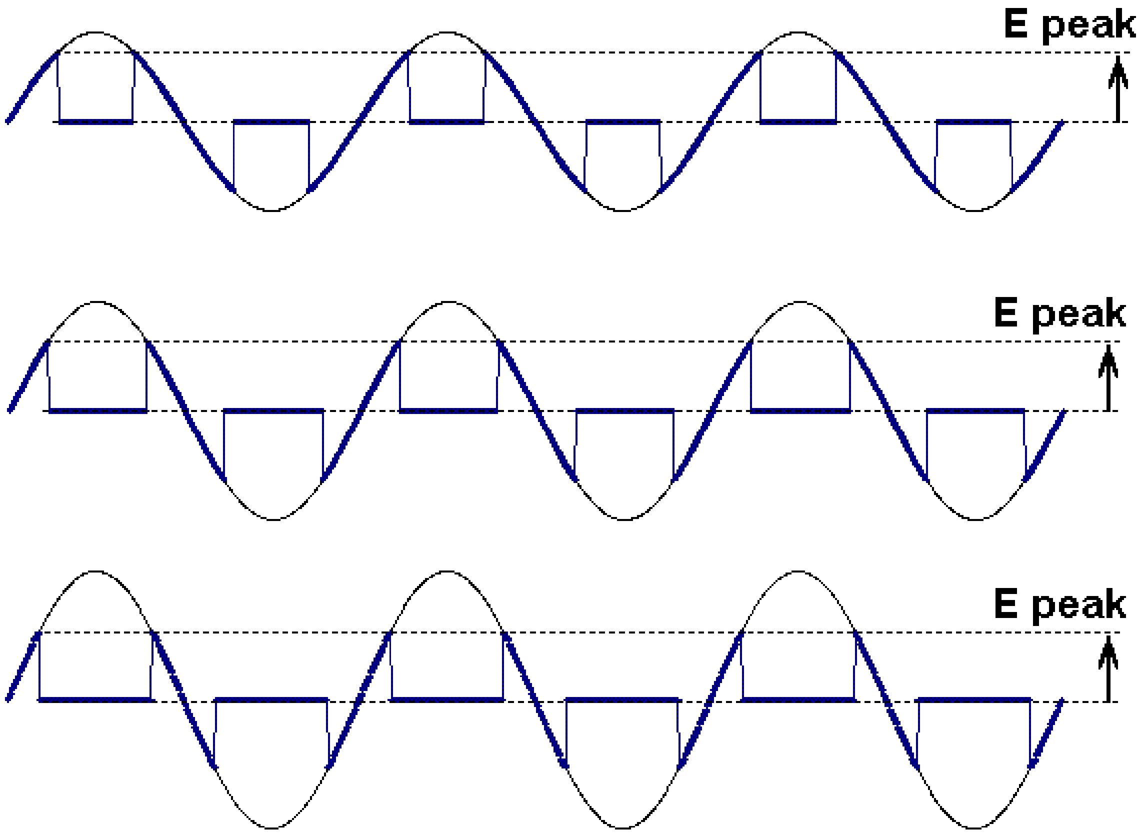
Peak-Regulated Pre-regulator Output



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Power Factor for Sinusoidal Vin

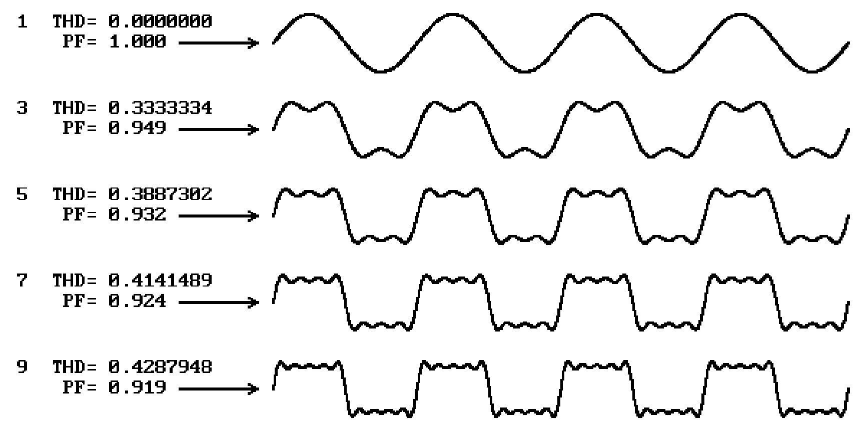
$$Thd = \frac{\sqrt{(i_2^2 + i_3^2 + \dots + i_n^2)}}{i_1}$$

Thd = Total harmonic distortion expressed as a fraction.

(15% distortion --> Thd = 0.15)

$$\text{Power Factor} = \frac{1}{\sqrt{1 + Thd^2}} \times \cos(\Theta)$$

For Θ = Zero:



The Power Factor Issue

```
10 CLS:SCREEN 9:COLOR 15,1:PI=3.14159265#
20 PRINT "save "+CHR$(34)+"pcheck10.bas"+CHR$(34):PRINT
30 PRINT "save "+CHR$(34)+"a:\pcheck10.bas"+CHR$(34):PRINT:PRINT
40 C$="M= #.##    Power= #.#####":GOTO 90
50 NCYCLES=100!:POWER=0:N=0:FOR THETA=0 TO 360*NCYCLES

60 VOLTS=SIN(THETA*PI/180):AMPS=SIN(M*THETA*PI/180)
```

This is the key!

```
70 POWER=POWER+VOLTS*AMPS:N=N+1:NEXT THETA:POWER=POWER/(N-1)
80 PRINT USING C$;M,POWER:RETURN:DATA 1,1.01,1.5,2,3,4
90 FOR XX=1 TO 6:READ M:GOSUB 50:NEXT XX

M= 1.00  Power= 0.50000

M= 1.01  Power= -.00000
M= 1.50  Power= -.00000
M= 2.00  Power= -.00000
M= 3.00  Power= 0.00000
M= 4.00  Power= 0.00000
```

There is power delivery only when the voltage and the current are of the same frequency. In other words, only when M = 1.

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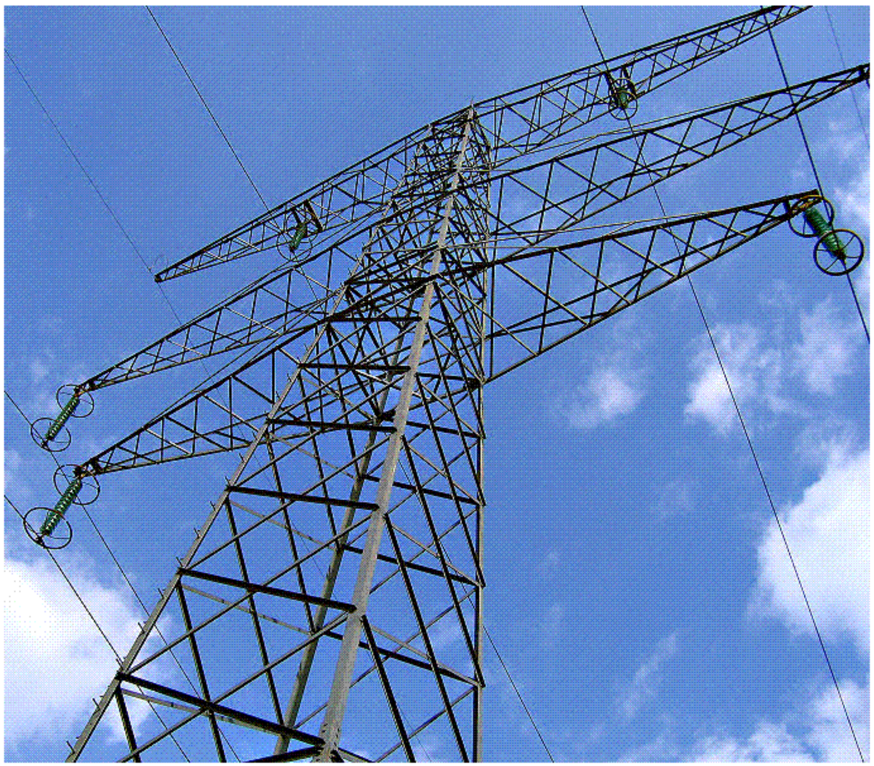
An Issue With High Voltage



Danger High Voltage

Peligro Alto Voltaje

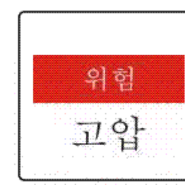
Danger Haute Tension

Periculum Altus Voltage

Perigo Alta Voltagem

Gefahr Hochstrom

Pericolo Alta Tensione



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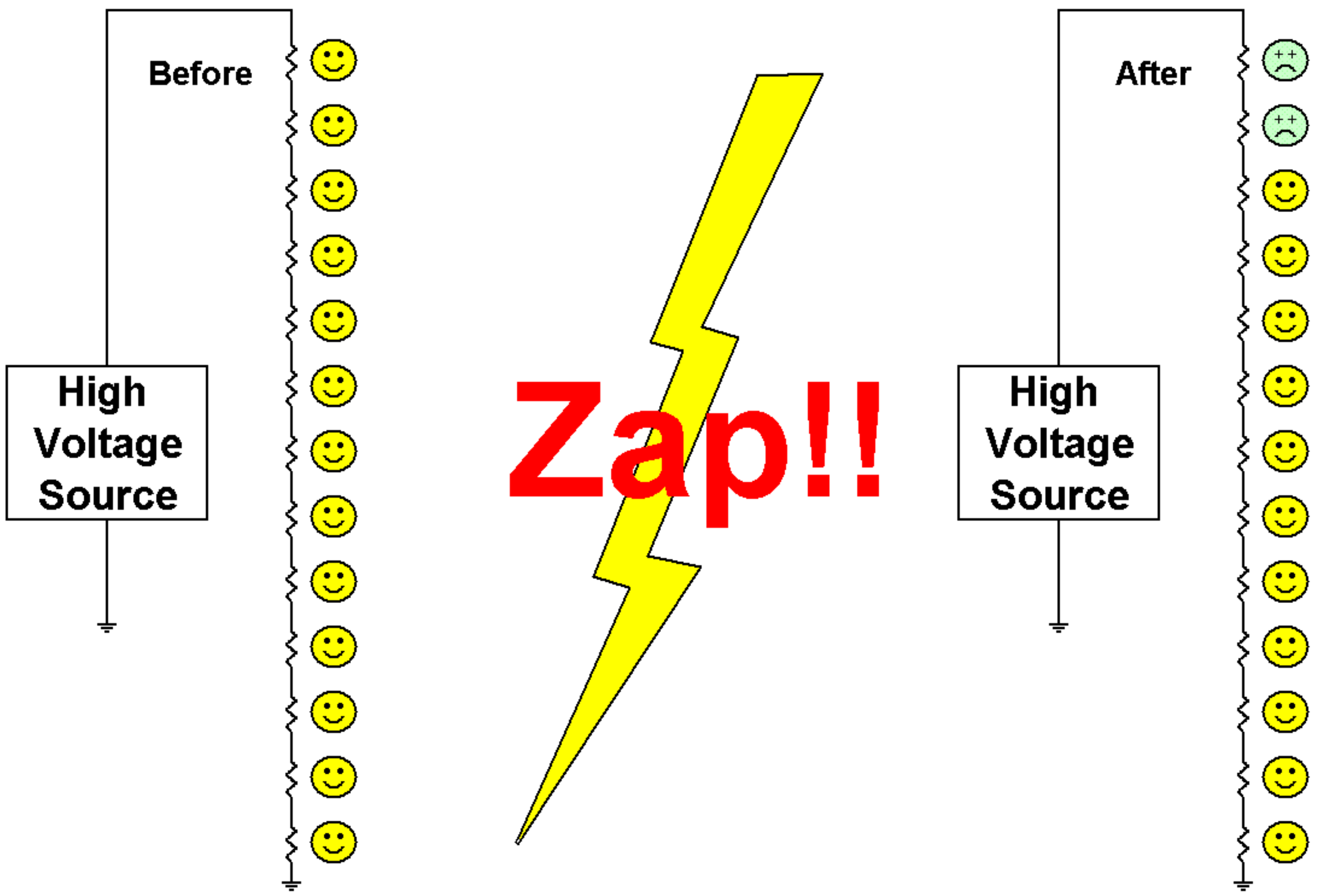
HV Resistor Damage



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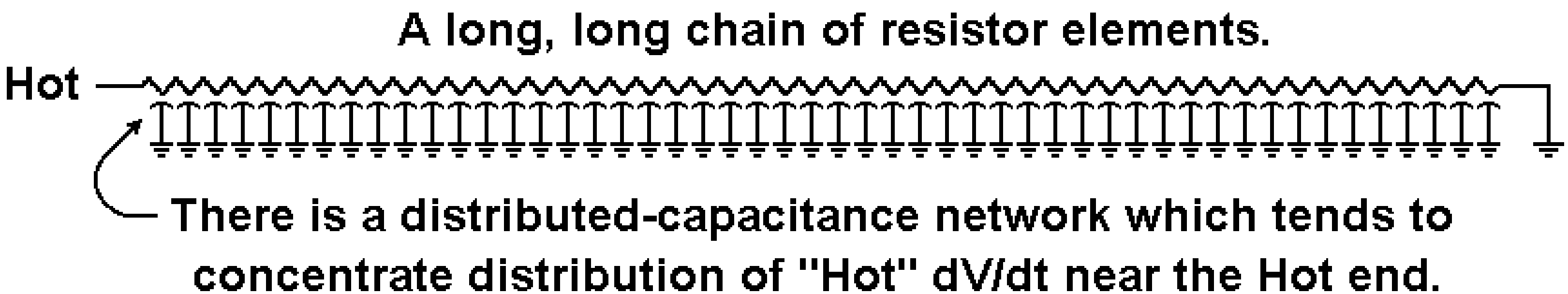
Distributed Capacitance



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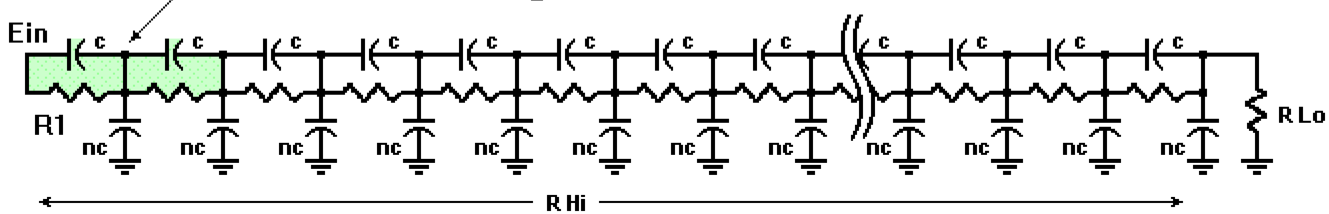
A Capacitive Ladder Network

Cshunt is the shunt capacitance to ground seen with respect to ground due to all of the capacitances to the right of this node.



c	nc	Cshunt	AC Div	AC Div R1
1	0.01	0.105	0.905	0.095
1	0.02	0.152	0.868	0.132
1	0.03	0.189	0.841	0.159
1	0.04	0.221	0.819	0.181
1	0.05	0.250	0.800	0.200
1	0.06	0.277	0.783	0.217
1	0.07	0.302	0.768	0.232
1	0.08	0.326	0.754	0.246
1	0.09	0.348	0.742	0.258
1	0.10	0.370	0.730	0.270
1	0.10	0.370	0.730	0.270
1	0.20	0.558	0.642	0.358
1	0.30	0.718	0.582	0.418
1	0.40	0.863	0.537	0.463
1	0.50	1.000	0.500	0.500

If n = 0.01, then R1 will see 0.095 of a voltag step that occurs at Ein.

If En goes from 50000 volts down to zero, resistor R1 will see 50000 x 0.095 which comes to 4750 volts.

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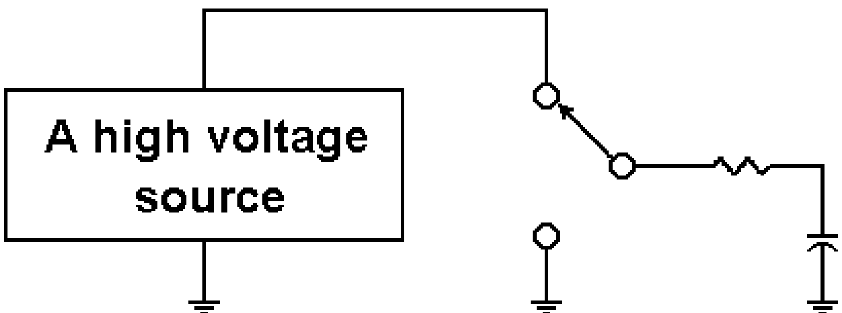
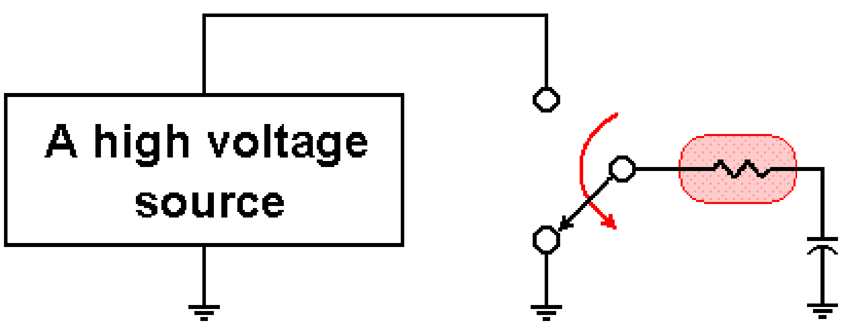
In the extreme case:



When the capacitance is fully charged, there is no voltage stress imposed across the resistor.



However, when the switch goes to the low side, the dV/dT across the resistor is virtually infinite and the resistor gets really stressed.

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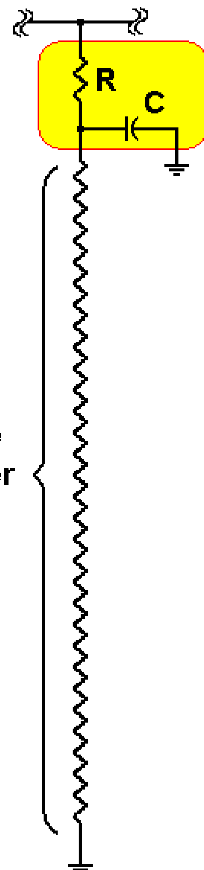
Protecting an HV Divider

High voltage node,
let's say at 50000 volts.

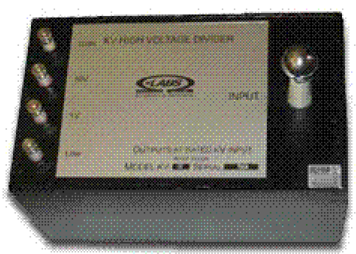


A protective resistance R which we let be 10K and a protective capacitance C with which we limit the top end of the large resistance to a maximum dV/dt of 1E11 volts per second.

For the given case, the C value would be 50 pF, but we find that 100 pF is the smallest value in at least one capacitor company's product line so we use that!

A nice large resistance of some voltage divider drawing 50 μA comes to 1000 Meg.

Treat These Things With Care!!



These dividers look rugged and they are very heavy. However, it is really easy to damage one by being just a little bit careless!!

Never, never, never allow a short circuit or an arc-over to happen while one of these super-duper-rise-and-shine-extra-fine-top-of-the-line voltage dividers is connected.

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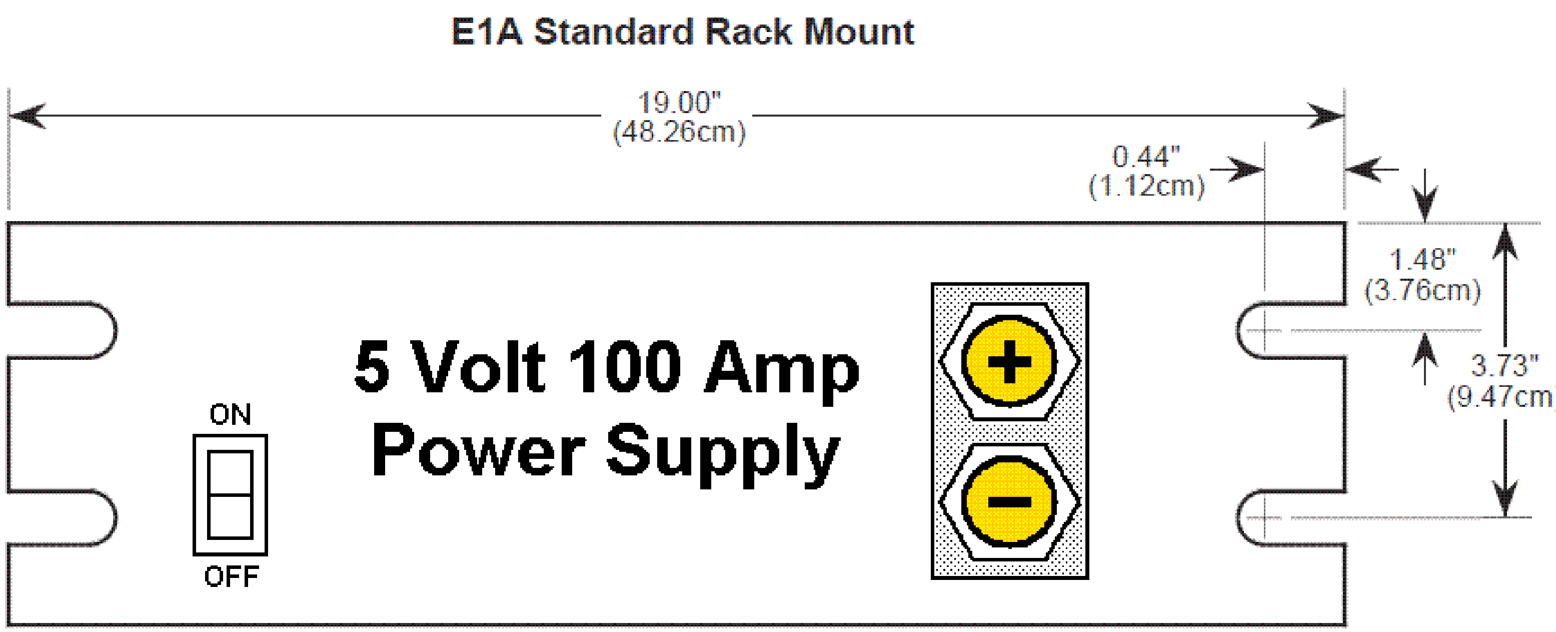
A Pretty Nice Design, Really



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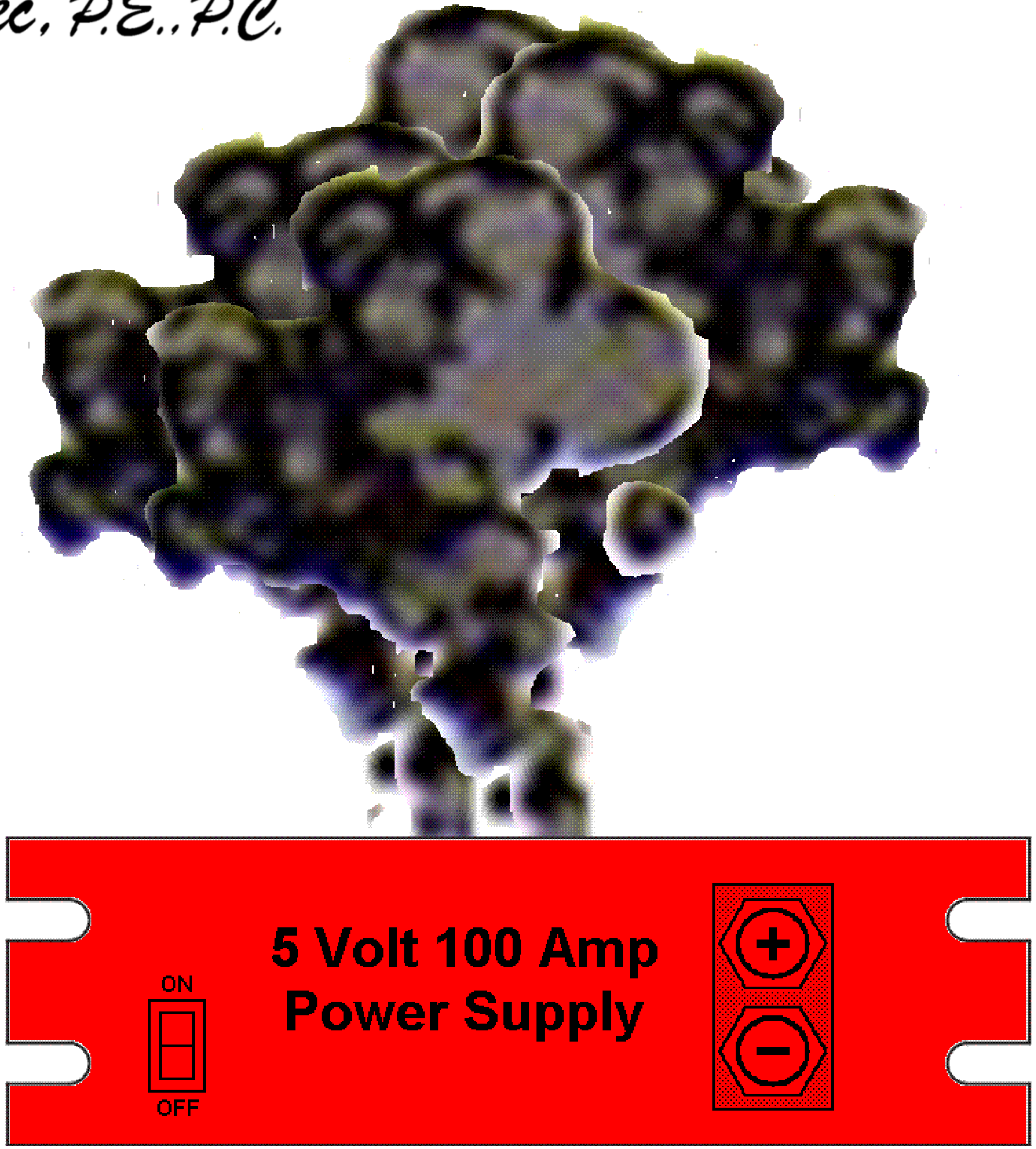

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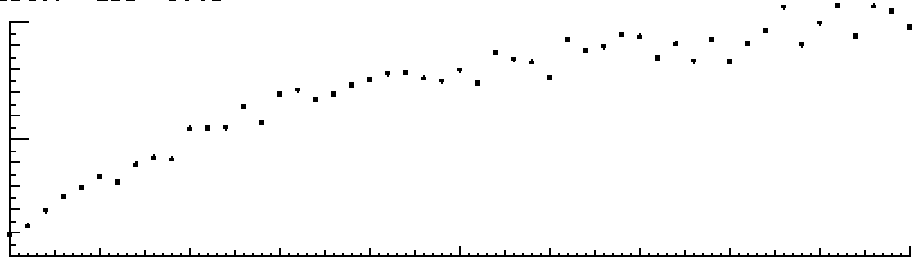
Kinda Messy Looking Data

0	9.1	2	12.8	4	19.6	6	25.5	8	29.2	10	34.0	12	31.7
14	39.0	16	42.0	18	41.2	20	54.3	22	54.3	24	54.9	26	63.8
28	56.9	30	69.0	32	71.1	34	66.8	36	69.3	38	73.1	40	75.6
42	78.0	44	78.4	46	75.9	48	74.9	50	79.6	52	73.9	54	86.9
56	84.1	58	82.8	60	75.9	62	92.2	64	87.6	66	89.6	68	94.4
70	93.5	72	84.5	74	90.5	76	83.4	78	92.3	80	82.9	82	90.6
84	96.0	86	106.5	88	90.4	90	99.6	92	106.8	94	93.8	96	106.5
98	104.7	100	97.8										



A collection of data points can be gathered. We take it that the process that yielded these data points is essentially exponential in nature.

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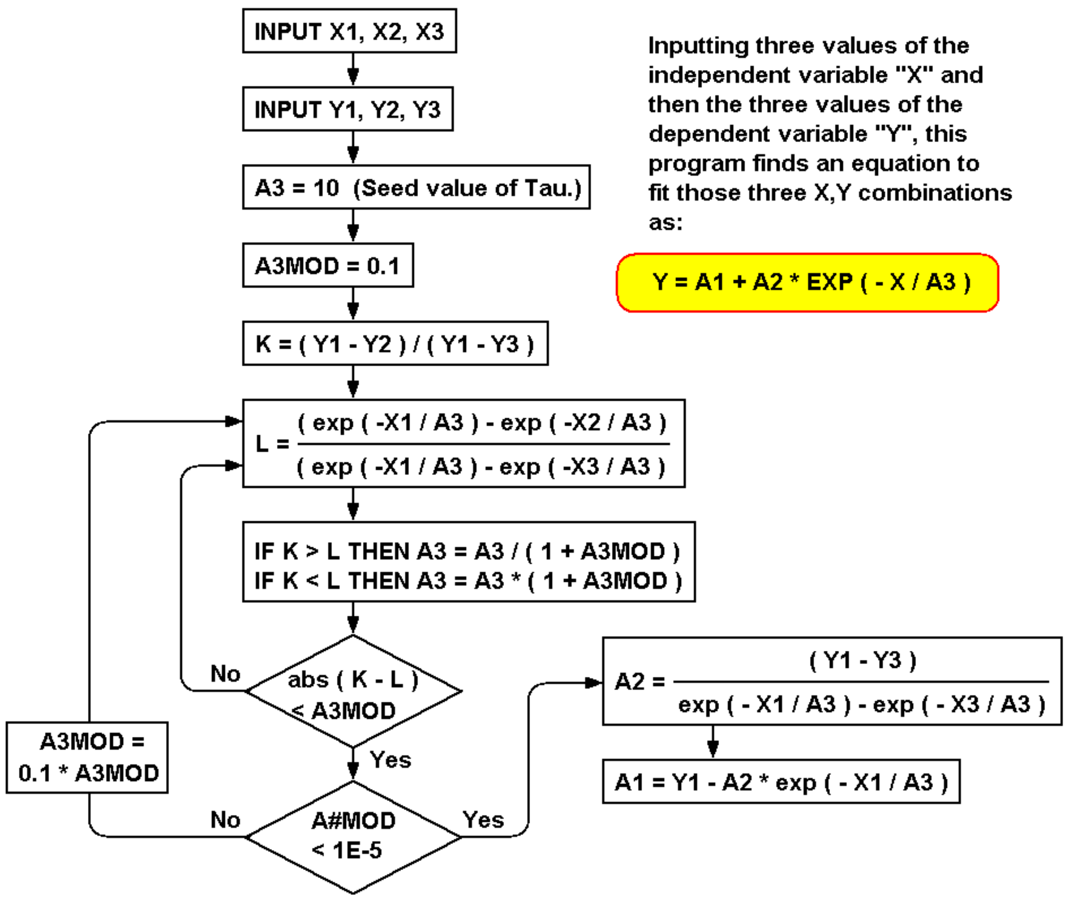
Finding An Exponential Equation

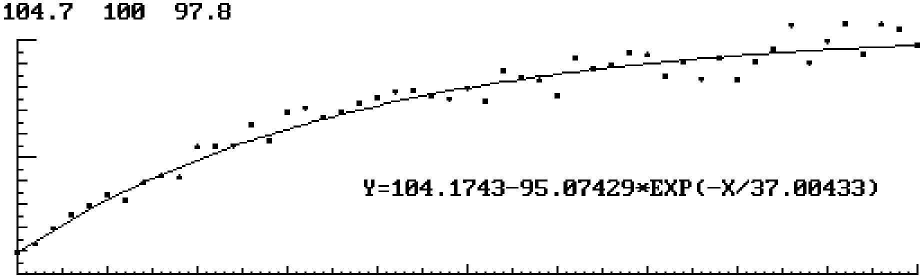
Inputting three values of the independent variable "X" and then the three values of the dependent variable "Y", this program finds an equation to fit those three X,Y combinations as:

Y = A1 + A2 * EXP (- X / A3)



The Equation Fits Pretty Well

0	9.1	2	12.8	4	19.6	6	25.5	8	29.2	10	34.0	12	31.7
14	39.0	16	42.0	18	41.2	20	54.3	22	54.3	24	54.9	26	63.8
28	56.9	30	69.0	32	71.1	34	66.8	36	69.3	38	73.1	40	75.6
42	78.0	44	78.4	46	75.9	48	74.9	50	79.6	52	73.9	54	86.9
56	84.1	58	82.8	60	75.9	62	92.2	64	87.6	66	89.6	68	94.4
70	93.5	72	84.5	74	90.5	76	83.4	78	92.3	80	82.9	82	90.6
84	96.0	86	106.5	88	90.4	90	99.6	92	106.8	94	93.8	96	106.5
98	104.7	100	97.8										



An exponential equation can be fitted to the data points by selecting just three of those data points and running the code "expestim.bas" or something like it.

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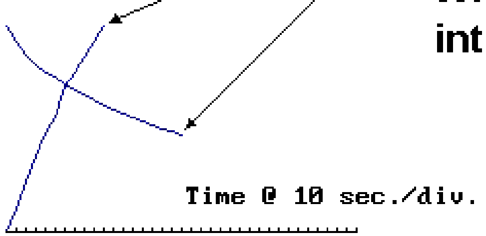
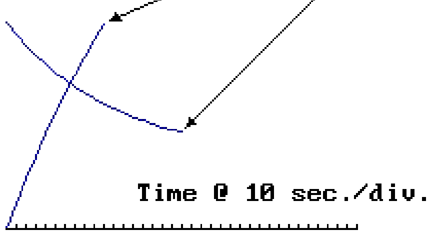
Thermal Rise and Fall

Plots of the actual data of temperature rise and temperature fall at time intervals of ten seconds.



Exponential equations fitted to the actual data as shown above.



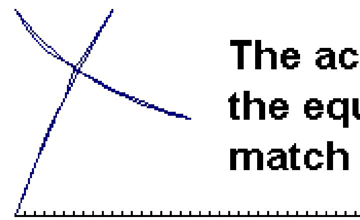
Rise:

$$\text{Deg C} = 159 - 134 * \exp(-\text{Tsec} / 200)$$

Fall:

$$\text{Deg C} = 42 + 35 * \exp(-\text{Tsec} / 110)$$

Note that the Tau of the temperature rise is almost twice that of the fall.



The actual data and the equation results match quite well.

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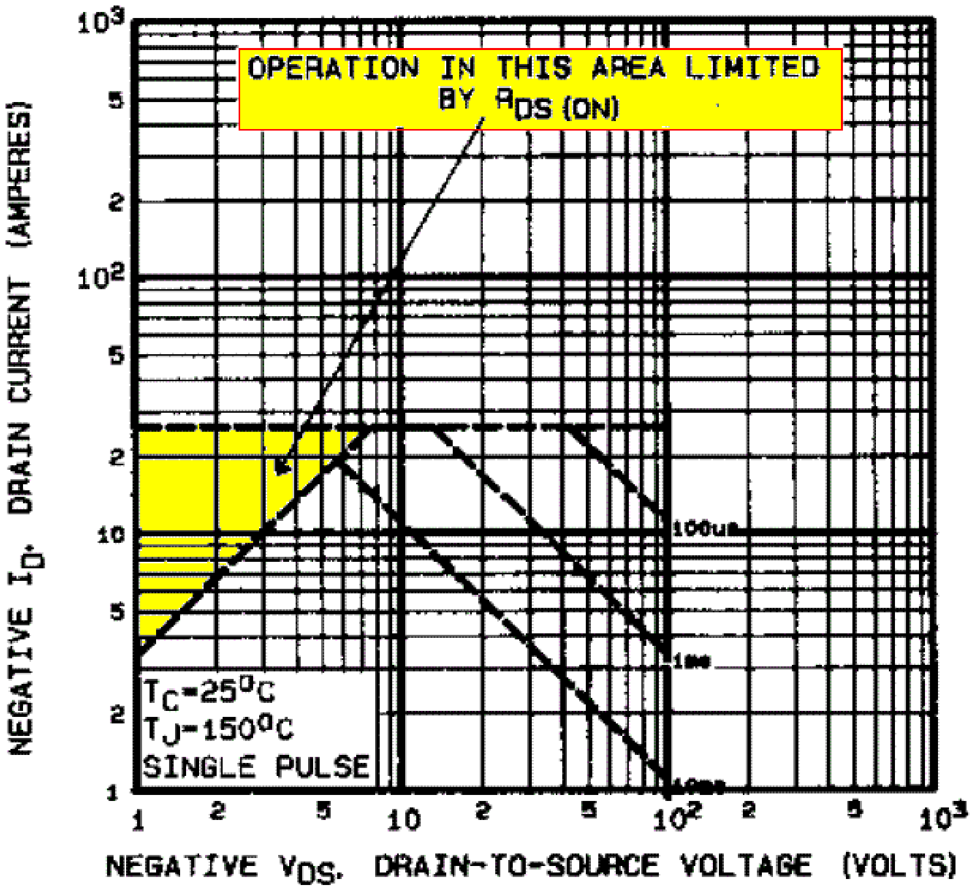
A Mixed Blessing



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Rdson Rises As Temp. Rises

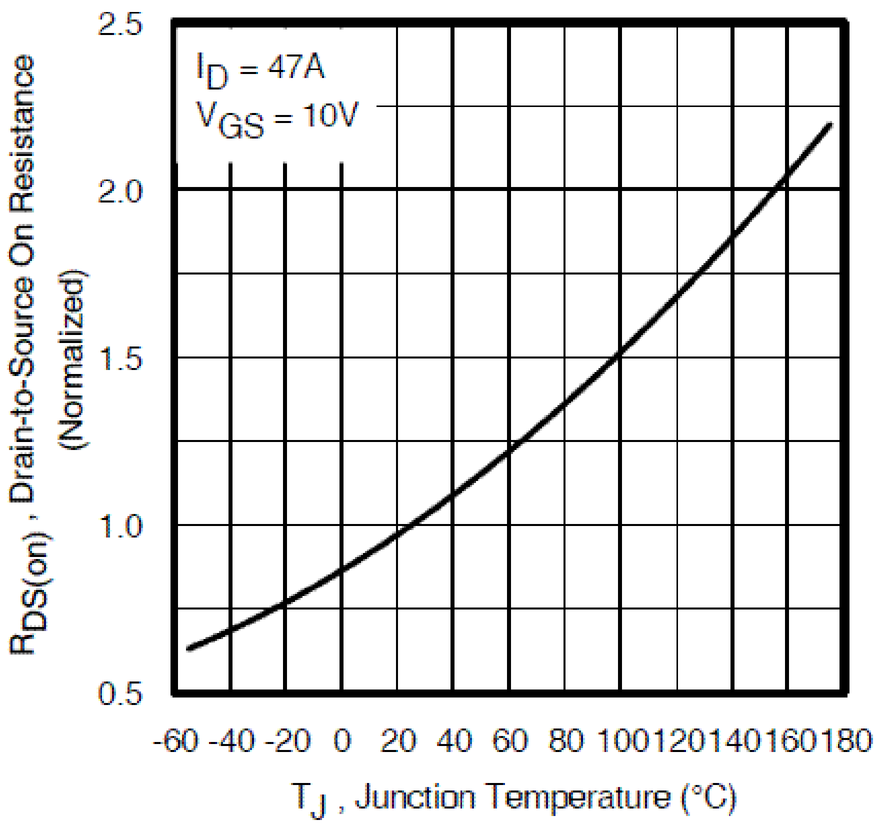

Fig 4. Normalized On-Resistance vs. Temperature

The on-resistance of a power MOSFET rises as temperature goes up. If you have drain-to-source current that is not particularly dependent on the value of on-resistance, then as the FET gets hotter, its resistance rises which makes for more power dissipation which makes the FET get hotter which makes ....

This is the path to thermal runaway!

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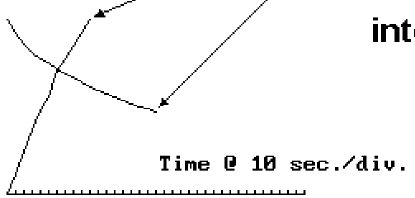
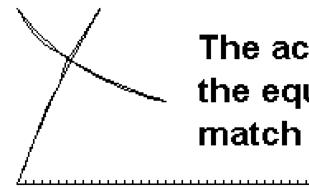
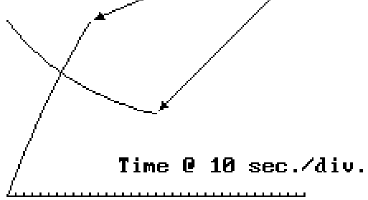
Temp. Rise and Fall Before Fix



Plots of the actual data of temperature rise and temperature fall at time intervals of ten seconds.



The actual data and the equation results match quite well.



Exponential equations fitted to the actual data as shown above.

Rise:
Deg C = 159 - 134 * exp (- Tsec / 200)

Fall:
Deg C = 42 + 35 * exp (- Tsec / 110)

Note that the Tau of the temperature rise is almost twice that of the fall.

The apparently larger value of the time constant of the temperature rise curve is an illusion. What happens is that the end-point value of the rising curve is itself rising, the final temperature value is climbing and that will eventually kill the power MOSFETs.

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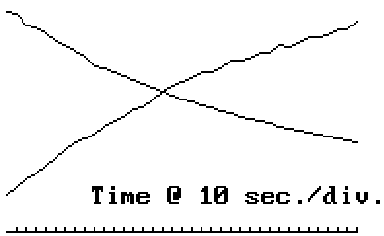
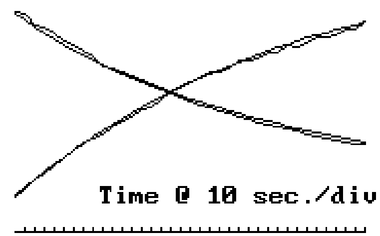
Temp. Rise and Fall After Fix

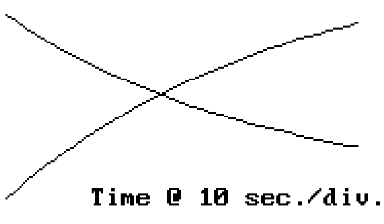
Plots of the actual data of temperature rise and temperature fall at time intervals of ten seconds.



The actual data and the equation results match quite well.



Exponential equations fitted to the actual data as shown above.



Rise:
Deg C = 96 - 62 * exp (- Tsec / 280)

Fall:
Deg C = 36 + 45 * exp (- Tsec / 260)

Note that the Tau values of the rise and fall are very nearly equal.

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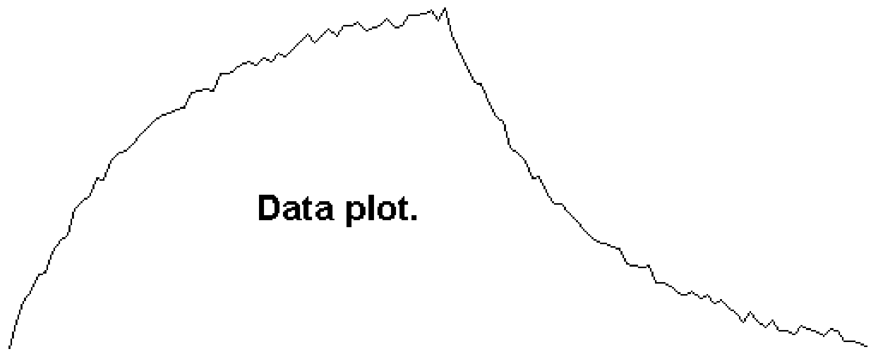
Plotting Some *Alleged* Data

Tabulated data of temperature rise and fall said to be taken at ten second intervals.

```
 23.1, 30.7, 36.3, 40.0, 44.6, 45.0, 50.9, 54.3, 56.0, 63.5
 65.3, 67.5, 72.5, 71.9, 77.6, 80.0, 80.3, 82.6, 85.2, 87.3
 89.4, 90.8, 91.5, 92.5, 93.2, 97.5, 97.9, 98.7, 98.1,102.8
102.8,104.1,106.0,106.6,105.4,107.4,106.6,109.2,107.8,110.1
111.9,114.6,111.8,114.2,116.1,113.9,117.0,117.0,118.1,115.5
116.4,116.8,118.8,116.5,116.9,119.9,119.8,120.3,121.7,118.6
121.9,114.4,108.6,104.9,100.4,100.0, 94.1, 90.7, 89.0, 81.5
 79.6, 77.5, 72.5, 73.1, 67.4, 65.1, 64.8, 62.4, 59.8, 57.7
 55.6, 54.2, 53.5, 52.5, 51.8, 47.5, 47.0, 46.3, 46.9, 42.1
 42.2, 40.9, 39.0, 38.4, 39.6, 37.6, 38.4, 35.8, 37.2, 34.9
 33.2, 30.4, 33.3, 30.9, 28.9, 31.1, 28.1, 28.0, 26.8, 29.5
 28.6, 28.2, 26.3, 28.5, 28.1, 25.1, 25.2, 24.7, 23.3, 26.4
```



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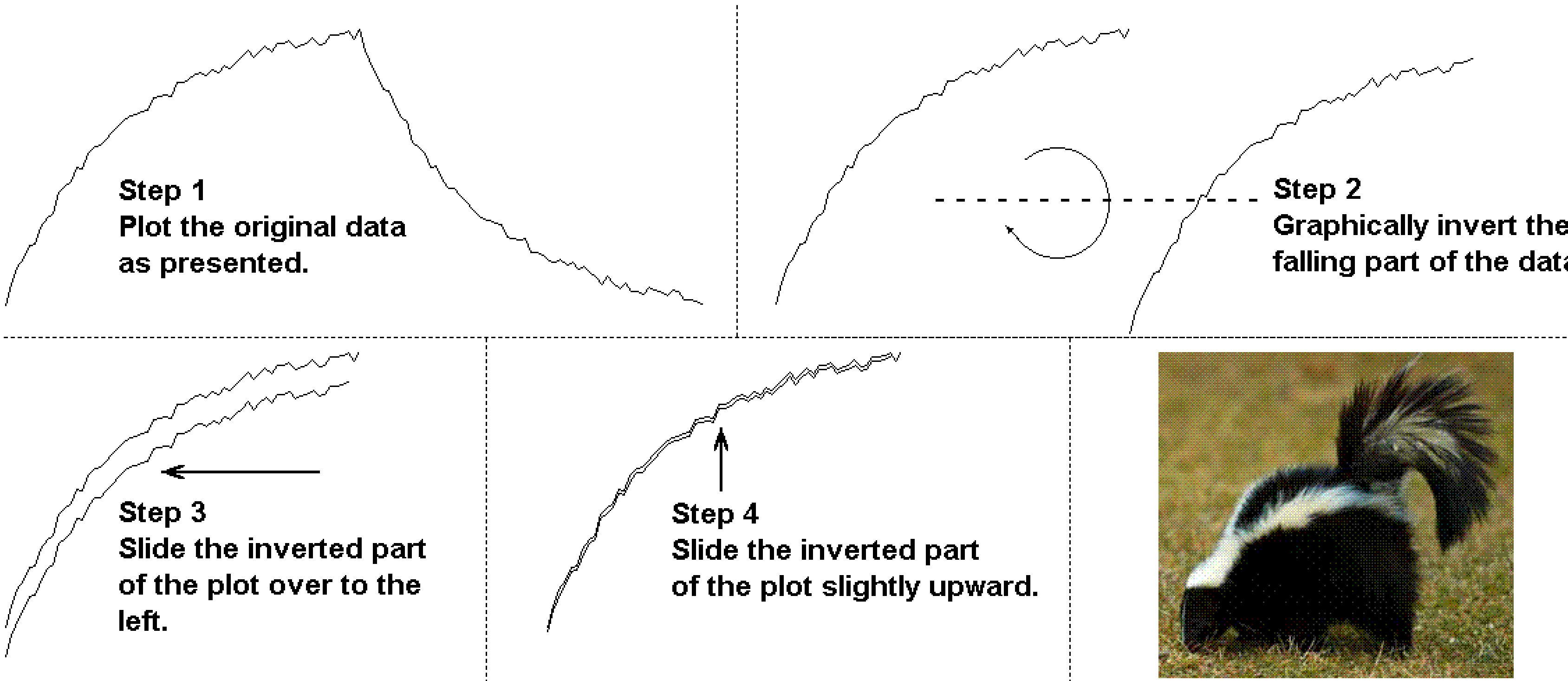
Dirty Doings Were Afoot!!!



Notice in Step 4 that all of the little ups and downs of the overlaid drawing sections are alike. Clearly, the data as presented was falsified!! (I did not confront my would-be client with his lie, I simply stated I could not be of service, left and never returned.)

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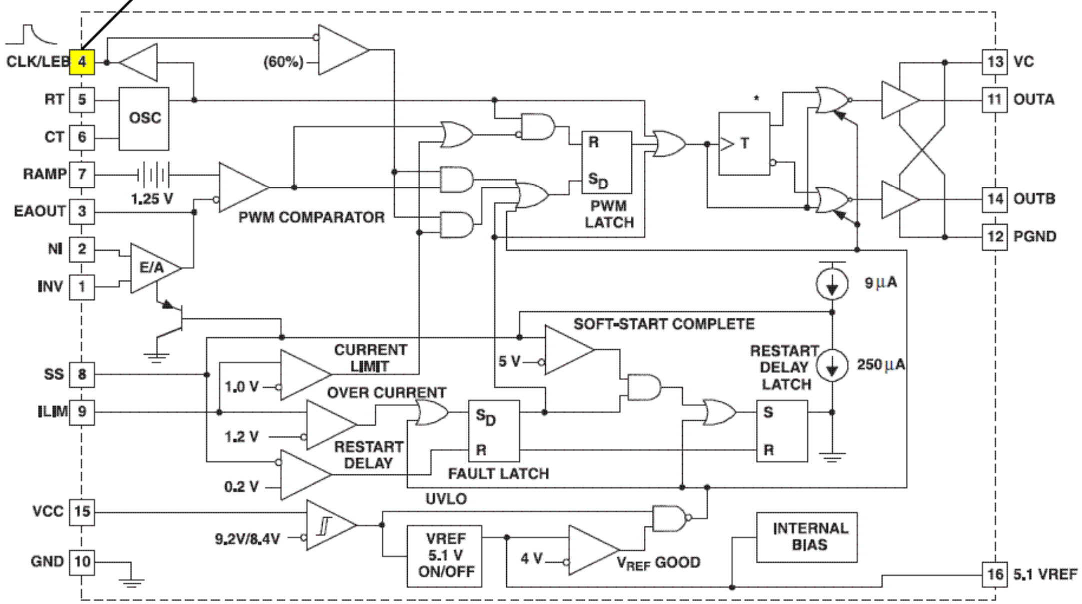
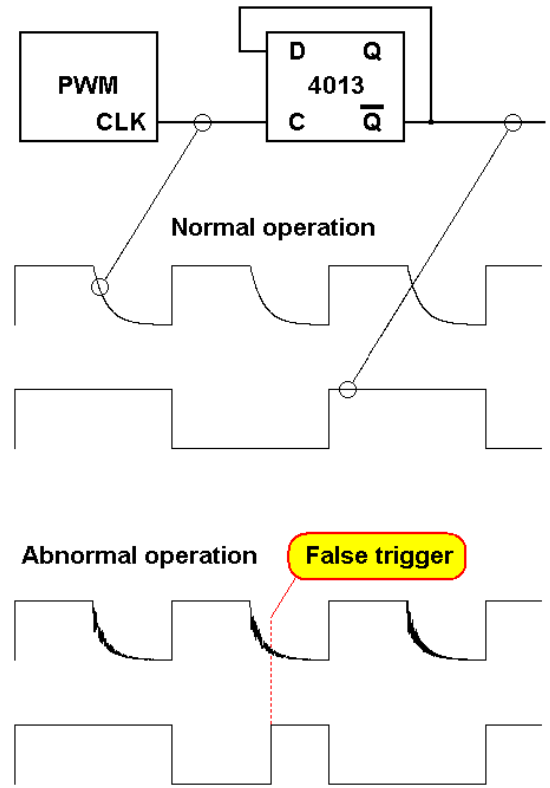
The D-type Flip-Flop Problem

The clock signal was being used to trigger a D-type flip-flop (a CD4013) which was supposed to do a divide-by-two on the clock signal's frequency. However, since the flip-flop had no Schmitt trigger on its input, it would respond to false triggering caused by noise on the clock waveform's falling edge.

The clock signal of the PWM chip has a sharp rising edge, but a slow-decay falling edge on which some measure of noise is found.





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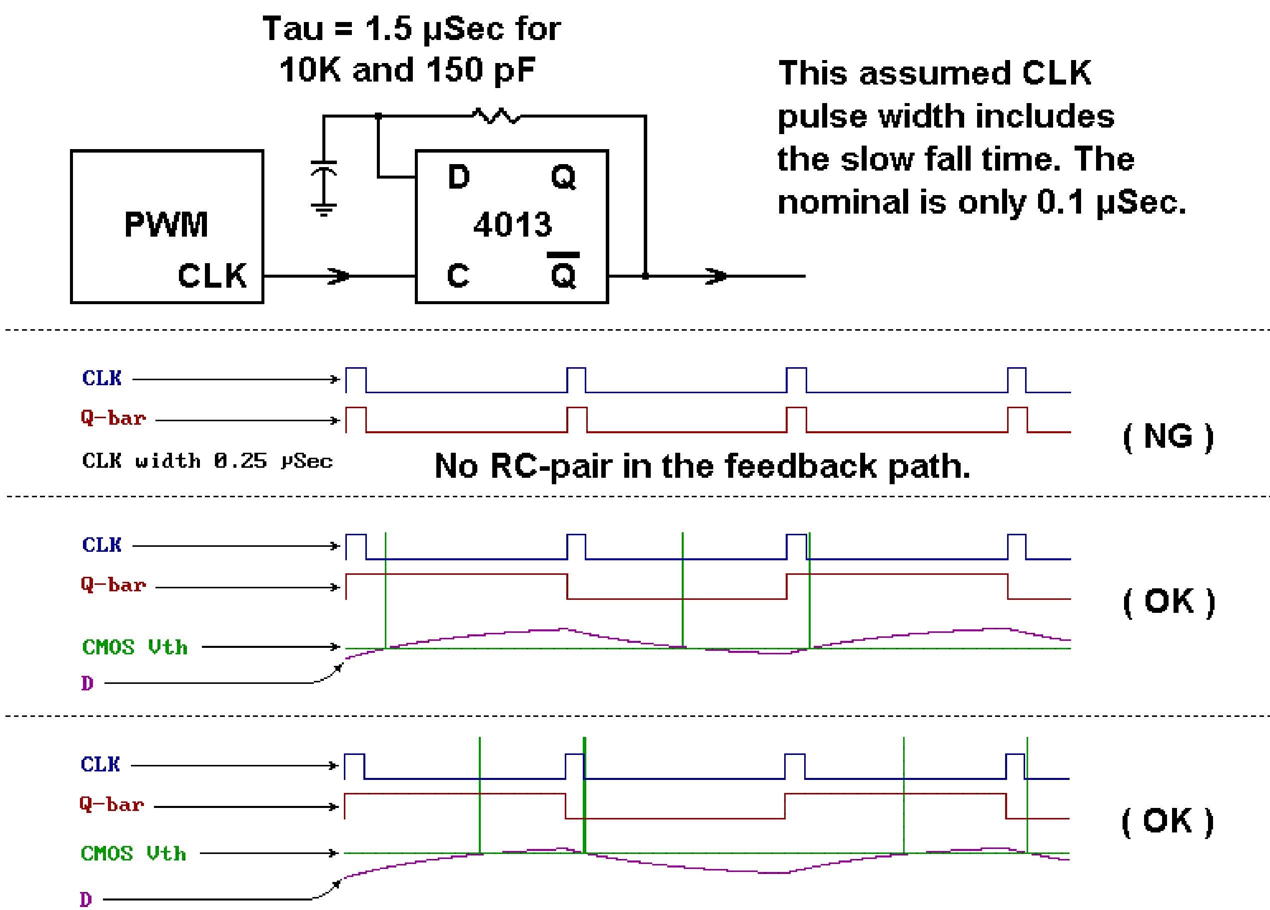
Using an RC in the Q* to D Path



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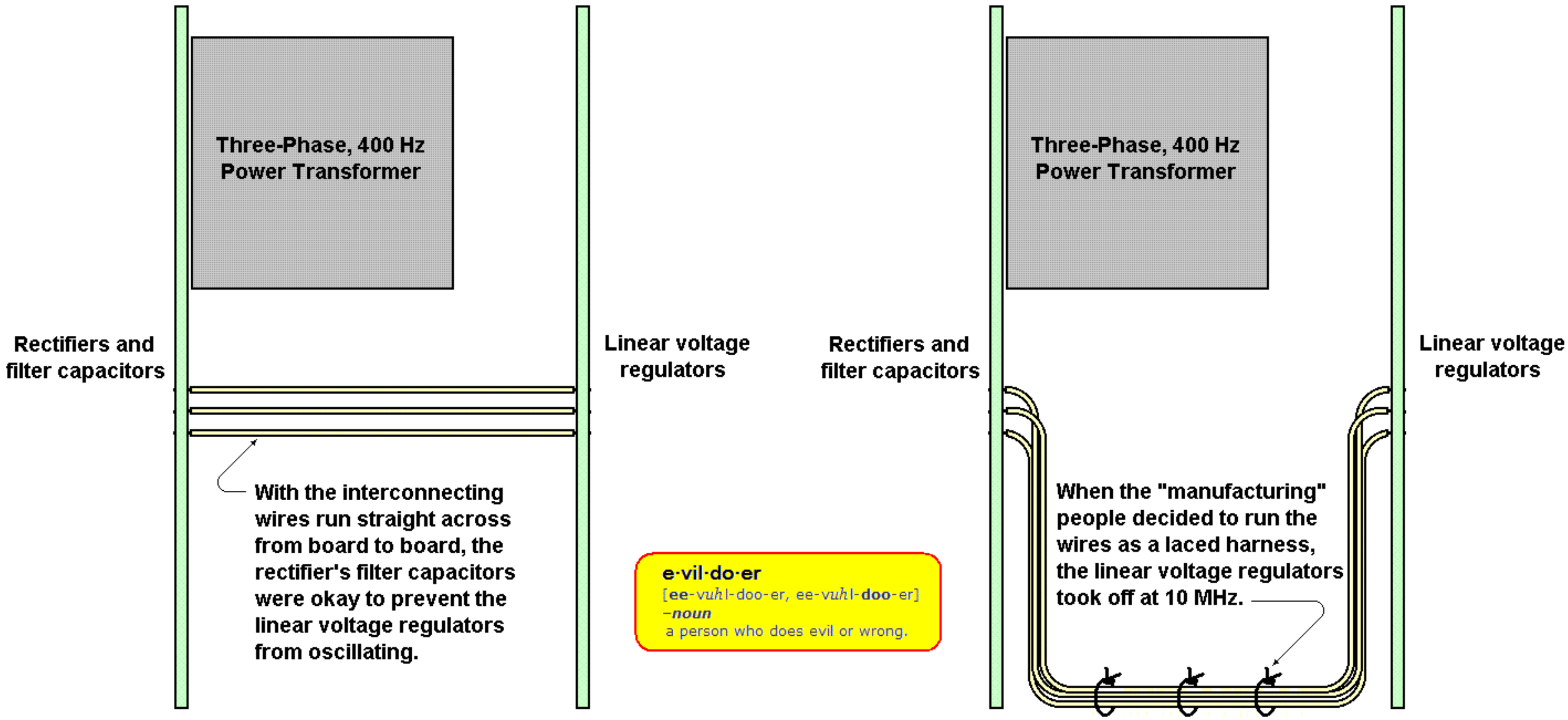
Making A 10 MHz Oscillator



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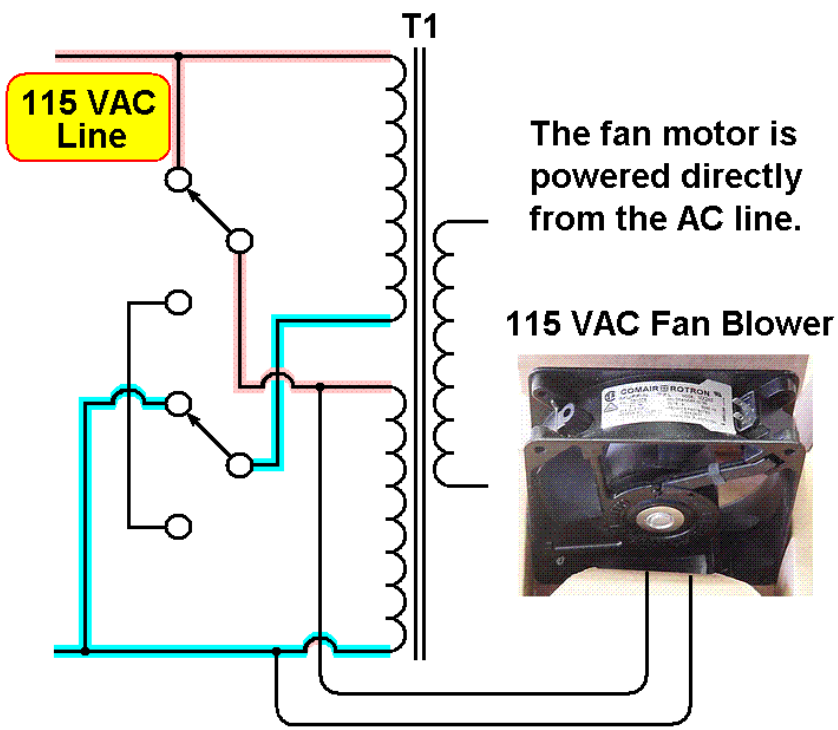
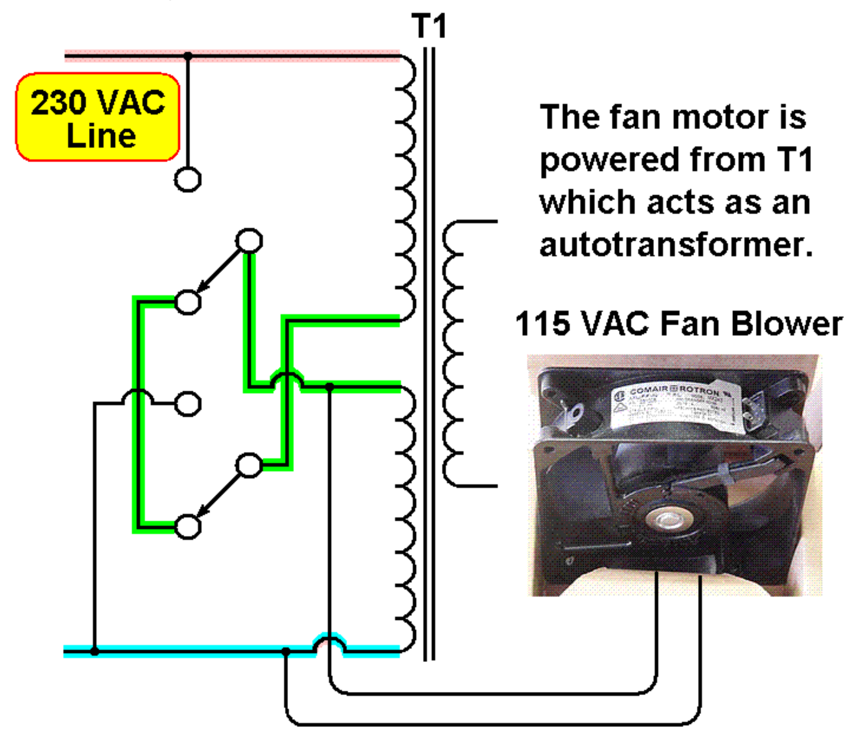
One Motor, Two Line Voltages





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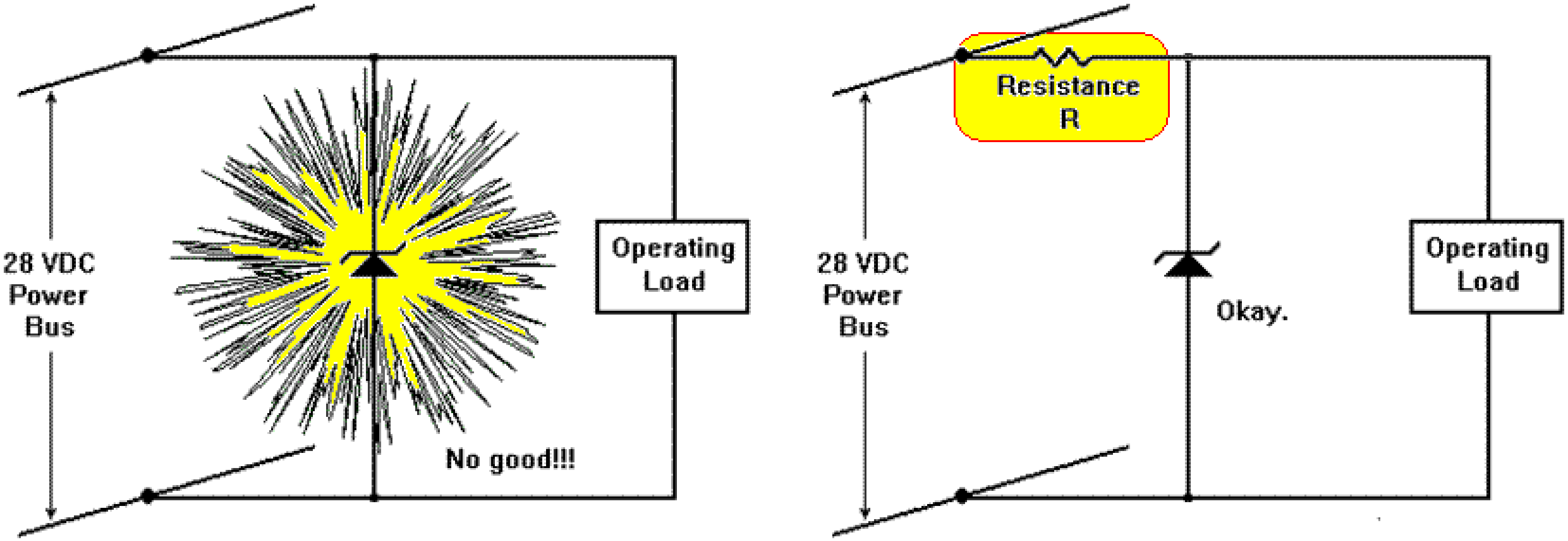
Transient Protector Peril



You can't safely just put a transient absorber across a power line without a safety impedance, usually a resistance, although some application notes do suggest using an inductance.

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From MIL-STD-704A

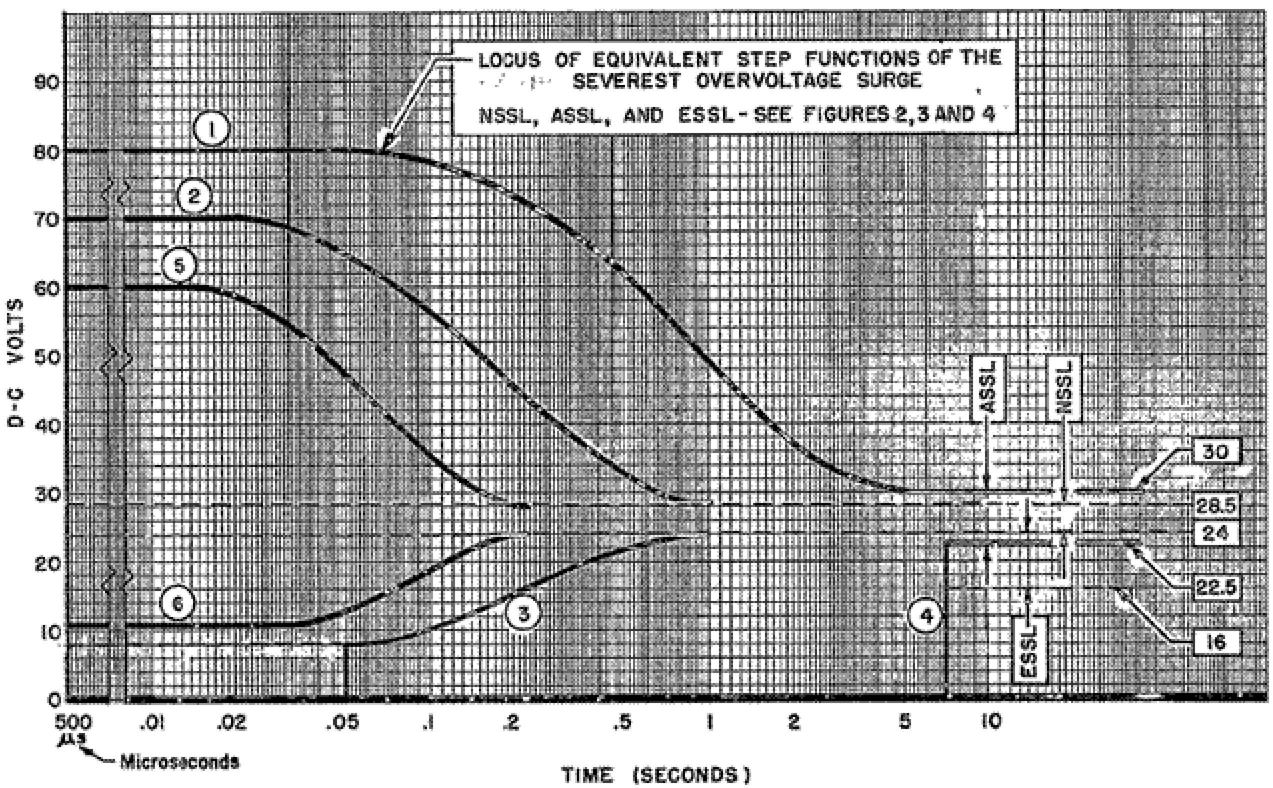

FIGURE 9. Transient surge dc voltage step function loci limits for category B equipment

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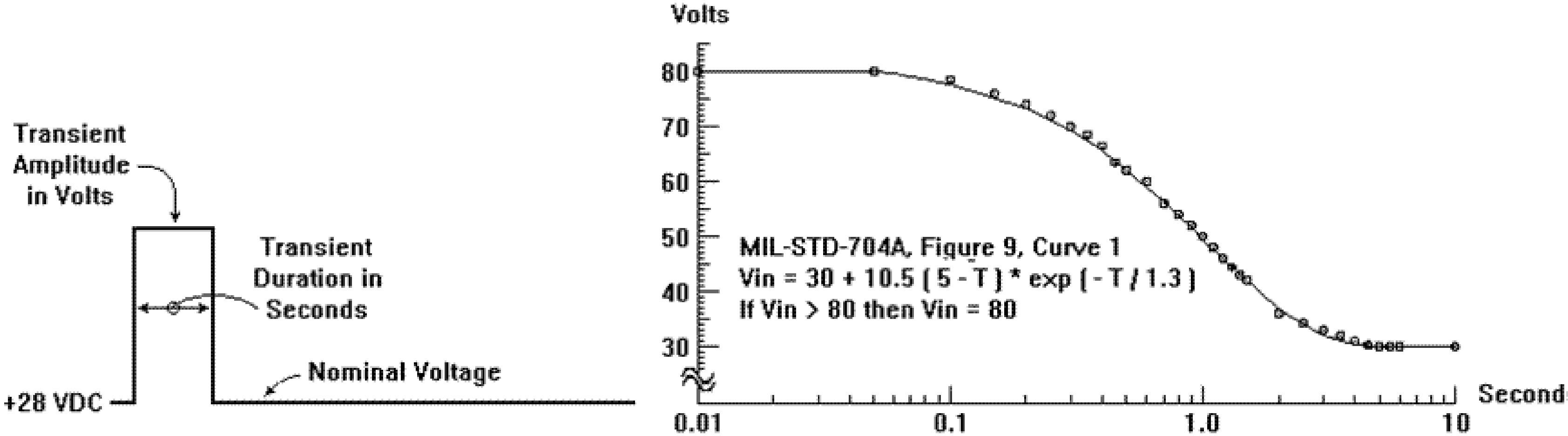
MIL-STD-704A Transients



Data points copied from the specification itself are plotted on top of a curve whose mathematical expression empirically describes the transients' properties.

Picking A Transient Protector

Electrical Characteristics (TA = 25°C unless otherwise noted)

JEDEC Type Number	General Semiconductor Part Number	Breakdown Voltage $V_{(BR)}$ (V)(1)		Test Current at I_T (mA)	Stand-off Voltage V_{WM} (V)	Maximum Reverse Leakage at V_{WM} I_D(4) (μA)	Maximum Peak Pulse Current I_{PPM}(2) (A)	Maximum Clamping Voltage at I_{PPM} V_C (V)	Maximum Temp. Coefficient of $V_{(BR)}$ (% / °C)
		Min	Max						
1N6267	+1.5KE6.8	6.12	7.48	10	5.50	1000	139	10.8	0.057
1N6267A	+1.5KE6.8A	6.45	7.14	10	5.80	1000	143	10.5	0.057
1N6268	+1.5KE7.5	6.75	8.25	10	6.05	500	128	11.7	0.061
[illegible]	+1.5KE7.5A	[illegible]	[illegible]	10	[illegible]	[illegible]	133	[illegible]	[illegible]
1N6283A	[illegible]	31.4	34.7	[illegible]	28.2	1.0	[illegible]	[illegible]	0.098
1N6284	+1.5KE36	32.4	39.6	1.0	29.1	1.0	28.8	52.0	0.099
1N6284A	+1.5KE36A	34.2	37.8	1.0	30.8	1.0	30.1	49.9	0.099
1N6285	+1.5KE39	35.1	42.9	1.0	31.6	1.0	26.6	56.4	0.100
1N6285A	+1.5KE39A	37.1	41.0	1.0	33.3	1.0	27.8	53.9	0.100
1N6286	+1.5KE43	38.7	47.3	1.0	34.8	1.0	24.2	61.9	0.101
[illegible]	+1.5KE43A	[illegible]	[illegible]	1.0	[illegible]	[illegible]	25.3	[illegible]	[illegible]
1N6289A	[illegible]	53.2	58.8	[illegible]	47.8	1.0	[illegible]	[illegible]	0.103
1N6290	1.5KE62	55.8	68.2	1.0	50.2	1.0	16.9	89.0	0.104
1N6290A	1.5KE62A	58.9	65.1	1.0	53.0	1.0	17.6	85.0	0.104
1N6291	1.5KE68	61.2	74.8	1.0	55.1	1.0	15.3	98.0	0.104

We select a candidate transient protector, in this case, a 1N6284A.

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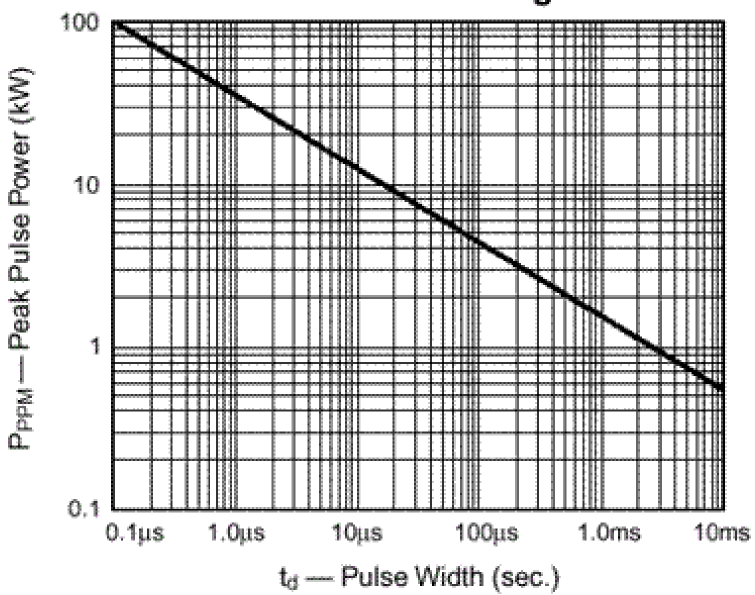
1N6284A Peak Power Equation

Peak Pulse Power Rating Curve



Let power P1 = 10^5 watts for duration T1 = 0.1 µSec.
Let power P2 = 560 watts for duration T2 = 10 mSec.

Let the form of the equation be: $P = \dfrac{K2}{T^{K1}}$

We use the above two data points to set up two equations in two unknowns:

$$P1 = \frac{K2}{T1^{K1}} \quad \text{and} \quad P2 = \frac{K2}{T2^{K1}}$$

First we solve for the coefficient K1:

$$\frac{P1}{P2} = \frac{T2^{K1}}{T1^{K1}} = \left(\frac{T2}{T1}\right)^{K1} \quad ; \quad K1 \times \mathrm{Log}\left(\frac{T2}{T1}\right) = \mathrm{Log}\left(\frac{P1}{P2}\right)$$

$$\therefore \quad K1 = \frac{\mathrm{Log}\left(\dfrac{P1}{P2}\right)}{\mathrm{Log}\left(\dfrac{T2}{T1}\right)} \quad \text{and} \quad K2 = P1 \times T1^{K1} \ \text{-- or --}\ K2 = P2 \times T2^{K1}$$

We derive for the 1N6284A that: $P = \dfrac{70.3823}{T^{0.45036}}$

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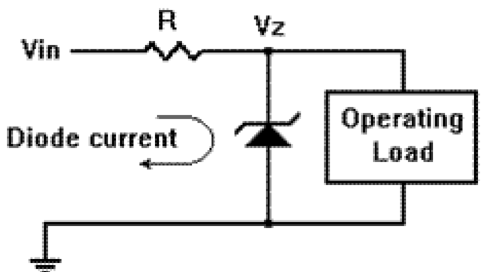
Finding The Value of "R"



Assume that the operating load is drawing no current at all.
Let the 28 VDC bus voltage transient be taken as a pulse of amplitude Vin and duration T.
Let the diode be assumed an ideal clamp at a voltage Vz.

The diode current will be $\frac{Vin - Vz}{R}$ for which the diode power will be $P = \left(\frac{Vin - Vz}{R}\right) Vz$.

The equation for power is then rearranged to be an equation for resistance: $R = \left(\frac{Vin - Vz}{P}\right) Vz$.

We next recall the equations for Vin versus time and P versus time and insert both of them into the equation for R:

$$R = \left(\underbrace{30 + 10.5 \left(5 - T \right) * \exp \left(- T / 1.3 \right)}_{\text{Maximum numerical value equals 80.}} - Vz \right) \frac{Vz \ T^{K1}}{K2}$$

This is now an equation for the value of R versus time. Let that relationship be defined as R = f (T).

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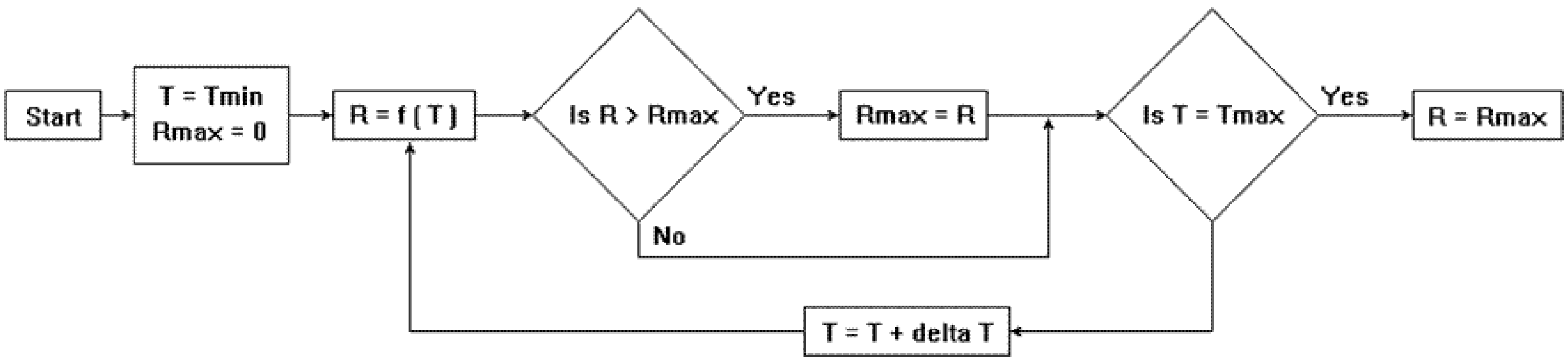
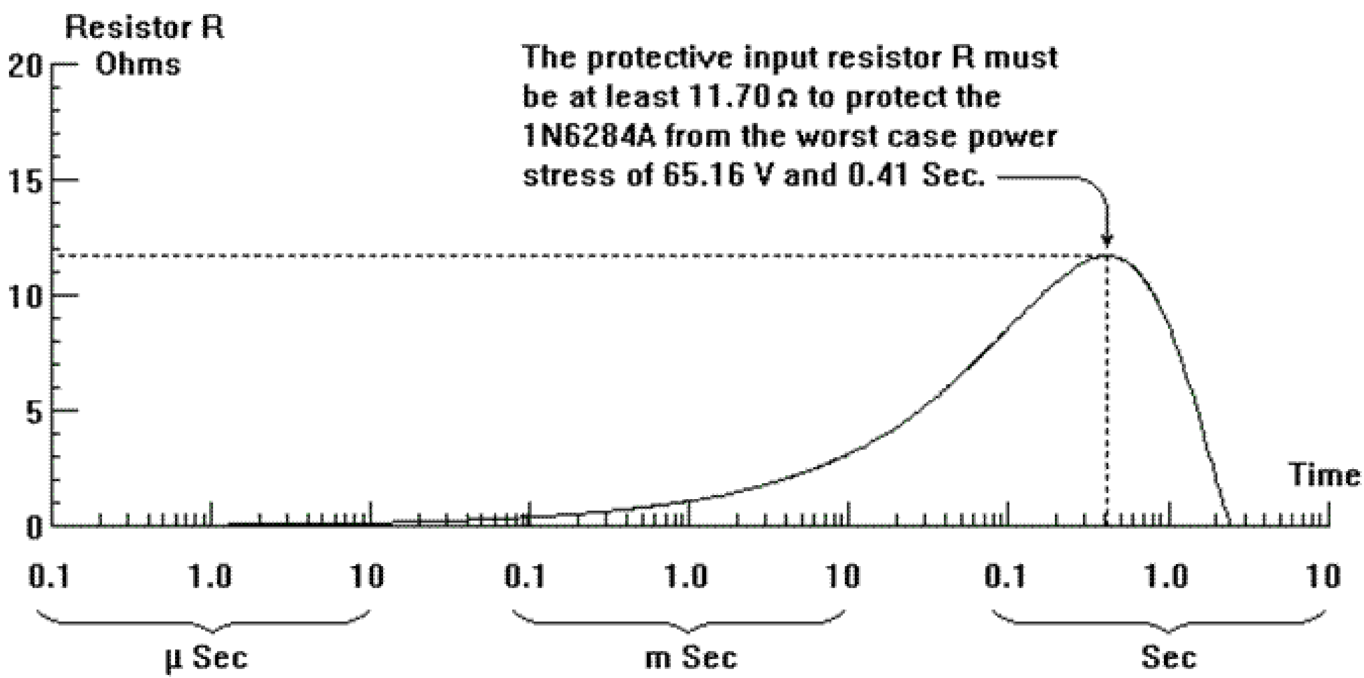
For T = 0 to Tmax, Find Rmax

We next take values of T from some minimum value, Tmin, to some maximum value, Tmax, and repeatedly calculate values of R while looking for the largest value of R than emerges from those calculations. The largest value of R can be called Rmax.



A Possibly Surprising Result

Finding the maximum value of the minimum resistance needed to protect the 1N6284A against transients per MIL-STD-704A, Figure 9, Curve 1.



The real threat is not the 80V maximum, but instead, somewhere around 65V.

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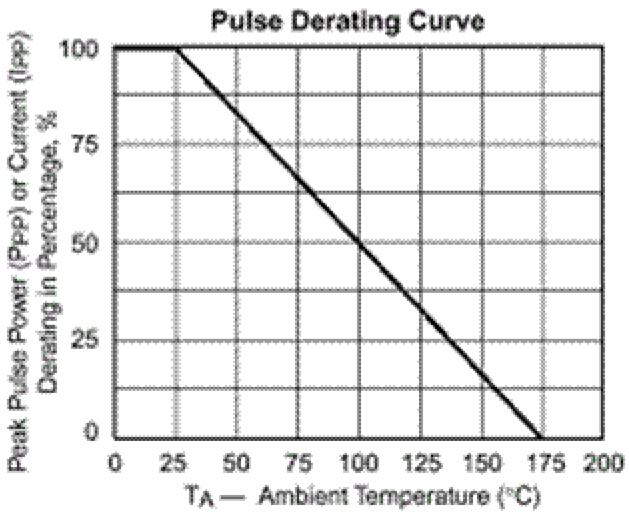
With Power Derating



Where we apply a derating factor ß, the power equation becomes:

$$P = ß \frac{K2}{T^{K1}}$$

At an ambient temperature of 100°C, the derating coefficient, ß, becomes 0.5 for which the required value of "R" must be increased.

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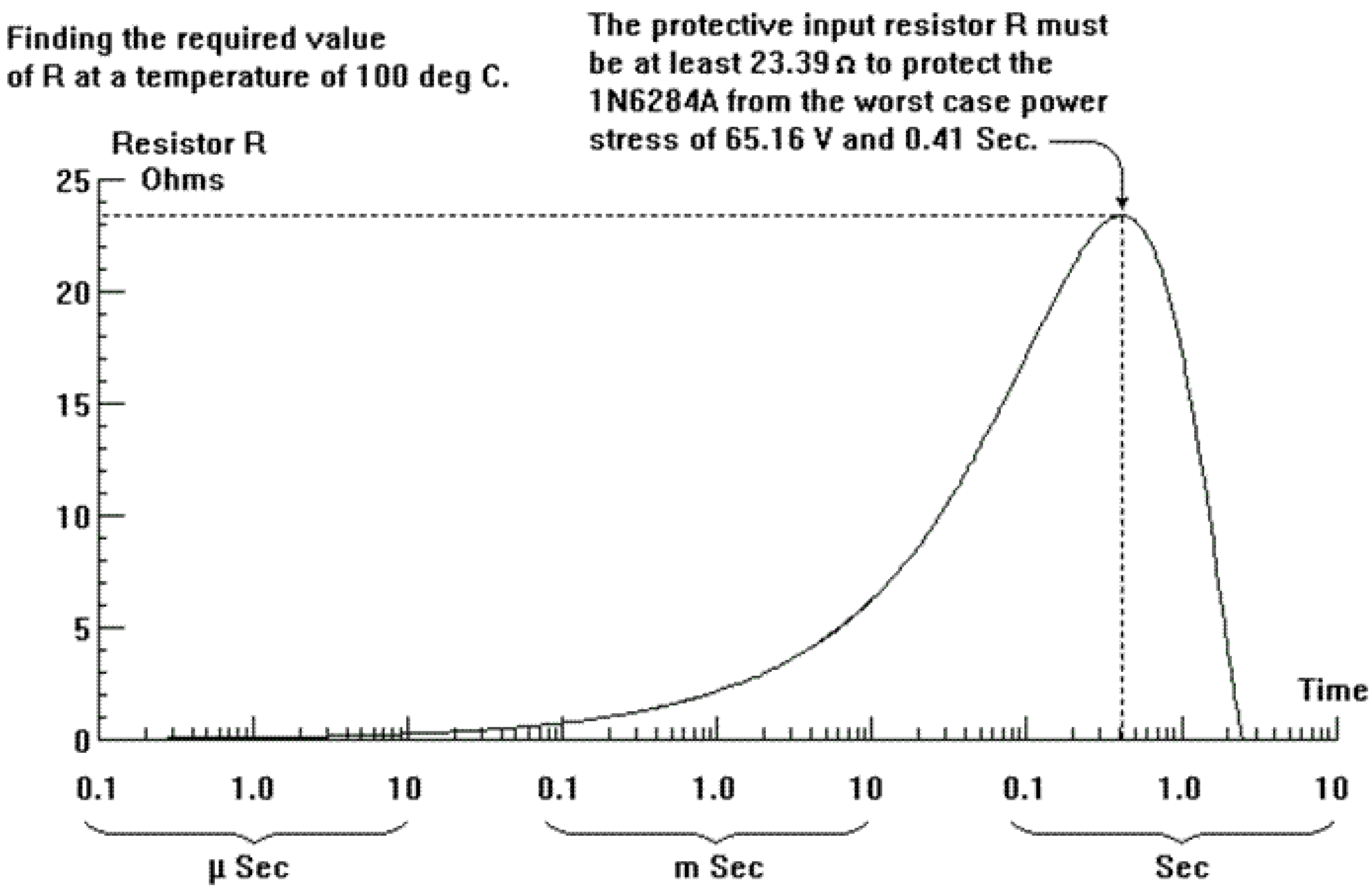
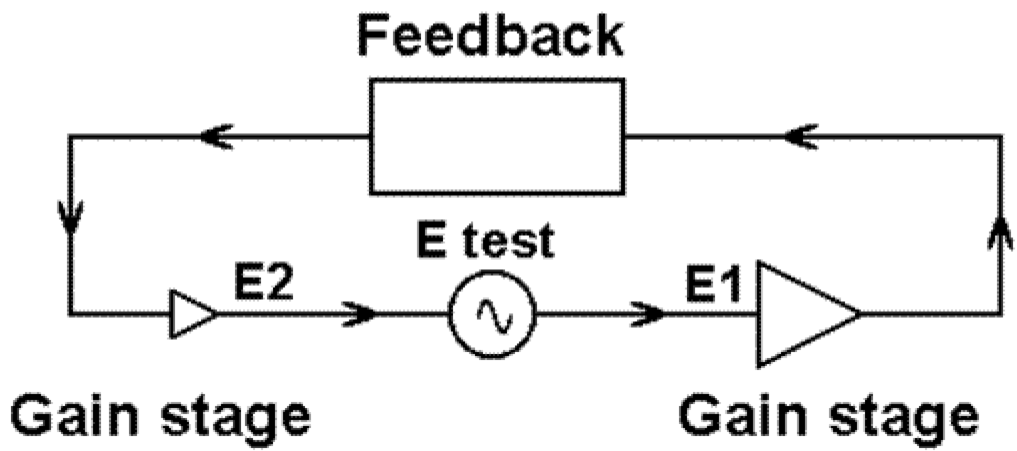
Diode Protection Resistance

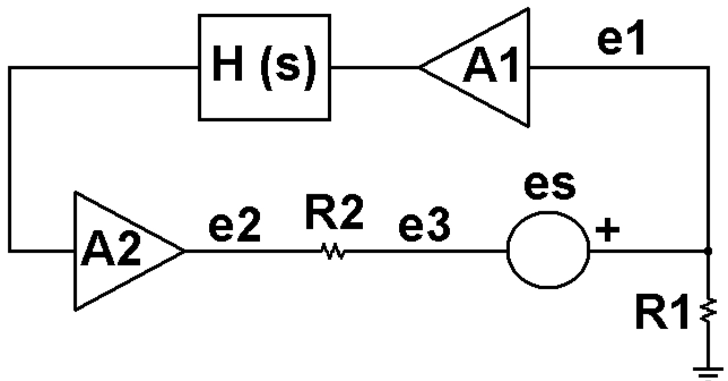


Measuring Loop Gain



Loop gain is measured by injecting a signal called E test and then measuring the ratio of signal E2 versus E1.

Measuring Loop Gain



$$\frac{(e2 - e3)}{R2} = \frac{e1}{R1}$$

Currents in R1 and R2 are equal.

$$\frac{e3}{R2} = \frac{e2}{R2} - \frac{e1}{R1} \;;\quad e3 = e2 - e1\,\frac{R2}{R1}$$

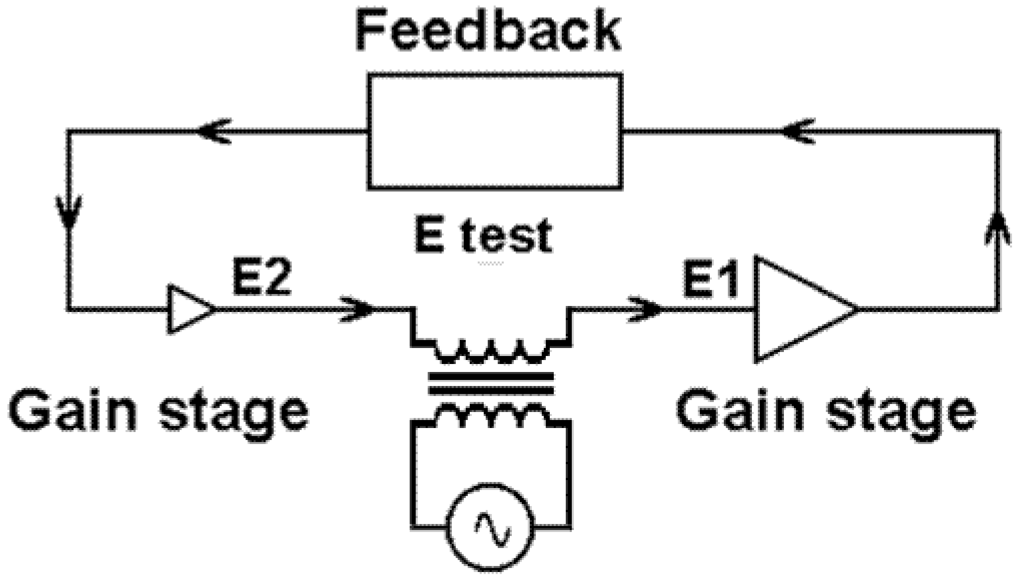
$$e3 = e1\ A1\ A2\ H(s) - e1\,\frac{R2}{R1}$$

$$\frac{e3}{e1} = A1\ A2\ H(s) - \frac{R2}{R1}$$

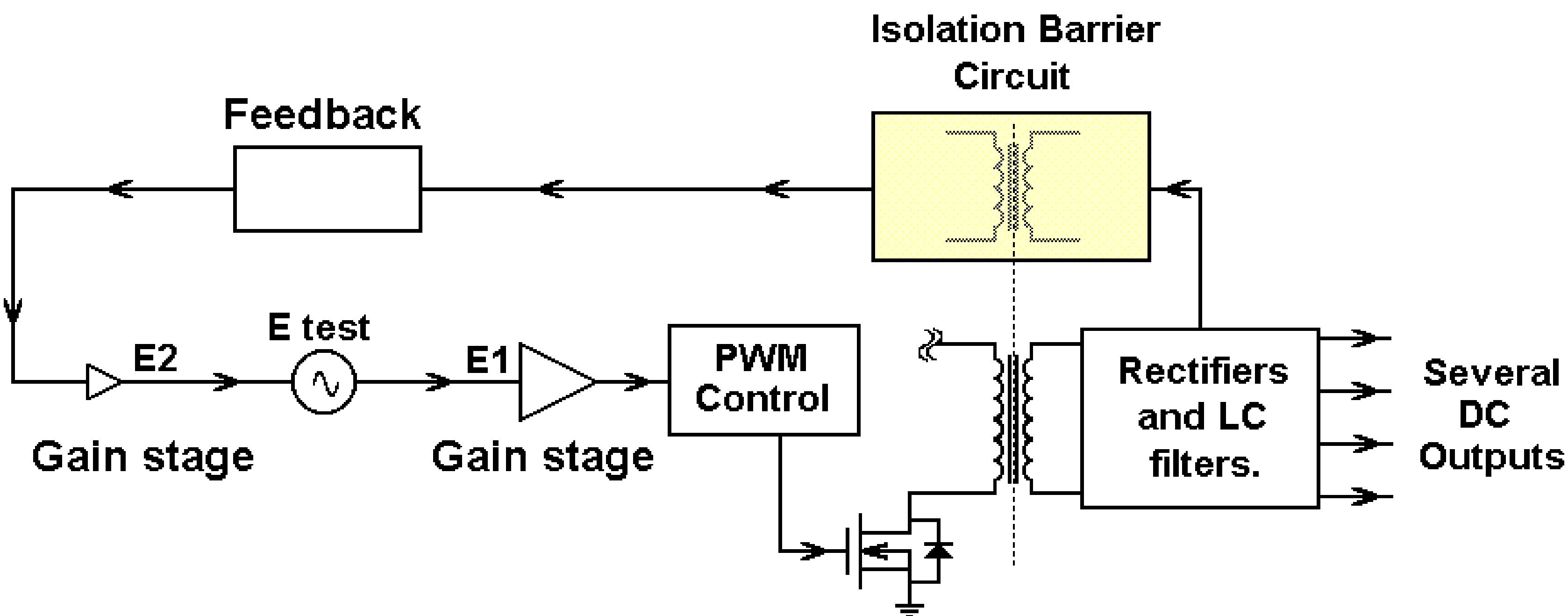
If R2 goes to zero, then e3/e1 is the loop gain, but if R2 is not zero, there is error in the measurement of loop gain.

Therefore, make sure that your test signal injection point has zero Thevenin impedance at the A2 stage.

Transformer Coupling of “E test”



Power Supply Loop Gain



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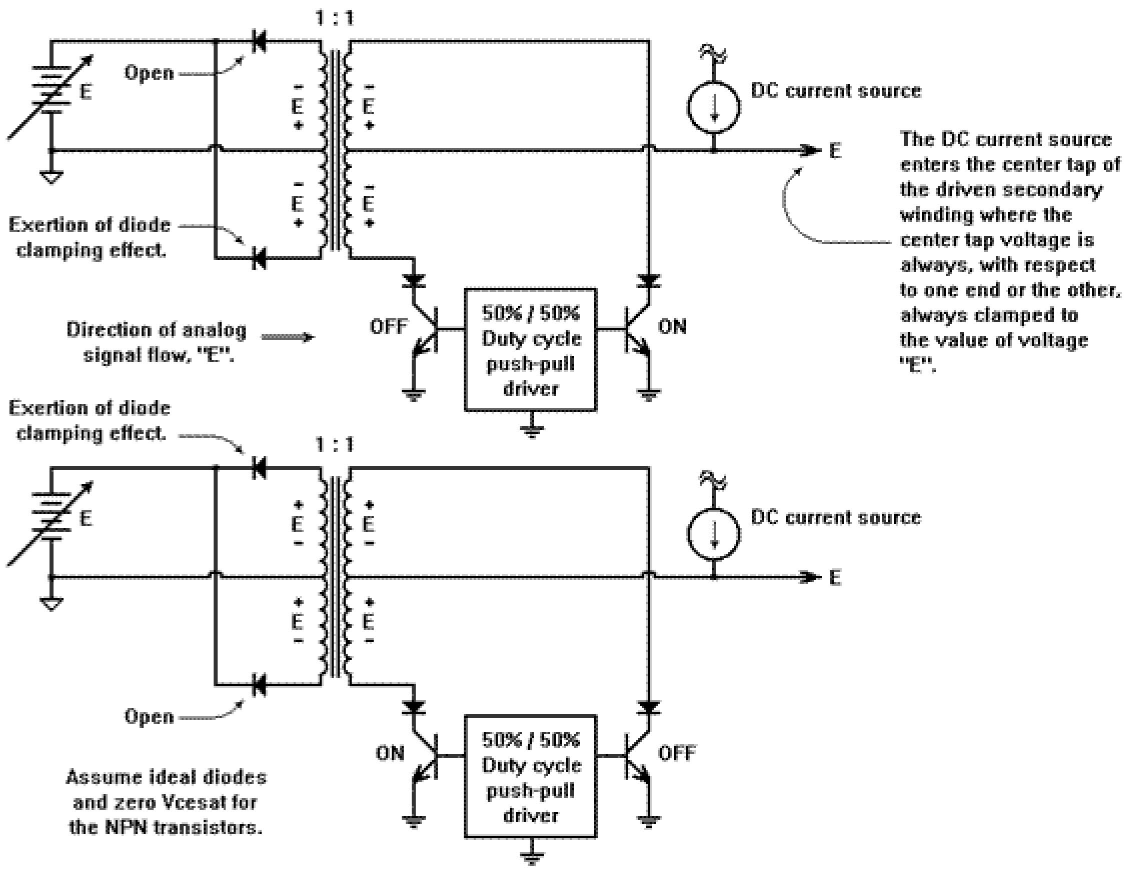
Isolation Barrier Circuit



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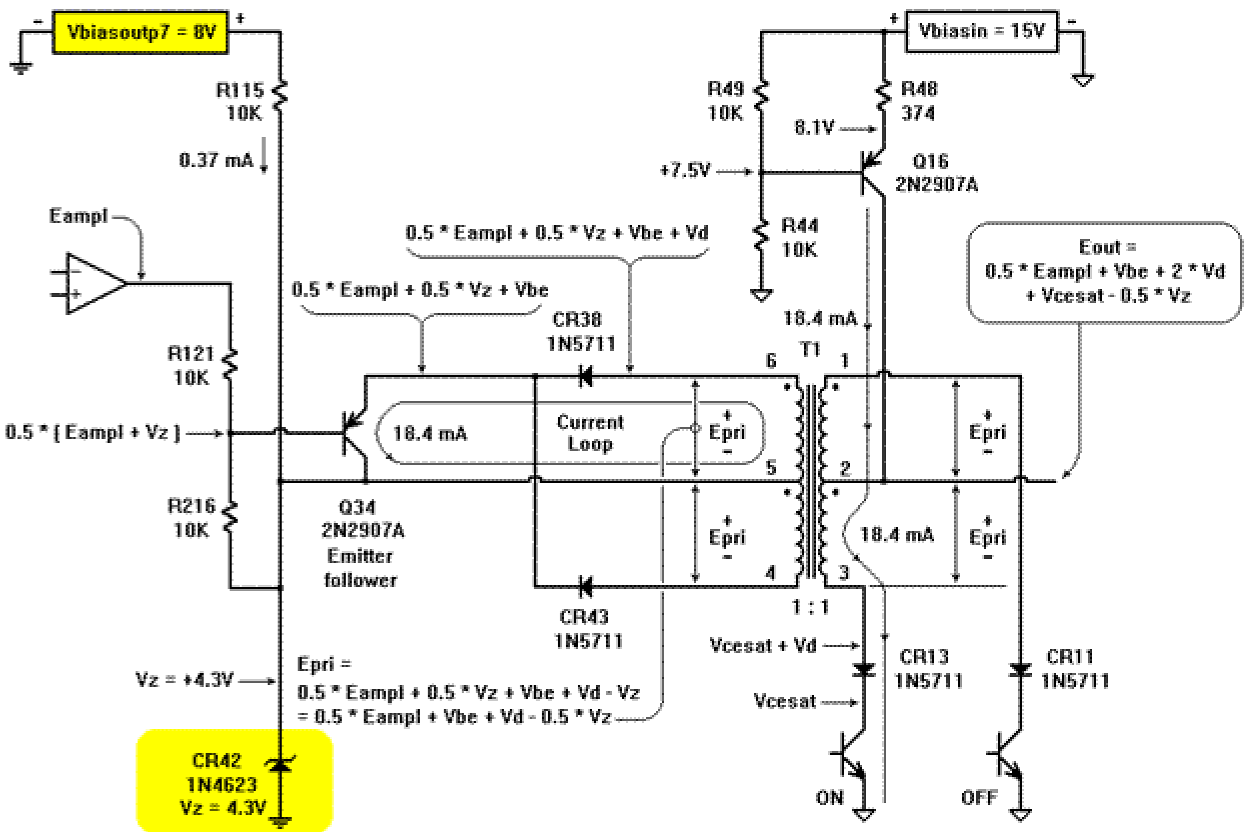
Isolation Barrier Circuit



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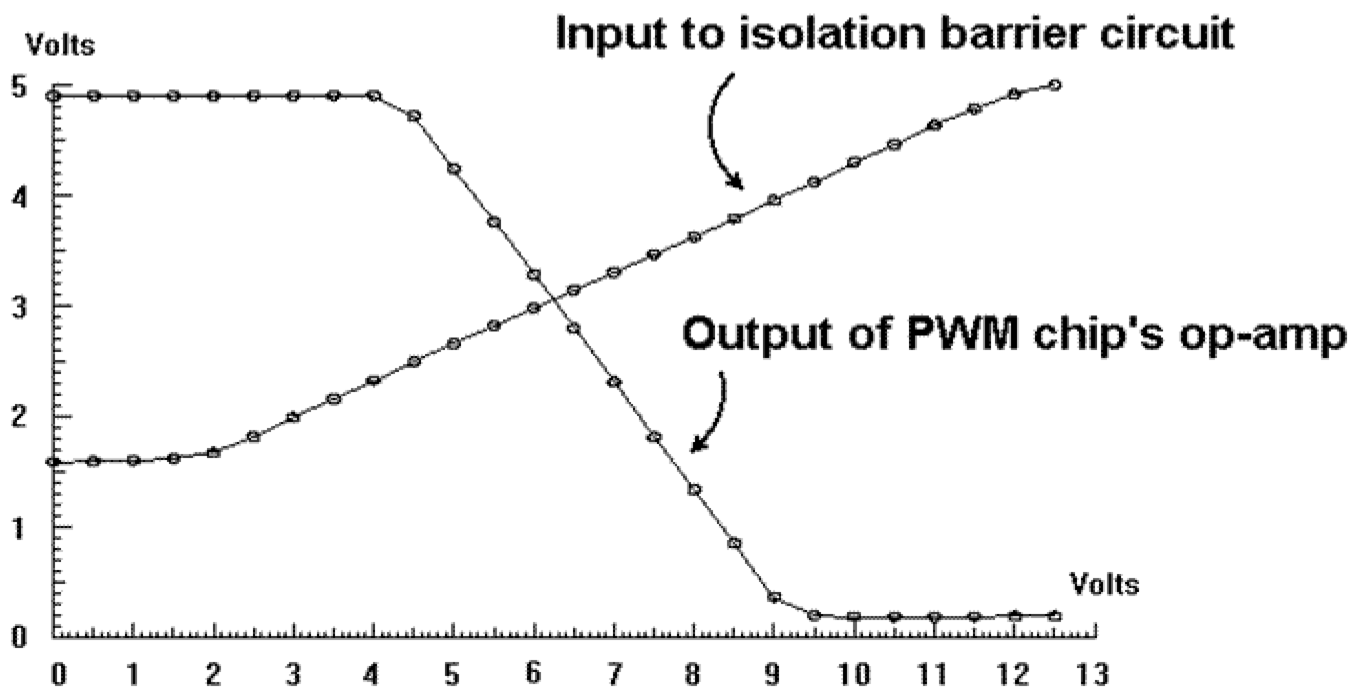
Isolation Barrier Circuit



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Agilent 4395A Analyzer

The RF output port gives a swept frequency signal of selectable amplitude.

The input ports have a Zin = 50 Ohms, but there are high-Z probes that can be used as buffers.

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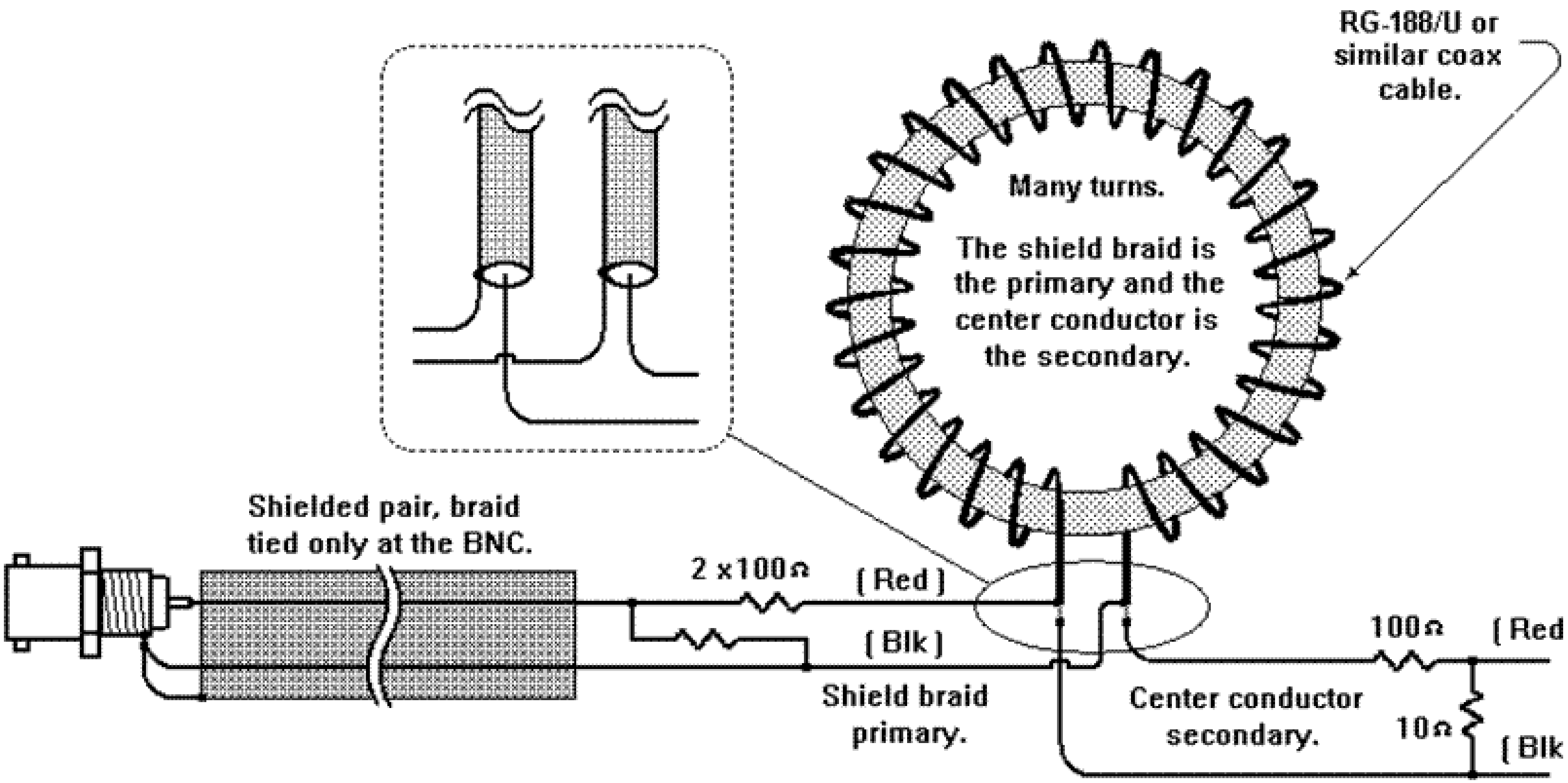
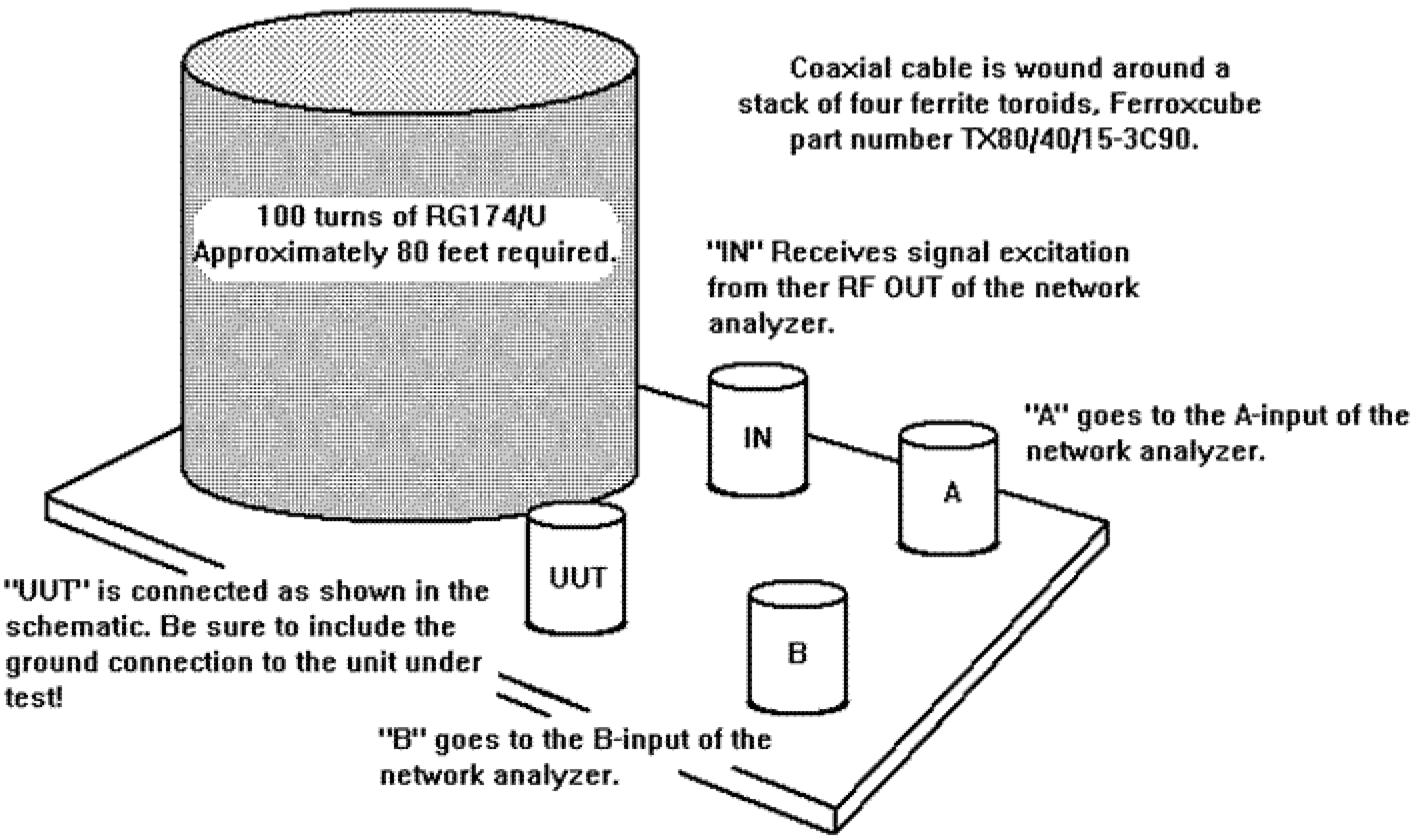
Making The Transformer



Making The Transformer



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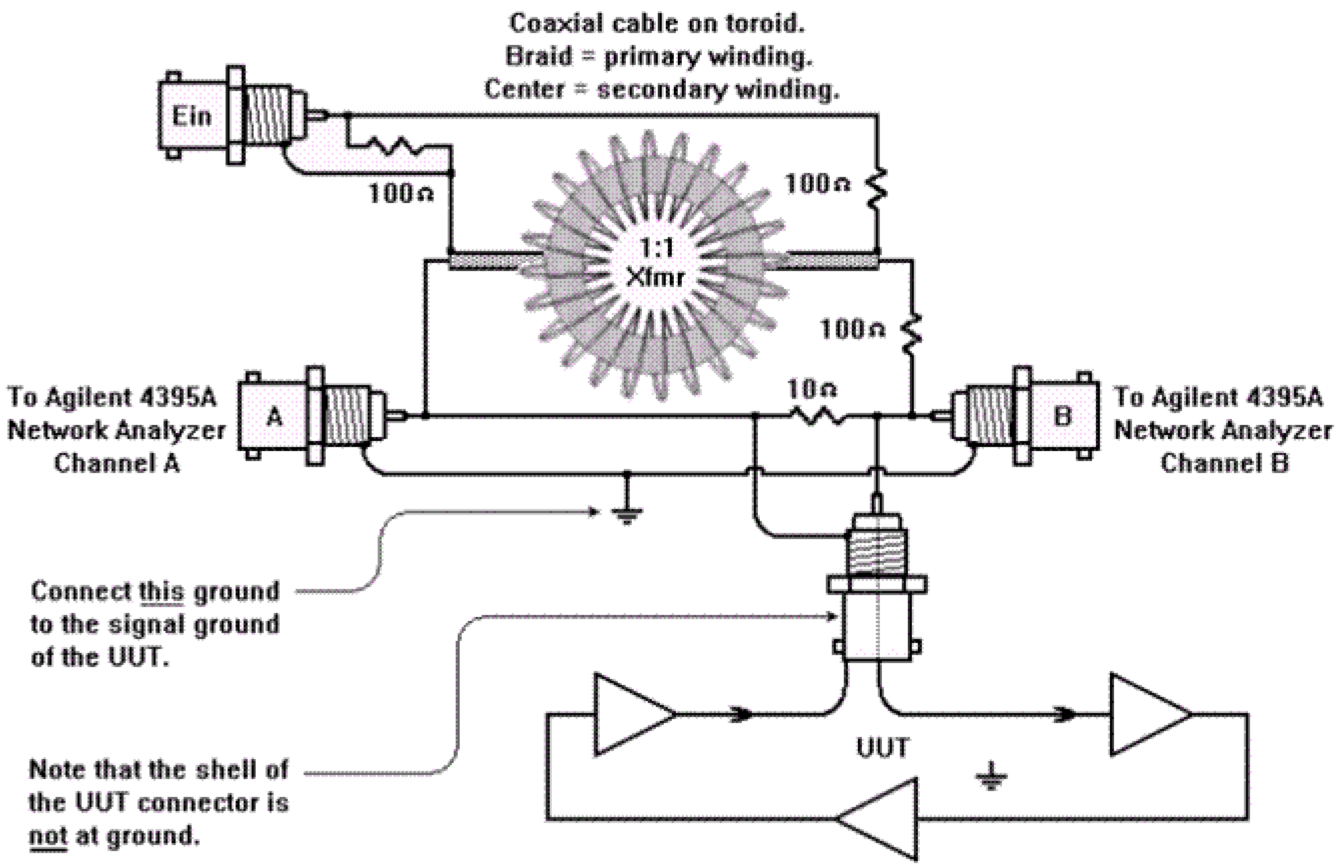
Gain Measurement Set-Up



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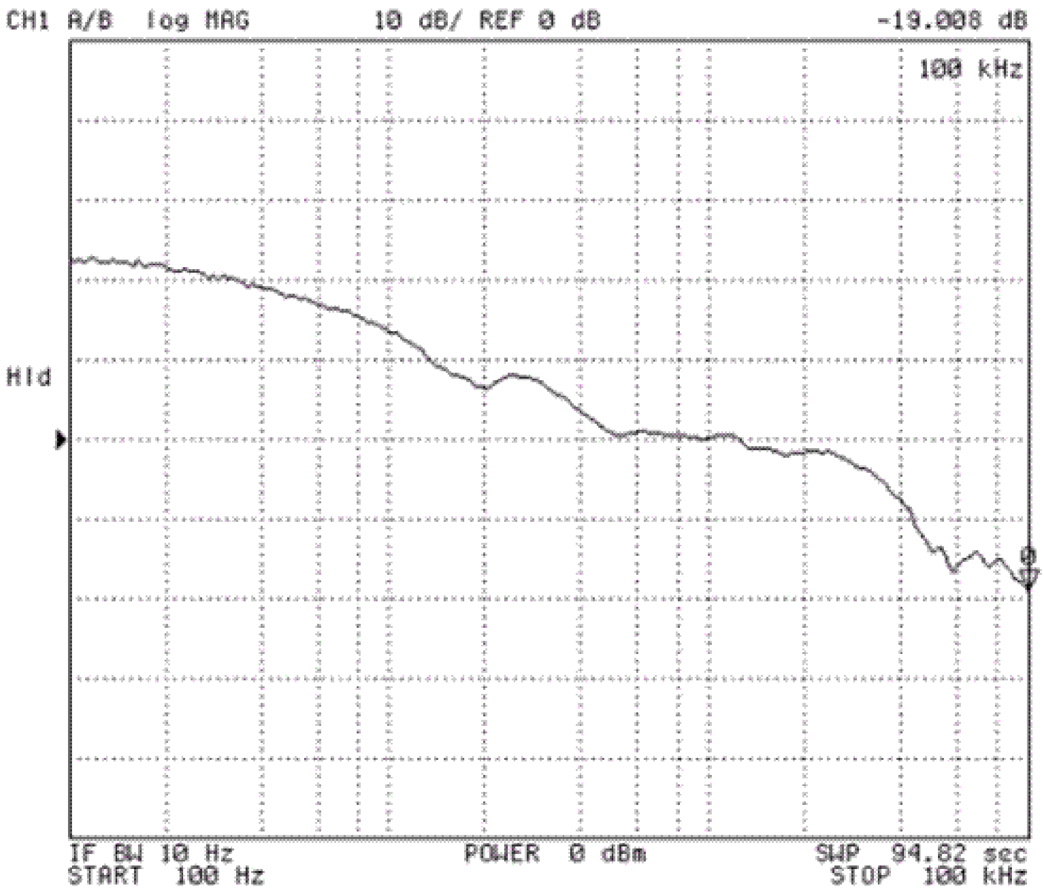
Gain plot with 0 dBm



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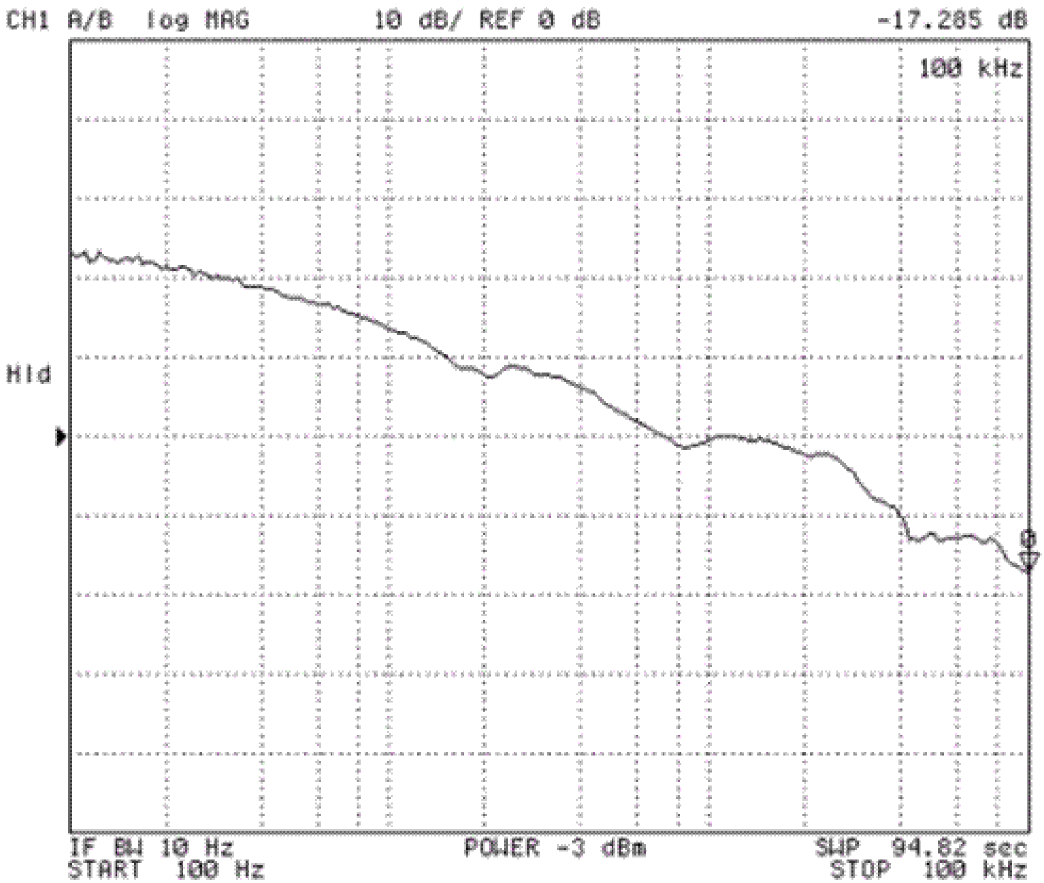
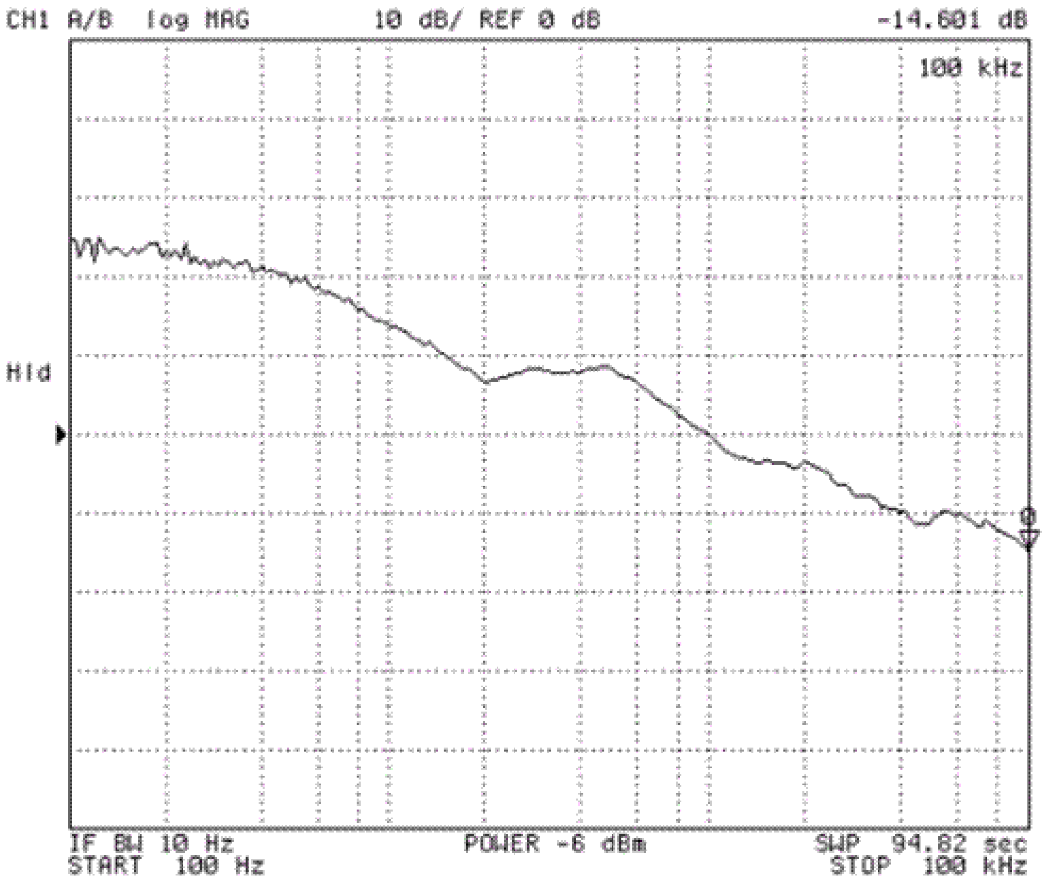
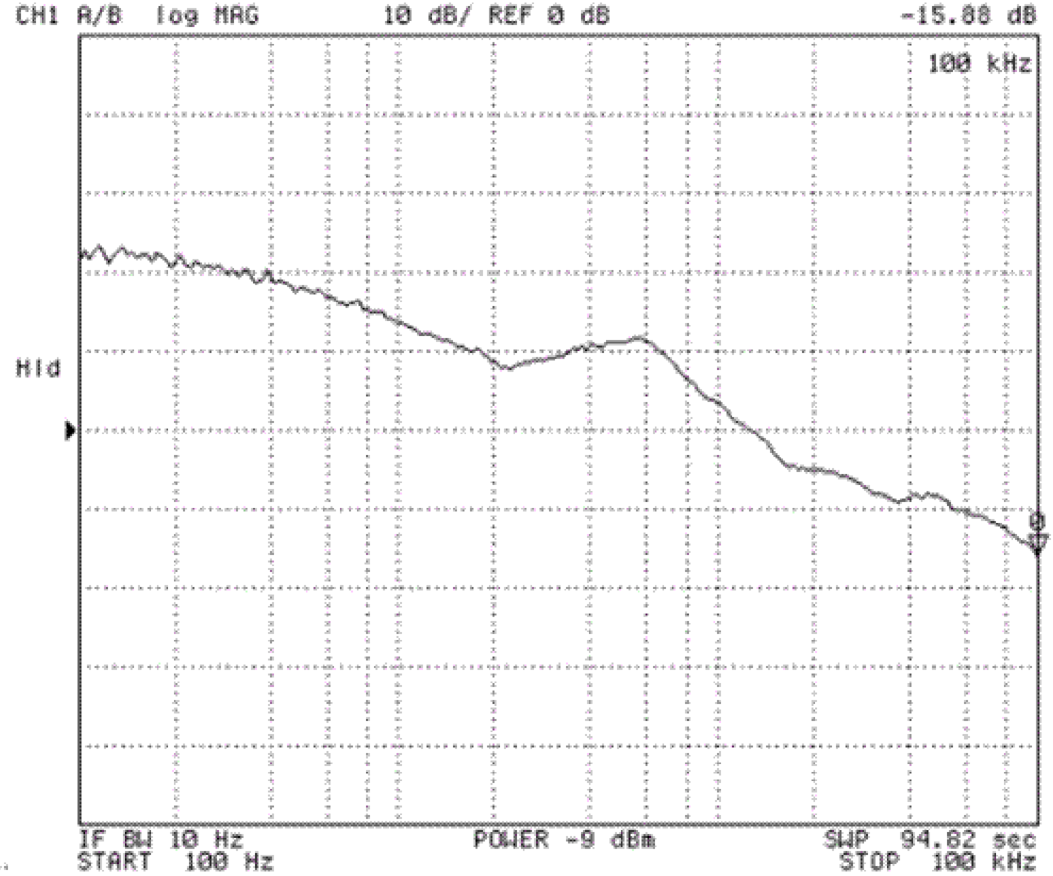
Gain plot with –3 dBm



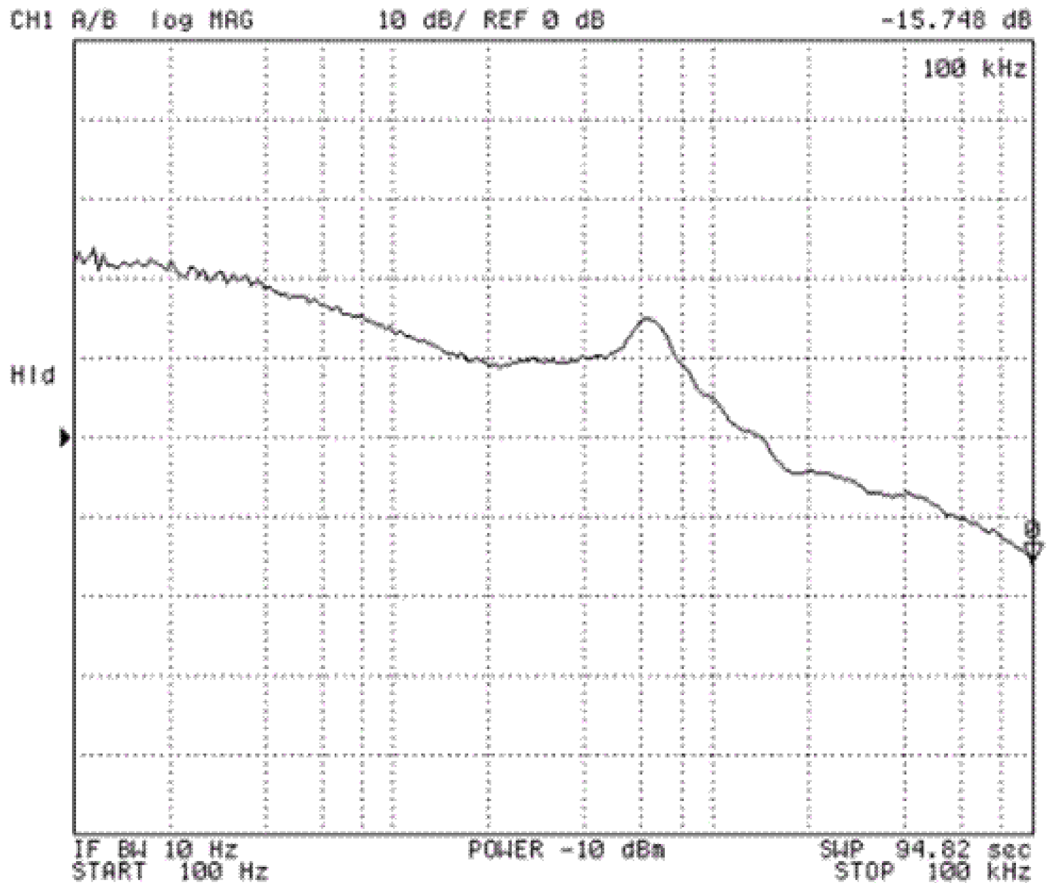
Gain plot with –6 dBm



Gain plot with –9 dBm



Gain plot with –10 dBm



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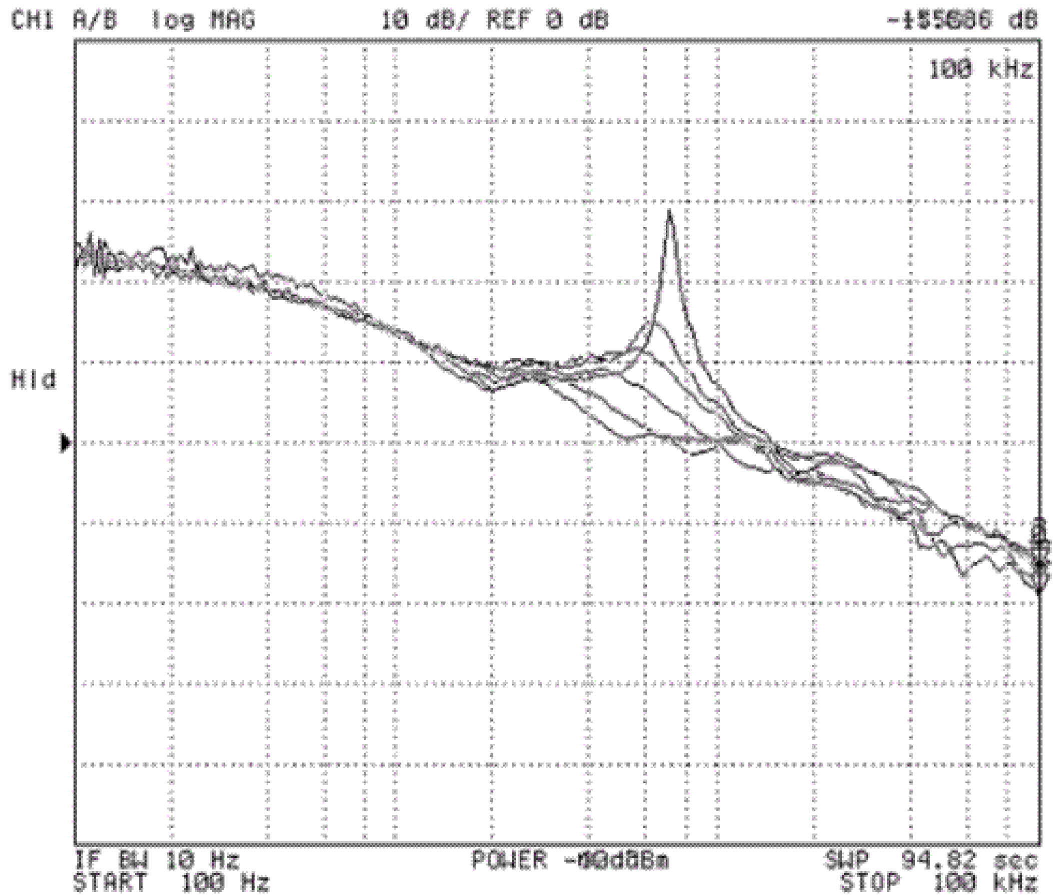
Gain plot with –12 dBm

The whole bunch of them.



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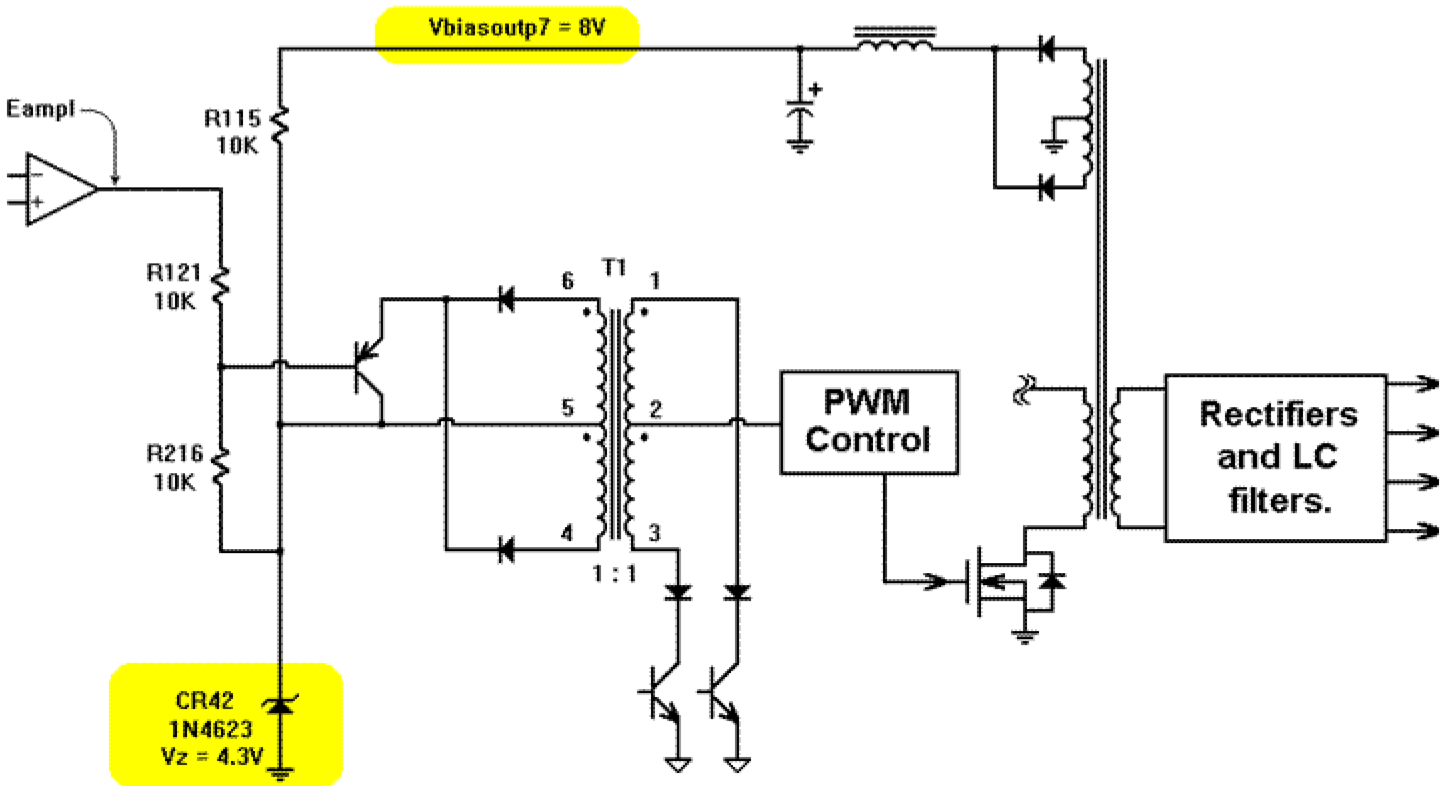
Bias for the primary side.



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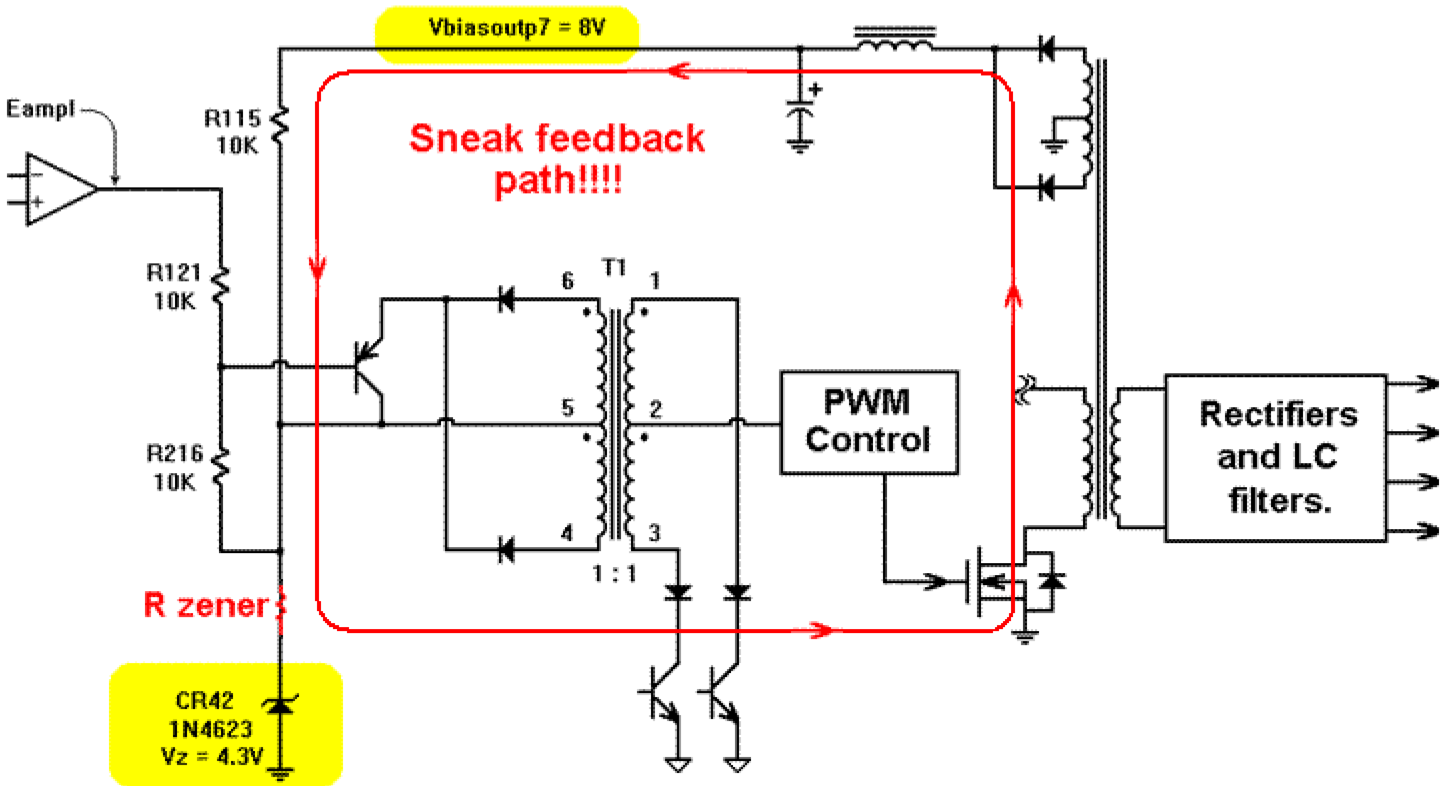
The culprit zener!



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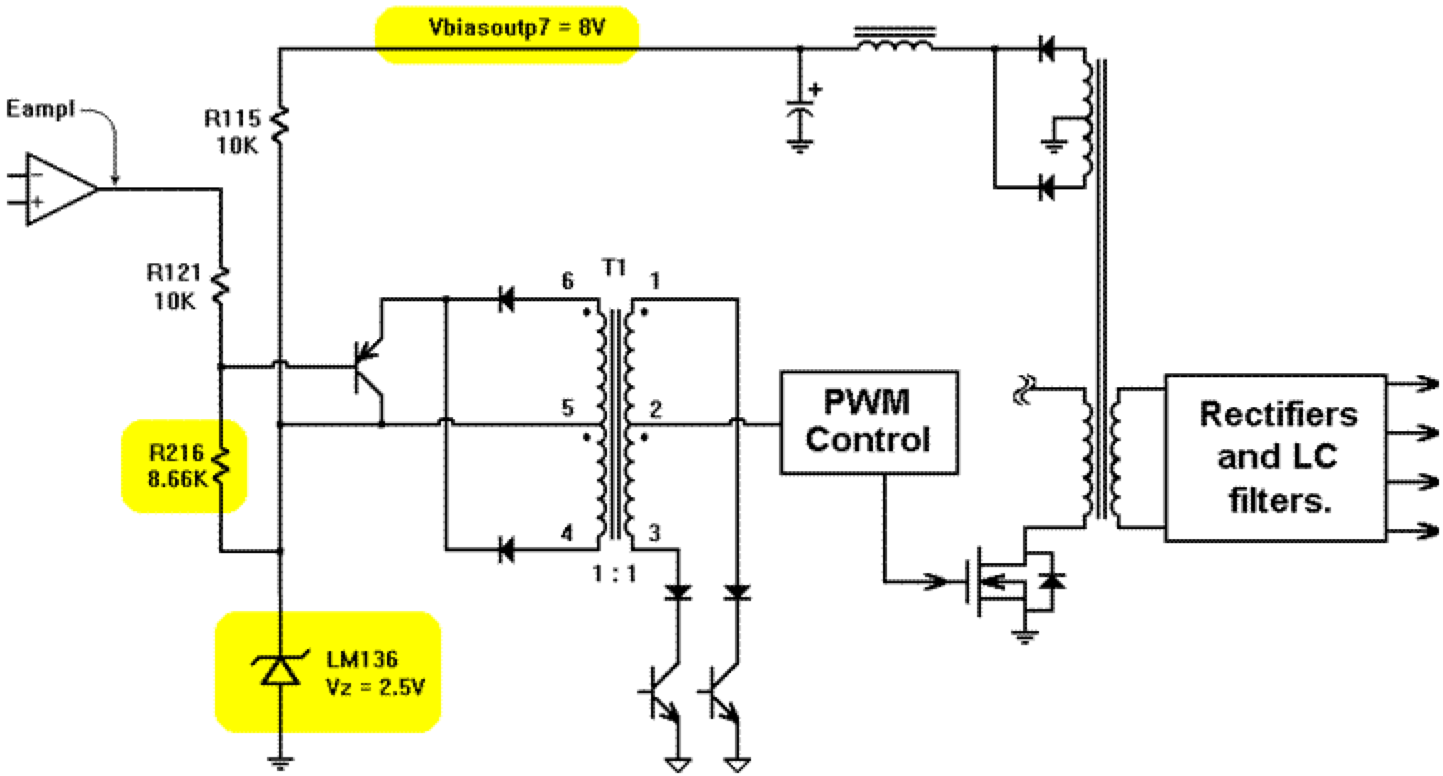
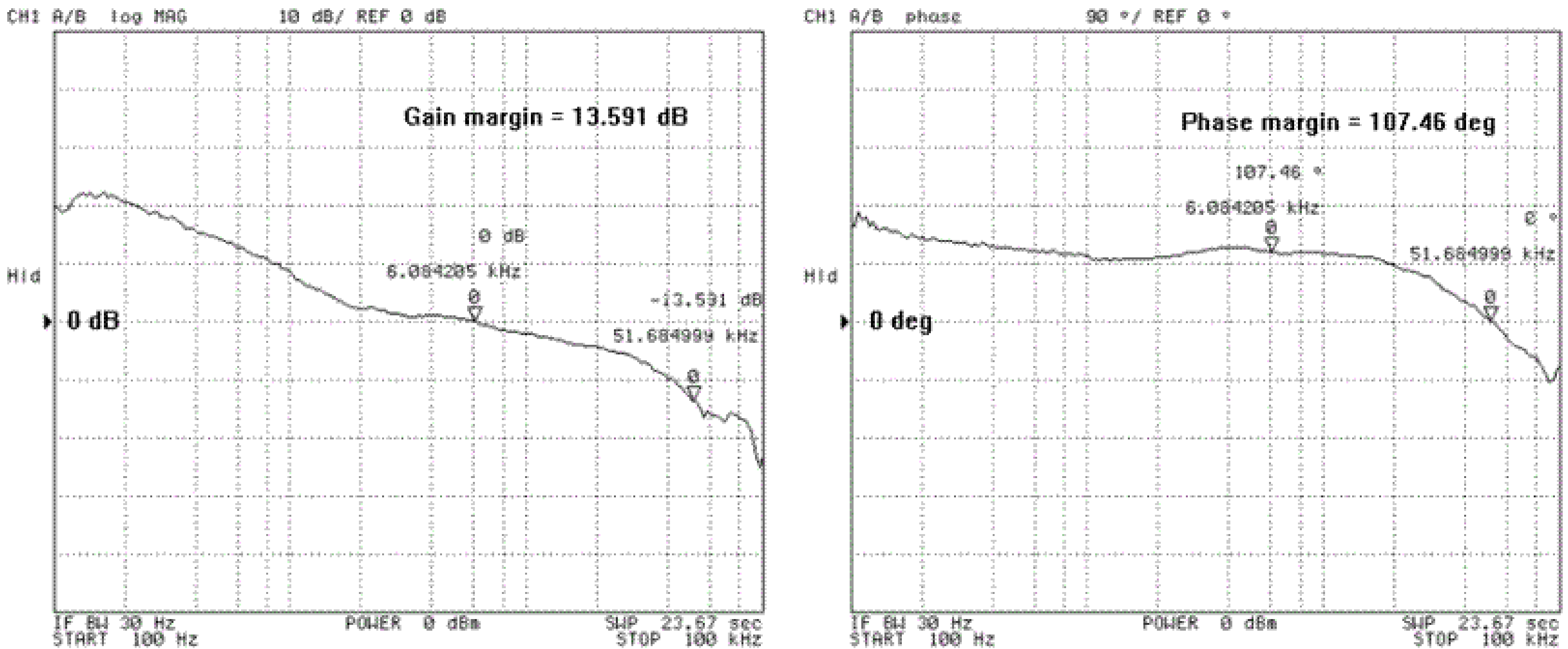
The remedy



Stabilized gain and phase



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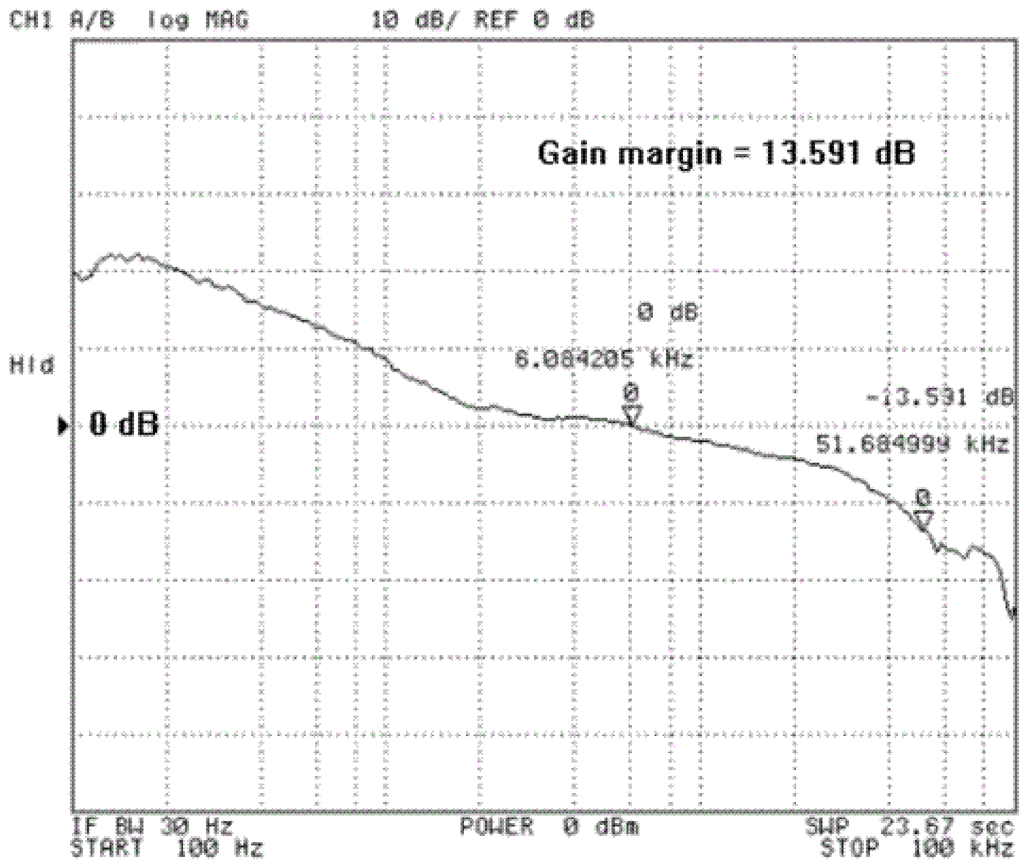
Stabilized gain



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