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RF Power Amplifier Design Using LDMOS Semiconductors

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Presentation Outline

- Introduction
- The Market
- Amplifier Concepts
- PA Fundamentals
- Digital Modulation Characterization
- Inside The RF Power Transistor
- Transistor Characteristics
- Pulsed Applications
- Application Circuits
- Thermal Resistance
- Reliability / Electro migration

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Market

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Market

The consumer wants:
- Higher data rates (wireless internet/video/e-mail)

The OEM/Service Provider wants:
- Higher network capacity
- Higher data rates
- More efficient amplifiers (electricity bill, heat generation)
- More quiet amplifiers (environmental noise; “fan-less”)
- Cheap solutions
- Small solutions

The design community of these base stations wants/needs:
- More integrated functionality / Building blocks / Easy of use
- Small solutions
- High efficiency / high gain / highly linear transistors
- Low cost

Market

- **Higher Subscriber Capacity**
  - Digital Modulation Techniques
    - Multiple users per carrier
  - Multi Carrier Applications
- **Higher data rate capacity**
  - To support wireless e-mail, wireless video, wireless internet access etc.
    - More bandwidth
- **All leads to digital wireless networks (GSM, Edge GSM, CDMA, UMTS/W-CDMA) which requires linear PA's**

Higher data rates and higher capacity

- Can be achieved by more complex modulation techniques.
- Can be achieved by "combining" or "using" multiple voice channels simultaneously.
- Higher data rates require more bandwidth.
  - Examples:
    - GSM carrier bandwidth = 200kHz
    - CDMAone carrier bandwidth = 1.2288MHz
    - UMTS carrier bandwidth = 3.84MHz

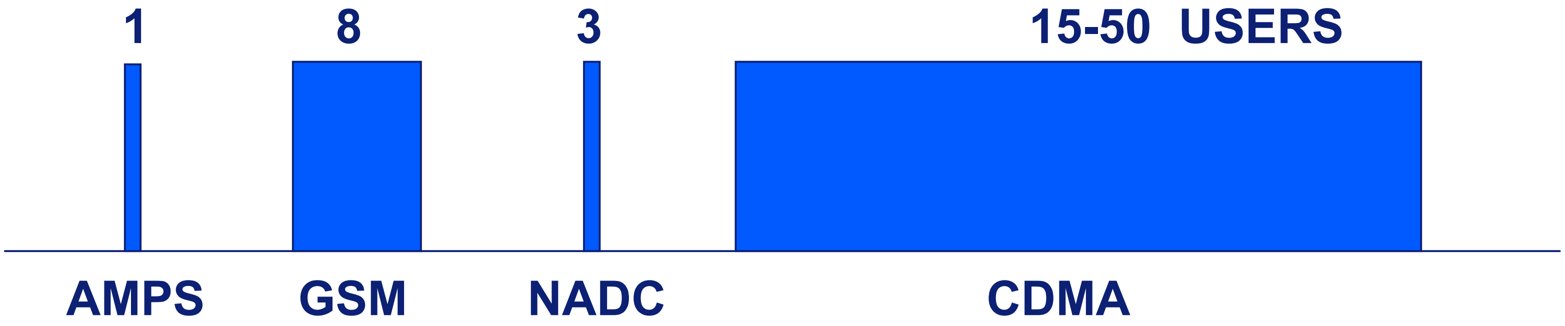
Higher Subscriber Capacity
Higher Data Rate Capacity

It is all about …….

Multi Carrier Applications
and/or
Digital Modulation Techniques
which puts a strain on …
Amplifier Linearity

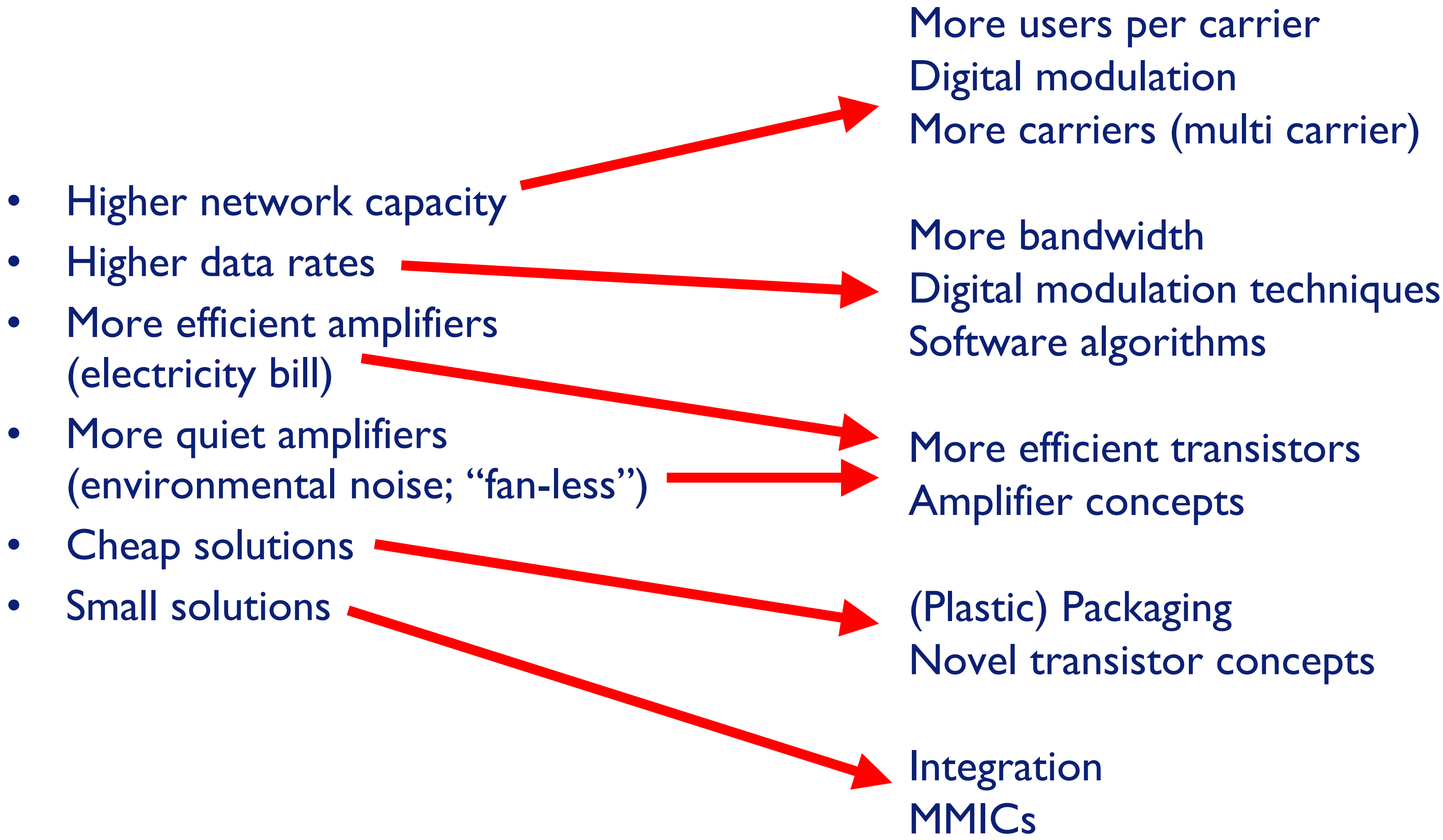
Higher Subscriber Capacity

System Standard	Users Per Carrier	Modulation	Channel Spacing
AMPS	1	FDMA	30 kHz
GSM	8	GMSK	200 kHz
NADC (IS-54)	3	$\pi/4$ DQPSK	30 kHz
CDMA	15-50	QPSK	1.25 MHz
W-CDMA	196	QPSK	3.84MHz



Frequency Spectrum

Market



- Higher network capacity
- Higher data rates
- More efficient amplifiers (electricity bill)
- More quiet amplifiers (environmental noise; “fan-less”)
- Cheap solutions
- Small solutions

More users per carrier
Digital modulation
More carriers (multi carrier)

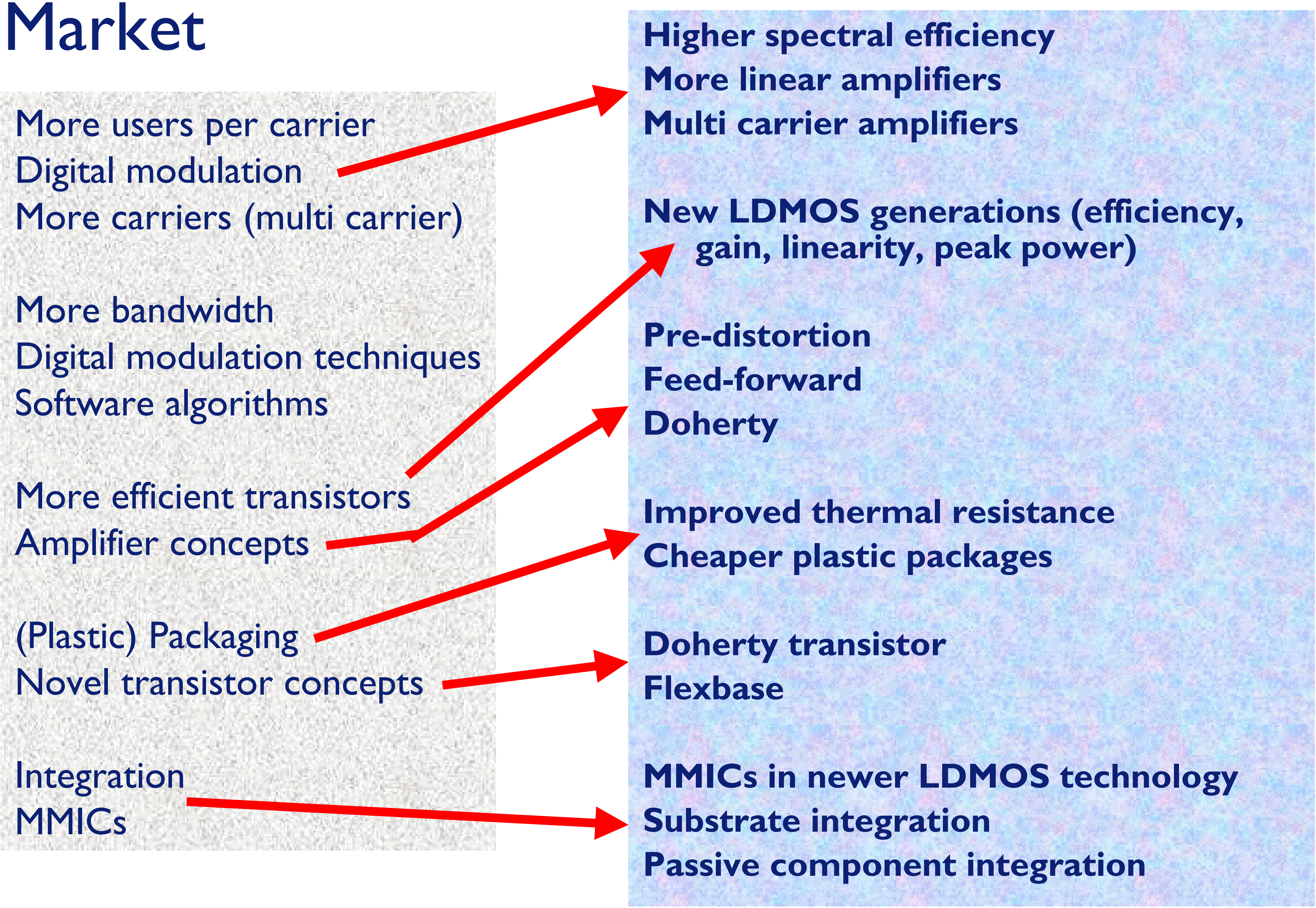
More bandwidth
Digital modulation techniques
Software algorithms

More efficient transistors
Amplifier concepts

(Plastic) Packaging
Novel transistor concepts

Integration
MMICs

Market



More users per carrier
Digital modulation
More carriers (multi carrier)

More bandwidth
Digital modulation techniques
Software algorithms

More efficient transistors
Amplifier concepts

(Plastic) Packaging
Novel transistor concepts

Integration
MMICs

Higher spectral efficiency
More linear amplifiers
Multi carrier amplifiers

New LDMOS generations (efficiency, gain, linearity, peak power)

Pre-distortion
Feed-forward
Doherty

Improved thermal resistance
Cheaper plastic packages

Doherty transistor
Flexbase

MMICs in newer LDMOS technology
Substrate integration
Passive component integration

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Amplifier Concepts

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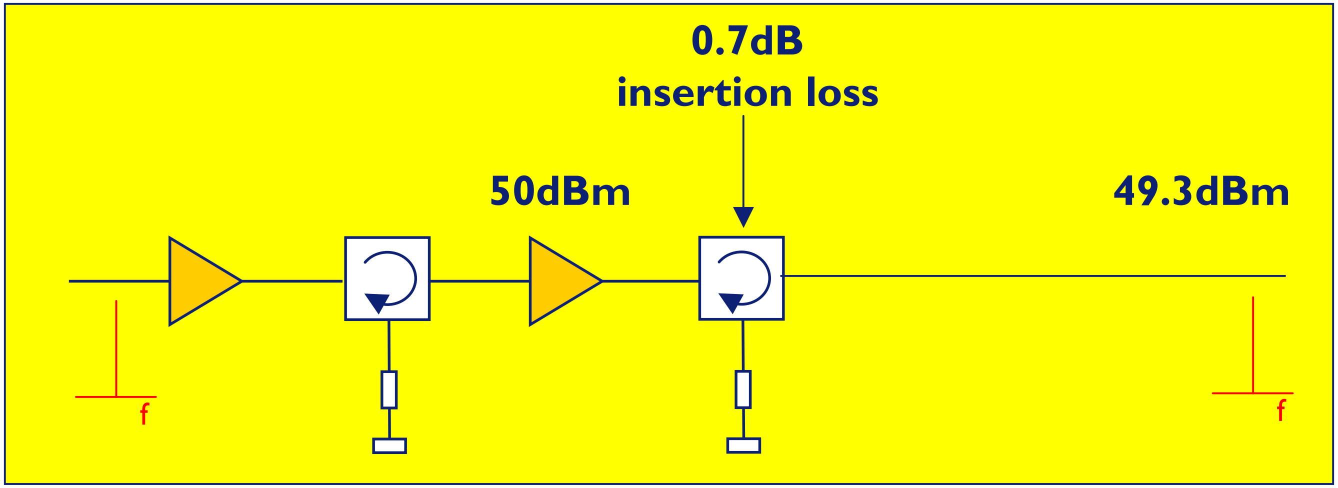
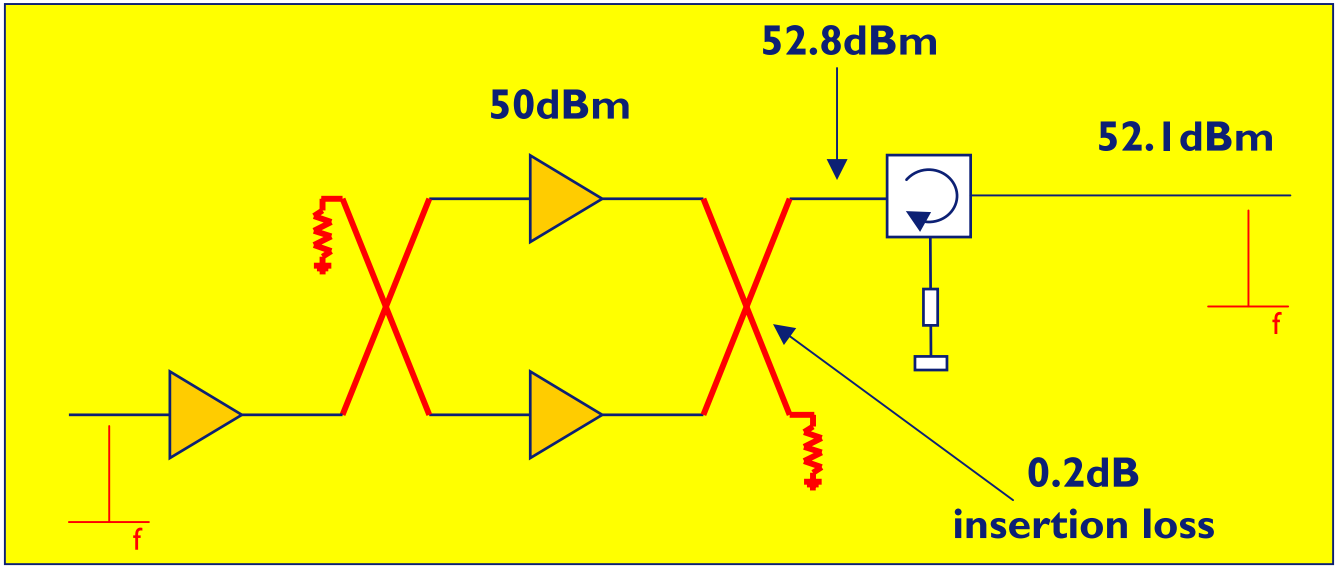
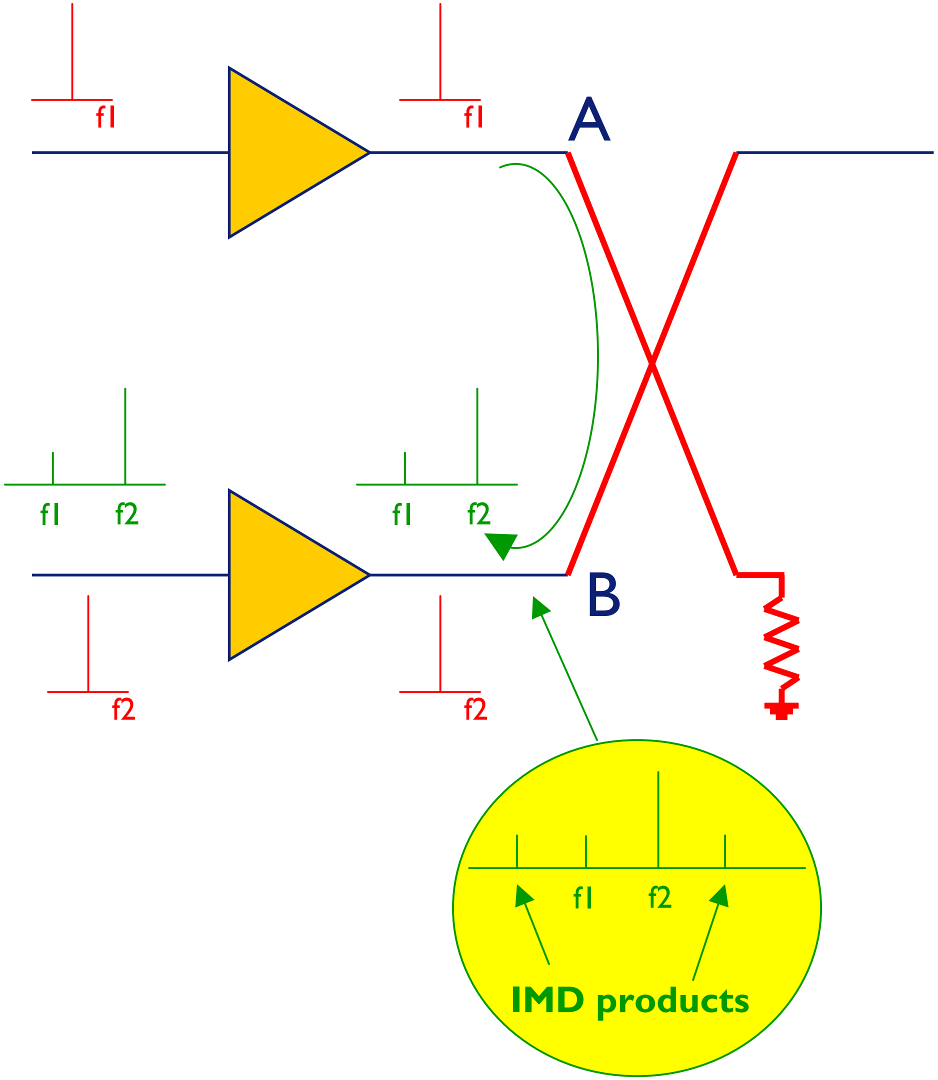
Single carrier amplifiers

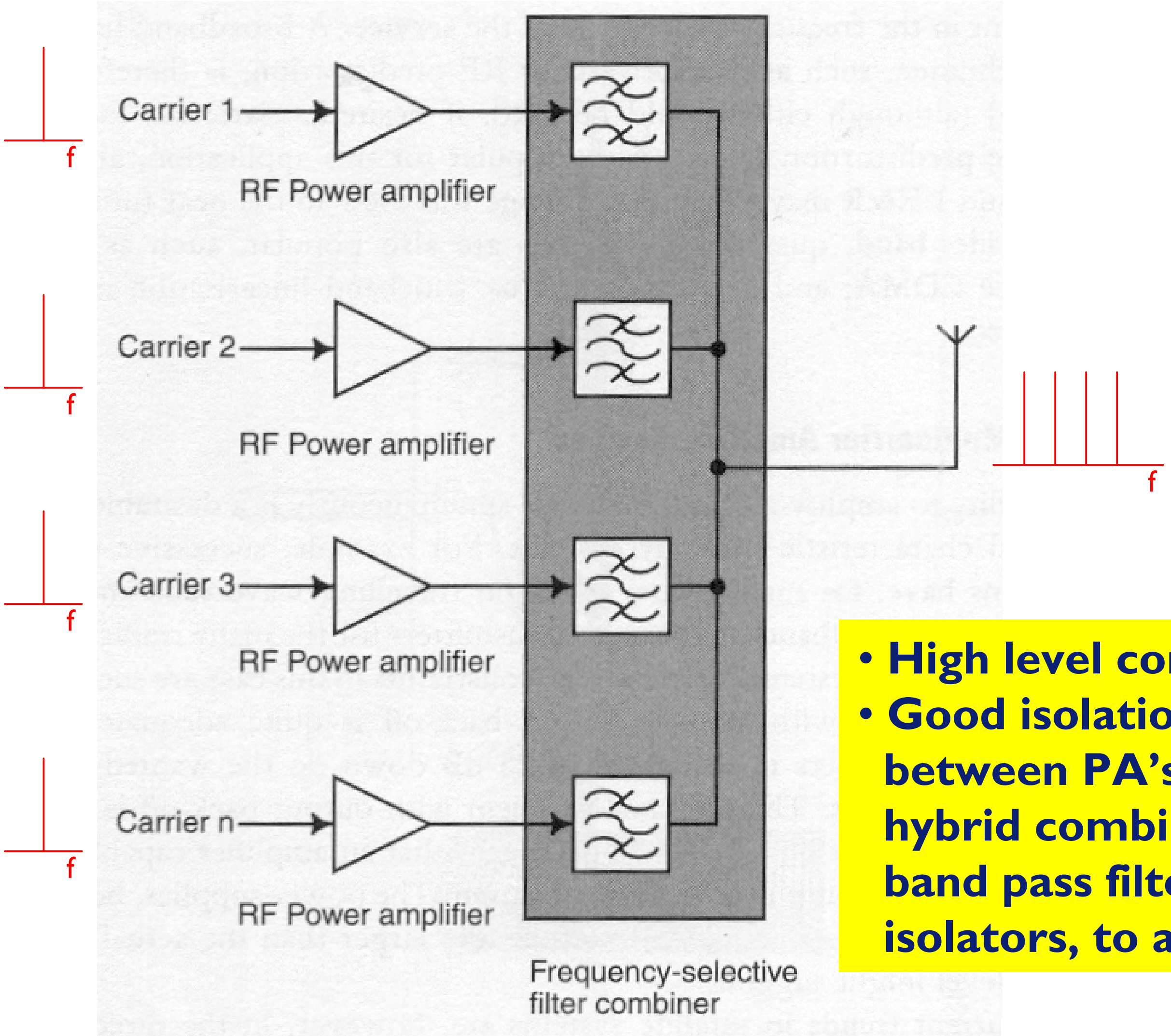




Reverse intermodulation

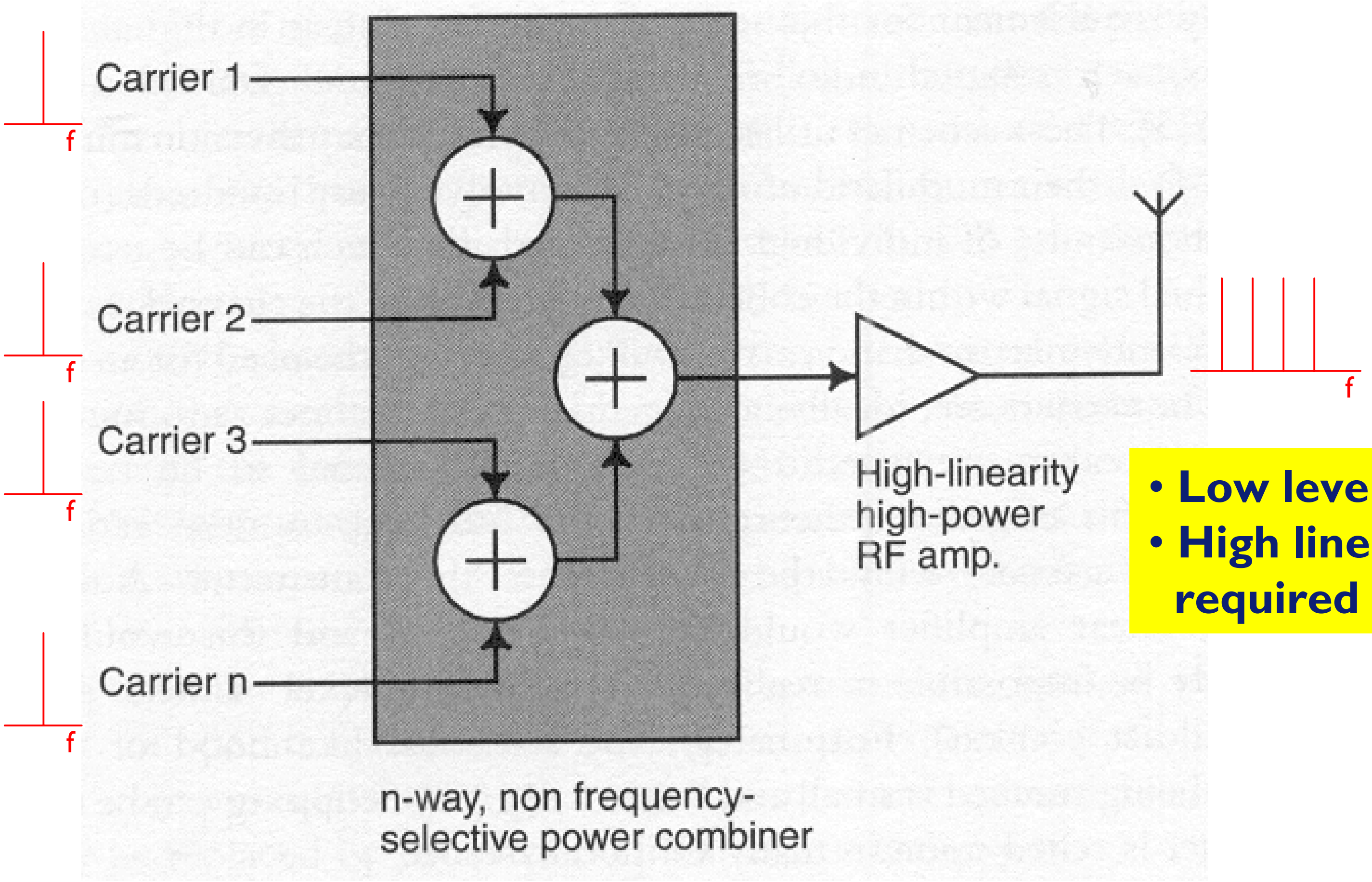


Combined single carrier amplifiers



- **High level combining**
- **Good isolation required between PA's with 3dB hybrid combiners, band pass filters and isolators, to avoid IMD.**

Multi carrier power amplifiers

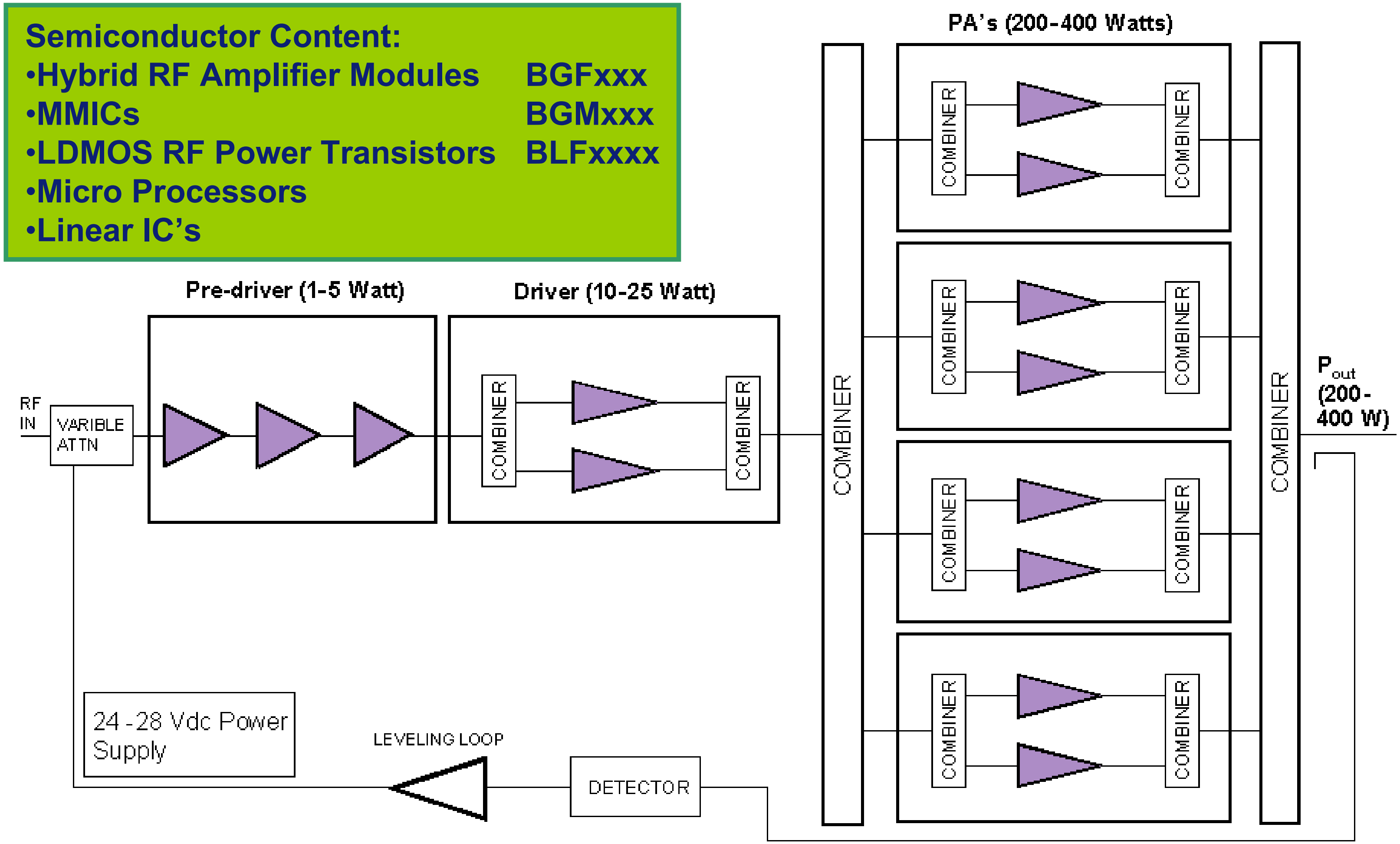


- Low level combining
- High linear PA required to avoid IMD

Multi Carrier Power Amplifier (MCPA)

Semiconductor Content:

•Hybrid RF Amplifier Modules	BGFxxx
•MMICs	BGMxxx
•LDMOS RF Power Transistors	BLFxxxx
•Micro Processors	
•Linear IC’s	



Peak Power in an MCPA

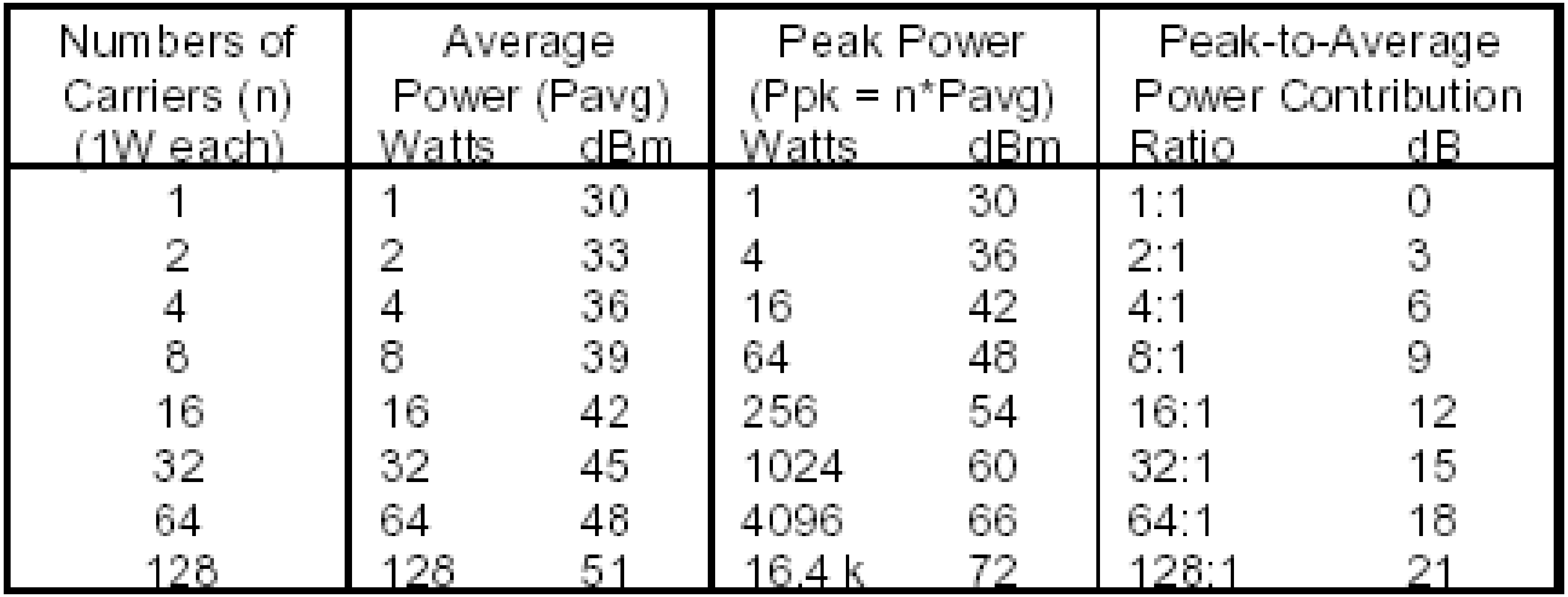
- In multi carrier amplifiers, the maximum peak power that occurs, when all carriers are phase aligned, can be expressed as:

$$P_{peak} = P_{average\,(all\ carriers\ combined)} \cdot n$$

$$where\ \ n\ \ is\ \ the\ \ number\ \ of\ \ carriers$$

- For instance: In case of two 10W carriers, the average power is 20W, the peak power is 40W (i.e. 3dB above $P_{average}$ of all carriers combined and 6dB above $P_{one\text{-}carrier}$)
- The above is valid for CW carriers. For digital modulated signal, the relation is much more complex and outside the scope of this training.

Peak Power in an MCPA

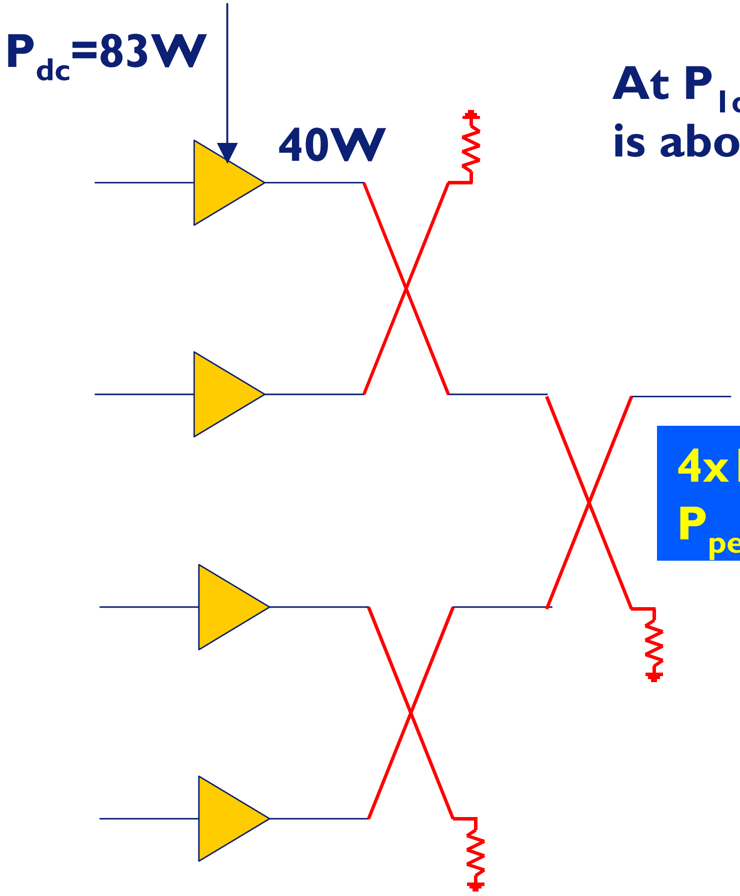


Numbers of Carriers (n) (1W each)	Average Power (Pavg)		Peak Power (Ppk = n*Pavg)		Peak-to-Average Power Contribution	
	Watts	dBm	Watts	dBm	Ratio	dB
1	1	30	1	30	1:1	0
2	2	33	4	36	2:1	3
4	4	36	16	42	4:1	6
8	8	39	64	48	8:1	9
16	16	42	256	54	16:1	12
32	32	45	1024	60	32:1	15
64	64	48	4096	66	64:1	18
128	128	51	16.4 k	72	128:1	21

Efficiency SCPA vs. MCPA

- Theoretical example
- Let’s assume we have four CW carriers with an output power of 10W each at the antenna of a base station.
- We can use two configurations:
  - four SCPA, combined with 3dB hybrids
  - combine the carriers at a low level, and amplify them with an MCPA.
- We’ll now calculate the overall amplifier efficiency for both.

SCPA solution with 3dB hybrids



At P_{1dB}, the drain efficiency is about 48% for a 2GHz device

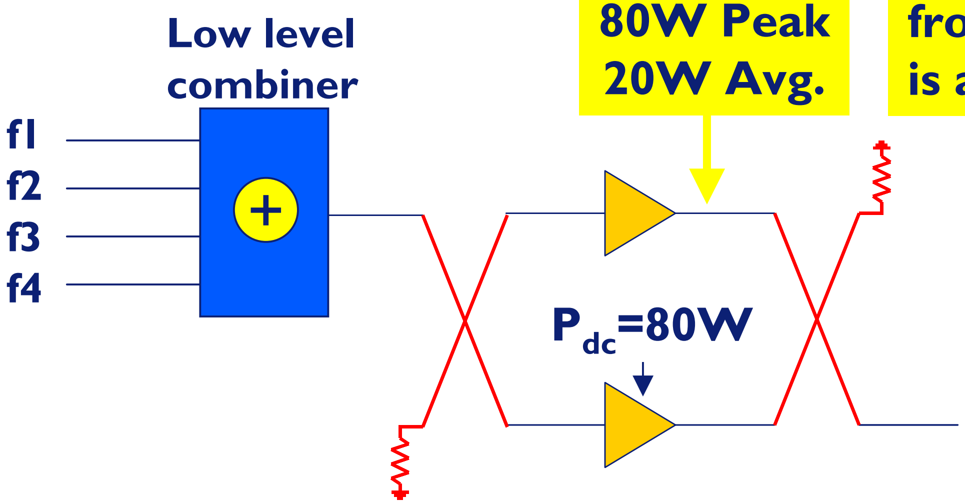
4x10W, i.e. 40W avg.
P_{peak}=4x40=160W

Total P_{dc} = 4x 83W = 332W

$$\eta_{amplifier} = \frac{P_{rf,out}}{P_{dc}} = \frac{40}{332} = 12\%$$

Each 3dB hybrid has 3dB loss

MCPA solution



80W Peak
20W Avg.

At 6dB (factor of 4) back-off from P_{1dB}, the drain efficiency is about 25% for a 2GHz device

4x10W, i.e. 40W avg.
P_{peak}=4x40=160W

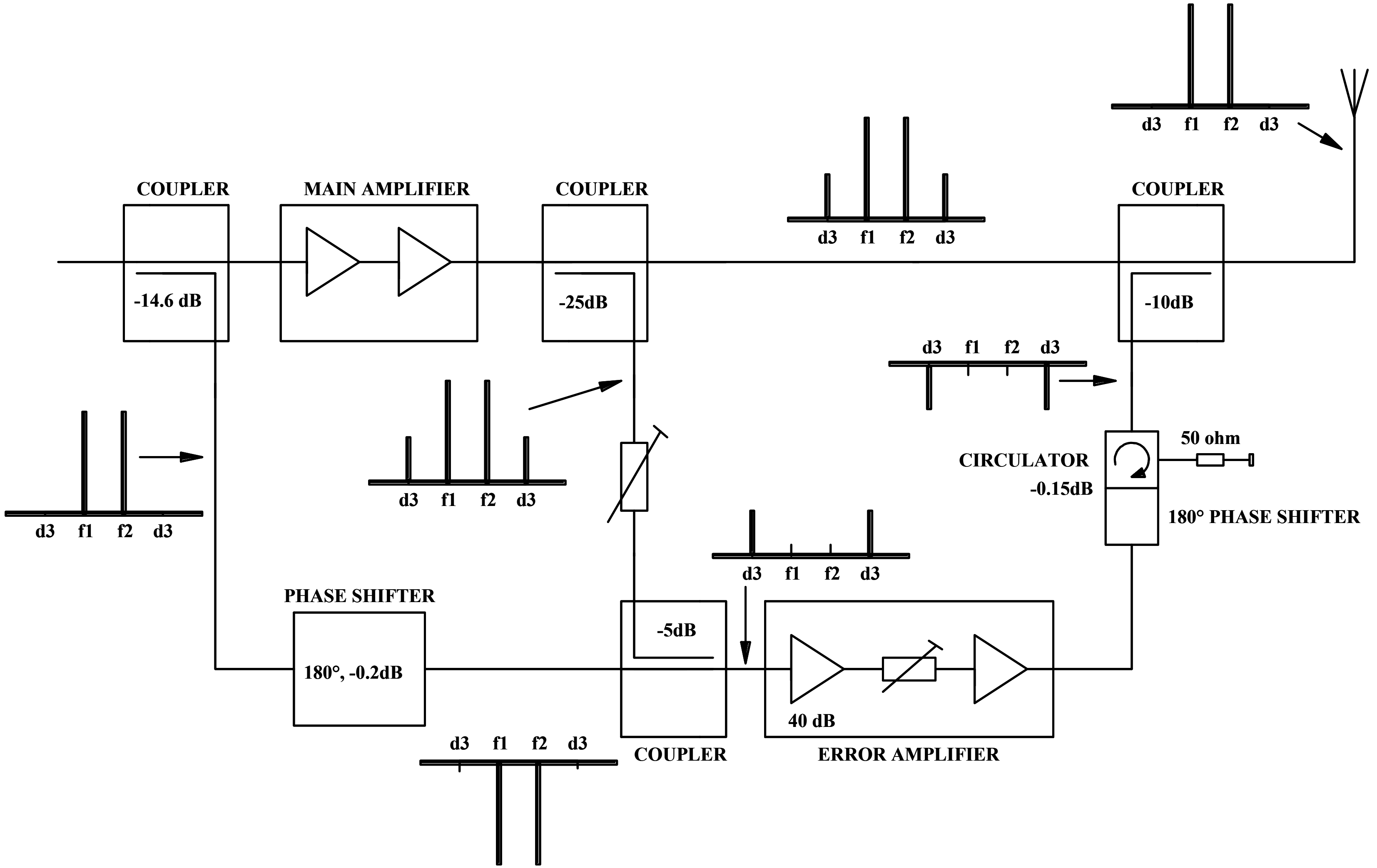
Total P_{dc} = 2x 80W = 160W

$$\eta_{amplifier} = \frac{P_{rf,out}}{P_{dc}} = \frac{40}{160} = 25\%$$

MCPA solution

- But, since we are now sending 4 carriers through an amplifier, we are generation distortion (IMD) products.
- Since we have designed the amplifier for 6dB back-off (PAR=6dB), the level of the IMD products will be about –30dBc.
- FCC requires –60dBc, so we need to fix this.
- This can be done with a feed-forward amplifier.

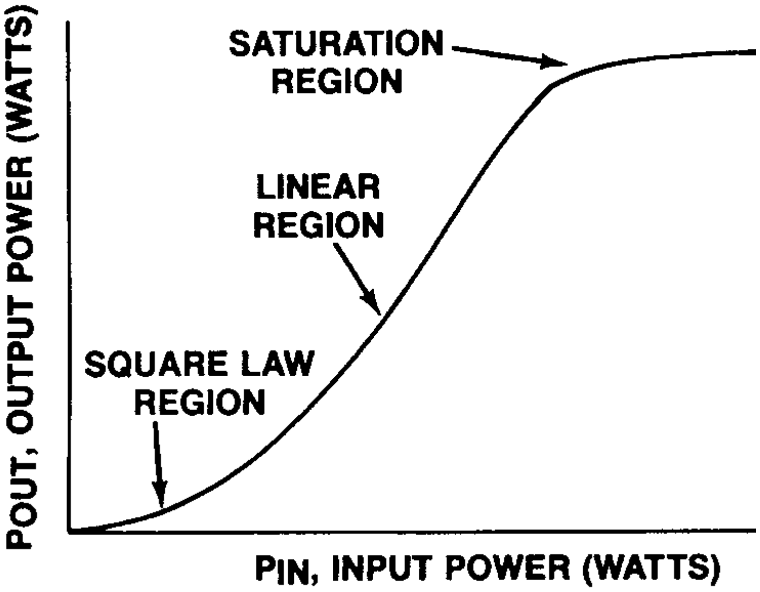
Feed Forward Principle



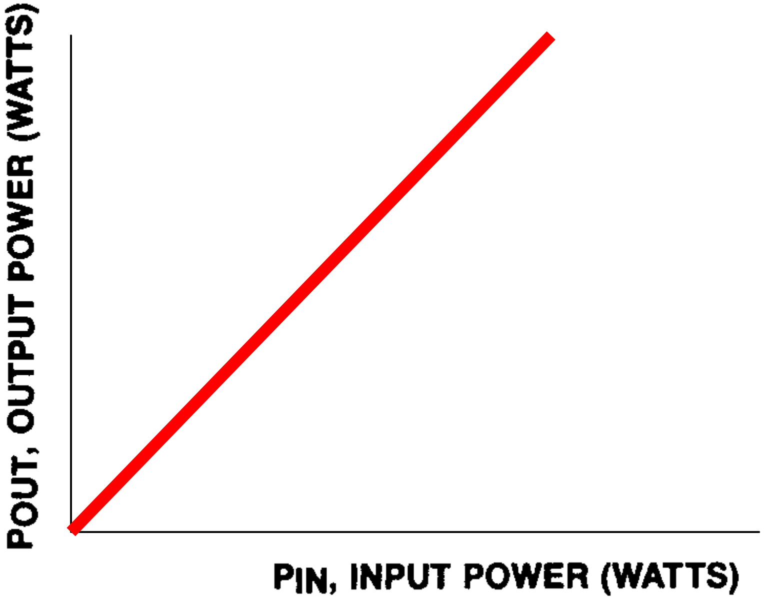
Feed Forward MCPA

- If we assume that the error amplifier consumes 40W, the overall MCPA efficiency degrades to 20%, still a significant savings.
- With a $0.10 kWh price, the annual cost to run the:
  - SCPA $290.83
  - MCPA $175.20, a 40% energy savings
- Other disadvantage is the more complex MCPA design obviously.
- But, the higher MCPA efficiency also requires less cooling (smaller heatsink, less environmental noise)

Pre-Distortion

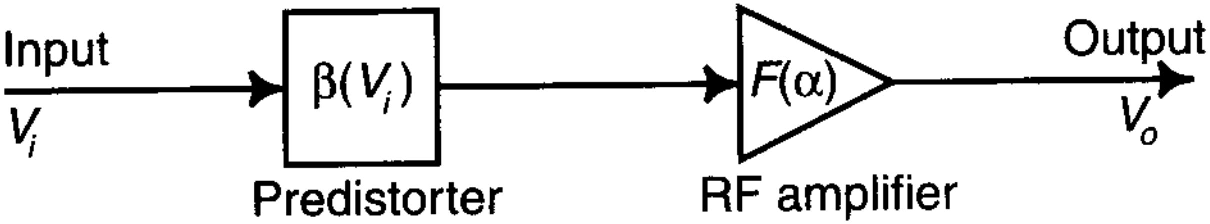


REAL

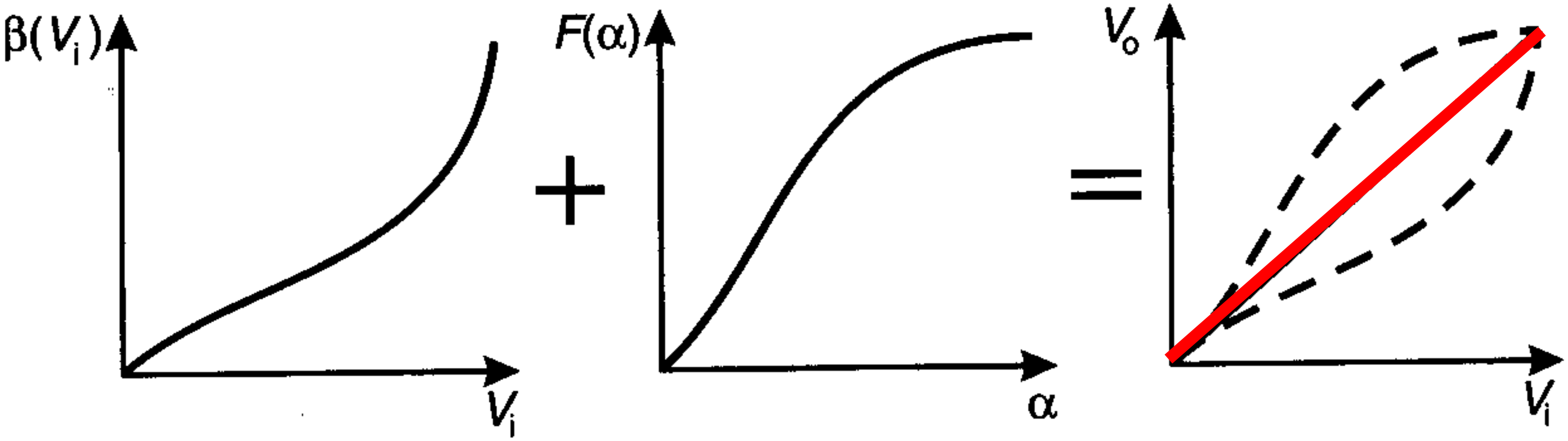


IDEAL

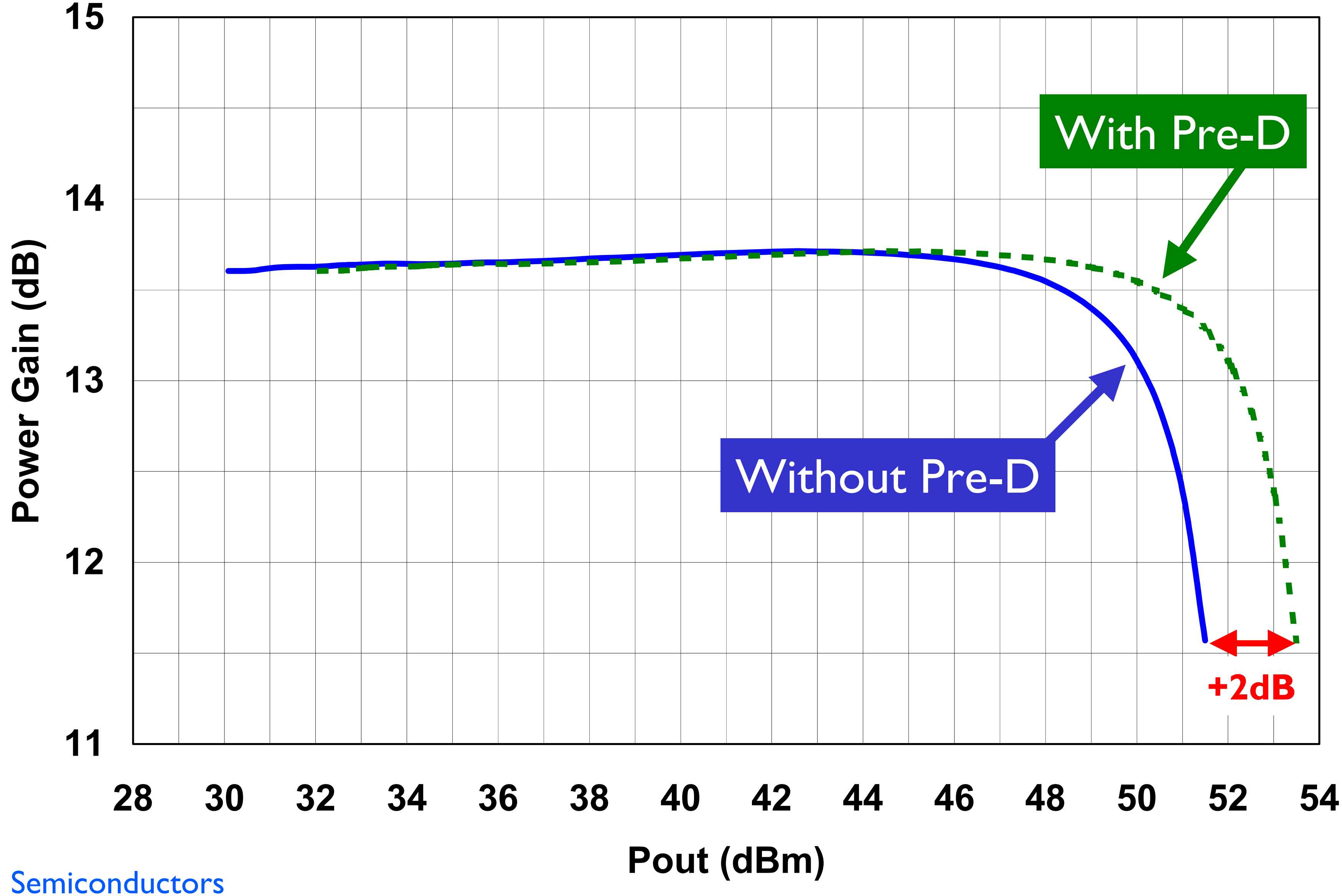
Pre-Distortion



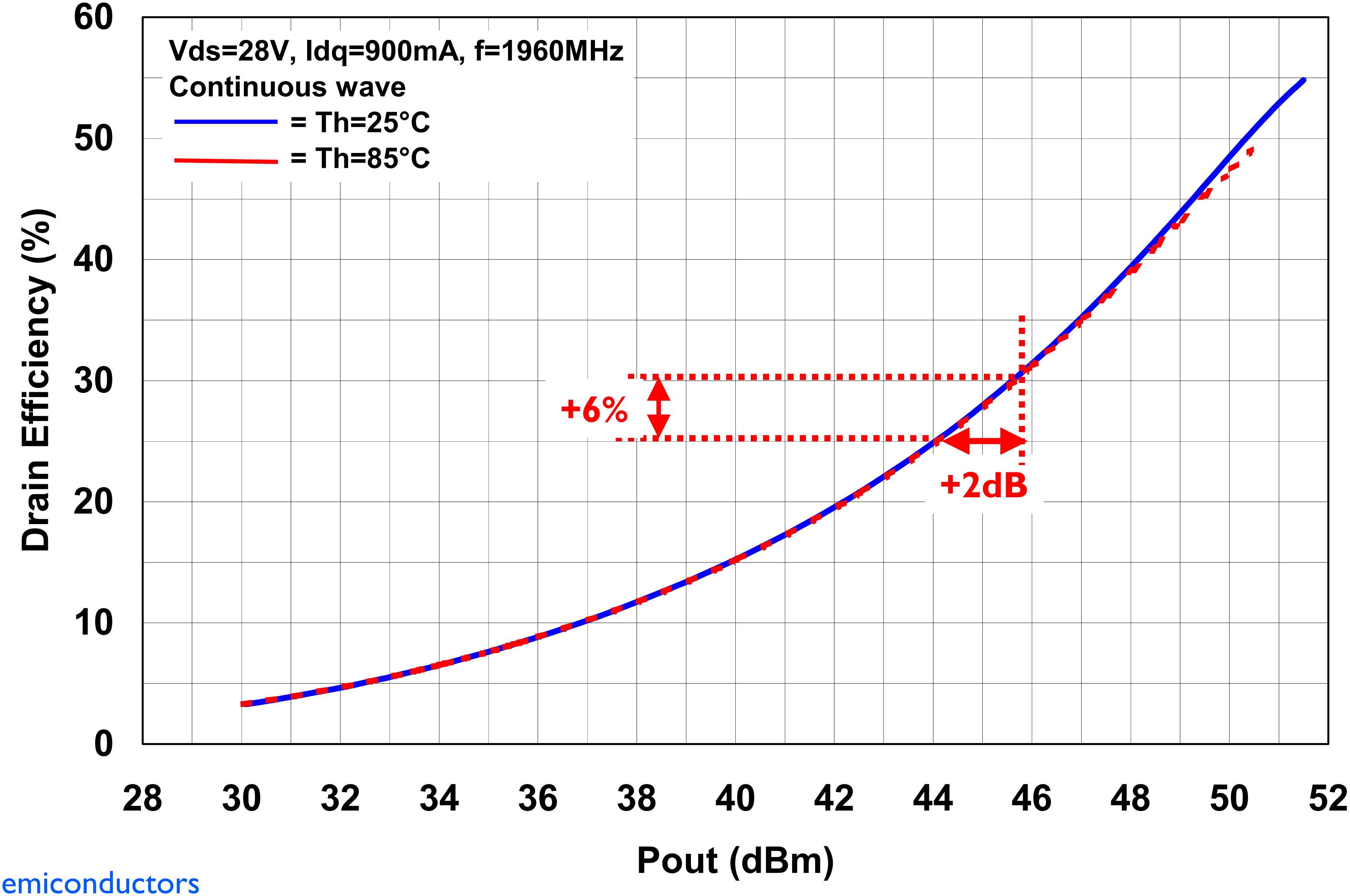
$$F\{\beta(V_i)\} = A$$



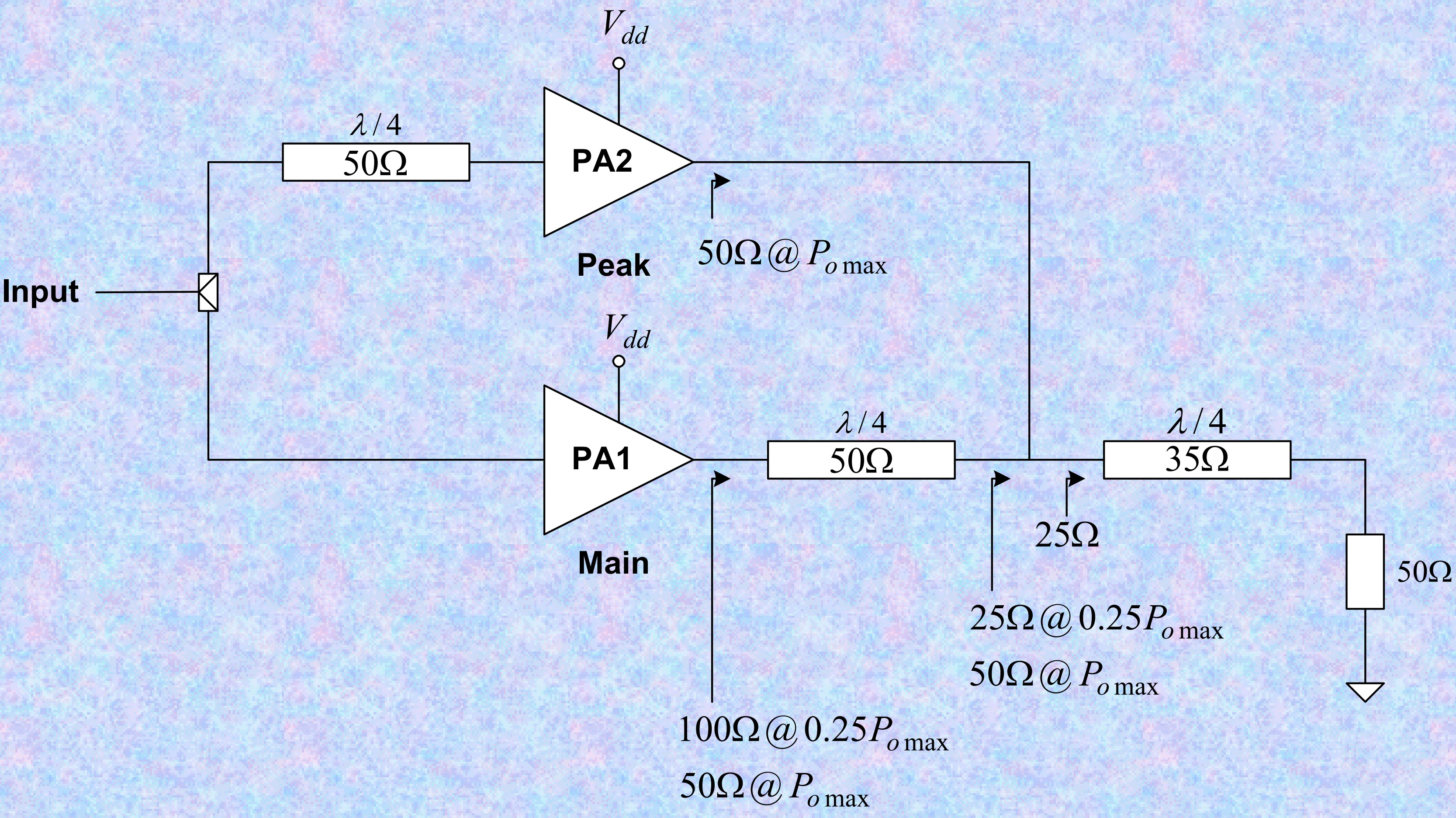
Pre-Distortion



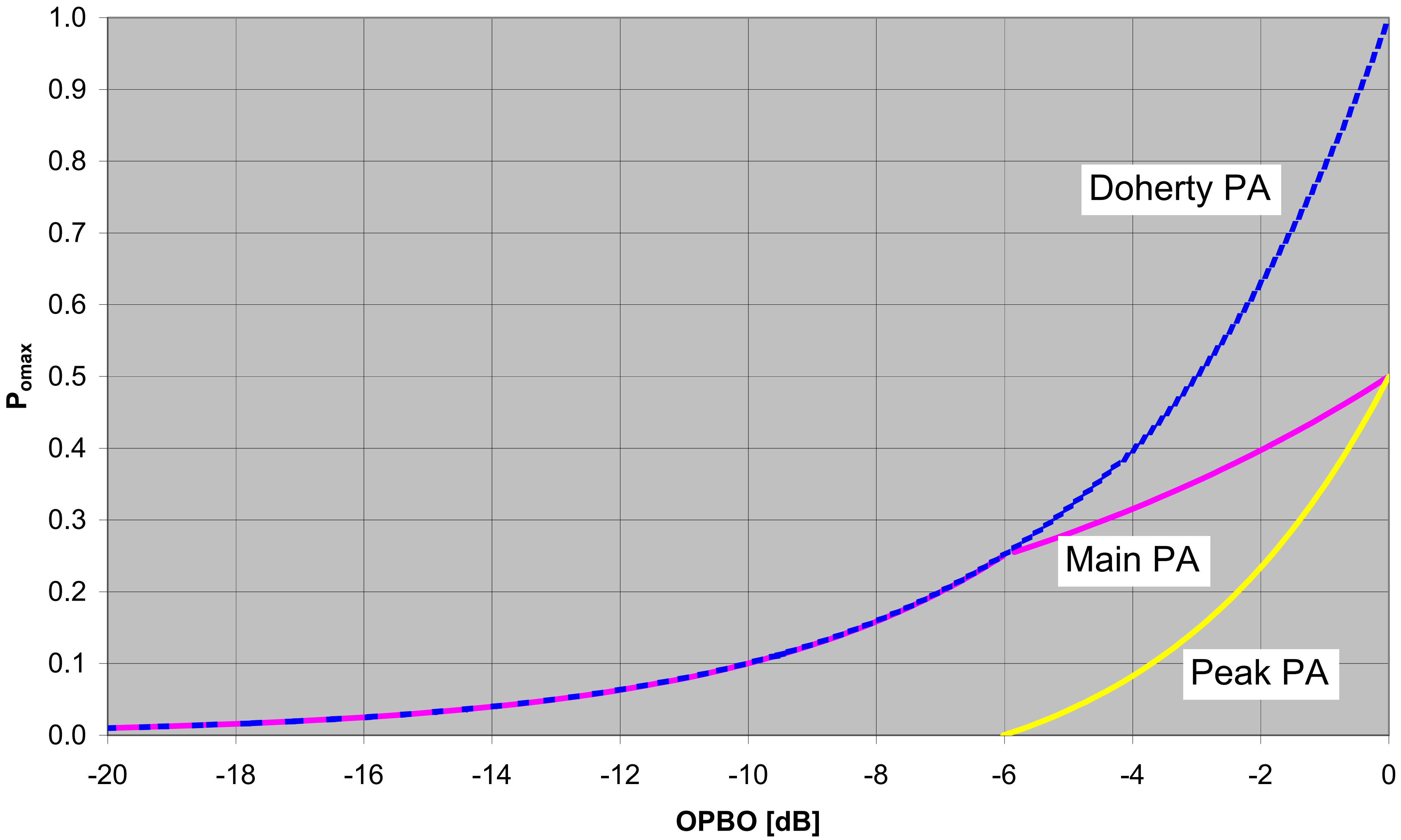
Pre-Distortion



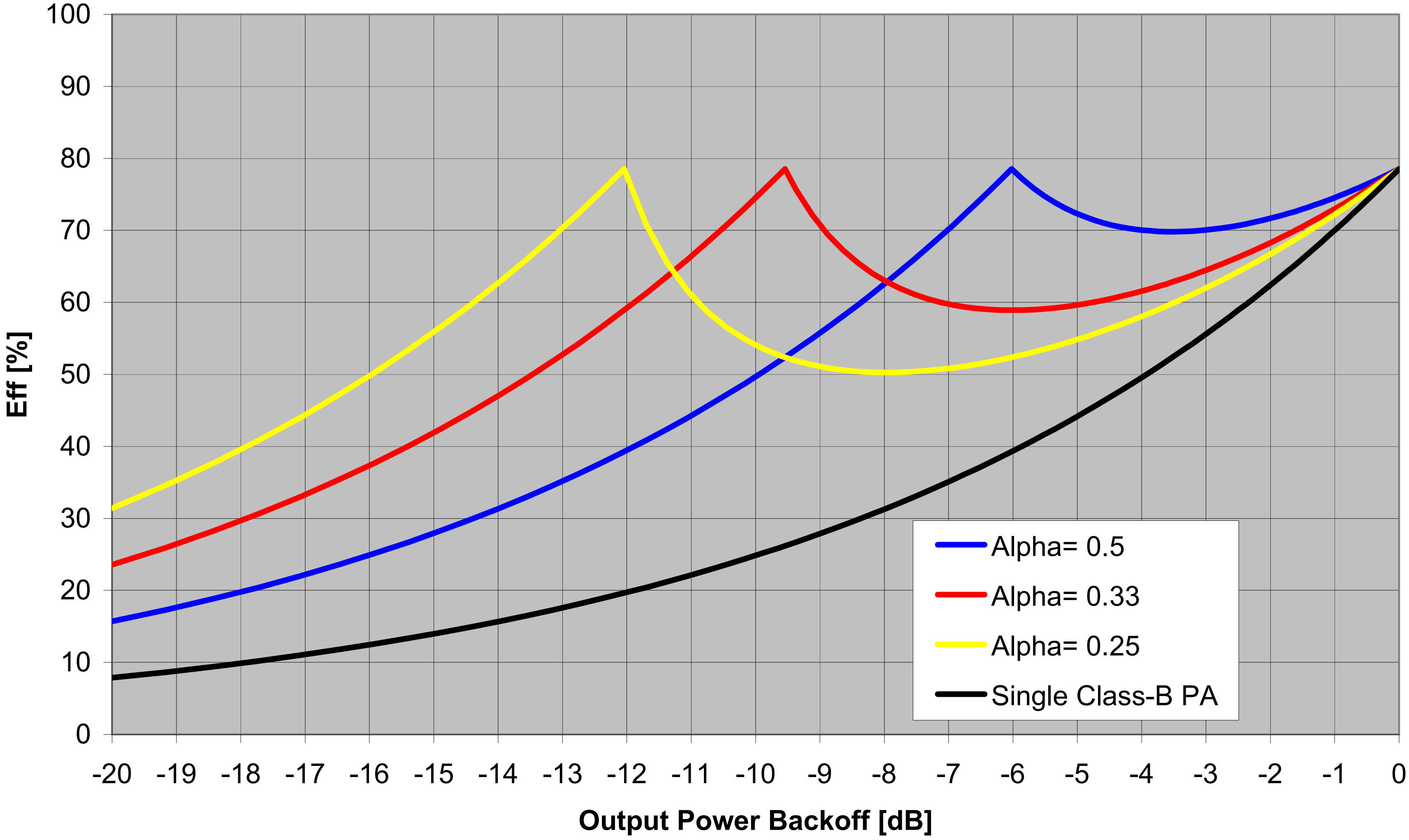
Doherty (Classical)



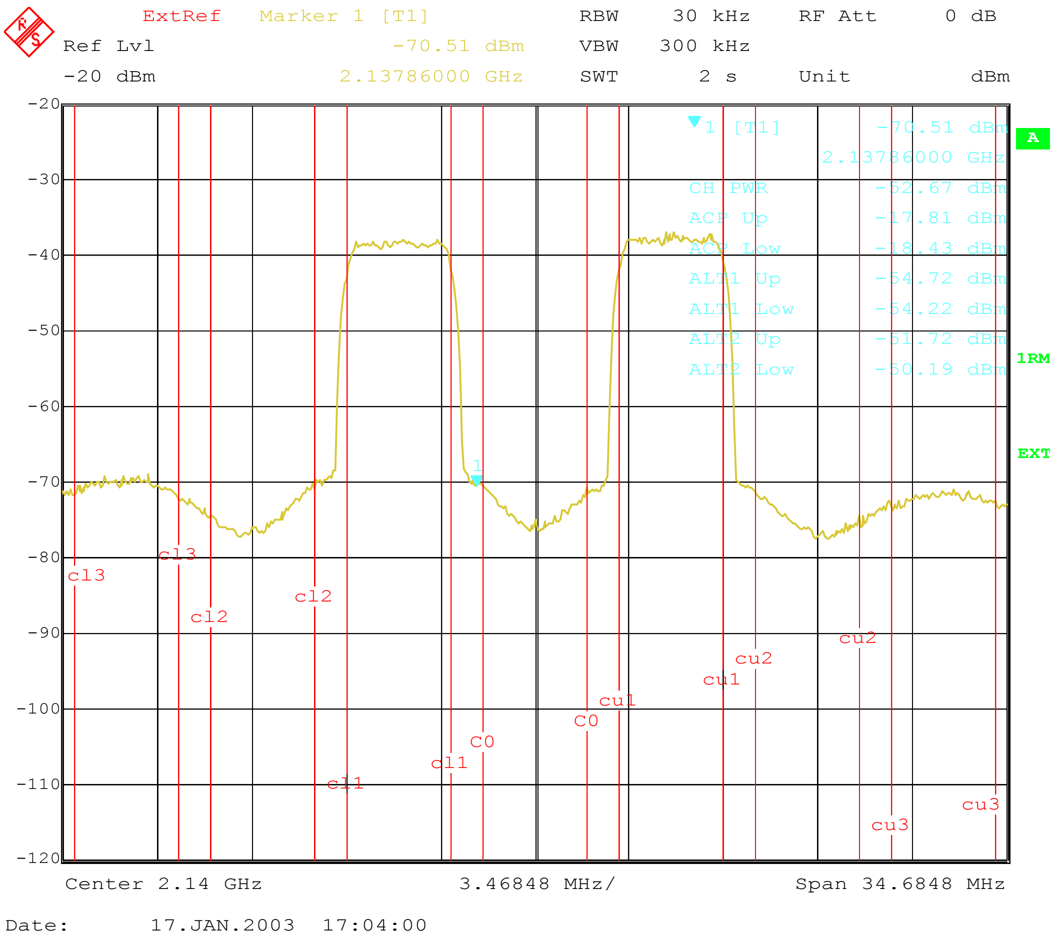
Doherty


1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
P_{omax}
-20
-18
-16
-14
-12
-10
-8
-6
-4
-2
0
OPBO [dB]
Doherty PA
Main PA
Peak PA

Doherty – Theoretical Efficiency



2C-WCDMA Doherty Performance



```
     ExtRef    Marker 1 [T1]          RBW     30 kHz    RF Att      0 dB
Ref Lvl                 -70.51 dBm    VBW    300 kHz
-20 dBm             2.13786000 GHz    SWT      2 s      Unit          dBm

                                   1 [T1]               -70.51 dBm
                                                    2.13786000 GHz
                                   CH PWR               -52.67 dBm
                                   ACP Up               -17.81 dBm
                                   ACP Low              -18.43 dBm
                                   ALT1 Up              -54.72 dBm
                                   ALT1 Low             -54.22 dBm
                                   ALT2 Up              -51.72 dBm
                                   ALT2 Low             -50.19 dBm

Center 2.14 GHz            3.46848 MHz/            Span 34.6848 MHz

Date:      17.JAN.2003   17:04:00
```

Vds= 28V, Idq= 825mA, Id= 5.22A,
f1= 2135MHz, f2=2145MHz

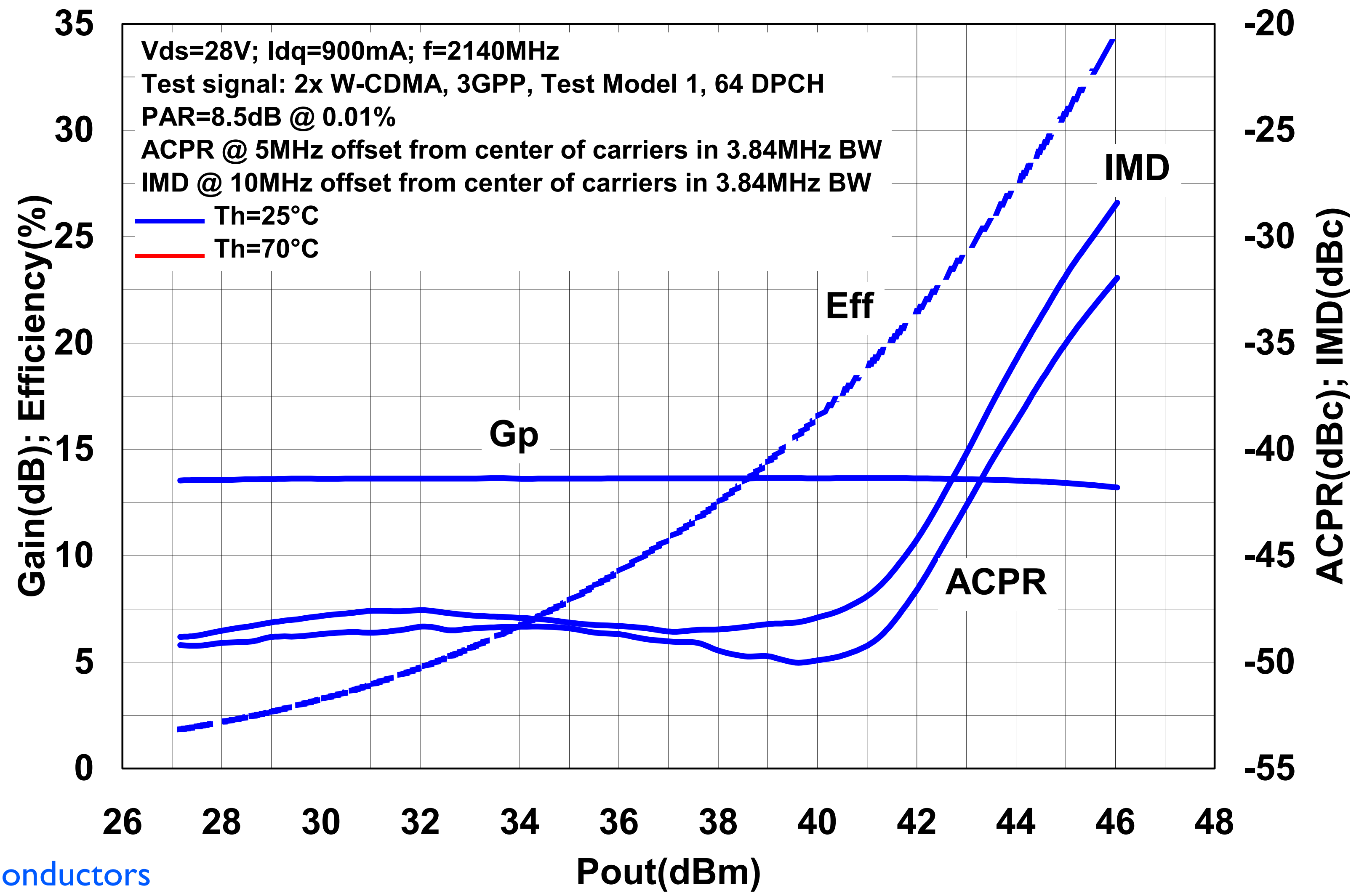
Po-avg= 50W, Eff= 34.2%

ACLR5_up= -36.9dBc
ACLR5_low= -35.8dBc

IM3_up= -33.9dBc
IM3_up= -31.8dBc

Carrier: 3GPP Testmodel1, 64 DPCH,
46% Clipping

2C WCDMA Class-AB amplifier.



Quick comparison
Conventional vs. Doherty PA

- At 44.6dBm, one final stage has an efficiency of about 30% (@ -33dBc IMD). So at 47dBm (50W), two of these are needed.
- Total required DC power is therefore 192.3W. This translates into an efficiency of 26% for the finals only (drivers not taken into account).
- The Doherty amplifier gives 34%, an 8% improvement!

Conclusions

- Higher efficiency:
  - reduces required power (cost)
  - keeps the transistor cooler (reliability)
  - requires less heatsink or airflow
- Other ways to improve efficiency
  - devices with higher gain (reduces driver size)
  - devices with higher peak power capability (ability to pre-distort)
- Combinations of the amplifier concepts presented.

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PA Fundamentals

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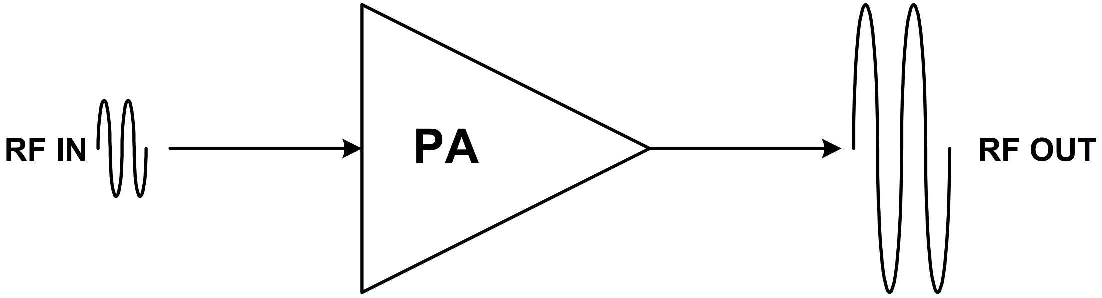
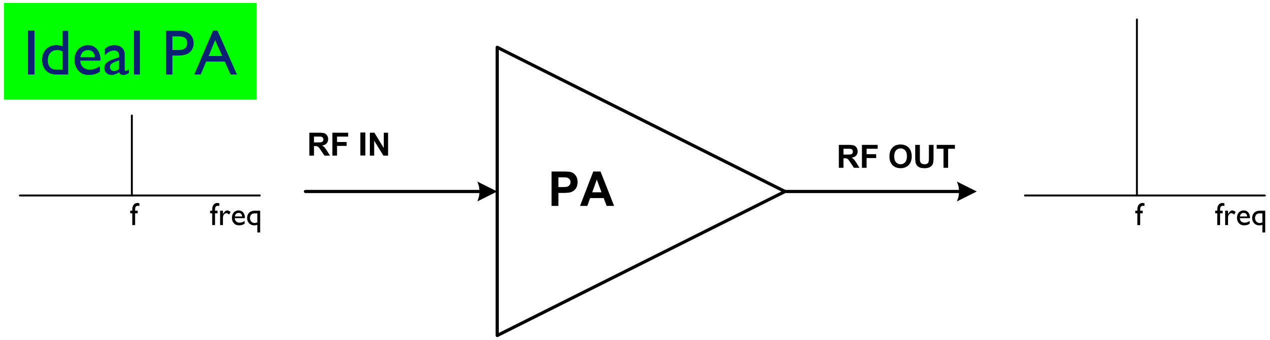
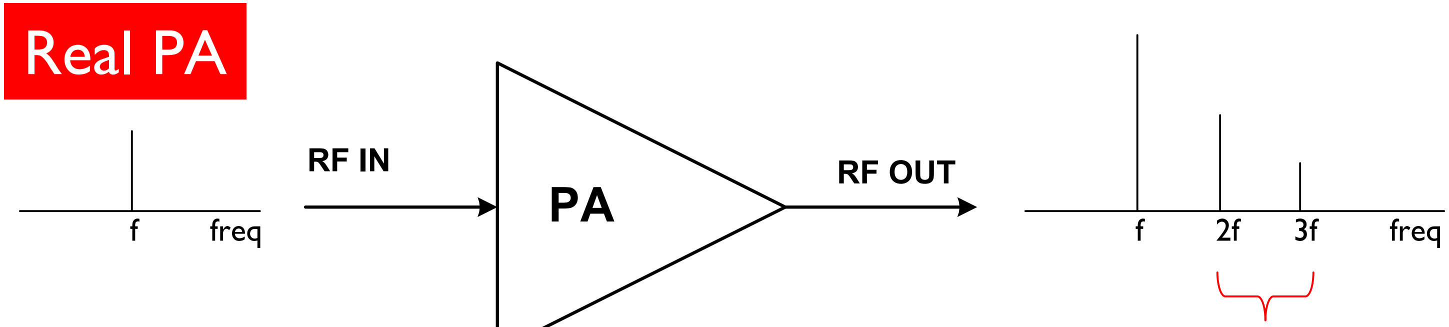
Power Amplifier (PA)



A Power Amplifier serves one fundamental function:
It amplifies the incoming signal. In an *ideal case* no distortion, noise or spurious is added by the PA

Ideal and Real PA (single carrier)

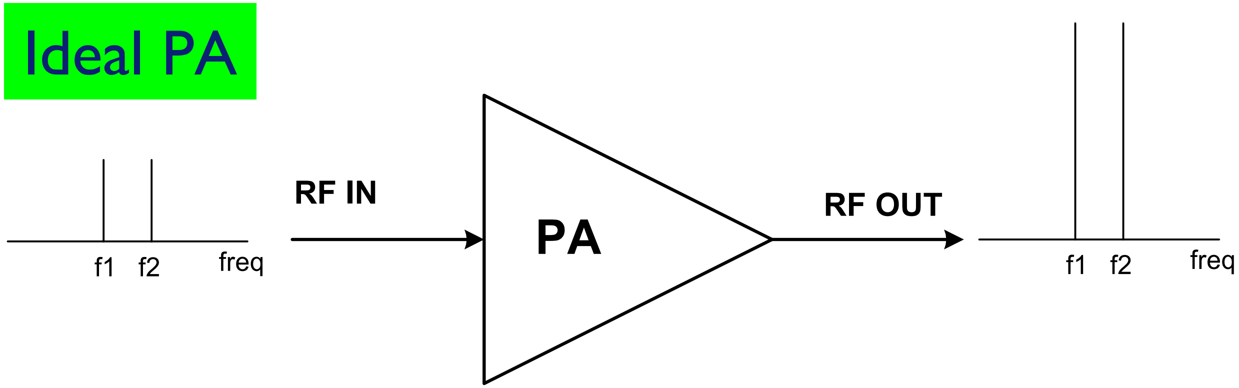




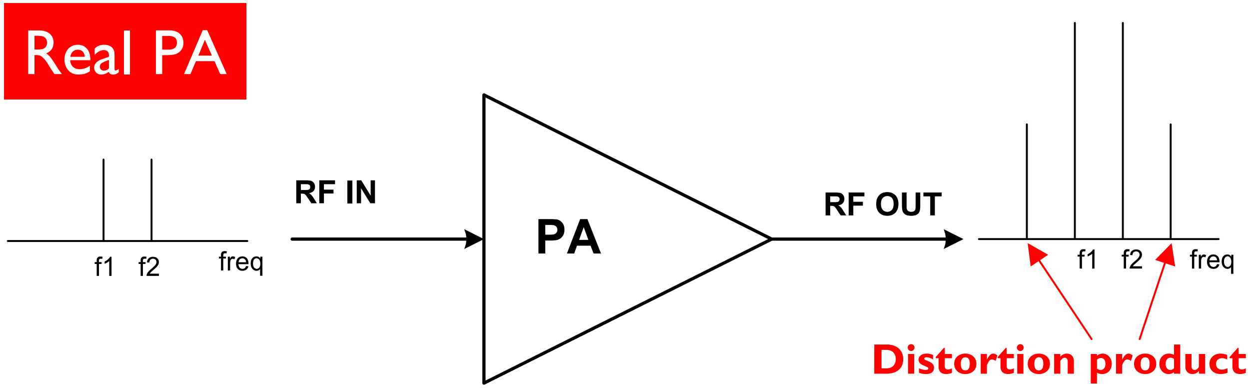
Harmonics can be filtered out

Ideal and Real PA (Multi Carrier)

Ideal PA



Real PA



Distortion products can not be filtered out

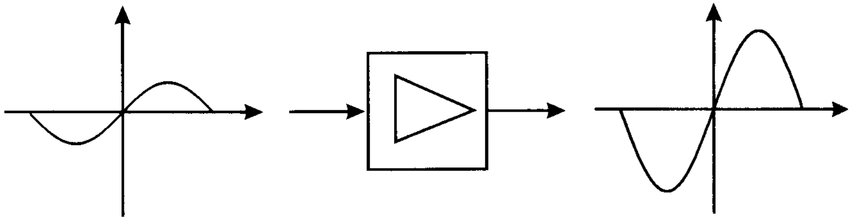
Distortion

- Multi carrier signals and every modulated signal (non constant envelope) that is amplified by a power amplifier creates distortion:
  - harmonics ($2f_0$, $3f_0$, etc.)
  - intermodulation distortion (unwanted products in close proximity to f_0)
- Constant envelope signals create harmonics, but these can be filtered out.
- Non-constant envelope signals create intermodulation distortion (IMD), and can not be filtered out.

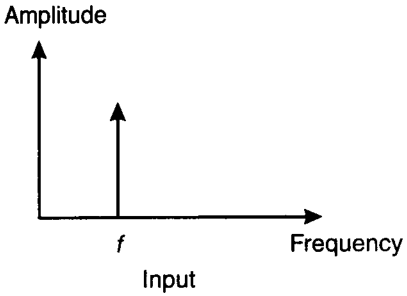
Intermodulation Distortion (IMD)

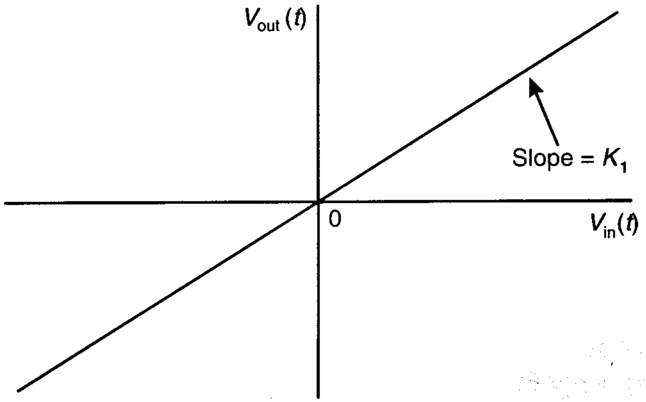
- IMD needs to be kept at a minimum to avoid interference (in neighboring channels for instance – FCC requirements).
- The amount of intermodulation distortion is determined by the power amplifier, and thus the power transistor used.
- Intermodulation is caused by non-linearity in the transfer characteristic of the RF power transistor.

The perfect amplifier



(a)

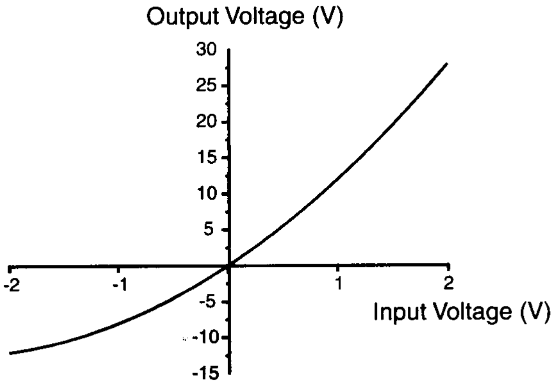




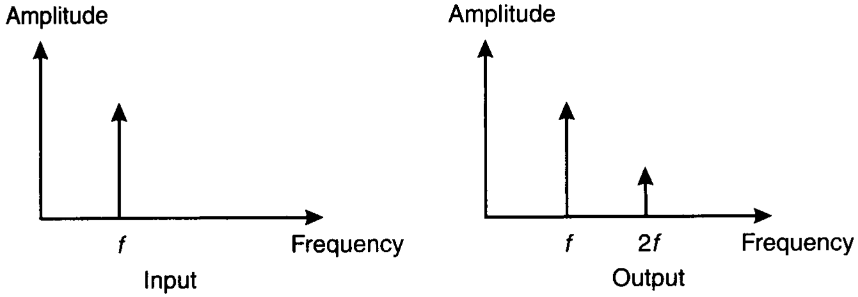
(b)

$$V_{out}(t) = K_1 \cdot V_{in}(t)$$

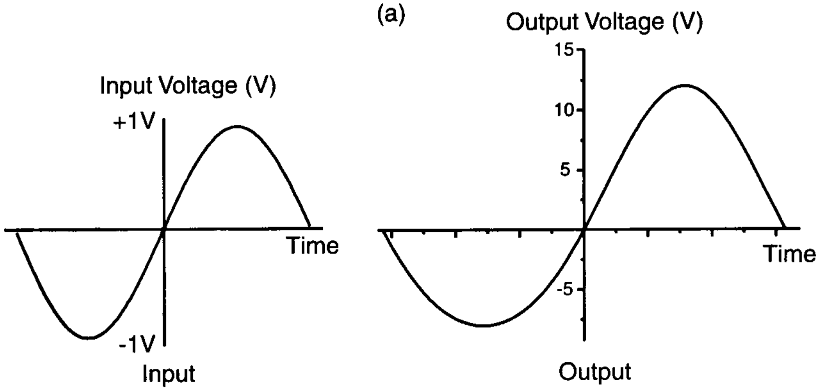
Square-Law Characteristic or Second Order Characteristic



(a)



(c)

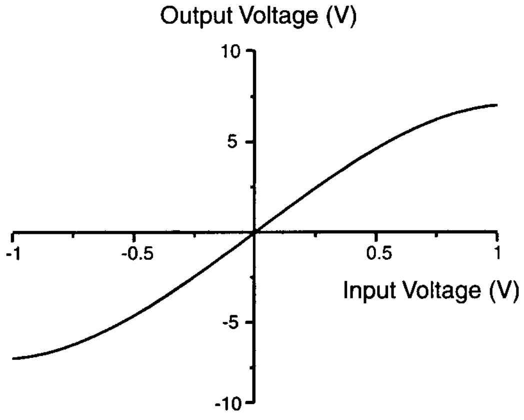


(b)

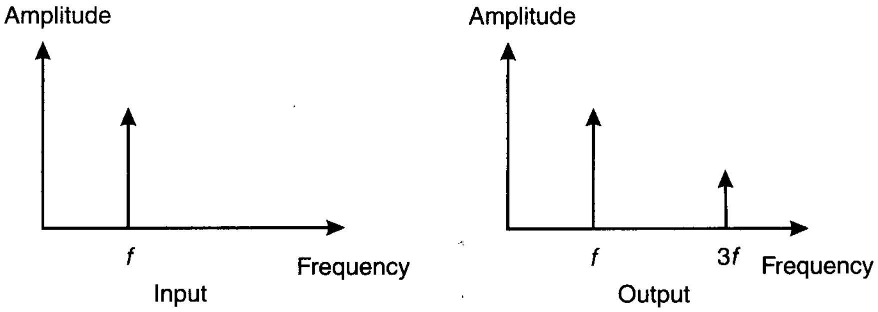
$$V_{out}(t) = K_1 \cdot V_{in}(t) + K_2 \cdot V^2{}_{in}(t)$$

$$K_1 = 10; K_2 = 2$$

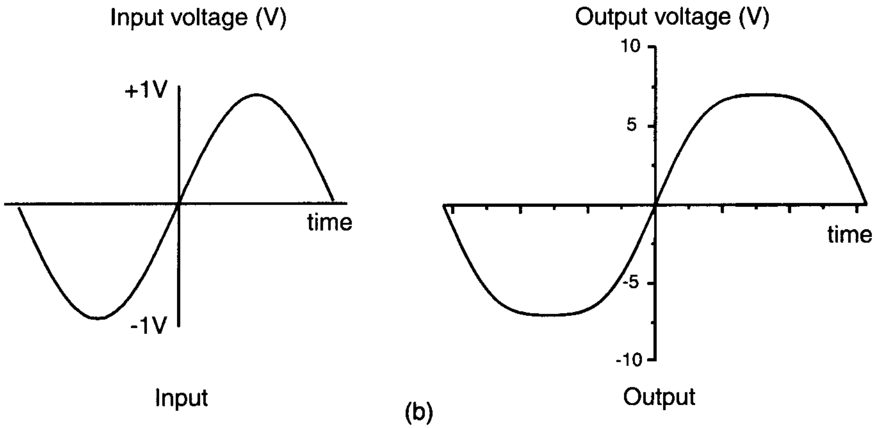
Third Order Characteristic



(a)



(c)

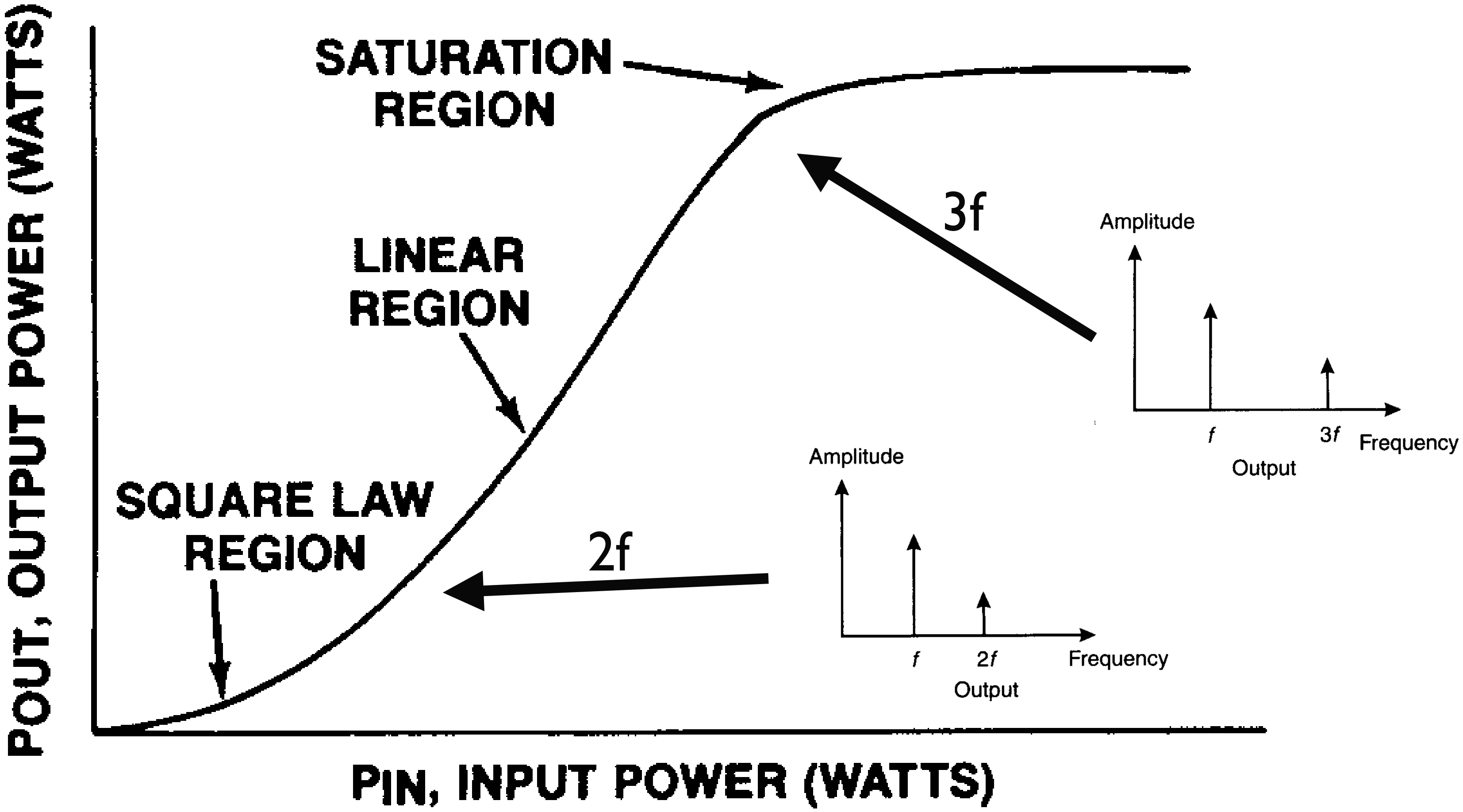


(b)

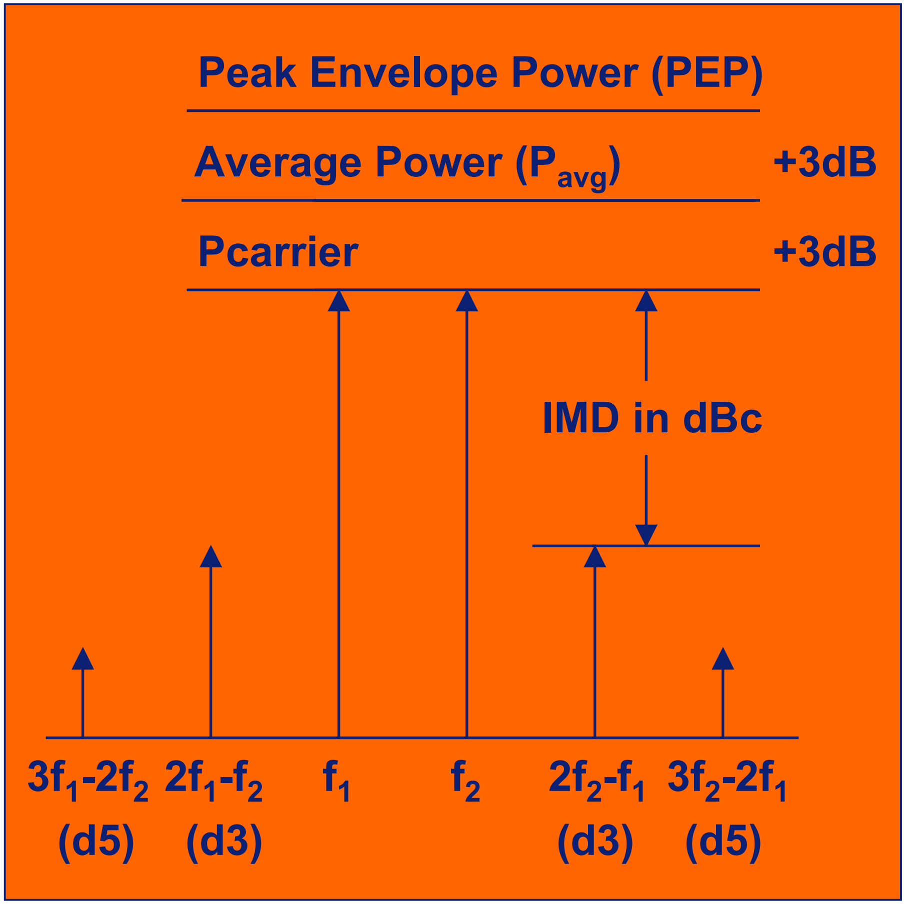
$$V_{out}(t) = K_1 \cdot V_{in}(t) + K_3 \cdot V^3{}_{in}(t)$$

$$K_1 = 10; K_3 = -3$$

The complete transfer characteristic



Intermodulation Distortion Products



Peak Envelope Power (PEP)

Average Power (P_{avg}) **+3dB**

Pcarrier **+3dB**

IMD in dBc

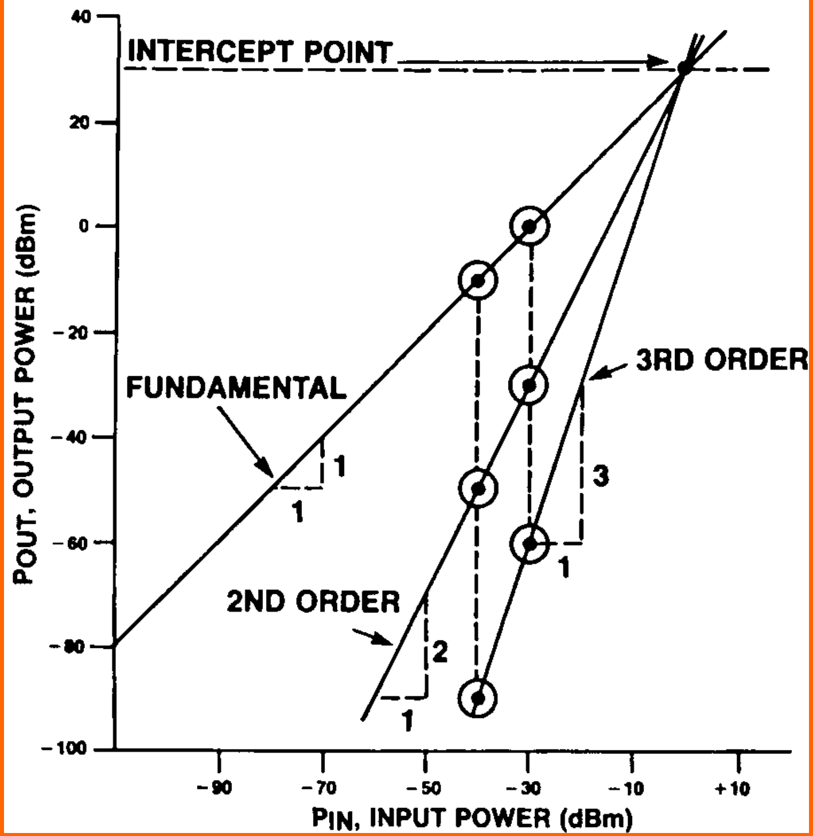
$3f_1$-$2f_2$ (d5) **$2f_1$-f_2 (d3)** **f_1** **f_2** **$2f_2$-f_1 (d3)** **$3f_2$-$2f_1$ (d5)**

f_x = fundamental
$2f_x$ = second harmonic (square law)
$3f_x$ = third harmonic (third order)

d3 = third order IMD product
d5 = fifth order IMD product

IMD is expressed in "dBc", which means relative to one of the two carriers f_l or f_2

Intercept Points



Intercept points are THEORETICAL power levels that are a measure for the linearity of an amplifier (transistor)

ITO2 (2nd order intercept) is the point where fundamental and 2nd order line (2:1 slope) meet

ITO3 (3rd order intercept) is the point where fundamental and 3rd order line (3:1 slope) meet

ITO3 (dBm) = Pout (dBm) + 1/2 IMD3 (dBc)

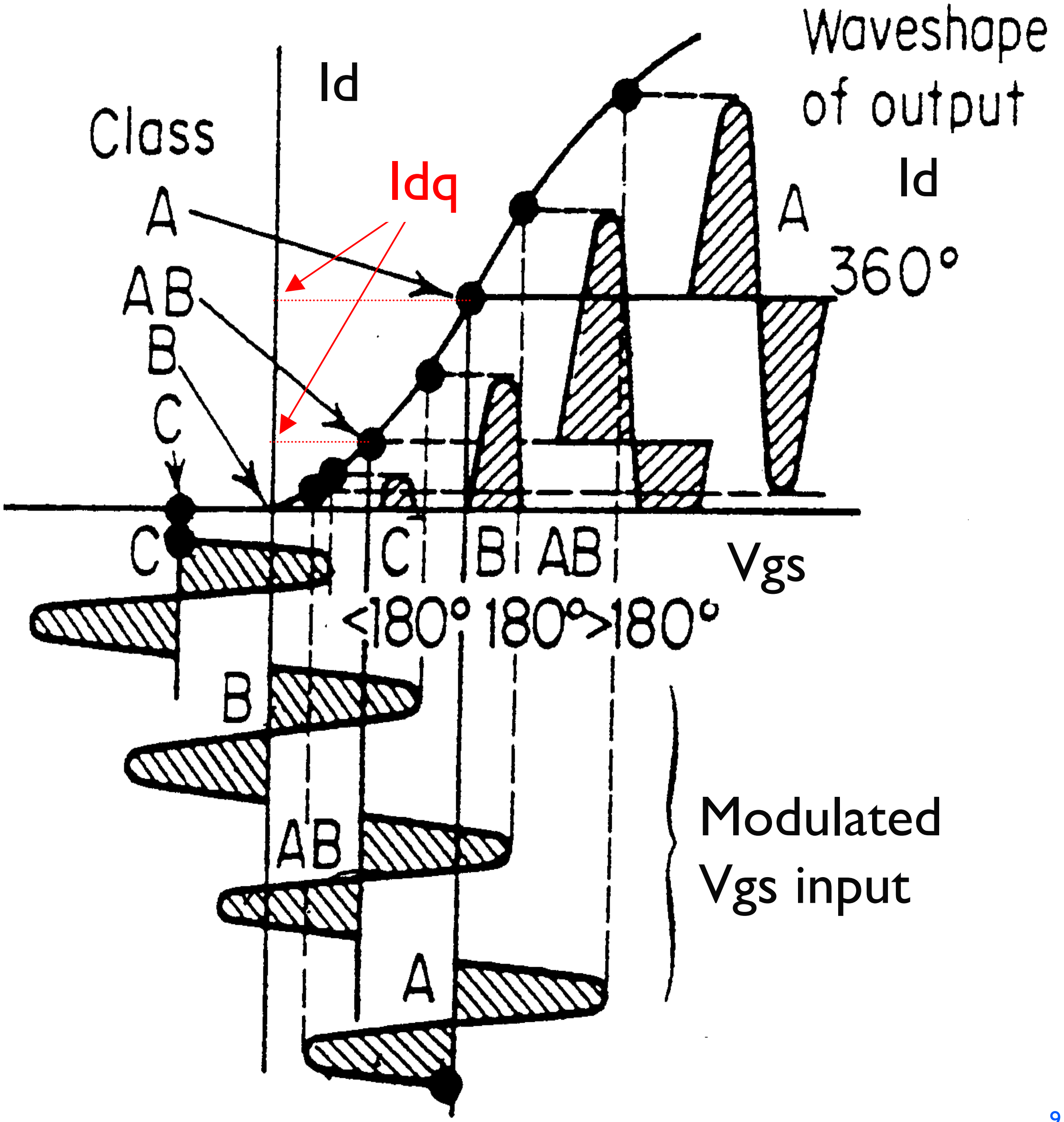
How to improve linearity

- Use a linear transistor technology such as LDMOS
- Adjust the class of operation of the PA (class A, class AB, etc
- Use a feed-forward amplifier
- Use (digital) pre distortion (DPD)

Classes of Operation

Class-A
Class-AB
Class-B
Class-C
Class-D,E,F,G,H

The class of operation is defined by the conduction angle, i.e. the time the transistor conducts current



Overview classes of operation

- Class A
- Ultra Linear Amplifier
- Extremely High Power Gain
- Low Efficiency (50% max)
- Conduction Angle 360°

- Class B
- Non-Linear Amplifier
- Low Power Gain
- High Efficiency (78.5%)
- Conduction Angle 180°

- Class AB
- Linear Amplifier
- High Power Gain
- Medium Efficiency (50-78.5%)
- Conduction Angle 180-360°

- Class C
- Extremely Non-Linear Amplifier
- Extremely Low Power Gain
- Extremely High Efficiency (90%)
- Conduction Angle <180°

RF Power

- Can be expressed in Watts or dBm
- 0dBm = 1mW in 50Ω

1GW	(Gigawatt)	1 x 10^{9} Watt
1MW	(Megawatt)	1 x 10^{6} Watt
1kW	(kilowatt)	1 x 10^{3} Watt
1W	(Watt)	1 x 10^{0} Watt
1mW	(milliwatt)	1 x 10^{-3} Watt
1µW	(microwatt)	1 x 10^{-6} Watt
1nW	(nanowatt)	1 x 10^{-9} Watt
1pW	(picowatt)	1 x 10^{-12}Watt

Conversion between Watts and dBm

$$P_{out}\,[\,Watts\,] = \frac{10^{\frac{P_{out}\,[\,dBm\,]}{10}}}{1000}$$

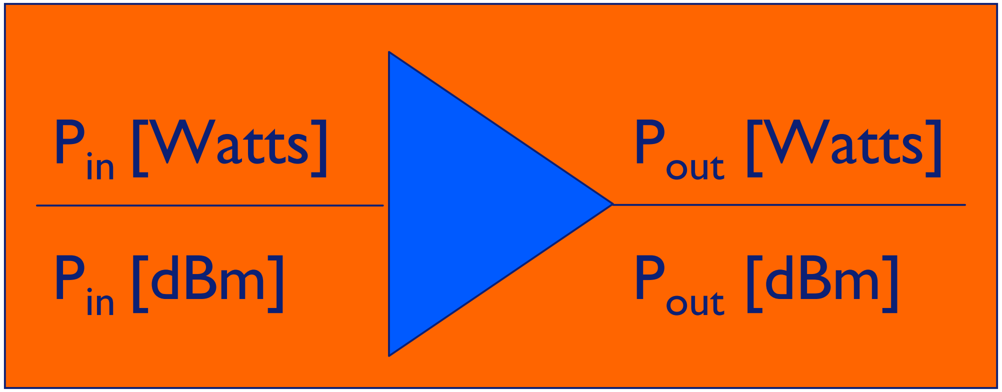
dBm → Watts

$$P_{out}\,[\,dBm\,] = 10\log\frac{P_{out}\,[\,Watts\,]}{0.001}$$

Watts → dBm

Examples:
0 dBm = 1mW
20 dBm = 100mW
43 dBm = 20W
100W = 50dBm

Power Gain



$$G_p[dB] = 10\log\frac{P_{out}[Watts]}{P_{in}[Watts]}$$

or

$$G_p[dB] = P_{out}[dBm] - P_{in}[dBm]$$

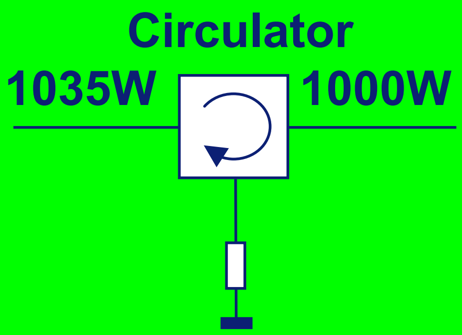
Power Gain Conversions / Insertion Loss

$$P_{in} = \frac{P_{out}[\,in\,Watts]}{10^{\frac{Gp[\,in\,dB]}{10}}}[\,in\,Watts\,]$$

$$P_{out}[\,Watts\,] = P_{in}[\,Watts\,]\cdot 10^{\frac{G_p[\,dB\,]}{10}}$$

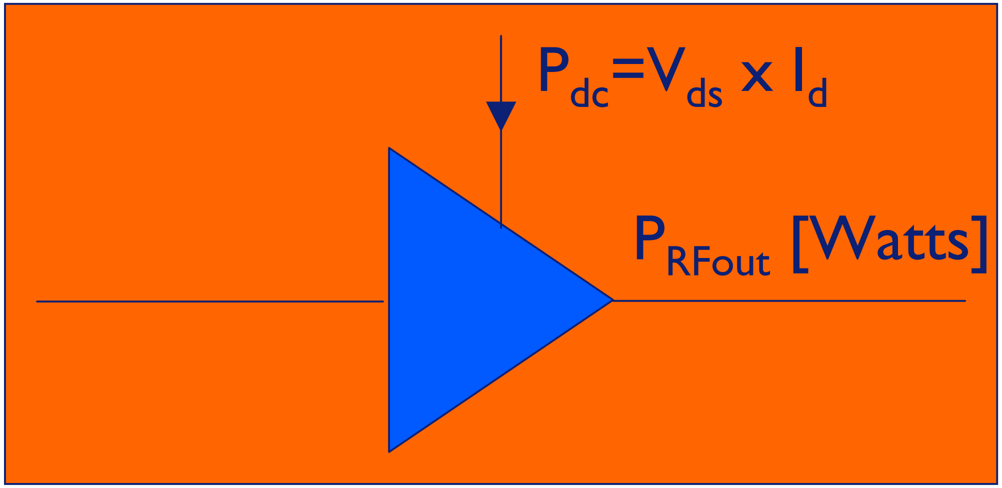
- Insertion loss is ***negative*** power gain (loss), i.e P_{out} is lower than P_{in}

Example:



$$G_p = 10\log\frac{1000}{1035} = -0.15dB$$

Efficiency



- Efficiency (often referred to as *drain efficiency*) is the ratio between RF output power and DC input power.

$$\eta_D[\%] = \frac{P_{RFout}[Watts]}{P_{dc}[Watts]} \cdot 100 = \frac{P_{RFout}[Watts]}{V_{ds}[V] \cdot I_d[A]} \cdot 100$$

Example: V_{ds}=50V, I_d=8.8A, P_{RFout}=277W

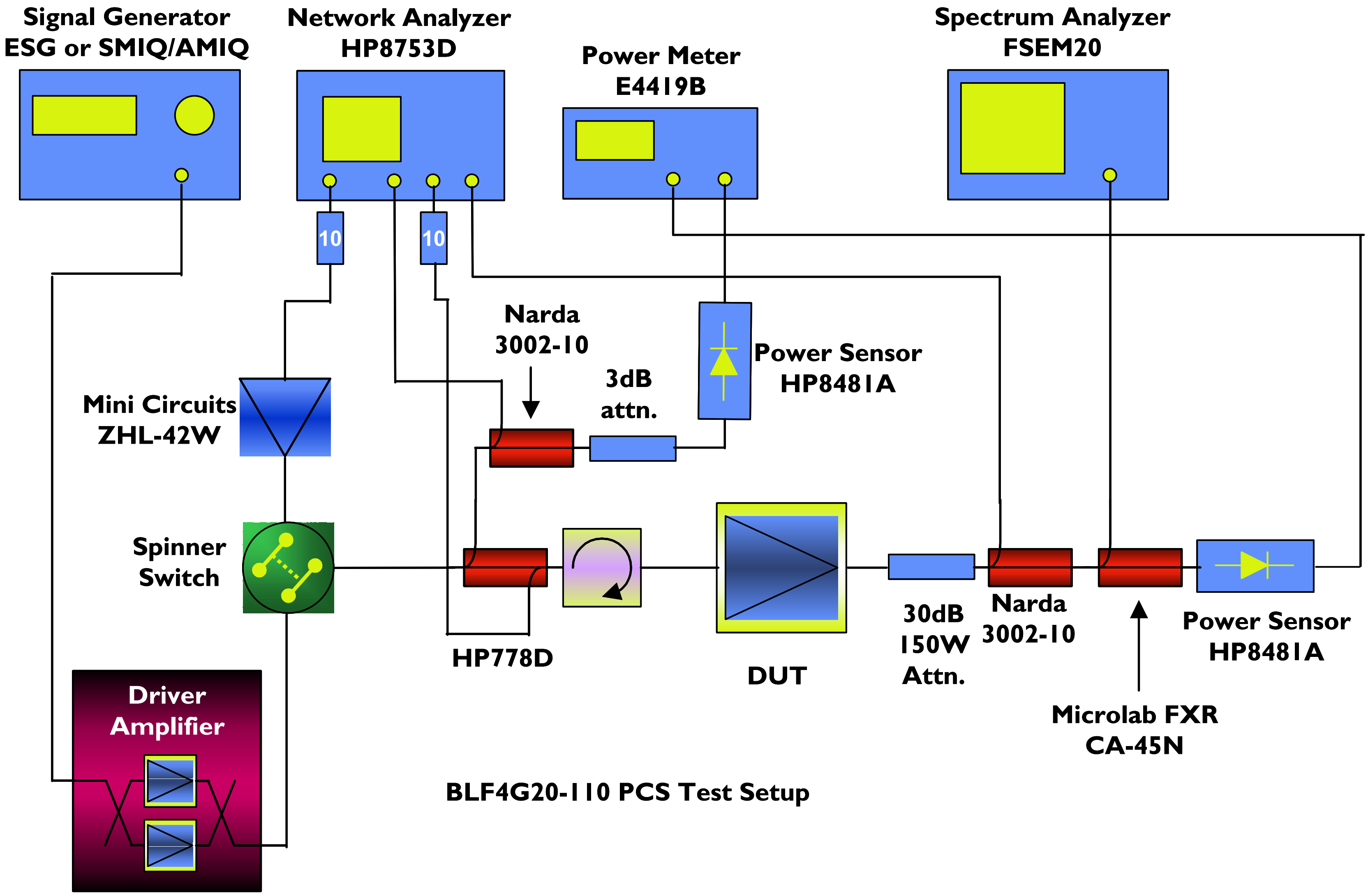
$$\left.\begin{array}{l} V_{ds}=50V, \\ I_d=8.8A, \\ P_{RFout}=277W \end{array}\right\} \eta_D = \frac{277W}{50V \cdot 8.8A} \cdot 100 = 63\%$$

PHILIPS

Digital Modulation Characterization

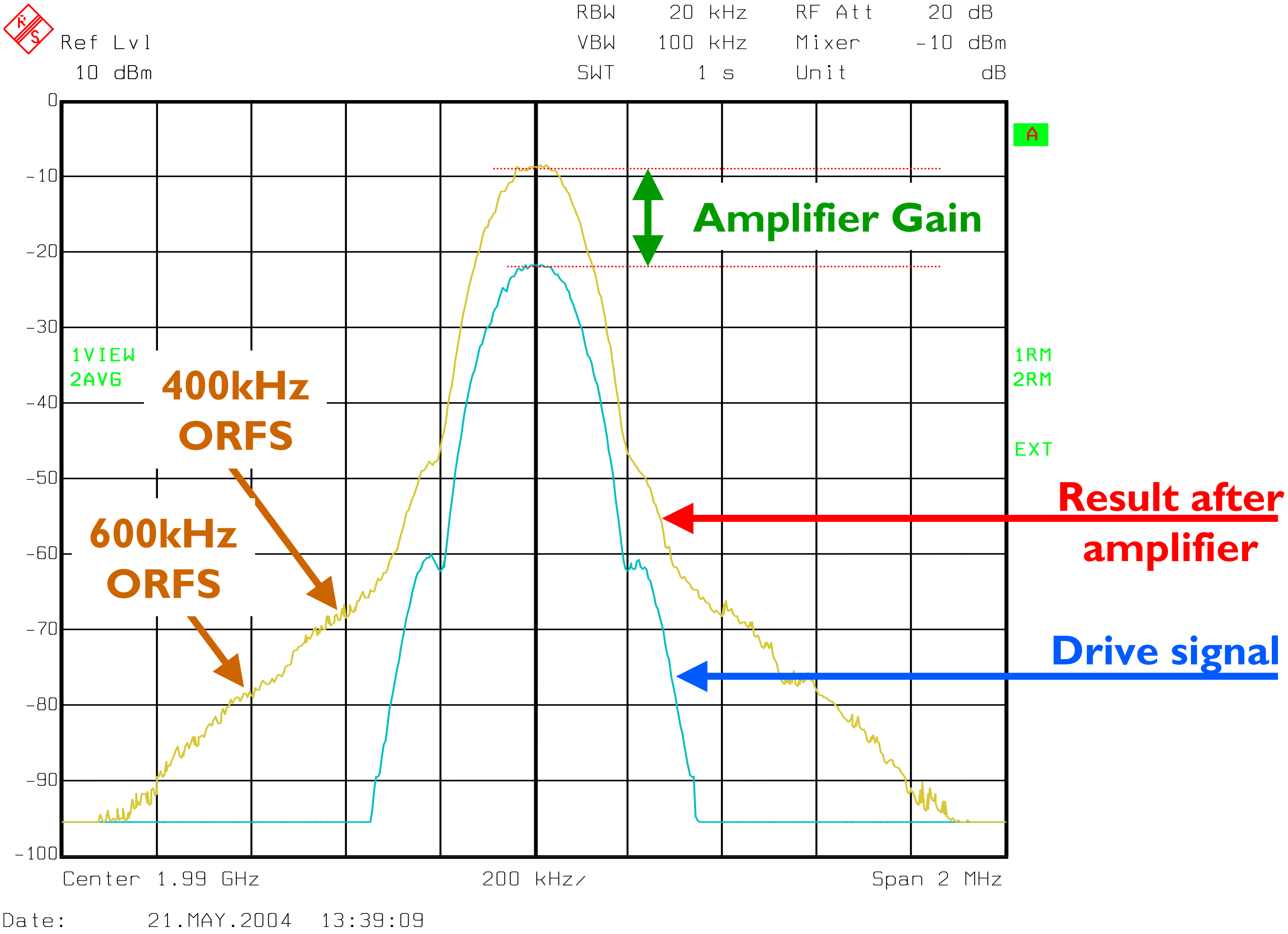
Korné Vennema
Marketing Application Engineer RF Power Transistors and Modules
Philips Semiconductors
25 Forbes Boulevard,
Foxborough MA 02035

Typical RF Power Test Setup



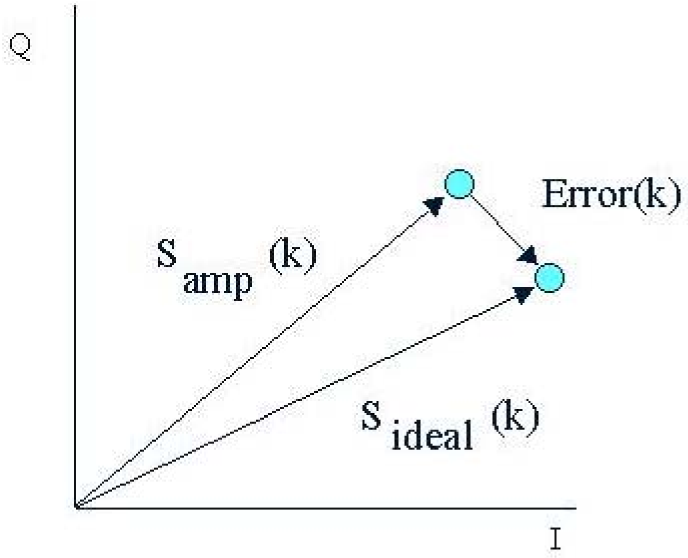
BLF4G20-110 PCS Test Setup

Edge GSM

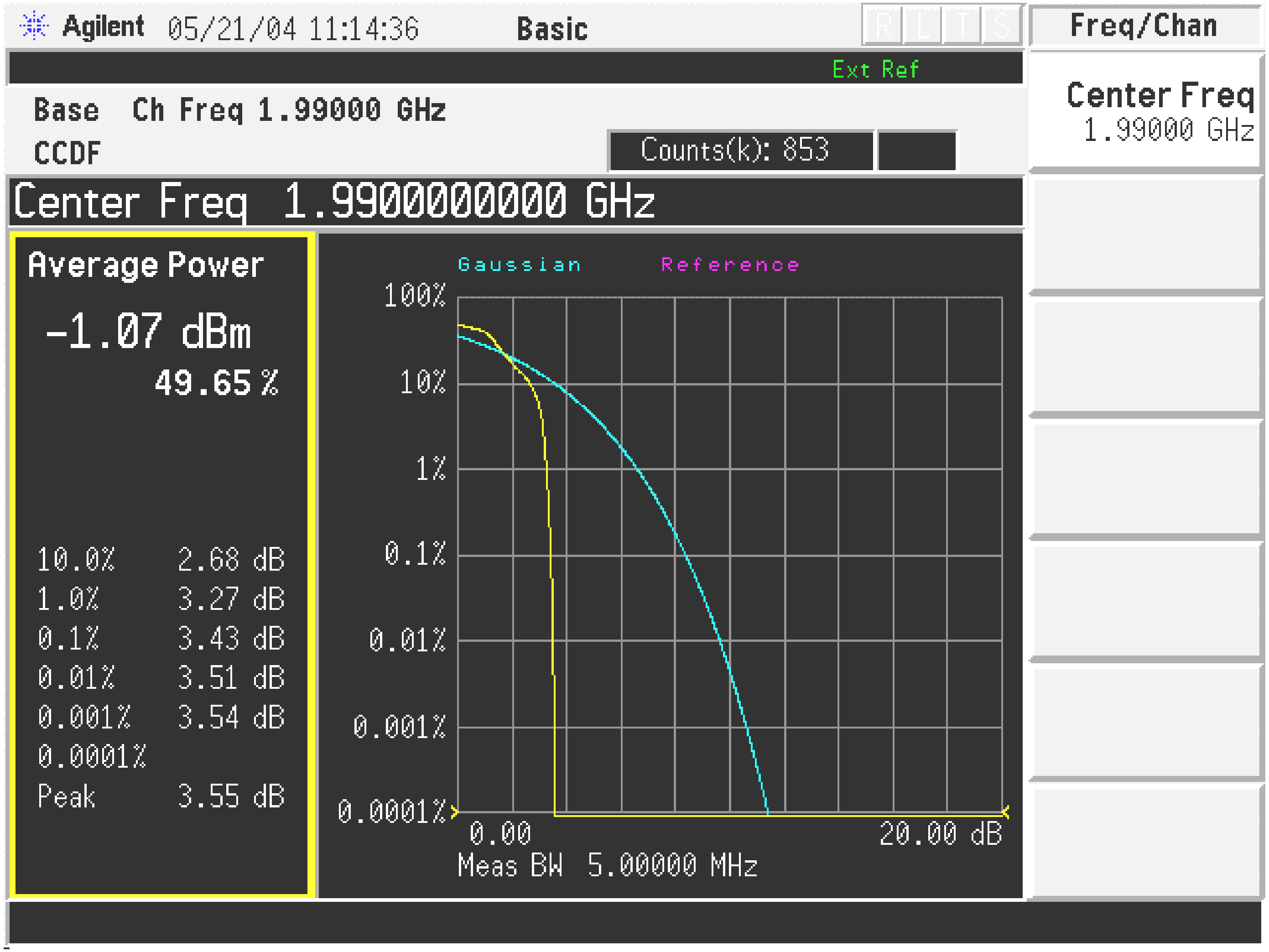

Ref Lvl
10 dBm
RBW 20 kHz
VBW 100 kHz
SWT 1 s
RF Att 20 dB
Mixer -10 dBm
Unit dB
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
A
1VIEW
2AVG
1RM
2RM
EXT
Amplifier Gain
400kHz ORFS
600kHz ORFS
Result after amplifier
Drive signal
Center 1.99 GHz
200 kHz/
Span 2 MHz
Date: 21.MAY.2004 13:39:09

Edge GSM Characterization

- Modulation: 8-PSK
- PAR=3.2-3.5dB
- Linearity:
  - EVM (Error Vector Magnitude)[%]
  - ORFS (Output RF spectrum)[dBc]
    - at offsets with 200kHz increments.
    - 400kHz and 600kHz are most critical ones



Edge GSM PAR



Agilent 05/21/04 11:14:36 Basic

Ext Ref

Base Ch Freq 1.99000 GHz

CCDF

Counts(k): 853

Center Freq 1.9900000000 GHz

Average Power

-1.07 dBm

49.65 %

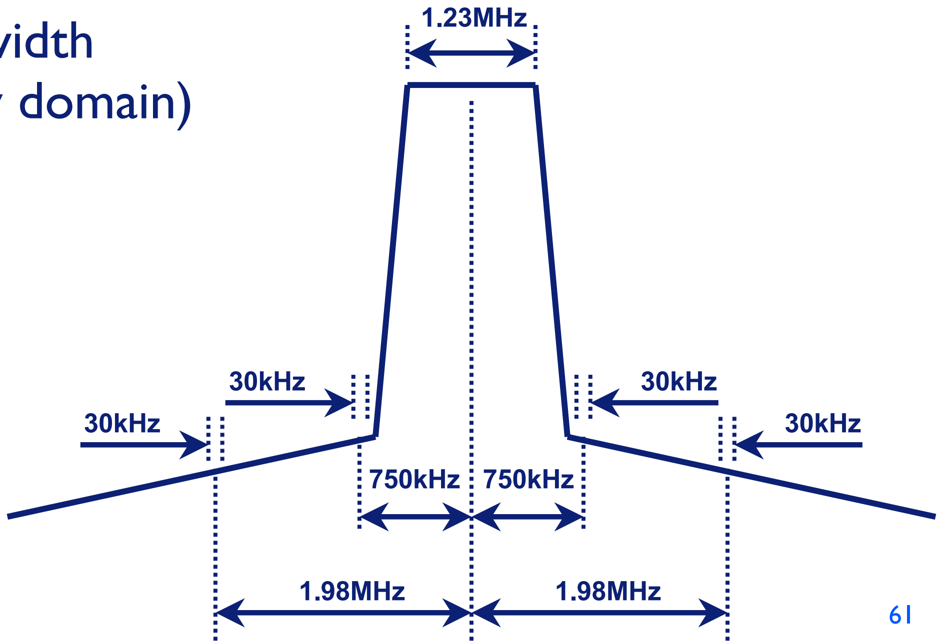
10.0%	2.68 dB
1.0%	3.27 dB
0.1%	3.43 dB
0.01%	3.51 dB
0.001%	3.54 dB
0.0001%	
Peak	3.55 dB

Meas BW 5.00000 MHz

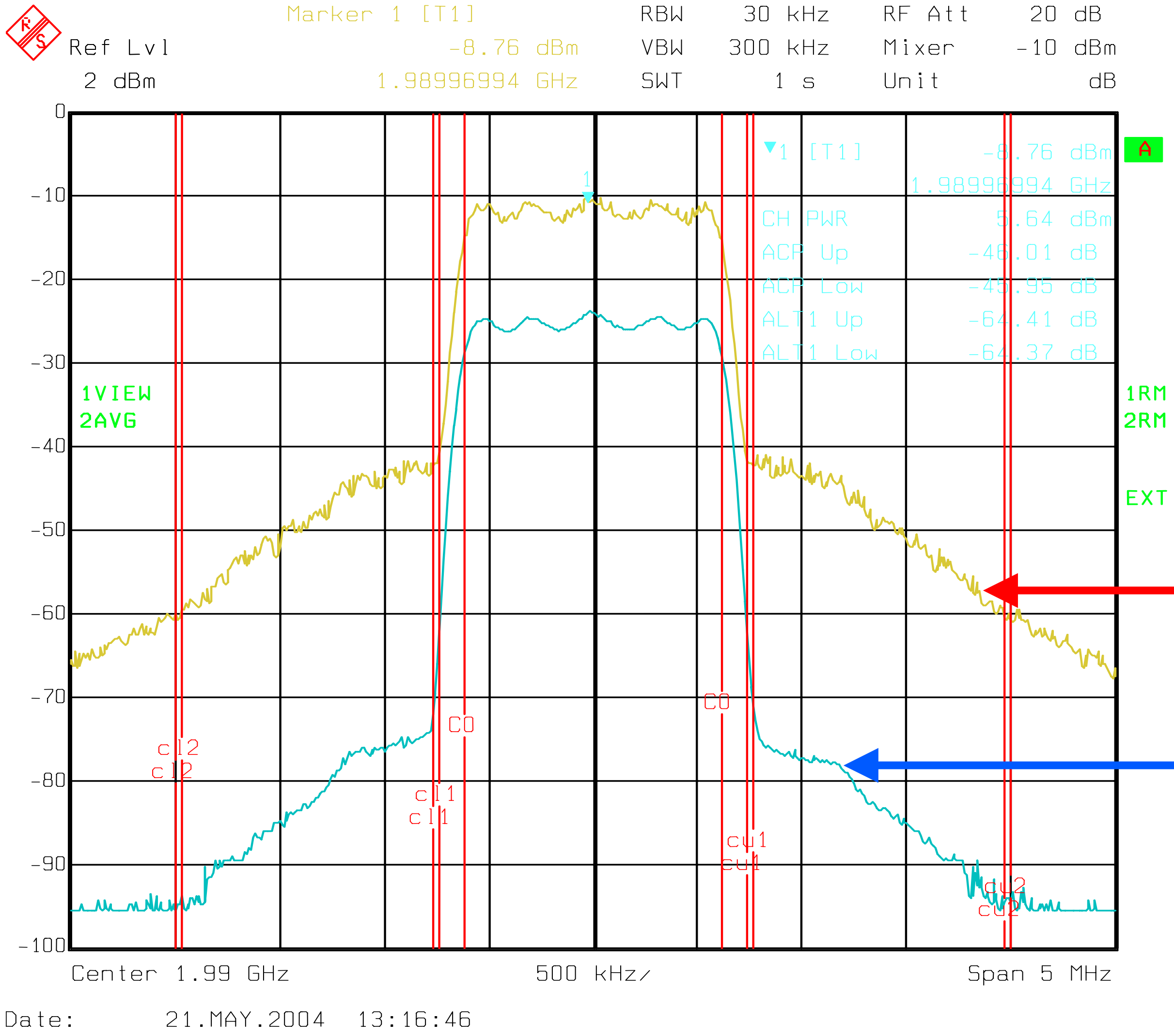
Center Freq 1.99000 GHz

CDMA

- Modulation: QPSK
- Channel bandwidth: 1.23MHz
- PAR=9.8dB (single carrier, not clipped)
- Linearity:
  - ACPR (Adjacent Channel Power Ratio)
    - at multiple offsets, 750kHz, 885kHz, 1.98MHz
    - in a certain integration bandwidth
      (a small slice in the frequency domain)



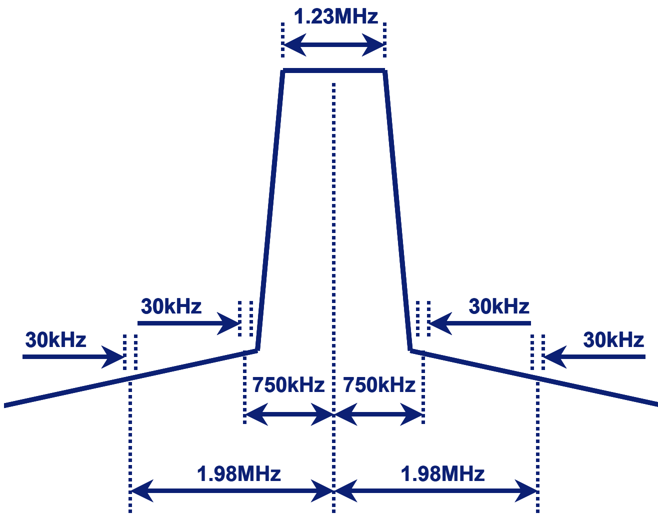
CDMA



```
Marker 1 [T1]              RBW    30 kHz     RF Att     20 dB
Ref Lvl        -8.76 dBm   VBW   300 kHz     Mixer     -10 dBm
 2 dBm    1.98996994 GHz   SWT       1 s     Unit          dB
```

```
▼1 [T1]              -8.76 dBm
                1.98996994 GHz
CH PWR                5.64 dBm
ACP Up              -46.01 dB
ACP Low             -45.95 dB
ALT1 Up             -64.41 dB
ALT1 Low            -64.37 dB
```

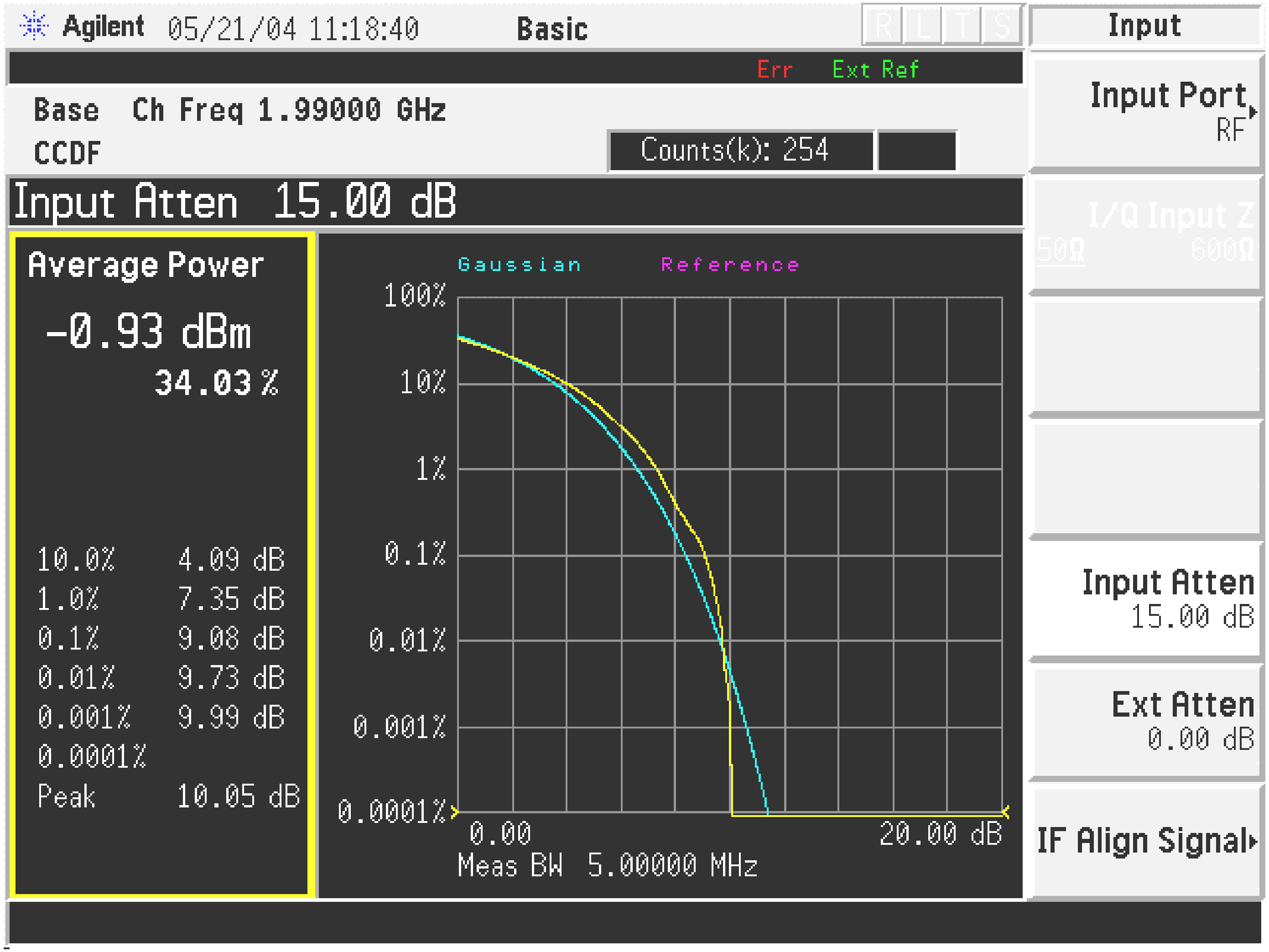
```
Center 1.99 GHz          500 kHz/          Span 5 MHz
Date:       21.MAY.2004   13:16:46
```



Result after amplifier

Drive signal

CDMA PAR



Agilent 05/21/04 11:18:40 Basic

Base Ch Freq 1.99000 GHz

CCDF

Counts(k): 254

Input Atten 15.00 dB

Average Power

-0.93 dBm

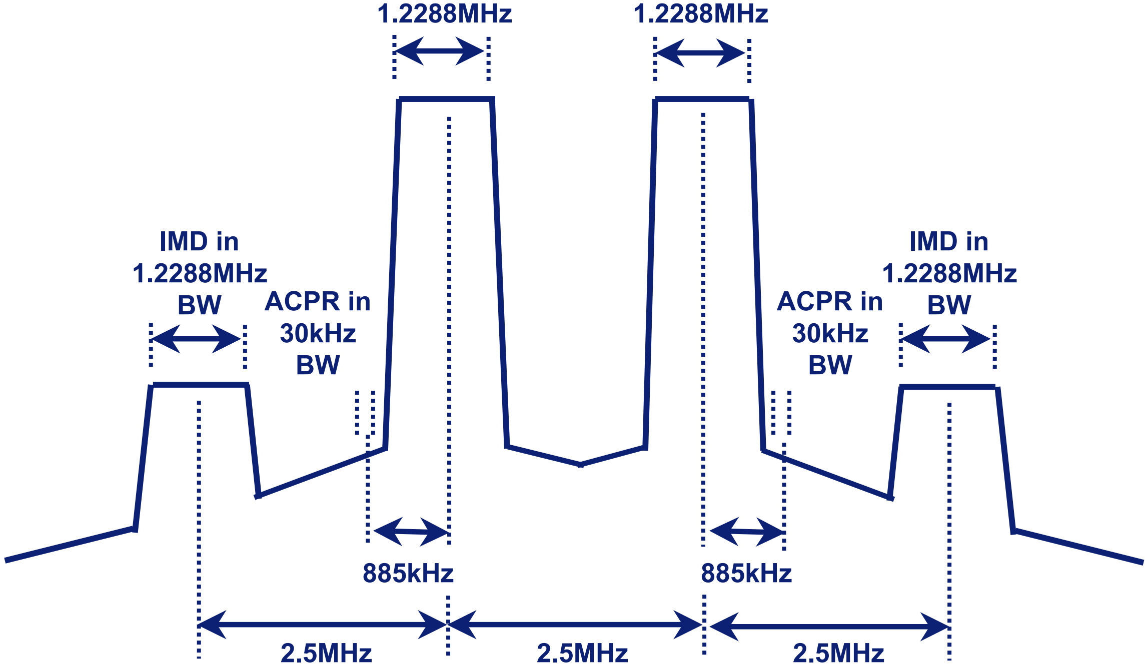
34.03 %

```
10.0%      4.09 dB
1.0%       7.35 dB
0.1%       9.08 dB
0.01%      9.73 dB
0.001%     9.99 dB
0.0001%
Peak      10.05 dB
```

Meas BW 5.00000 MHz

CDMA (Multi Carrier)

- Linearity:
  - ACPR (Adjacent Channel Power Ratio)
    - at 885kHz offset in 30kHz IBW
  - IMD (Intermodulation Distortion)
    - at offset depending on carrier spacing in 1.2288MHz IBW



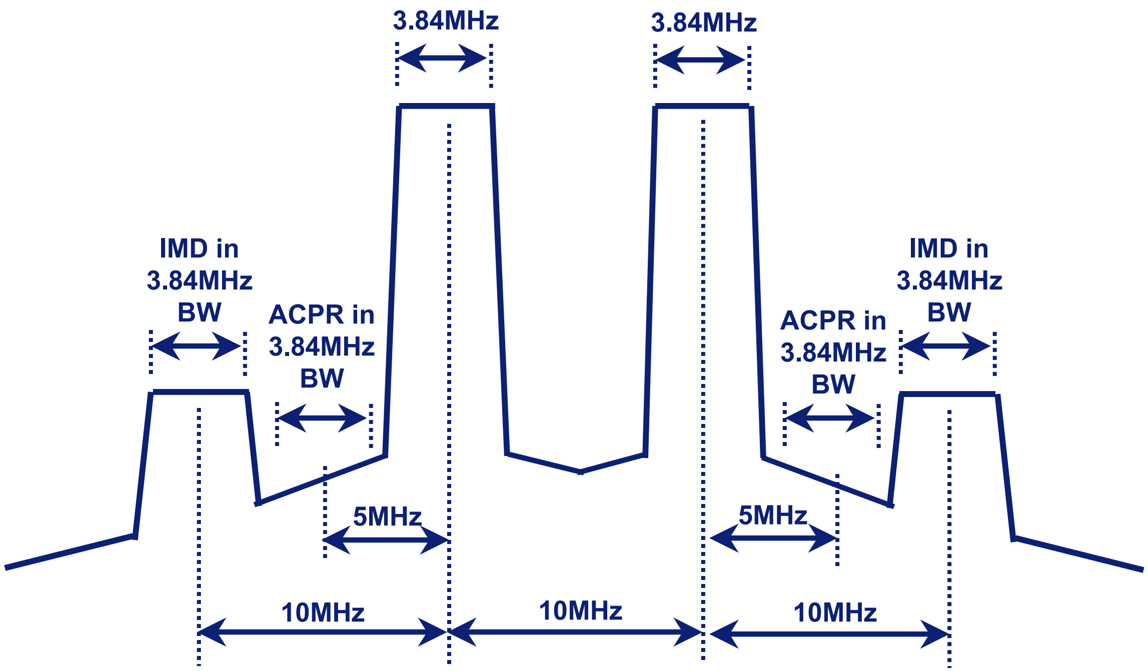
CDMA (Multi Carrier)

- Both ACPR and IMD are relative figures, with as reference one of the two (equal) carriers.
- Therefore, both ACPR and IMD are expressed in dBc.
- The offsets are defined from the center of the carriers.
- As can be seen is the IBW for the ACPR and IMD different. The IBW is defined by the standard.
- Sometimes the ACPR and/or IMD are also expressed in dBm, an actual power level. For that purpose the spectrum analyzer needs to be calibrated to read actual power levels.

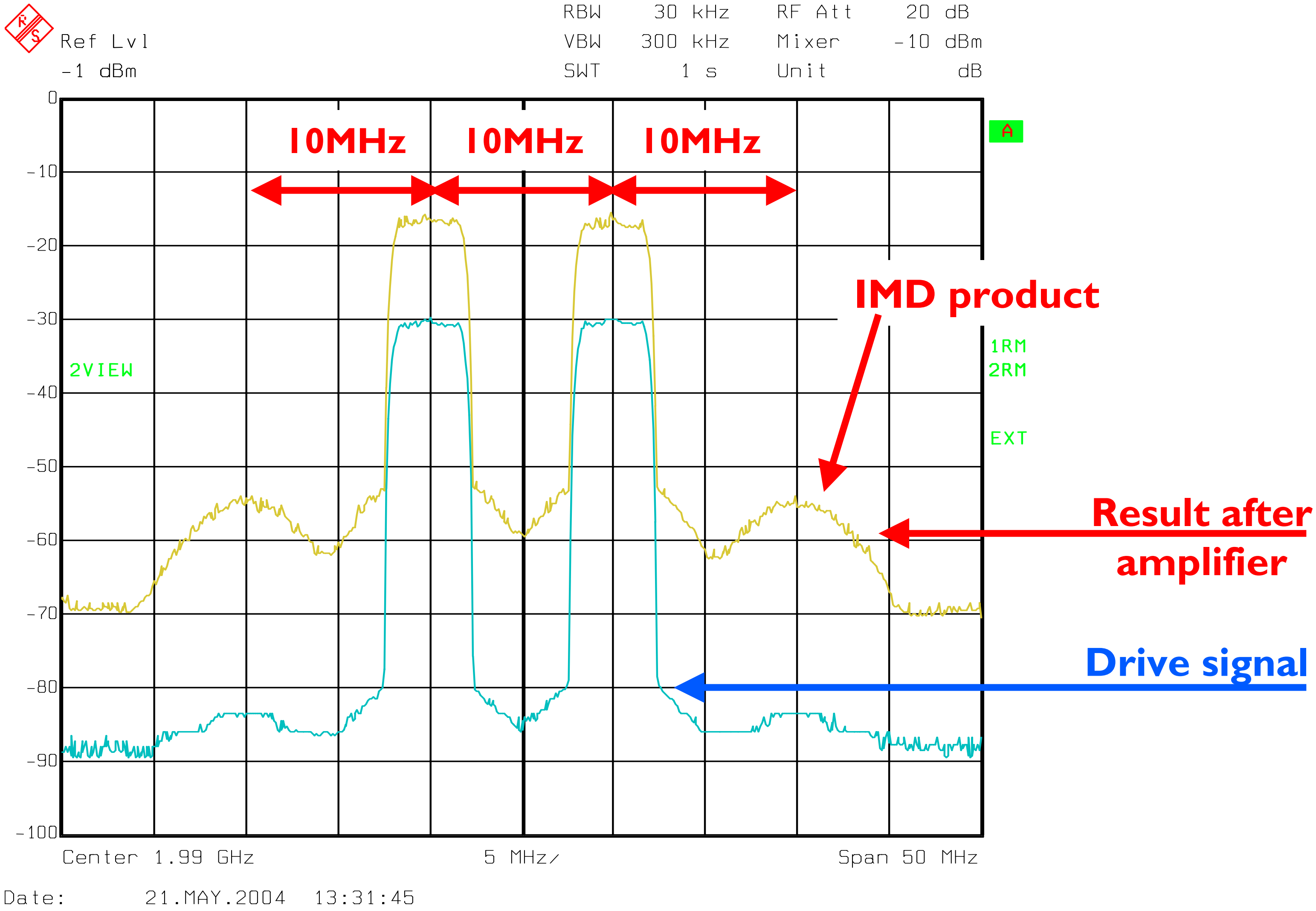
UMTS (Multi Carrier)

- Modulation: QPSK
- Channel bandwidth: 3.84MHz
- PAR=7-10dB (single carrier, depending on clipping)
- Linearity:
  - ACPR (Adjacent Channel Power Ratio)
    - at 5MHz offset in 3.84MHz IBW
  - IMD (Intermodulation Distortion)
    - at 10MHz offset for 10MHz carrier spacing in 3.84MHz IBW

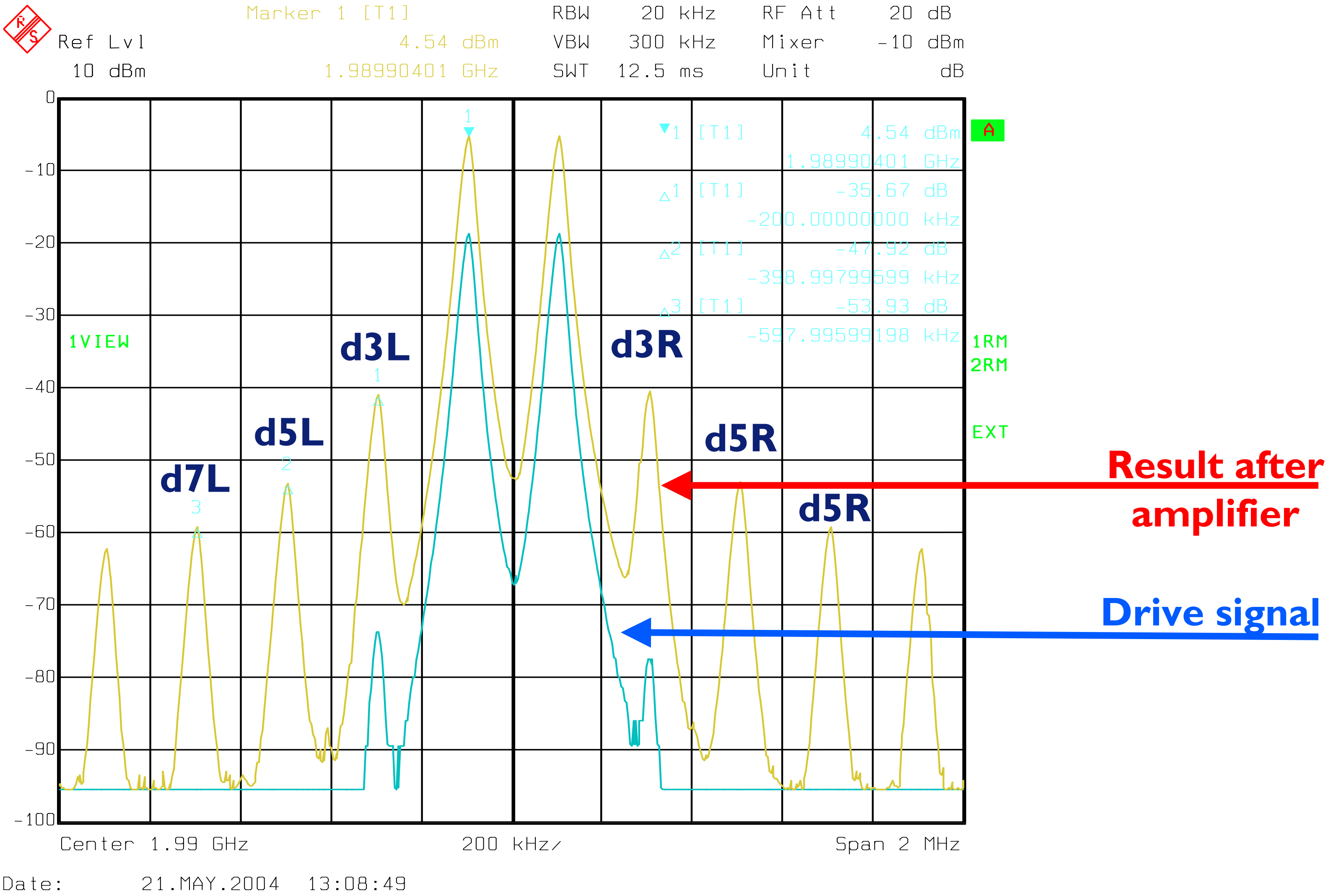
UMTS (Multi Carrier)



UMTS (Multi Carrier)



Two Tone CW

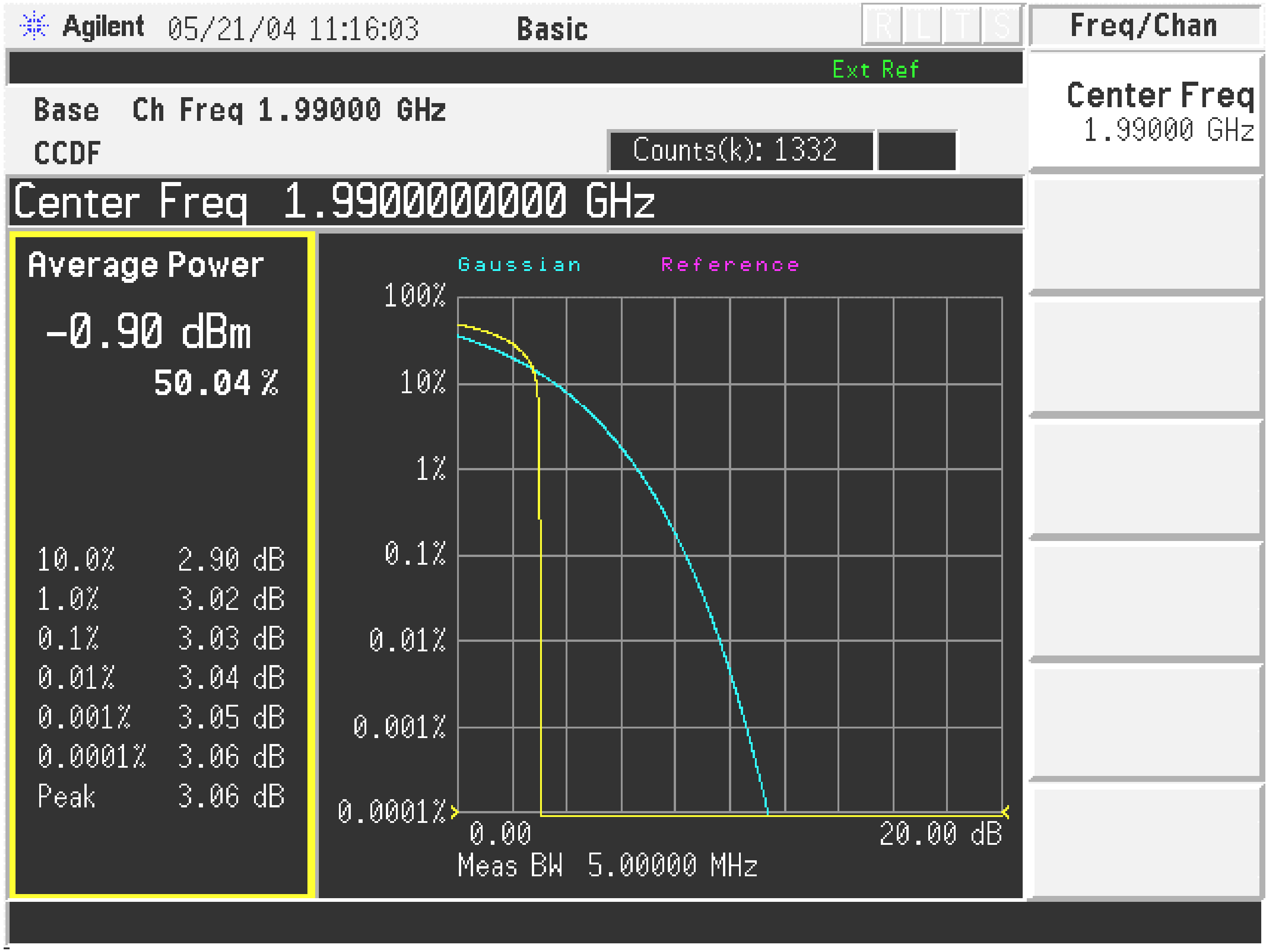


```
                 Marker 1 [T1]          RBW    20 kHz    RF Att    20 dB
Ref Lvl                 4.54 dBm        VBW   300 kHz    Mixer    -10 dBm
 10 dBm          1.98990401 GHz         SWT  12.5 ms     Unit        dB

▼1  [T1]         4.54 dBm
           1.98990401 GHz
Δ1  [T1]       -35.67 dB
      -200.00000000 kHz
Δ2  [T1]       -47.92 dB
      -398.99799599 kHz
Δ3  [T1]       -53.93 dB
      -597.99599198 kHz

Center 1.99 GHz            200 kHz/            Span 2 MHz

Date:      21.MAY.2004   13:08:49
```

Result after amplifier

Drive signal

Two Tone PAR



Agilent 05/21/04 11:16:03 Basic

Ext Ref

Base Ch Freq 1.99000 GHz

CCDF

Counts(k): 1332

Center Freq 1.9900000000 GHz

Average Power

-0.90 dBm

50.04 %

10.0%	2.90 dB
1.0%	3.02 dB
0.1%	3.03 dB
0.01%	3.04 dB
0.001%	3.05 dB
0.0001%	3.06 dB
Peak	3.06 dB

Meas BW 5.00000 MHz

Center Freq 1.99000 GHz

PHILIPS

Inside the RF Power transistor

Korné Vennema

Marketing Application Engineer RF Power Transistors and Modules

Philips Semiconductors
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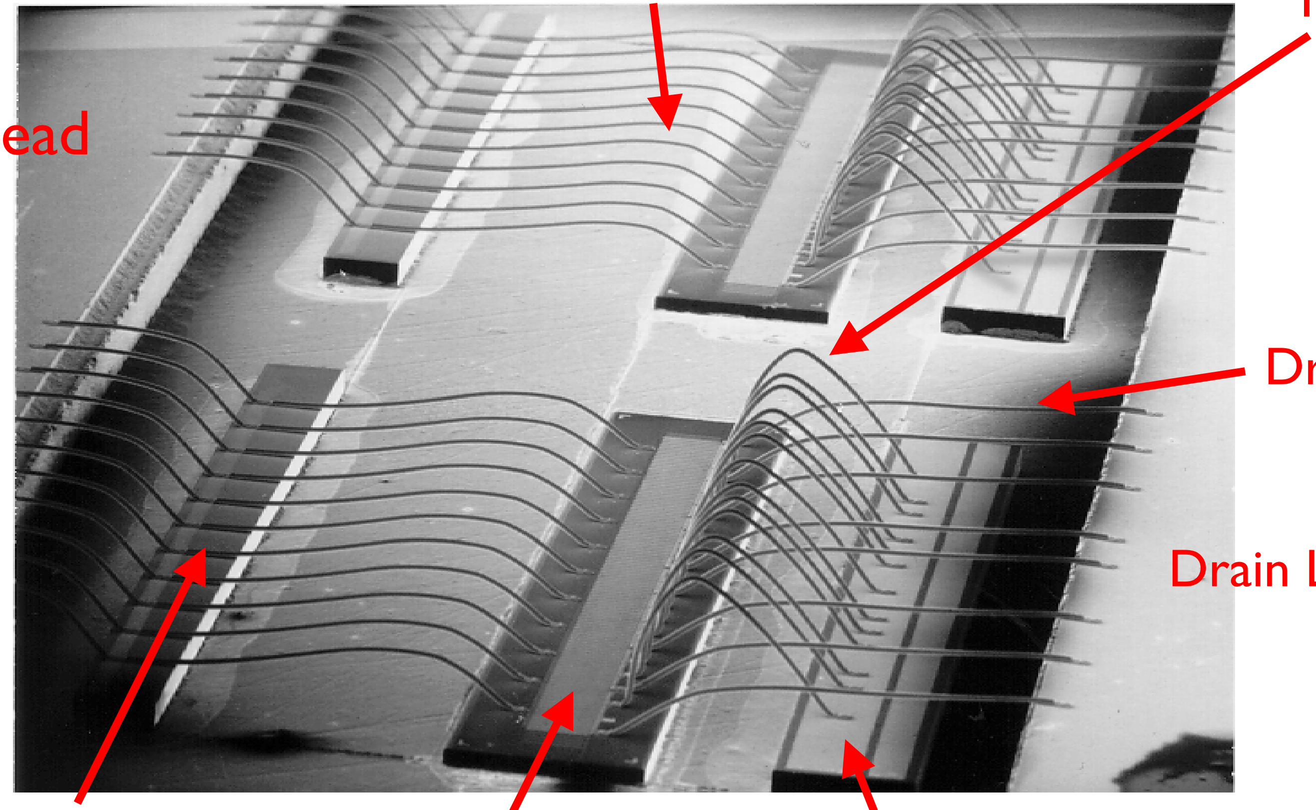
Foxborough MA 02035

A look inside the RF Power transistor



Gate wires

INSHIN wires

Gate Lead

Drain wires

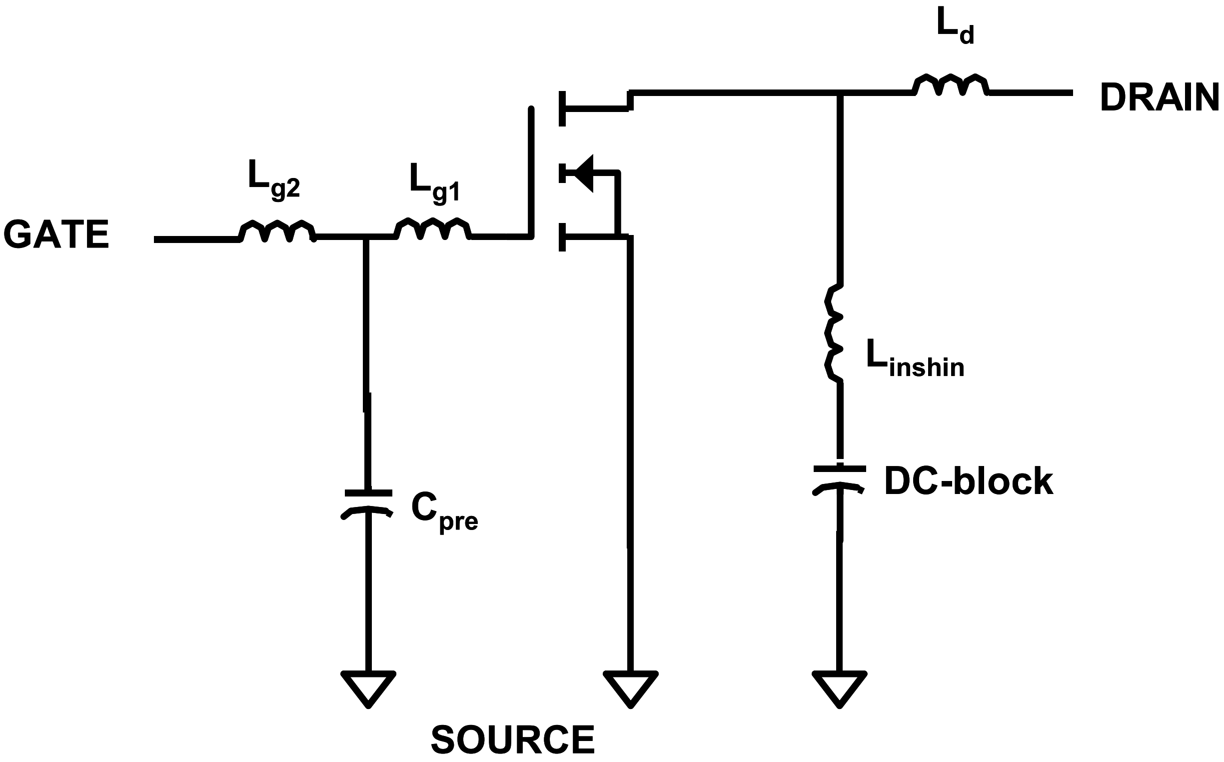
Drain Lead

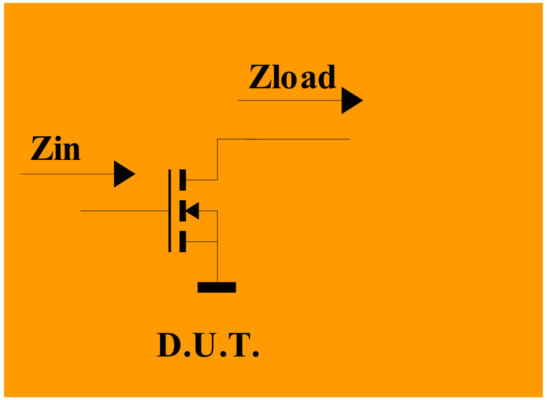
Pre-Match CMOS Capacitor

LDMOS Die

INSHIN CMOS Capacitor

Schematic



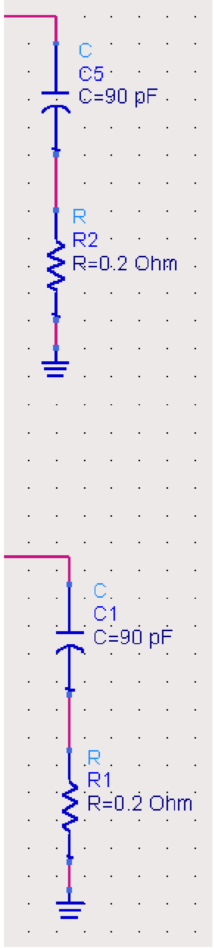


Z_{in} =R±jX
Z_{load} =R±jX

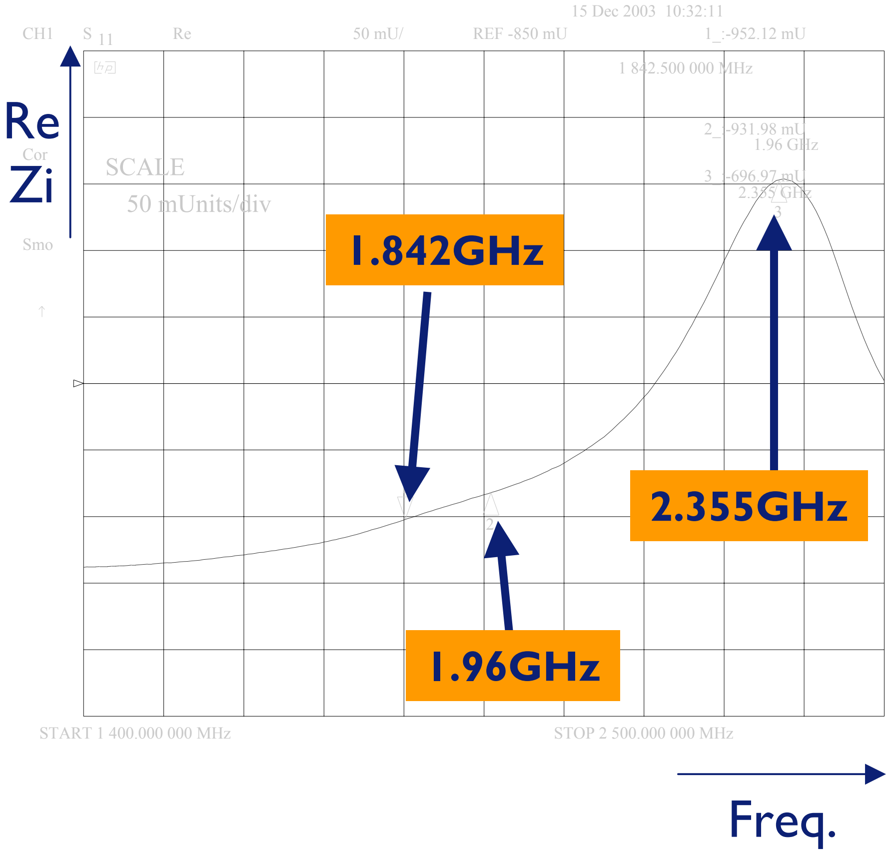
Why internal matching ?

- Impedance levels at the die are low. Extremely low. Internal matching brings these impedances to an acceptable level at the transistor terminals (leads) so the part can be matched more easily (also enable broadband matching) without too much insertion loss.
- To ensure a higher gain (transistor roll-off)

- The pre-match has a low pass characteristic. The output match has a high pass characteristic.
- Therefore, a transistor with pre- and output match inside has a band pass characteristic.



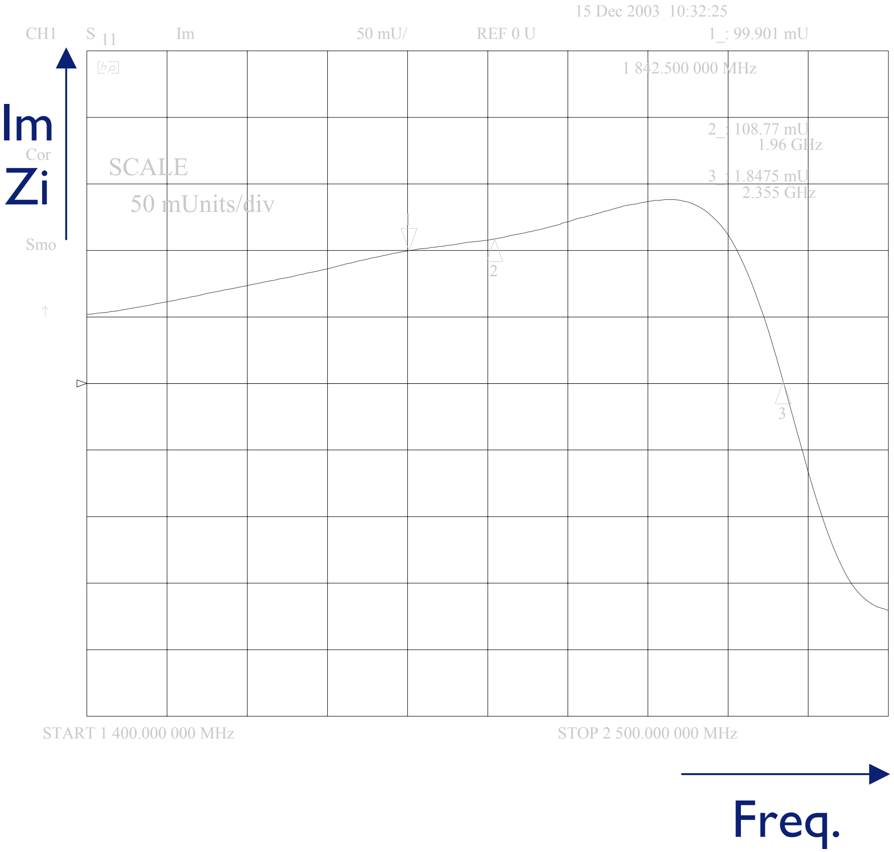
Input Resonance Frequency



1.842GHz

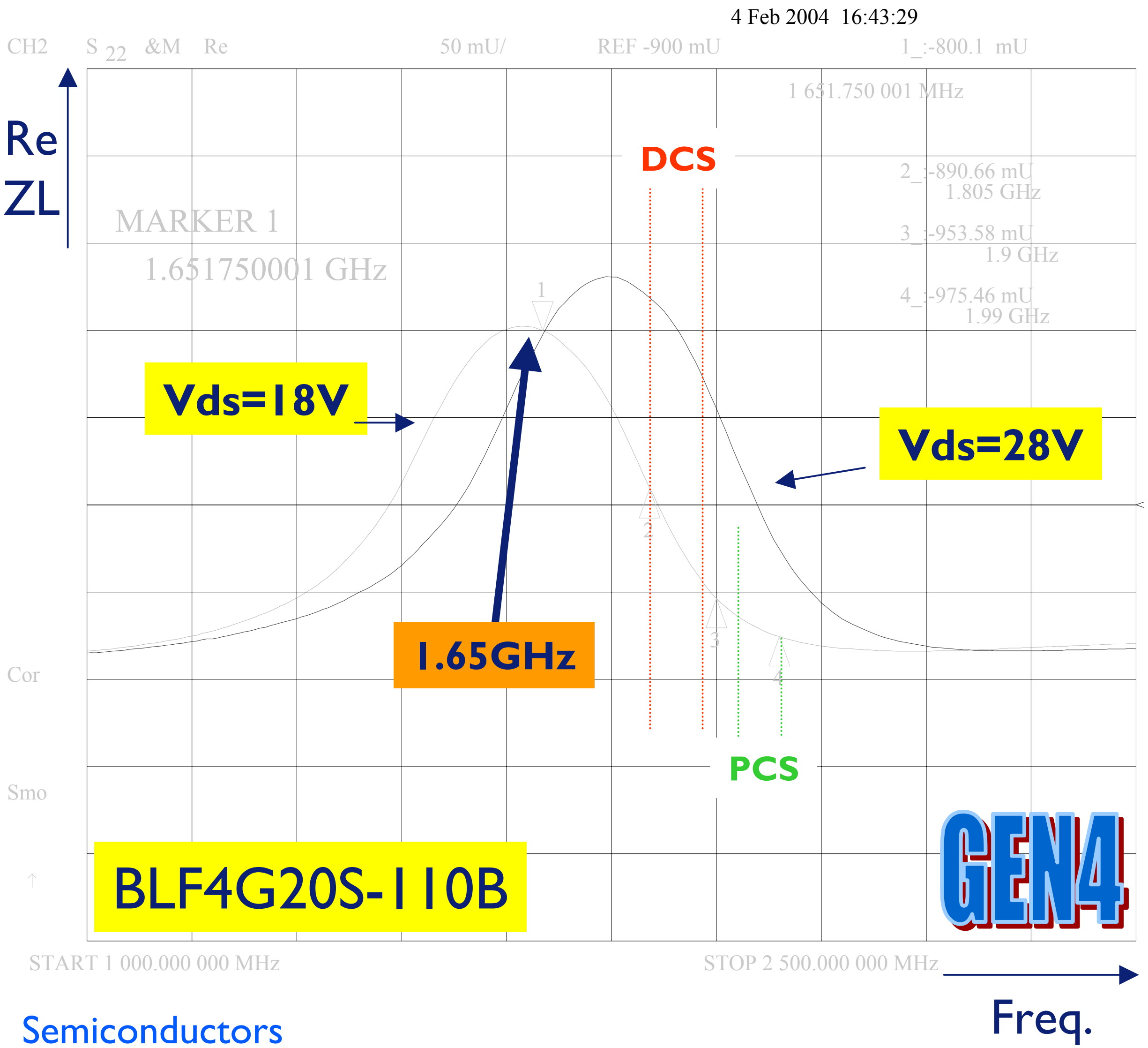
2.355GHz

1.96GHz



BLF4G20-110B

Output Resonance Frequency

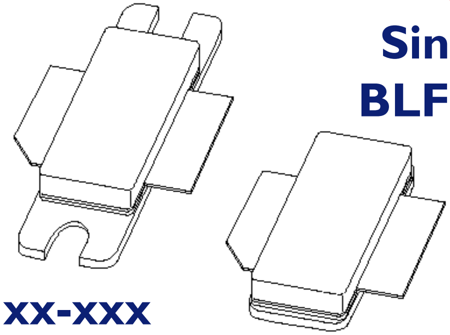


Typically:

Input resonance lies above the band of interest

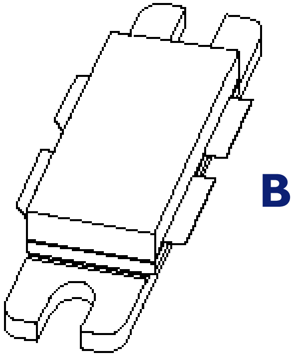
Output resonance lies below the band of interest.

Single Ended vs. Push-Pull



Single ended
BLF4Gxx-xxx

Earless
Single Ended
BLF4GxxS-xxx



Push-Pull
BLF4Gxx-xxx

A push-pull transistor is the same as two independent single ended transistors in one package (in most cases), operated 180° out of phase.

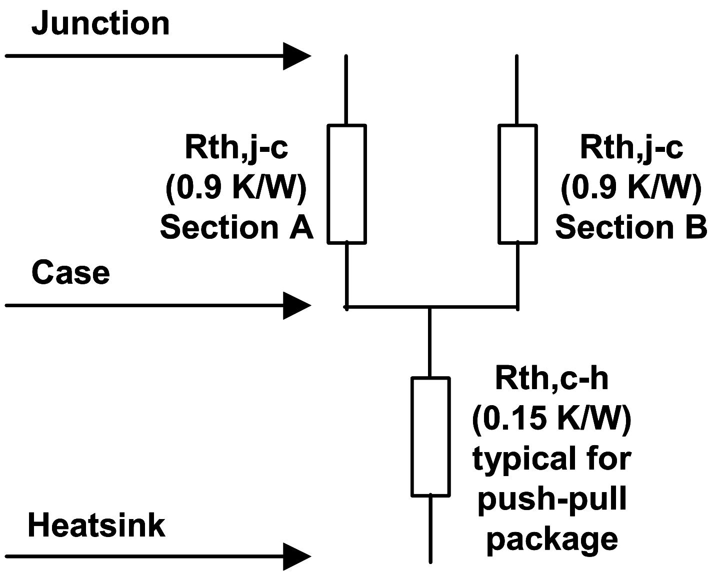
The advantages are:

- Higher impedances (between the two sections)
- Matched die
- 2^{nd} harmonic suppression

The disadvantages are

- More heat in a small area
- More expensive package

Thermal Resistance Push-Pull Transistor



Junction

Rth,j-c
(0.9 K/W)
Section A

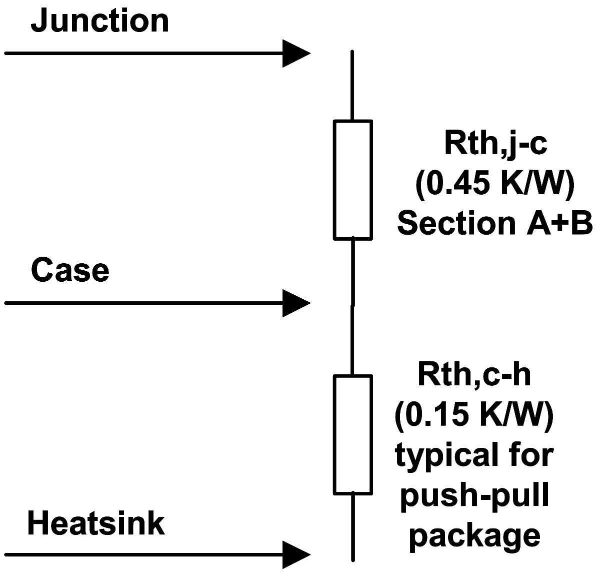
Rth,j-c
(0.9 K/W)
Section B

Case

Rth,c-h
(0.15 K/W)
typical for
push-pull
package

Heatsink

“Schematic” Thermal Resistance
Push-Pull Transistor
(split out per section)



Junction

Rth,j-c
(0.45 K/W)
Section A+B

Case

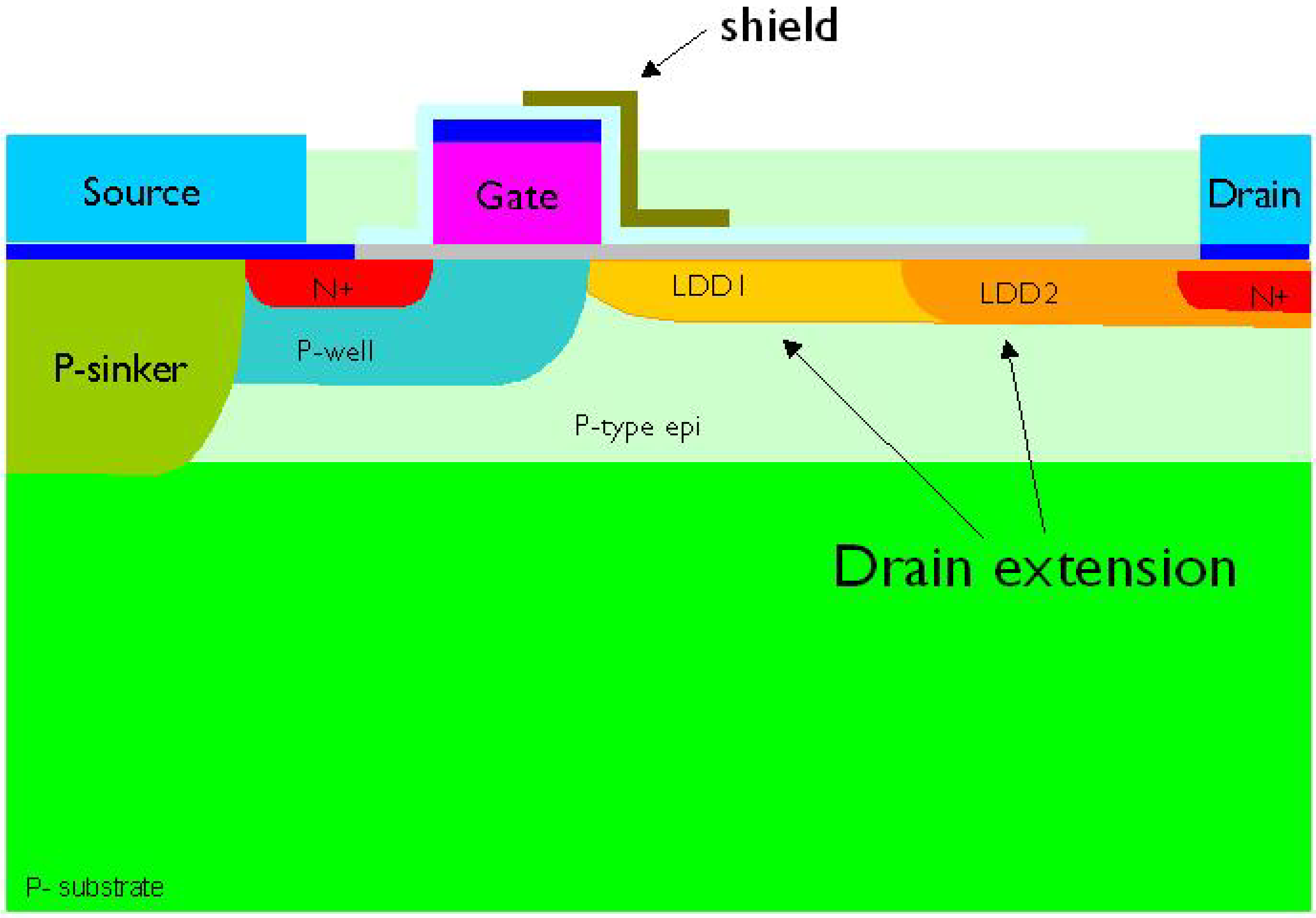
Rth,c-h
(0.15 K/W)
typical for
push-pull
package

Heatsink

“Schematic” Thermal Resistance
Total Push-Pull Transistor

Definition thermal resistance push-pull transistor

LDMOS Structure

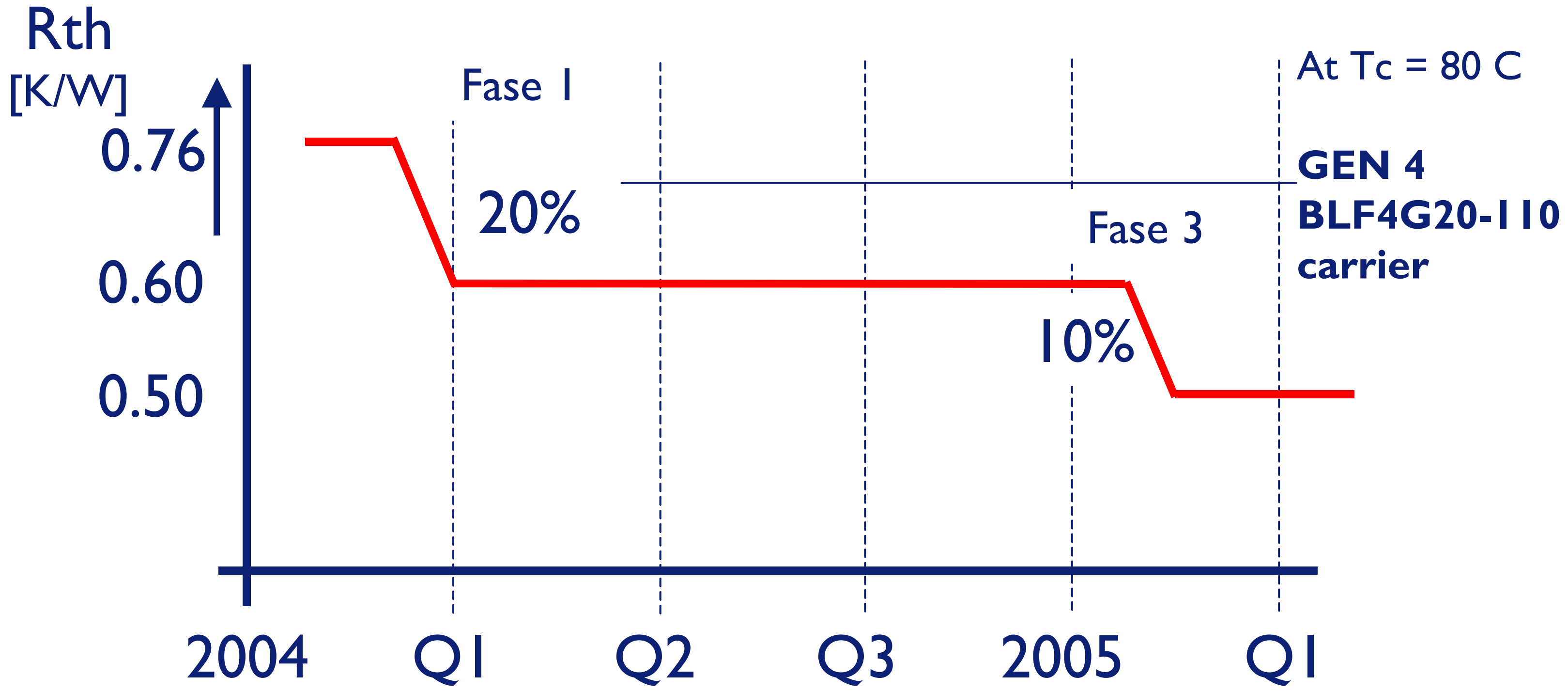


LDMOS Cross Section

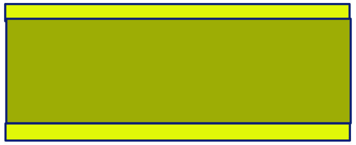
- Drain extension sets:
  - Idq drift
  - Breakdown voltage
  - Rds-on (doping amount)
  - Idsx (saturation current / peak power capability)
- Shield sets:
  - Feedback capacitance
  - Field distribution in drain extension (Idq-drift)

Packaging

- **Focus**
  - **lower thermal resistance**
    - **the package**
    - **the die layout**
  - **cheaper**
    - **plastic**
    - **cheaper package**

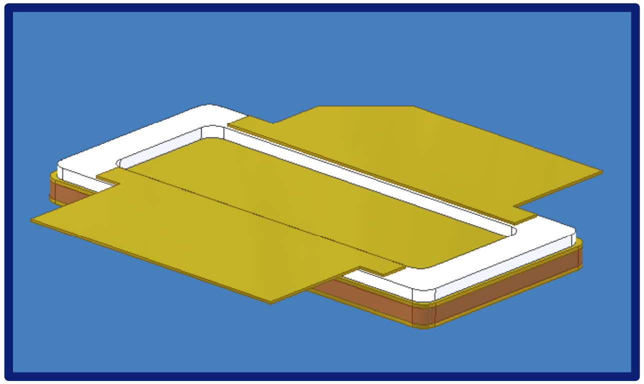


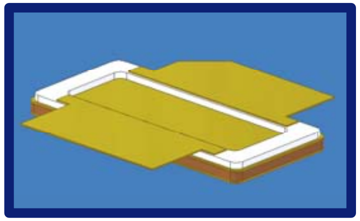
Packaging

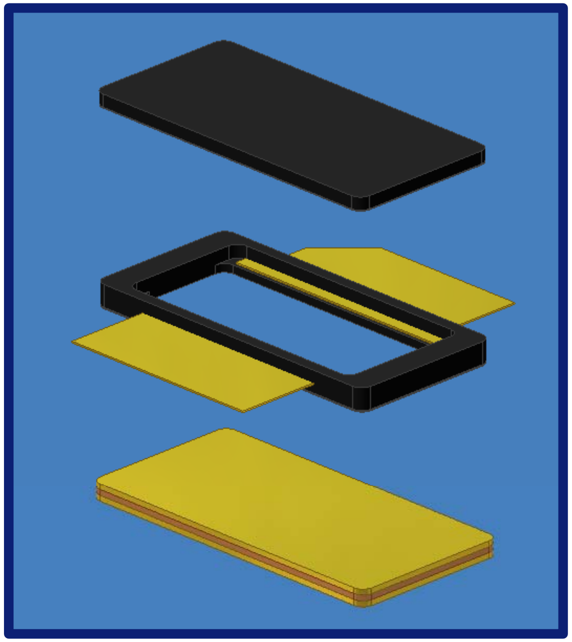


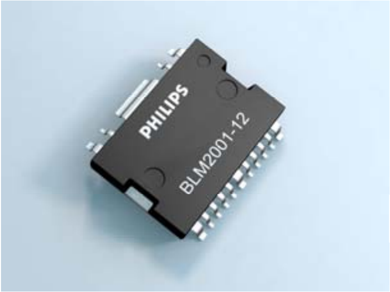
Cu - CuMO - Cu

CuW - Cu on top









PHILIPS

Transistor Characteristics

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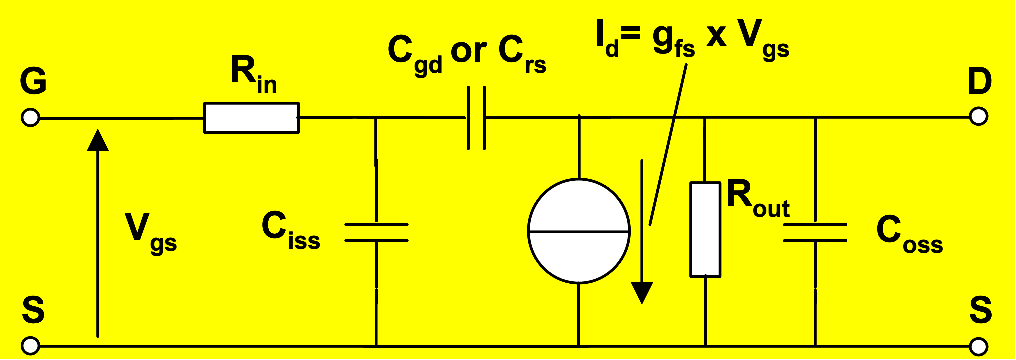
Marketing Application Engineer RF Power Transistors and Modules
Philips Semiconductors
25 Forbes Boulevard,
Foxborough MA 02035

Typical LDMOS Characteristics



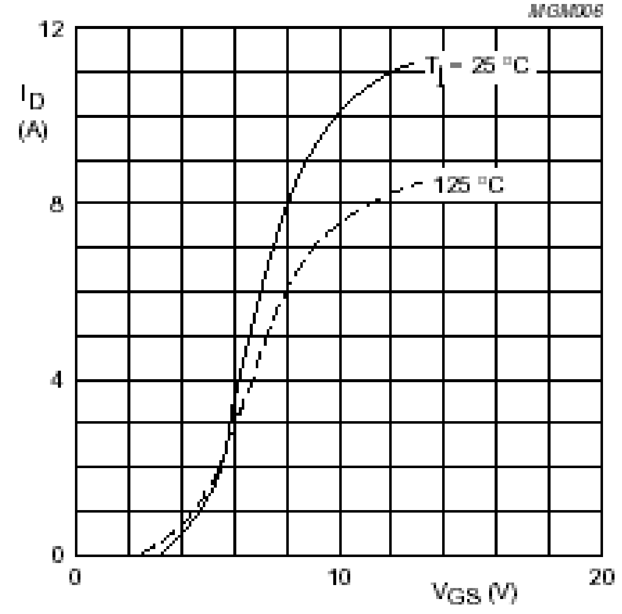
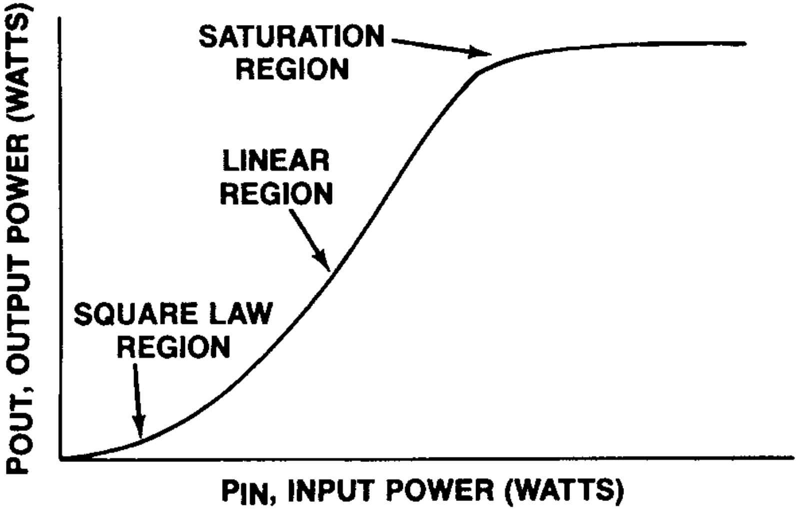
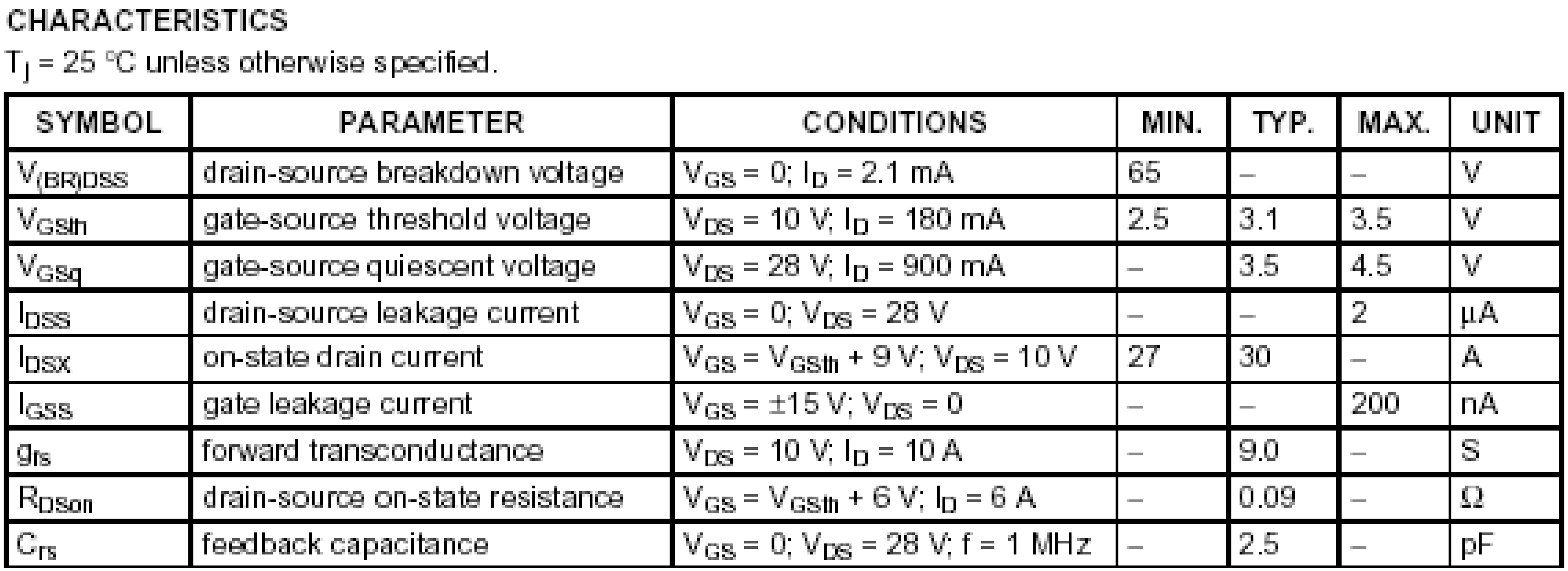


Fig.1-8 At high drain currents, the negative temperature coefficient of the drain current vs. gate voltage protects against thermal runaway.



LDMOS DC Characteristics



CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

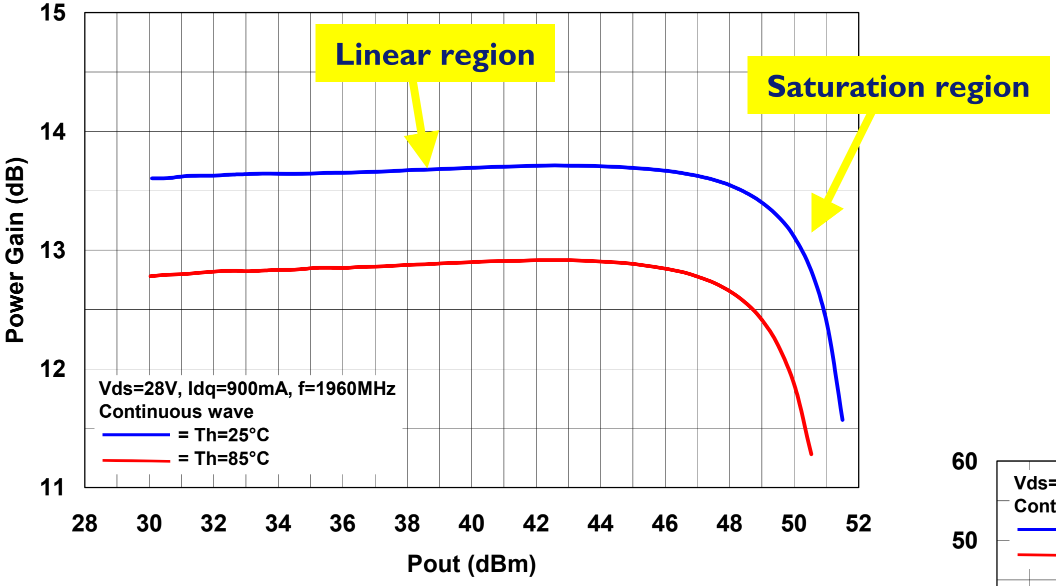
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$; $I_D = 2.1$ mA	65	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = 10$ V; $I_D = 180$ mA	2.5	3.1	3.5	V
V_{GSq}	gate-source quiescent voltage	$V_{DS} = 28$ V; $I_D = 900$ mA	–	3.5	4.5	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0$; $V_{DS} = 28$ V	–	–	2	µA
I_{DSX}	on-state drain current	$V_{GS} = V_{GSth} + 9$ V; $V_{DS} = 10$ V	27	30	–	A
I_{GSS}	gate leakage current	$V_{GS} = \pm 15$ V; $V_{DS} = 0$	–	–	200	nA
g_{fs}	forward transconductance	$V_{DS} = 10$ V; $I_D = 10$ A	–	9.0	–	S
R_{DSon}	drain-source on-state resistance	$V_{GS} = V_{GSth} + 6$ V; $I_D = 6$ A	–	0.09	–	Ω
C_{rs}	feedback capacitance	$V_{GS} = 0$; $V_{DS} = 28$ V; f = 1 MHz	–	2.5	–	pF

- $V_{(BR)DSS}$ = break down voltage DS-junction
- V_{gsth} = GS-voltage at which the device starts drawing current
- V_{gsq} = GS-voltage for a typical Idq (quiescent current)
- I_{dss} = Leakage current due to imperfections in epi-payer with no GS-voltage applied

LDMOS DC Characteristics

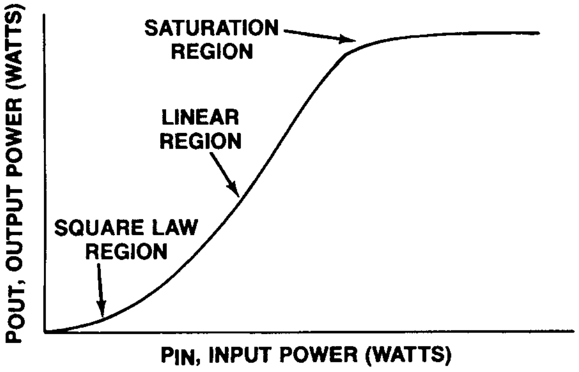
- I_{dss} = Leakage current due to imperfections in epi-payer with no GS-voltage applied
- Idsx = Maximum *saturated* drain current with high V_{gs}
- Igss = Gate leakage current (oxide and other imperfections)
- G_{fs} = Forward transconductance in Siemens (S = A/V)
- $R_{ds\text{-}on}$ = Drain source on-resistance (substrate / doping / wire bonds)
- C_{rs} = Feedback capacitance

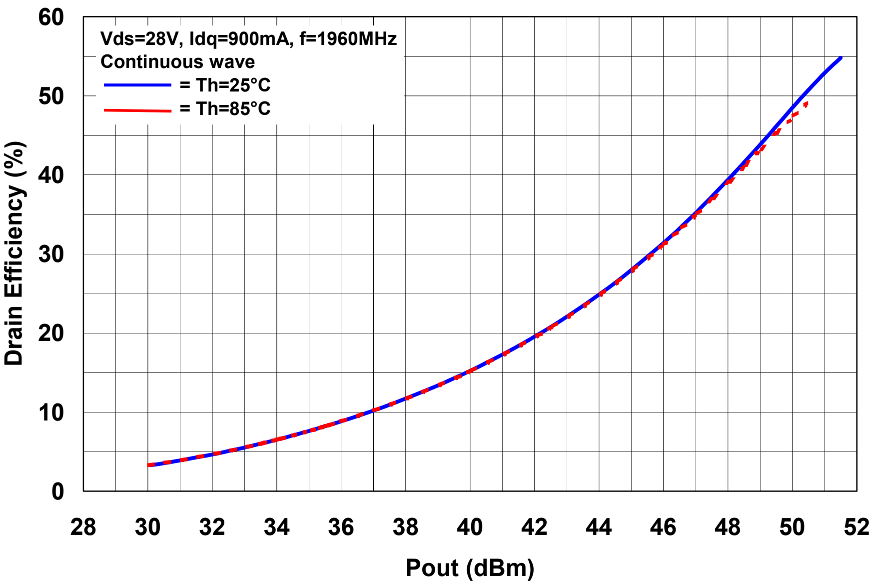
Typical RF Power Characteristics


Linear region

Saturation region

Power gain vs. Pout
&
Efficiency vs. Pout
at different Th
Continuous Wave (CW)

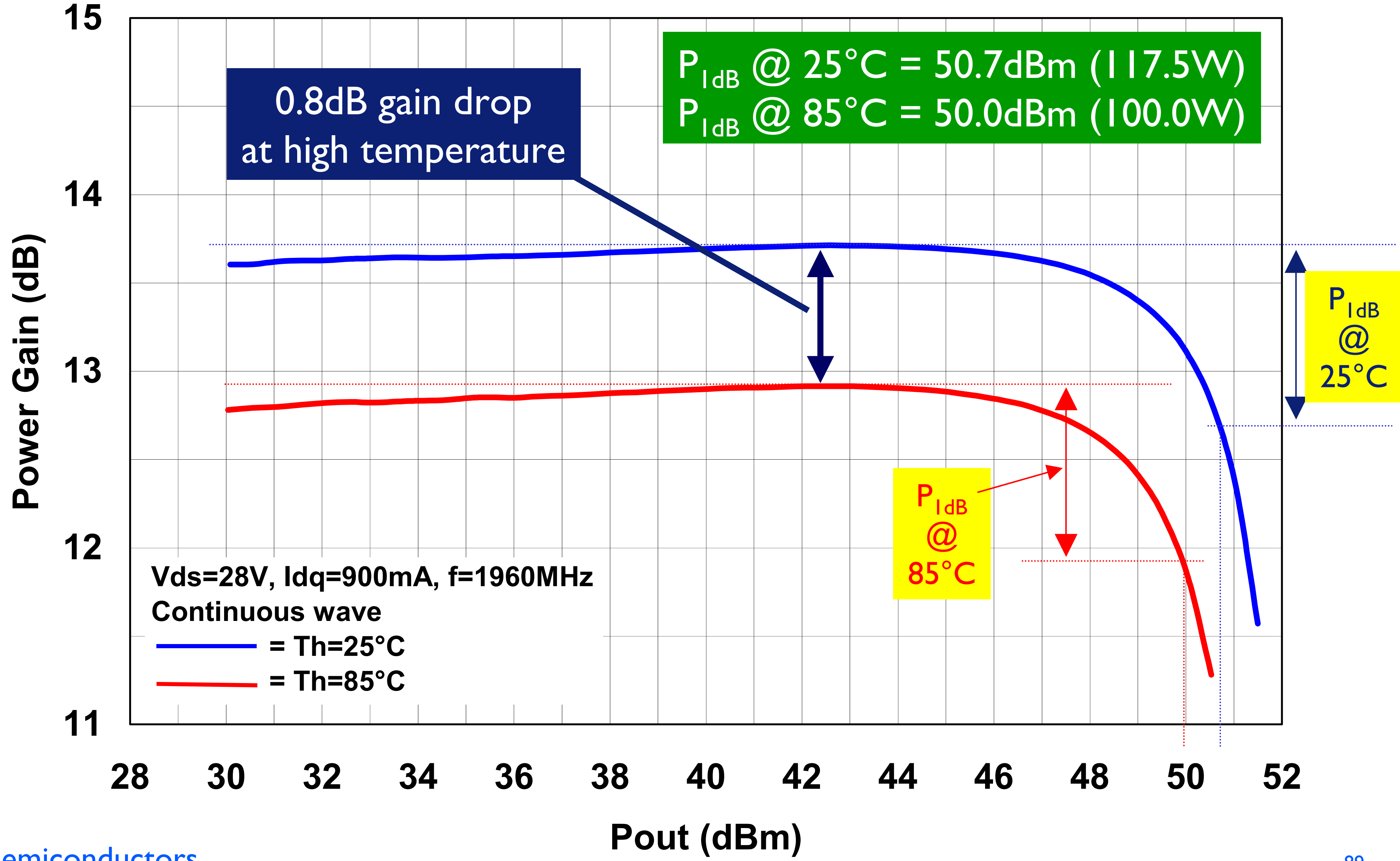




Typical RF Power Characteristics

- P_{1dB} is the output power level where the power gain is 1dB compressed.
- The saturation power (P_{sat}) is the output power level where ΔP_{out}: ΔP_{in}=1
- P_{1dB} and P_{sat} are (die) temperature dependent, which is the reason why the real P_{sat} is often determined under pulsed conditions to keep the average P_{out} –and thus the die temperature- low

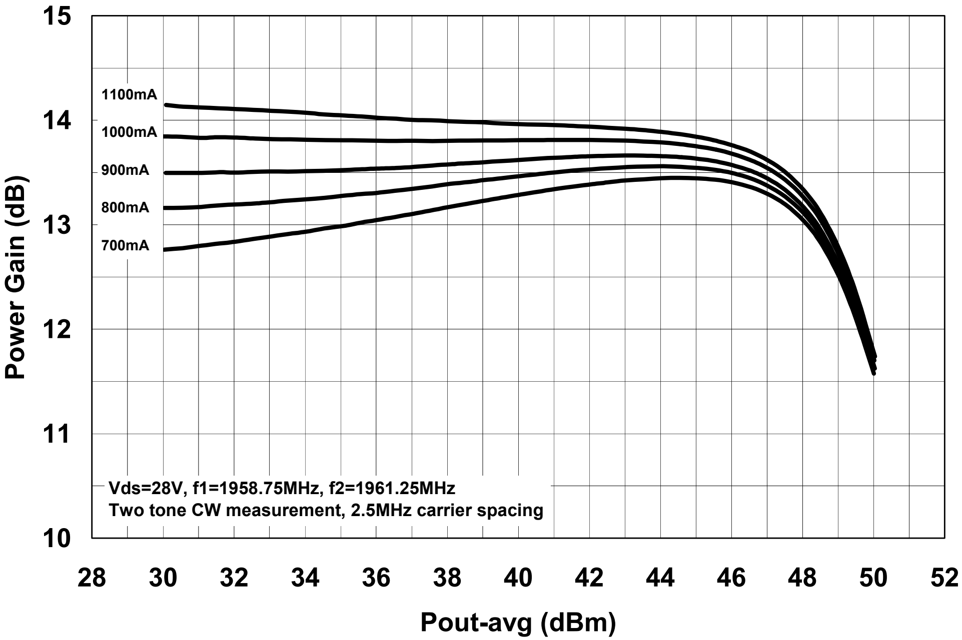
Typical RF Power Characteristics



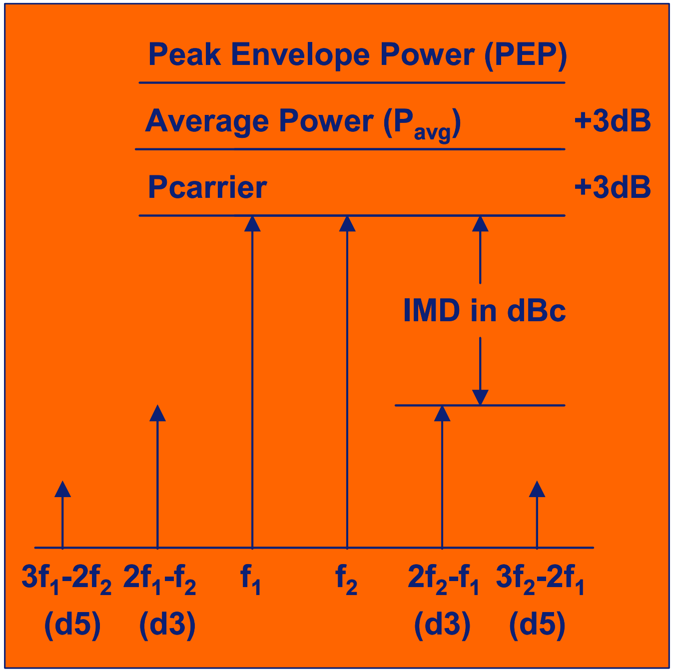
Considerations at high temperature

- The following transistor characteristics have to be accounted for during amplifier design:
  - The gain of a transistor is lower (ca. 0.8dB) at T_h=85°C. This requires a more powerful driver transistor.
  - The P_{1dB} and P_{sat} are lower at T_h=85°C. This has a negative effect on linearity.
  - The transistor life time reduces at higher temperatures.
  - The transistor efficiency does not change a lot at higher temperatures.

RF Power Characteristics



Vds=28V, f1=1958.75MHz, f2=1961.25MHz
Two tone CW measurement, 2.5MHz carrier spacing



Peak Envelope Power (PEP)

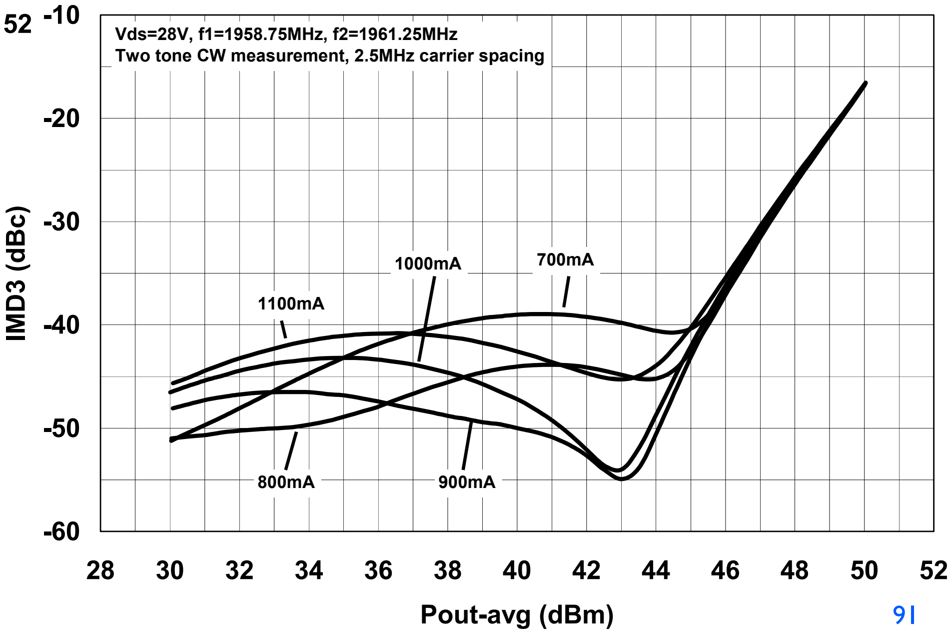
Average Power (P_{avg}) **+3dB**

Pcarrier **+3dB**

IMD in dBc

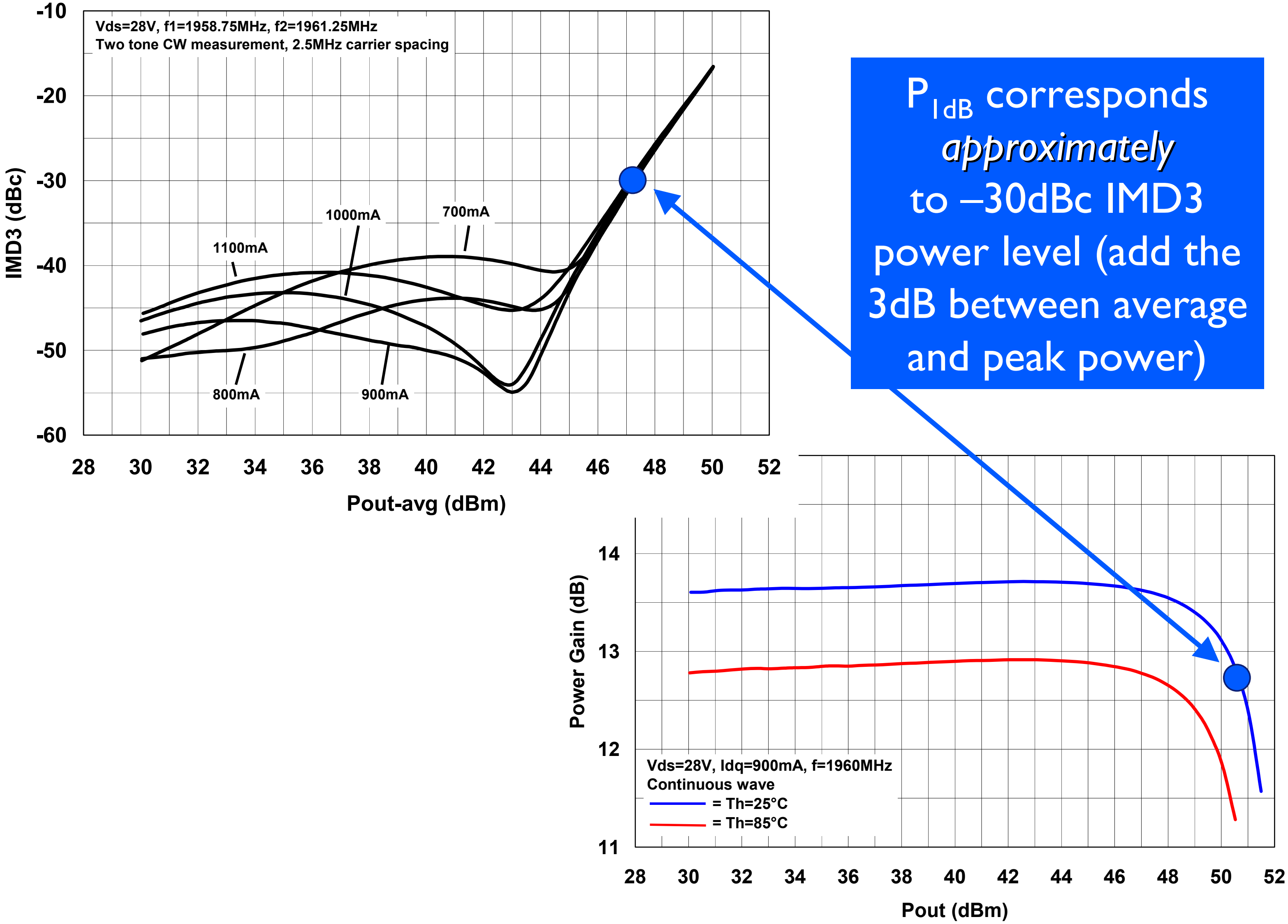
$3f_1$-$2f_2$ (d5) **$2f_1$-f_2 (d3)** **f_1** **f_2** **$2f_2$-f_1 (d3)** **$3f_2$-$2f_1$ (d5)**

Power gain vs. Pout
&
IMD3 vs. Pout
Two Tone CW



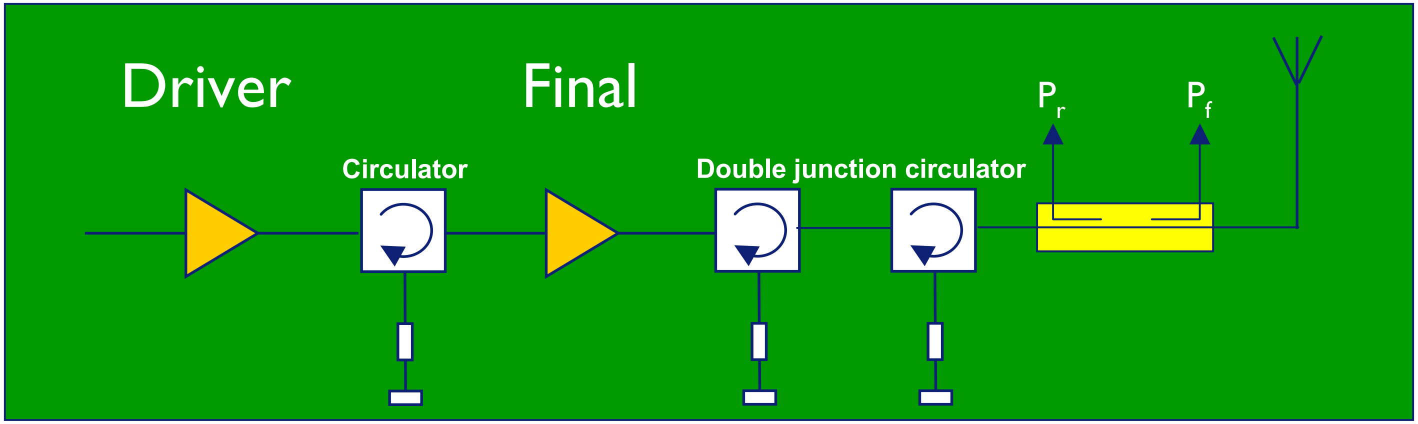
Vds=28V, f1=1958.75MHz, f2=1961.25MHz
Two tone CW measurement, 2.5MHz carrier spacing

P1dB and 2T CW linearity



P_{1dB} corresponds *approximately* to –30dBc IMD3 power level (add the 3dB between average and peak power)

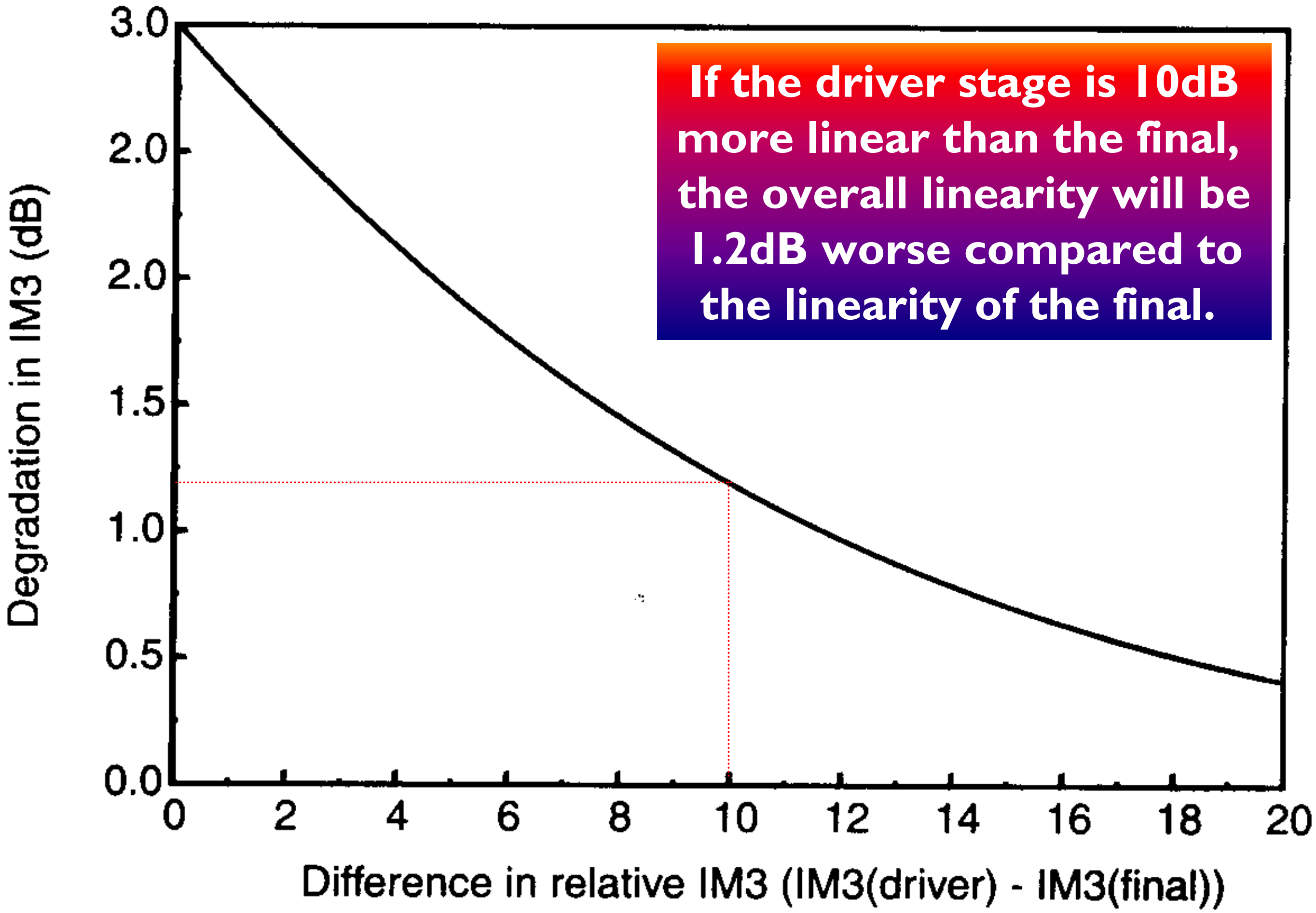
Two Tone Linearity & Multi Stage Amplifiers



- The overall (2T) linearity of an amplifier is determined by the linearity of both the final and driver stage. In this case we'll assume circulators don't degrade linearity which is not true.
- The degradation in IMD3 can be expressed as follows:

$$IMD3\ Degradation[dB] = 10\log\left[1 + 10^{\frac{IMD(Driver) - IMD3(Final)}{20}}\right]$$

Two Tone Linearity & Multi Stage Amplifiers



If the driver stage is 10dB more linear than the final, the overall linearity will be 1.2dB worse compared to the linearity of the final.

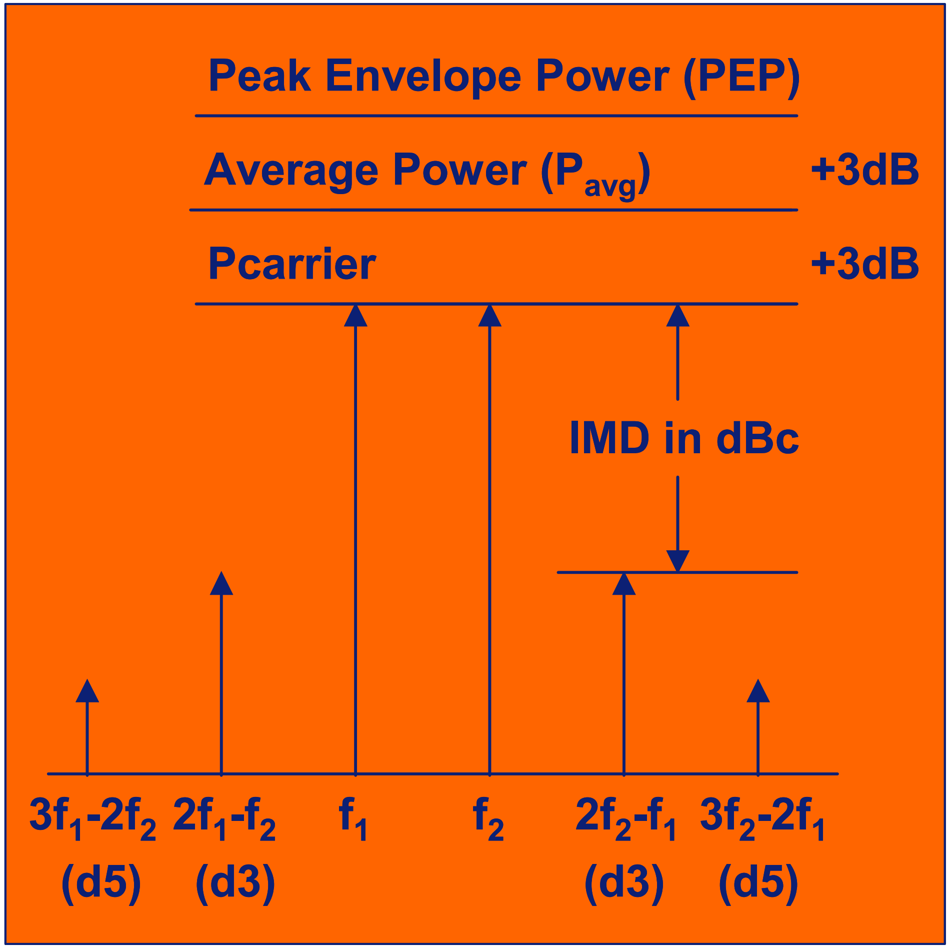
Notes on Peak-to-Average ratio (PAR)

- Peak-to-Average Ratio (PAR) is defined as the *ratio* of the peak power to ***average*** power.

$$\boxed{PAR = \frac{Peak\ \ Power}{Average\ \ Power}[-]}$$

- When the PAR=2, one also says often: The PAR=3dB (10log2).

Notes on PAR

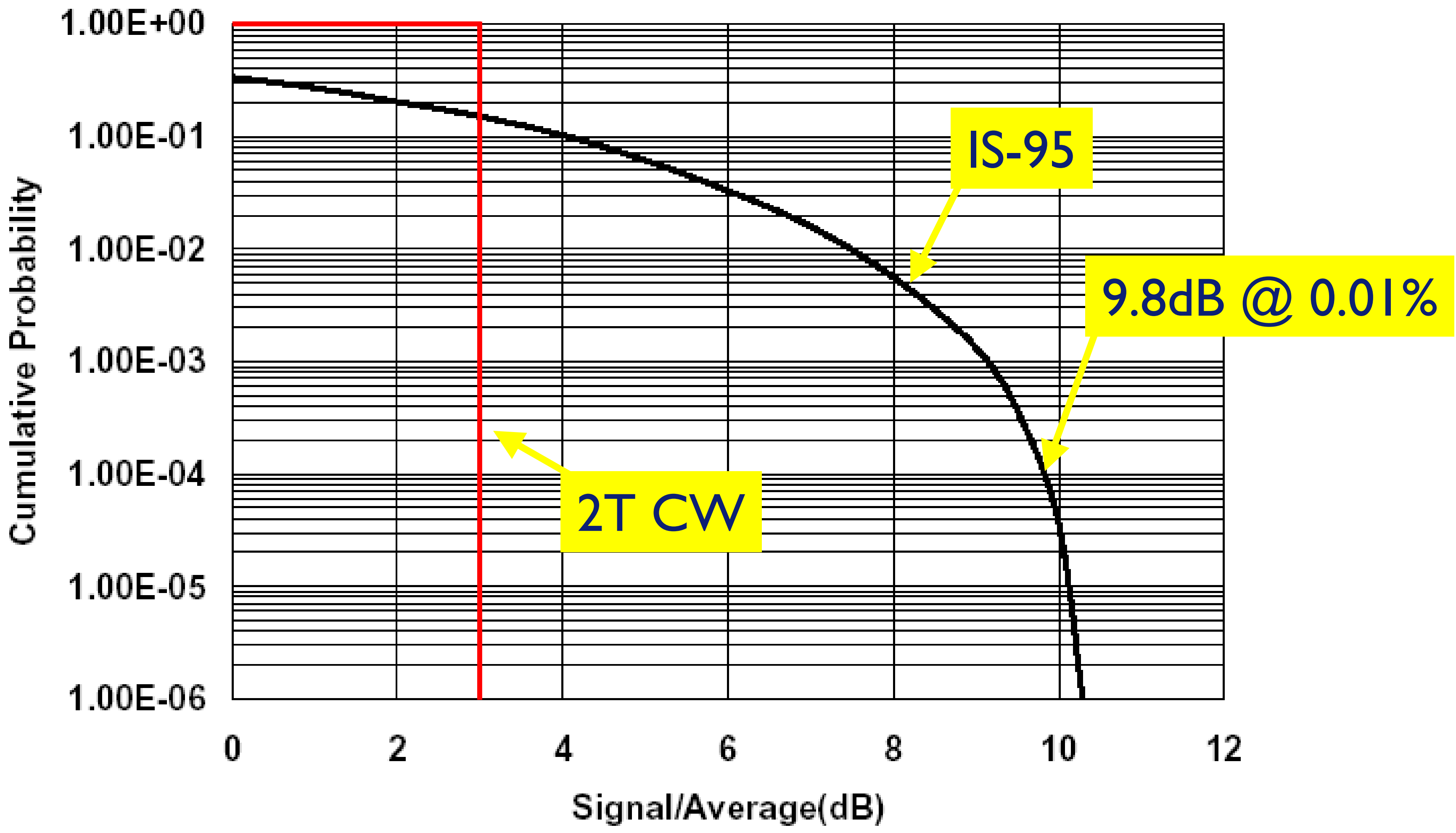


The PAR for a 2-tone CW signal is *always* 2 (or 3dB)

Notes on PAR

- For complex digital modulation schemes, the story is different.
- The PAR is specified at a certain level (in dB), with a certain probability (the chance a certain PAR is reached).
- This probability as a function of PAR is expressed in a *Cumulative Distribution Function* (CDF), often called CCDF (Complementary Cumulative Distribution Function). The probability is expressed in %.
- For instance, the PAR for an IS-95 signal (pilot, paging, sync and 6 traffic channels with Walsh codes 8-13) is: 9.8dB at 0.01% probability

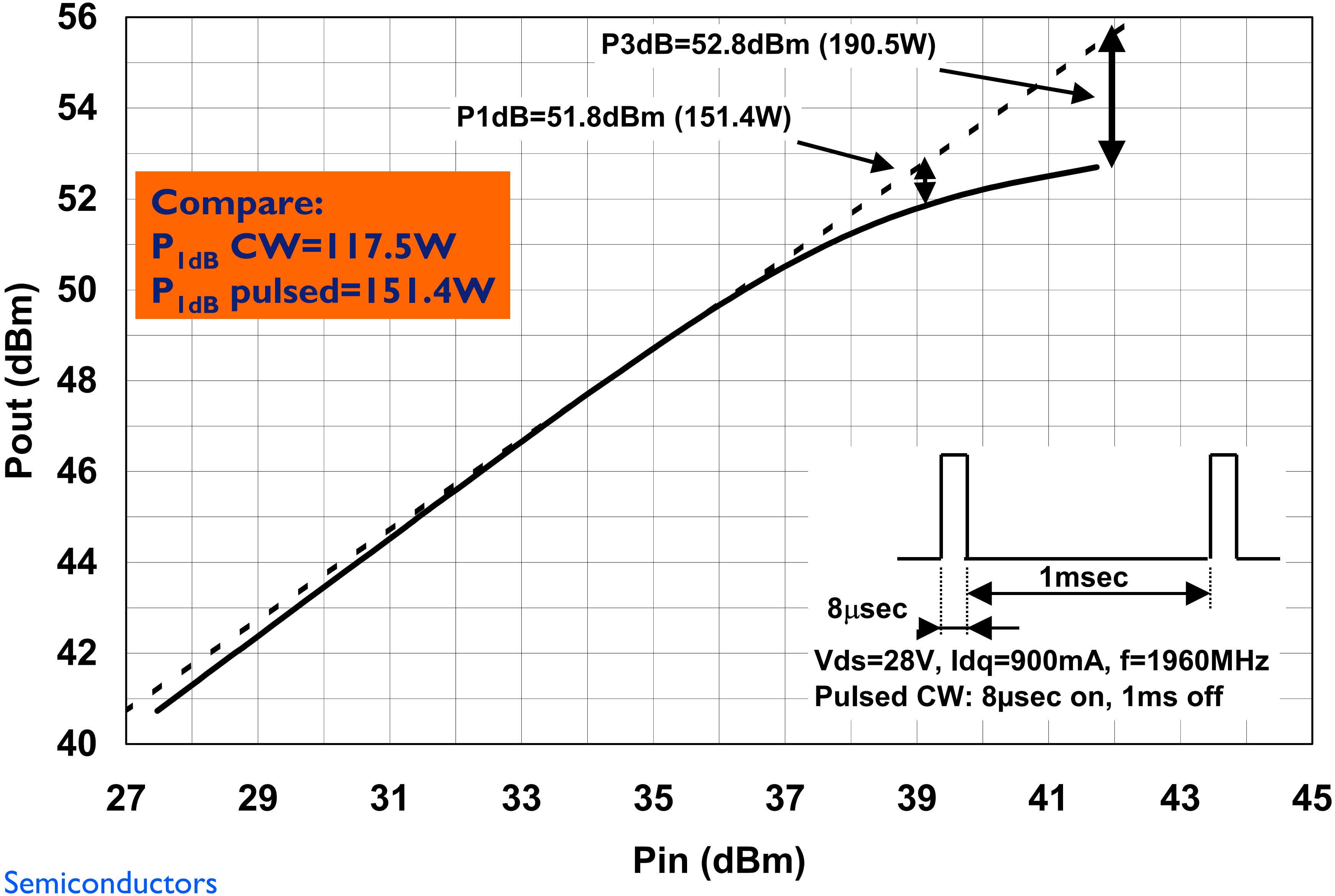
CDF for an IS-95 and 2-tone CW signal



P_{1dB}, P_{sat} and P_{peak}

- In the previous slides it was shown that P_{1dB} and P_{sat} are (die)temperature dependent, i.e.:
  - when the heatsink temperature is high
  - when the device is operating at a high output power, i.e. large current draw, and high dissipation
- That is the reason why the real peak power often is determined under pulsed conditions or at a low average power with spikes on top of that (for instance a CDMA signal).

Peak Power Capability



P3dB=52.8dBm (190.5W)

P1dB=51.8dBm (151.4W)

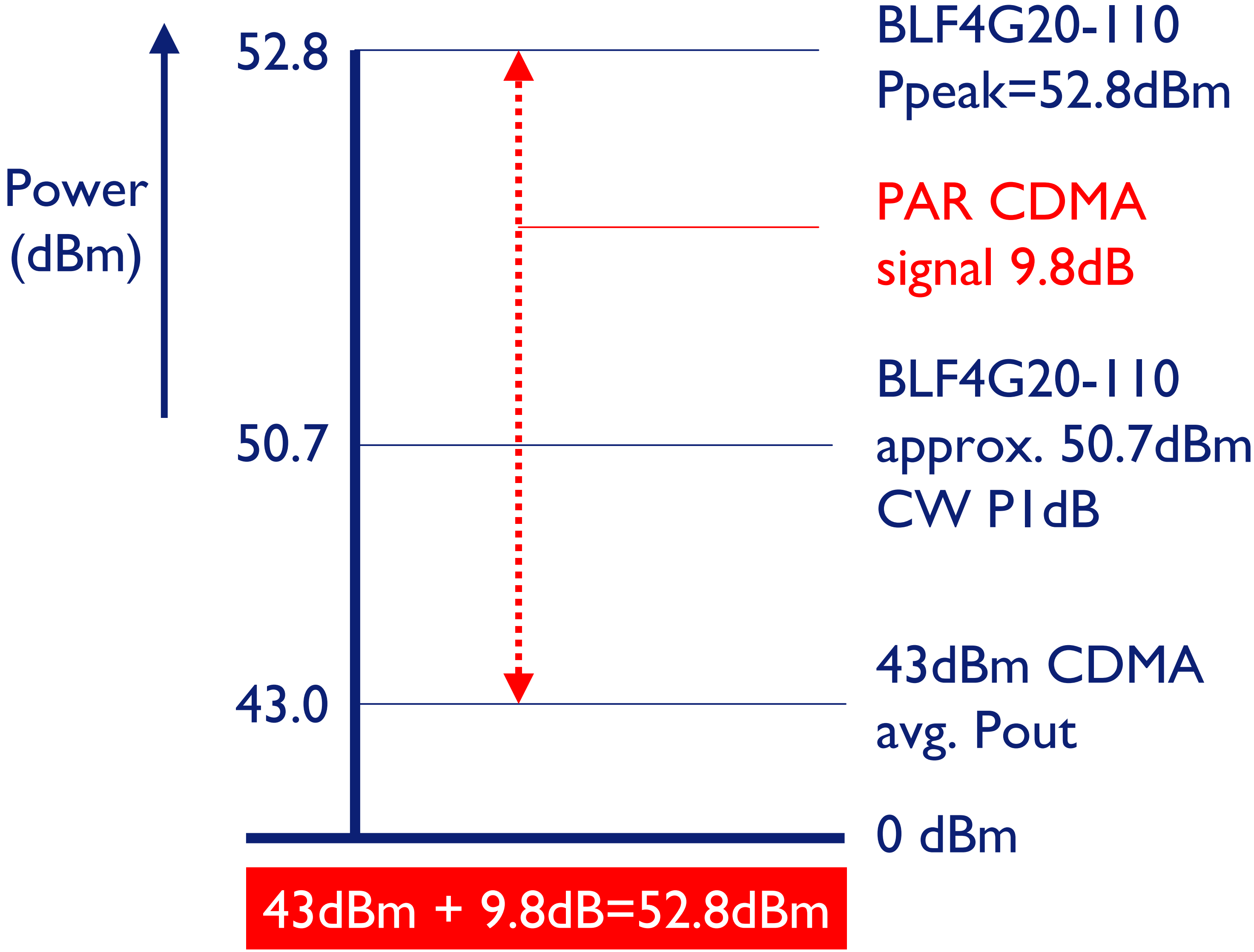
Compare:
P_{1dB} CW=117.5W
P_{1dB} pulsed=151.4W

Vds=28V, Idq=900mA, f=1960MHz
Pulsed CW: 8µsec on, 1ms off

The Importance Of Peak Power Capability

- Peak power capability is of particular interest when the amplifier is used with complex digital modulation signals with a high PAR.
- In that case, the average output power is relatively low, but high peaks can occur in the signal.
- If the high peaks exceed the peak power capability of the device, distortion is introduced.
- A 100W (P1dB, CW) transistor, can typically be used at 20-25W (depending on linearity requirements) average CDMA power with a PAR=9.8dB @ 0.01%.
- Peak power capability is also a measure for how well one can apply pre-distortion (discussed later).

BLF4G20-110B for CDMA (approximation)



Power (dBm)

52.8

50.7

43.0

BLF4G20-110
Ppeak=52.8dBm

PAR CDMA
signal 9.8dB

BLF4G20-110
approx. 50.7dBm
CW P1dB

43dBm CDMA
avg. Pout

0 dBm

43dBm + 9.8dB=52.8dBm

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Pulsed Applications

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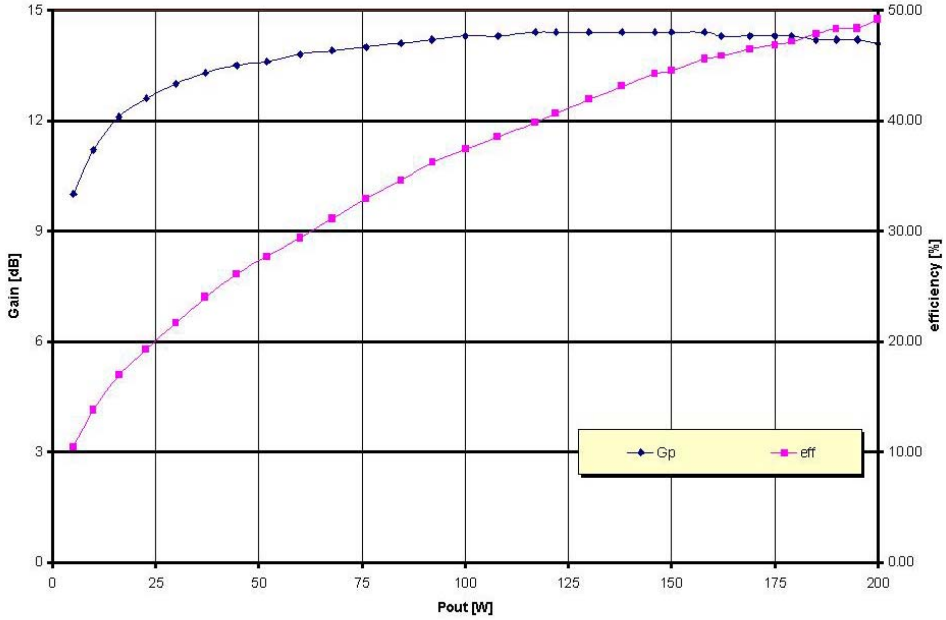
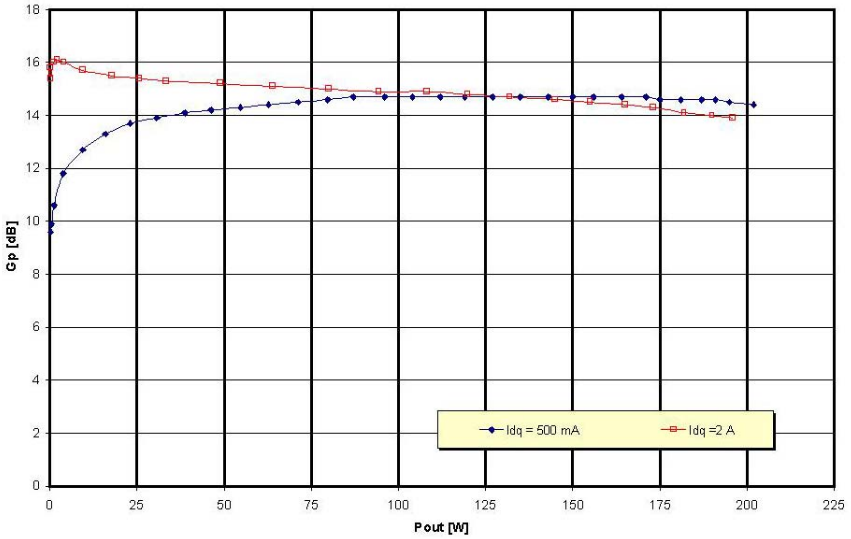
LDMOS for Pulsed Applications



Main advantages over bipolar

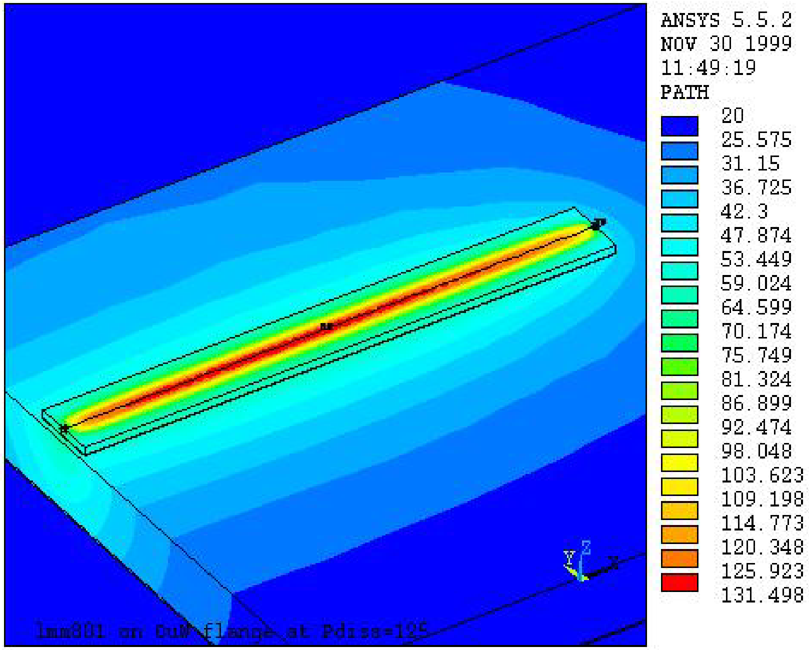
- High gain
- High efficiency
- Good linearity

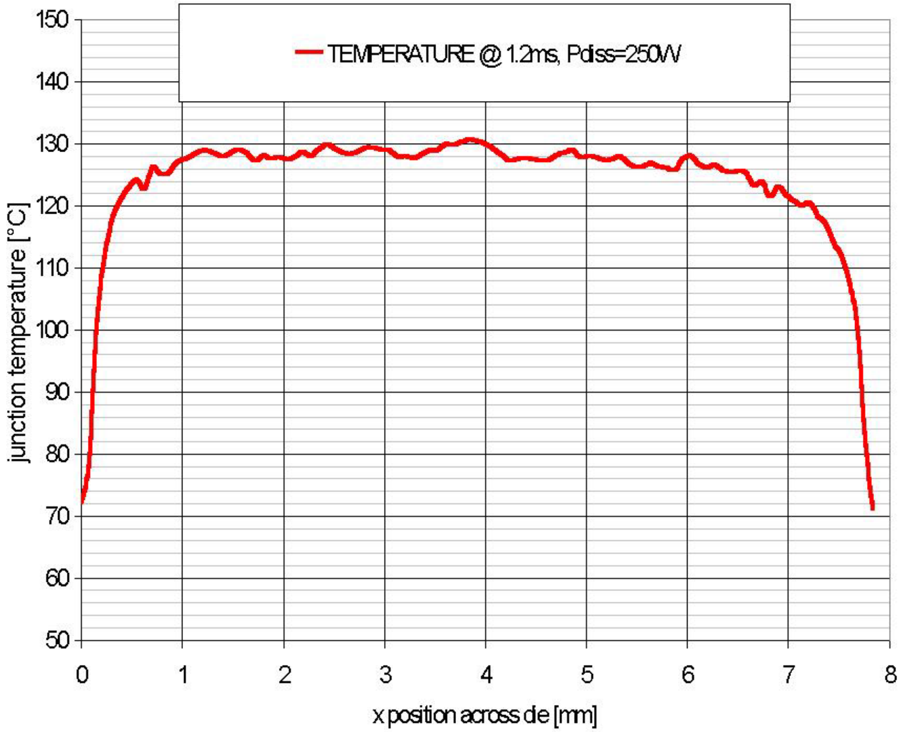


LDMOS vs. Bipolar (Pulsed)

- Excellent thermal stability: due to negative temperature coefficient
- Excellent ruggedness due to high breakdown voltage of die technology and its good thermal stability
- Pulse shaping easy compared to bipolars by modulating Vgs
- Package does not contain BeO, source mounted direct to flange – also better thermal properties.

Thermal Characteristics LDMOS (Pulsed)





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Application Circuits

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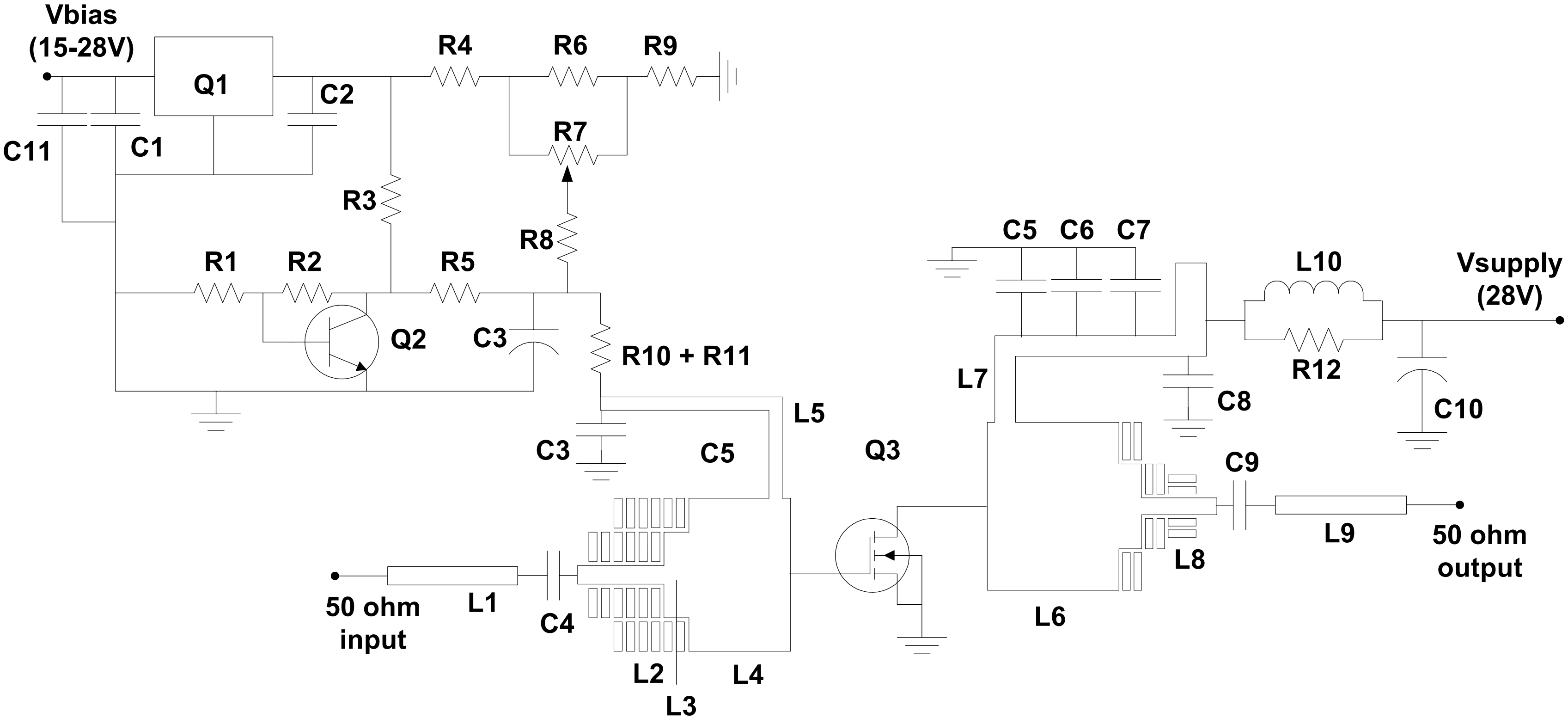
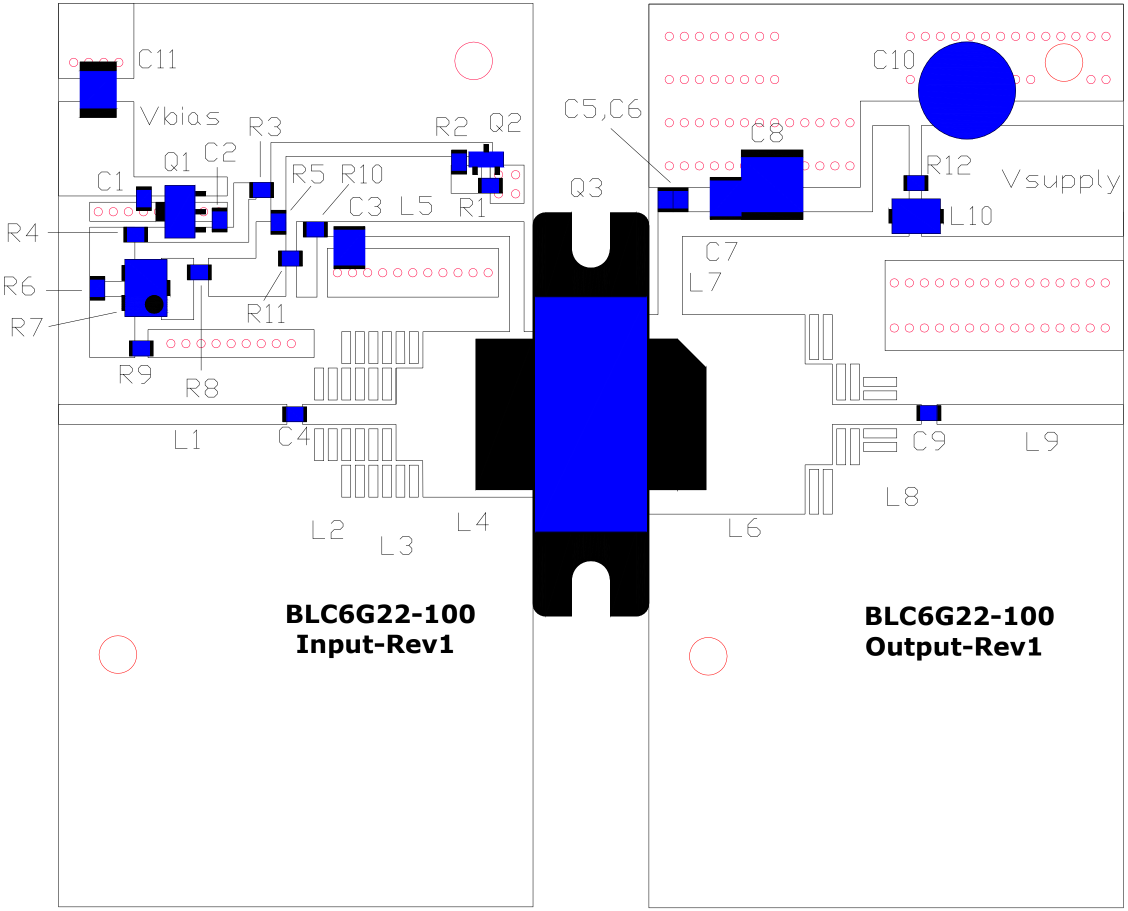
UMTS Application Circuit

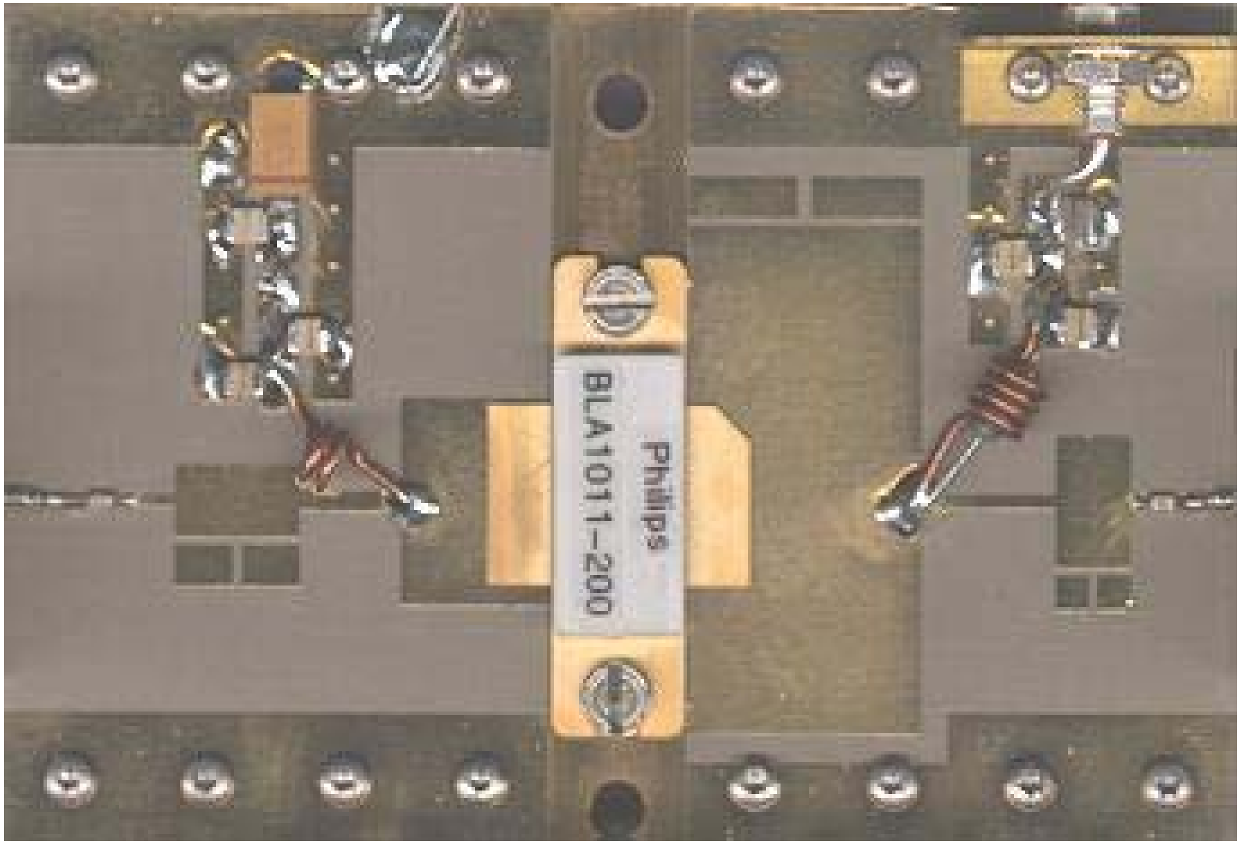


BLC6G22LS-100: 2110- 2170MHz – 100W

Application Circuit BLC6G22LS-100



Application Circuit BLA1011-200



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Thermal Resistance

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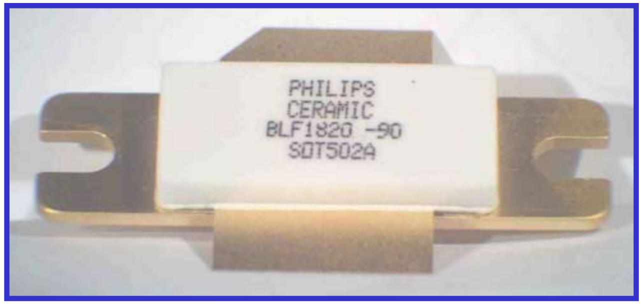
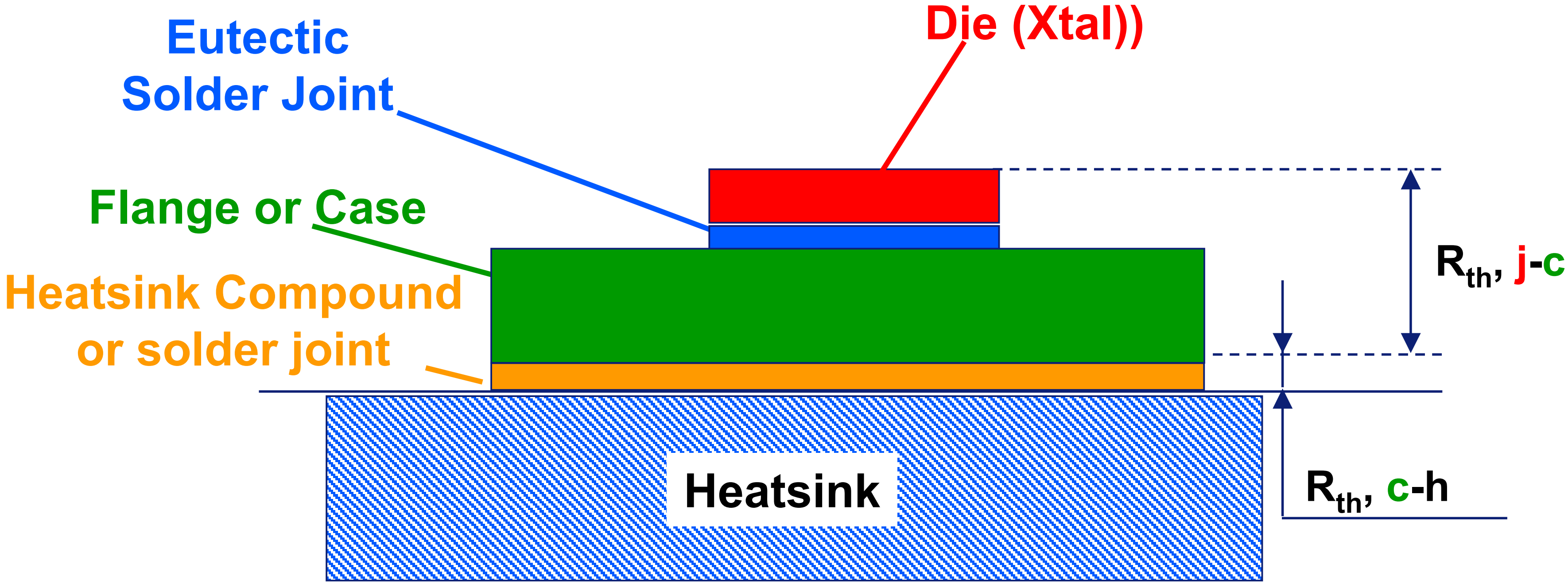
Transistor thermal resistance





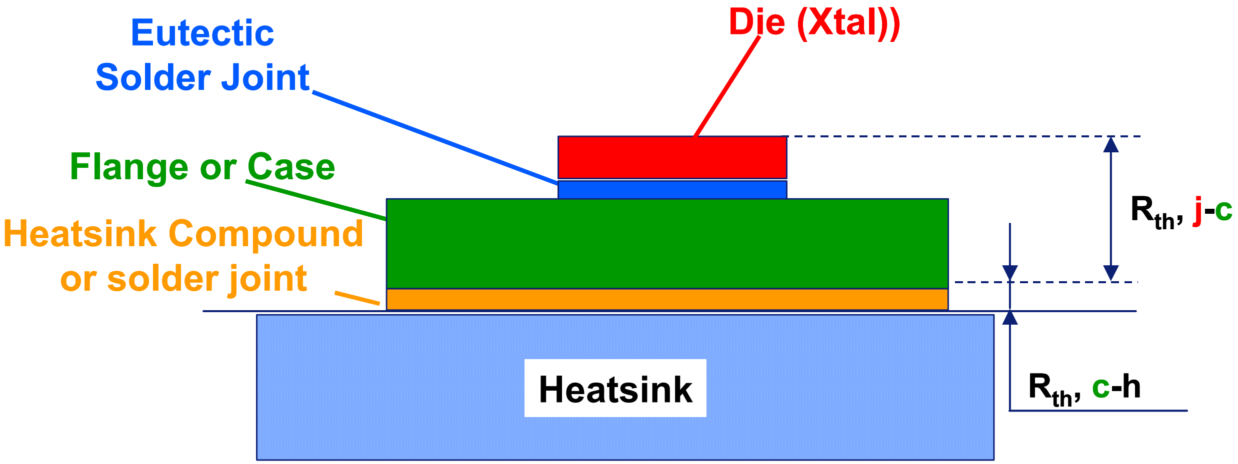
Transistor thermal resistance

$$R_{th} = \frac{\Delta T}{P_{diss}} \, [\,K/W \text{ or } {}^\circ C/W] \quad \text{or} \quad \Delta T = R_{th} \cdot P_{diss} \, [K \text{ or } {}^\circ C]$$

- R_{th} is thermal resistance, often also called θ
- ΔT is temperature rise due to thermal interface in K or °C
- P_{diss} is the dissipated power in Watts

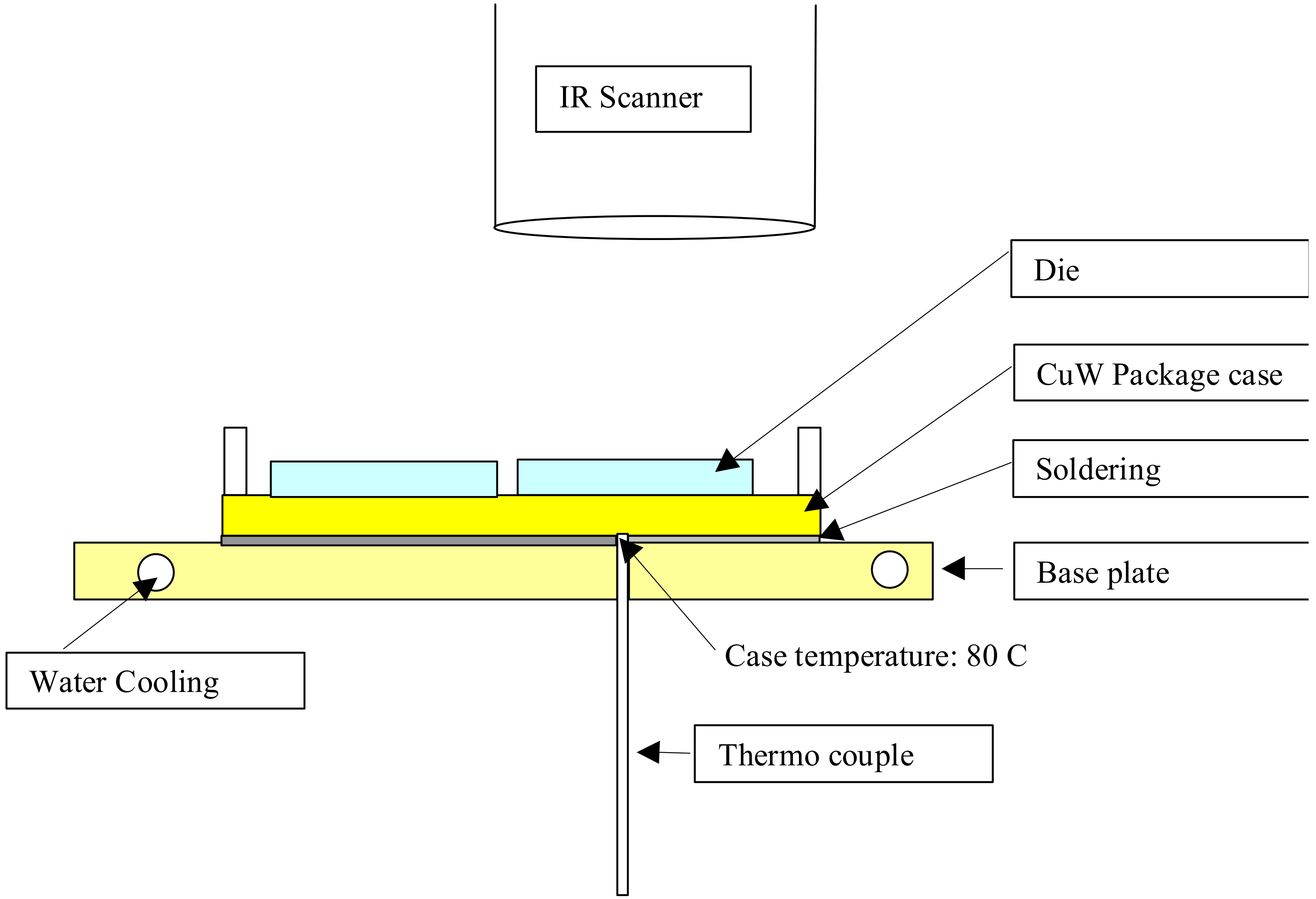
Example: If a transistor dissipates 100W, and the Rth is 0.35K/W, the temperature rise is 35°C

Transistor thermal resistance

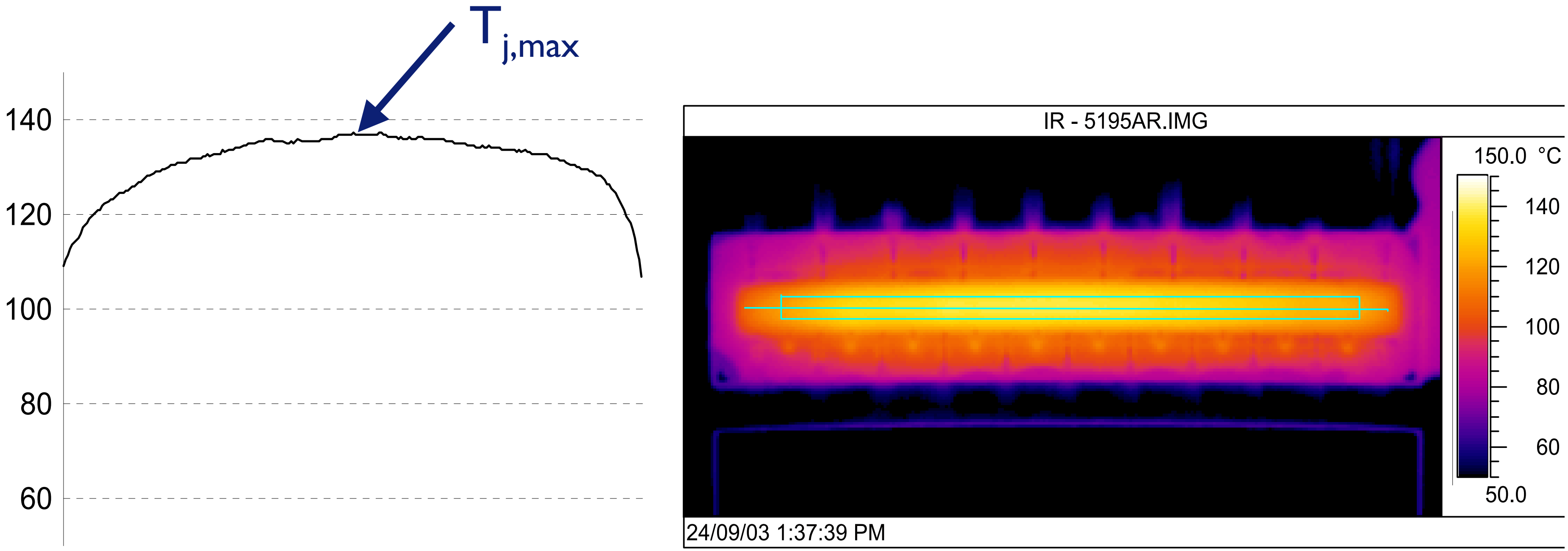


- One can define different thermal interfaces:
  - Rth,j-c : Junction to Case
  - Rth,c-h : Case to Heatsink
- In case of a solder joint, the Rth,c-h can be (almost) ignored

Infra Red Scanner Setup



Typical IR-scanner data



Rth figures are determined based on *maximum* junction temperatures, not average junction temperatures, thus truly reflecting the worse case situation.

Rth calculations

$$P_{diss} = P_{dc} - P_{rf,out} + P_{rf,in} [Watts]$$

$$P_{dc} = V_{ds} \cdot I_{ds} [Watts]$$

$$P_{diss} = \left(\frac{P_{dc}}{P_{rf,out}} - \frac{P_{rf,out}}{P_{rf,out}} + \frac{P_{in}}{P_{rf,out}} \right) \cdot P_{rf,out} [Watts]$$

$$P_{diss} = \left(\frac{1}{\eta_D} - 1 + \frac{1}{10^{\frac{Gp}{10}}} \right) \cdot P_{rf,out} [Watts]$$

$$\eta_D [no\ dimension],\ G_p [dB],\ P_{rf,out} [Watts]$$

Thermal Resistance

Rth

$$\Delta T = P_{diss} \cdot R_{th}$$

$$P_{diss} = \left(\frac{1}{\eta_D} - 1 + \frac{1}{10^{\frac{Gp}{10}}} \right) \cdot P_{rf,out} \, [Watts]$$

- Looking at the formulas above, one can conclude:
  - In order to minimize the temperature rise:
    - R_{th} should be as low as possible
    - η_D should be as high as possible
    - G_p should be as high as possible
- And that is exactly why our customers want:
  - An LDMOS technology with higher gain and efficiency
  - A die layout that ensures a low Rth
  - Thinner die to minimize Rth
  - Improved transistor packaging to lower the Rth

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Reliability / Electromigration

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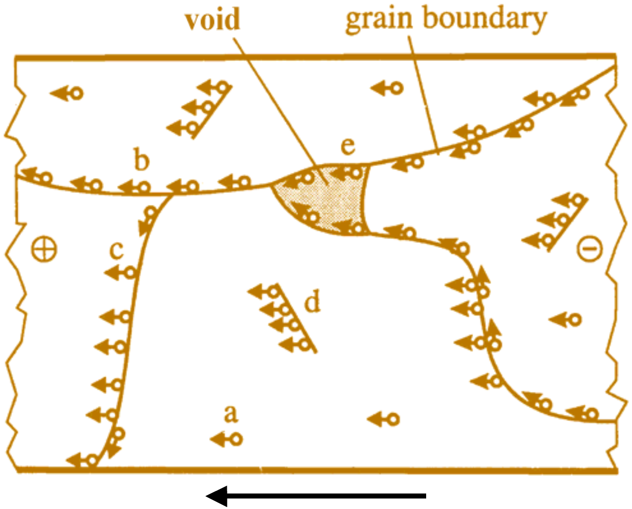
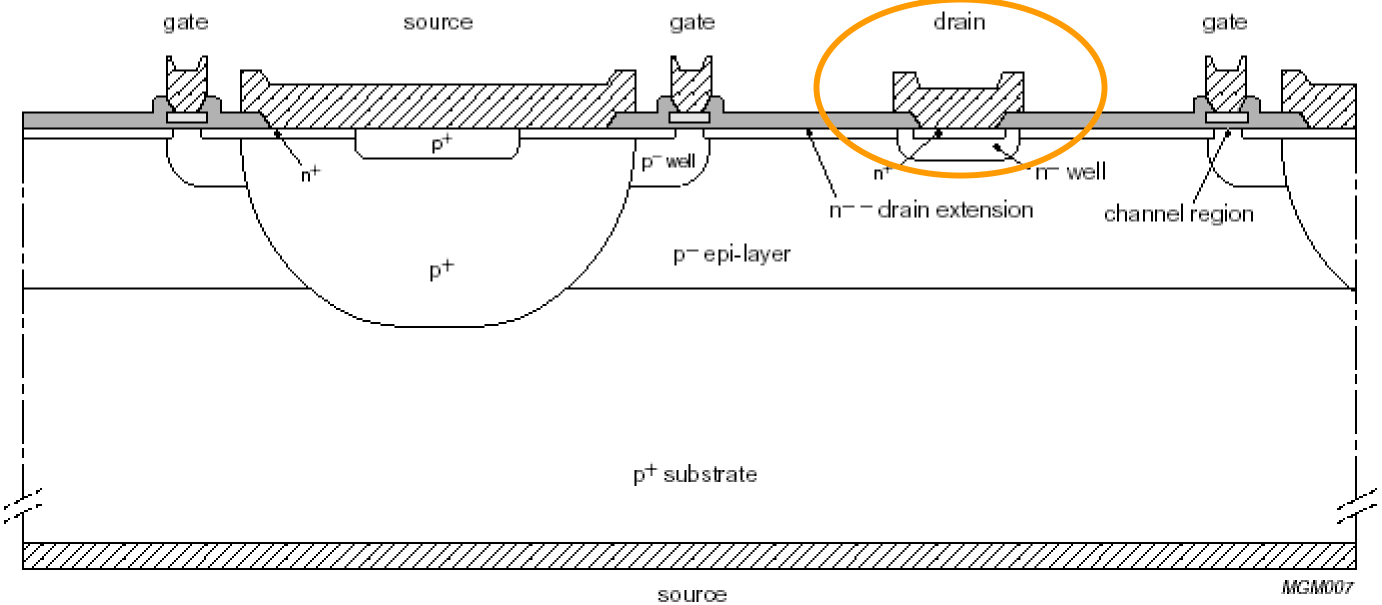
LDMOS Reliability

Electromigration

Electromigration is the dominant ware-out mechanism in LDMOS



Electron flow due to DC current



Acceleration Model

Black's equation: $$M(edian)\ T(ime)\ to\ F(ailure) = \frac{C}{J^n} e^{\frac{E_a}{\mathrm{k_B} T}}$$

$$or, \quad \ln(MTF \cdot J^n) = \ln(C) + \frac{E_a}{\mathrm{k_B} T}$$

J : Current density

n : Current density exponent (n=2)

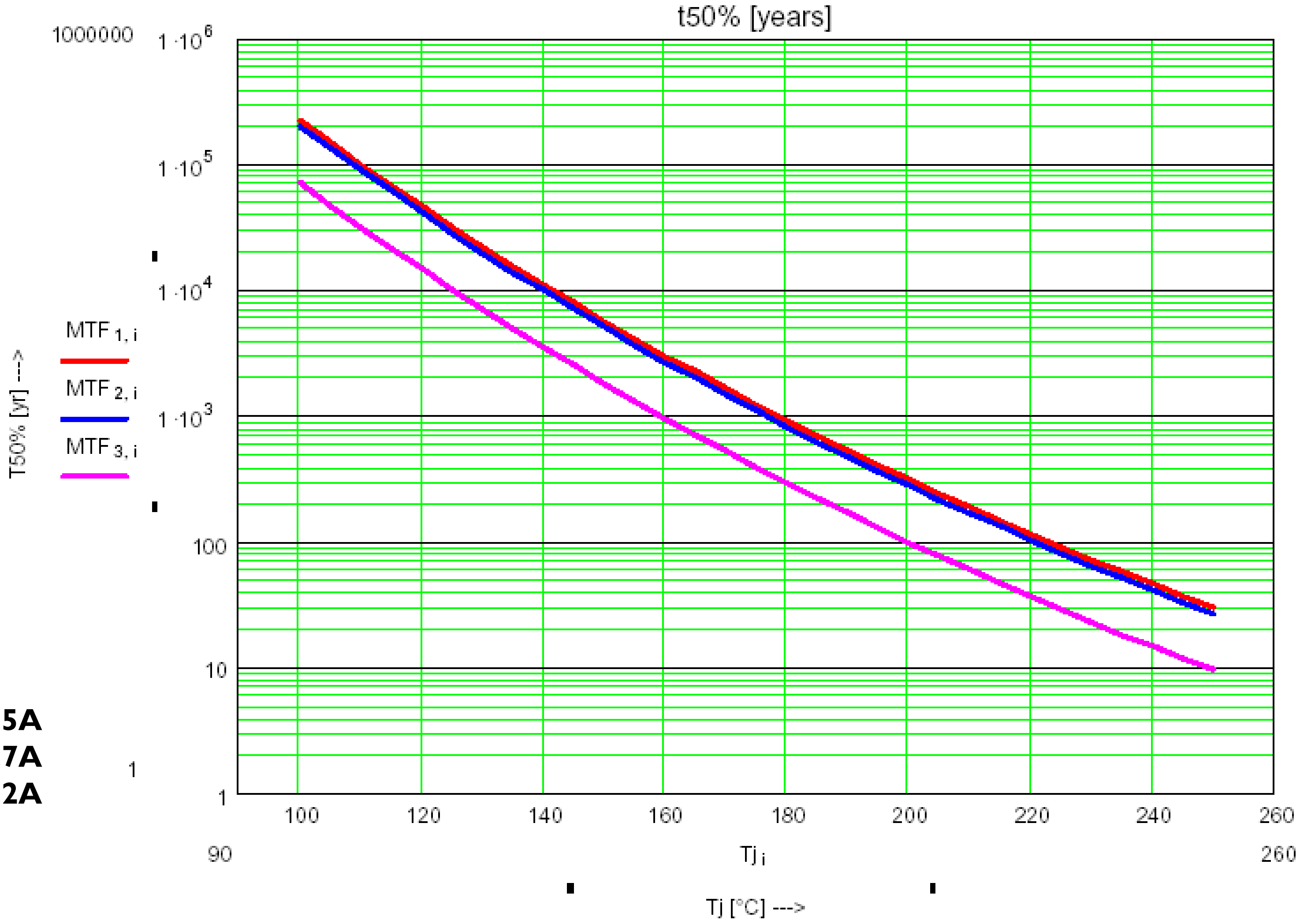
C : Constant

E_a : Activation energy (E_a=1.0eV)

k_B : Boltzmann's constant

T : Temperature

MTF for Generation 4 LDMOS



🟥	W-CDMA	**Ids=3.5A**
🟦	EDGE	**Ids=3.7A**
🟪	GSM	**Ids=6.2A**

Safe operating temperature GEN4

- There is not one single opinion in the industry about the safe operating temperature of LDMOS devices.
- Some customers want to stay around 150°C, some around 160°C.
- It is completely safe to use Philips LDMOS in excess of 170°, and even then the reliability of our parts is excellent.

Summary

Today, LDMOS is the technology of choice for any RF power amplifier design up to 3.5GHz. LDMOS is the cheap, it is (re) producible, mature and offers state-of-the-art performance characteristics. Further refinement and performance improvements are possible in this technology, however the theoretical limits are being approached.