

Design for Yield (DFY)



What is a Robust Design?

A design that is less sensitive to the manufacturing process



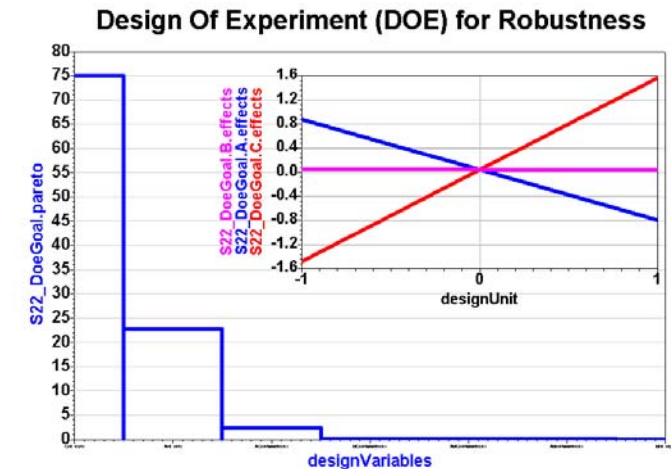
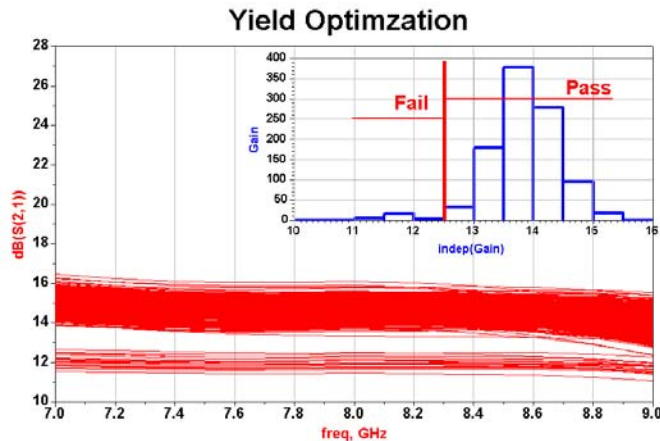
Advanced DFY Tools

No longer designers have to worry that their circuits have to be redesigned again.

No longer managers have to be concerned for the high costs of multi wafer runs.



ADS Advanced DFY Tools help designers achieve "First Pass Success".



Example: 2.4 GHz MIC LNA on Alumina Substrate

Optimum Noise Match

NEC 67383 FET

2-3 GHz

Freq, GHz	Γ_m	R_n	NF_{min}
2	$0.69 < 21^\circ$	0.58	0.3
3	$0.60 < 31^\circ$	0.57	0.5
4	$0.60 < 50^\circ$	0.51	0.6

Alumina Substrate

$\epsilon_r = 9.9$ H=25 mils

Design Spec:

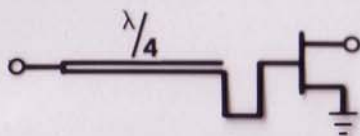
.7 dB NF @ 2.4 GHz



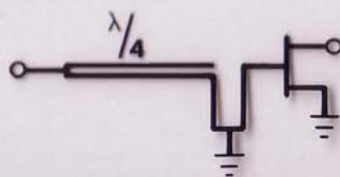
Example: 2.4 GHz LNA - MIC Design

Three of many different ways to match for optimum noise

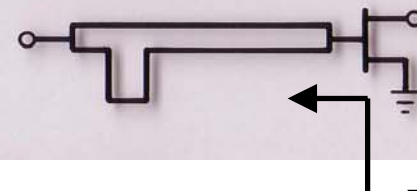
50Ω open shunt stub
 $\lambda/4$ series line, $Z_0 = 104\Omega$



50Ω shorted shunt stub
 $\lambda/4$ series line, $Z_0 = 104\Omega$

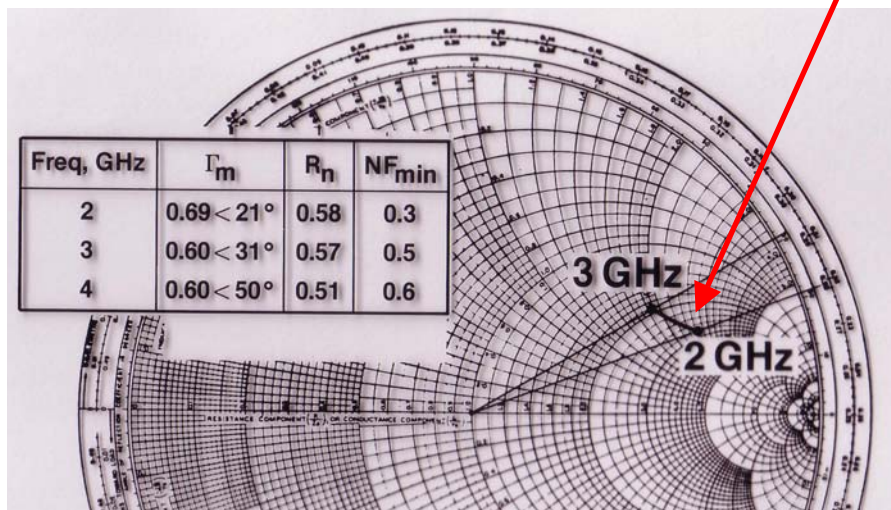


50Ω series line and
 50Ω open shunt stub

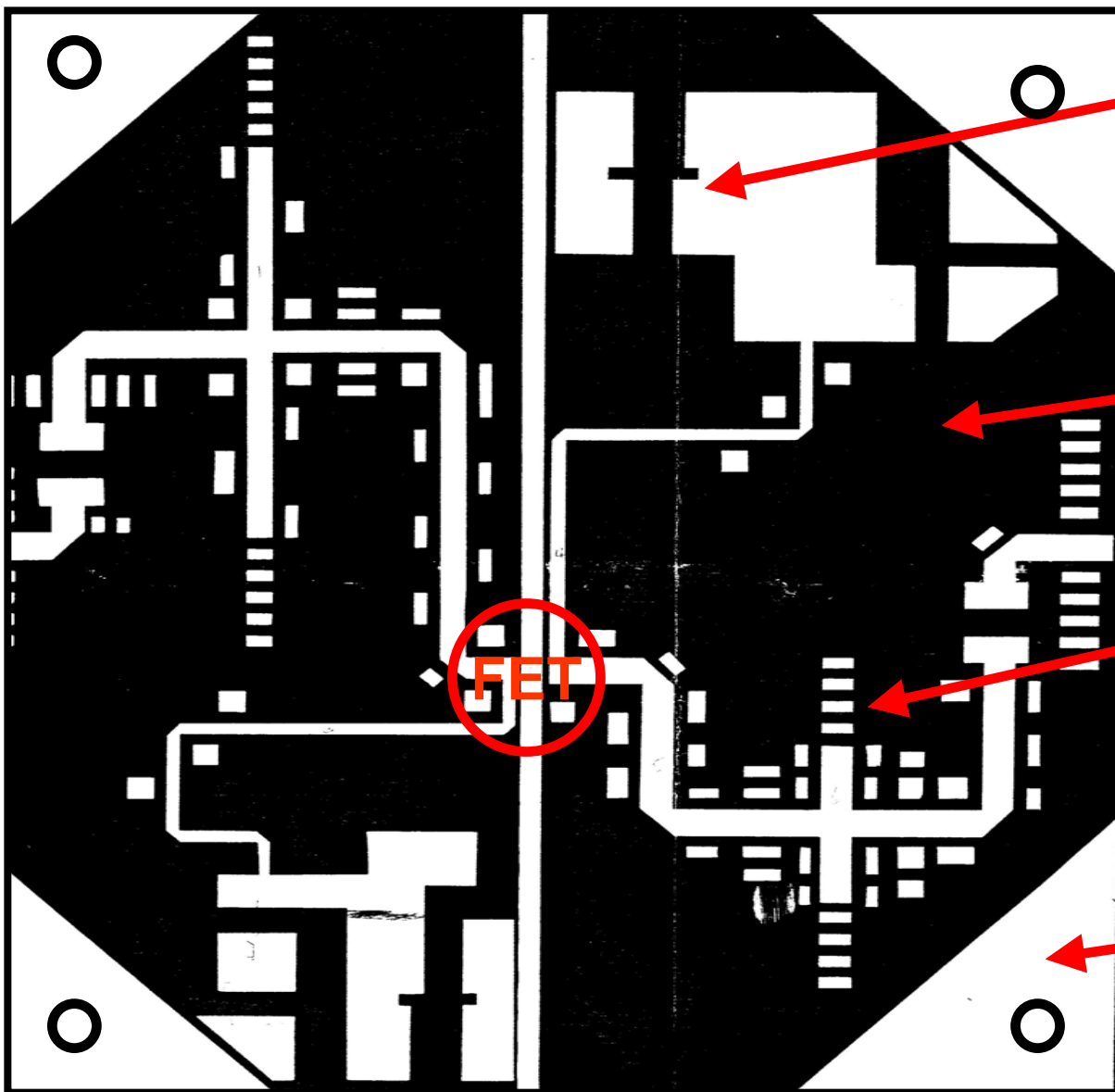


Γ_m

Goal is to have the matching network impedance coincide with the optimum noise figure impedance, Γ_m



Example: Ruby Mask - 2.4 GHz LNA



Bypass Caps

Drain bias

Alumina Substrate

Tuning Confetti

Carrier

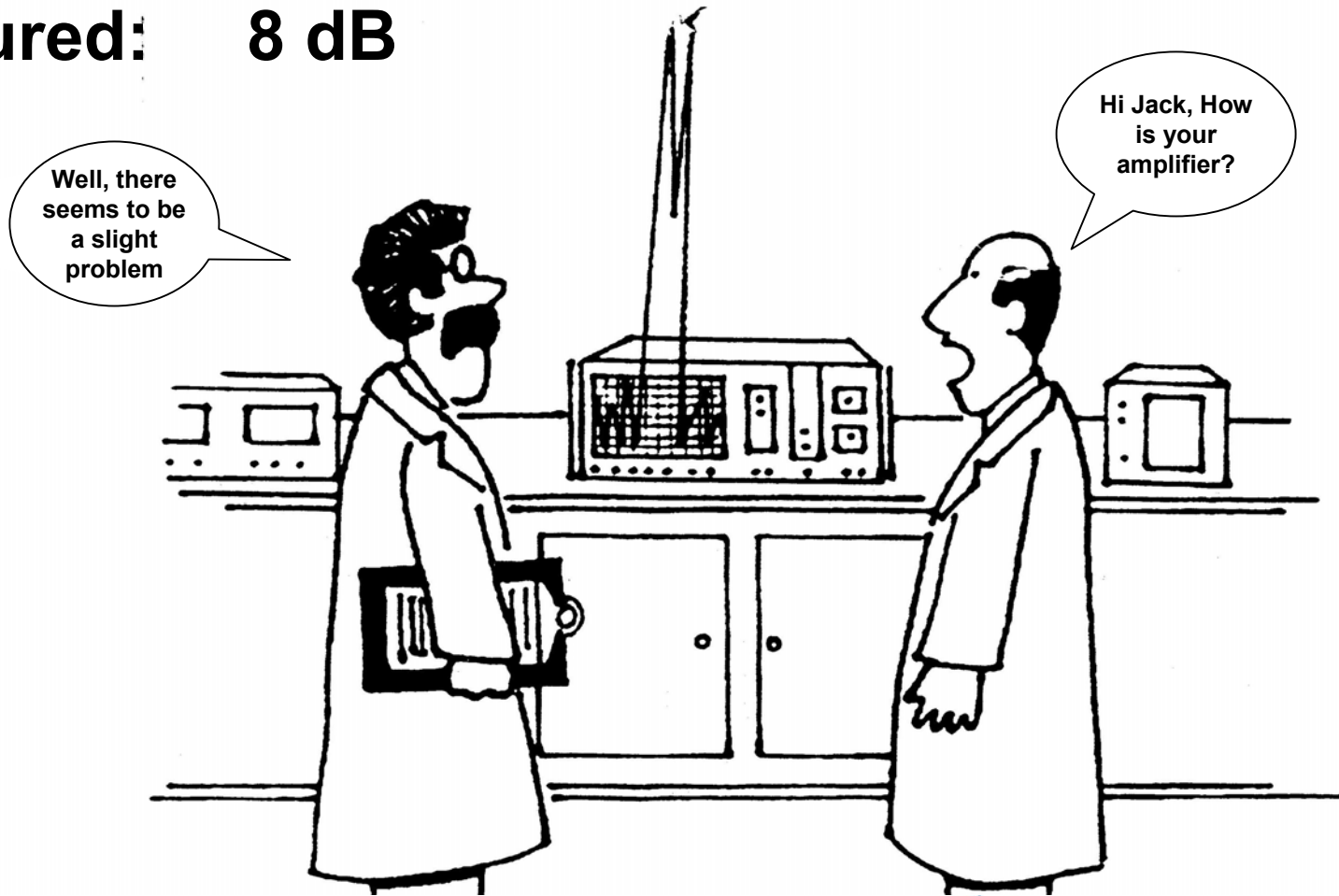


Agilent Technologies

Initial Test Results (Major Problem)

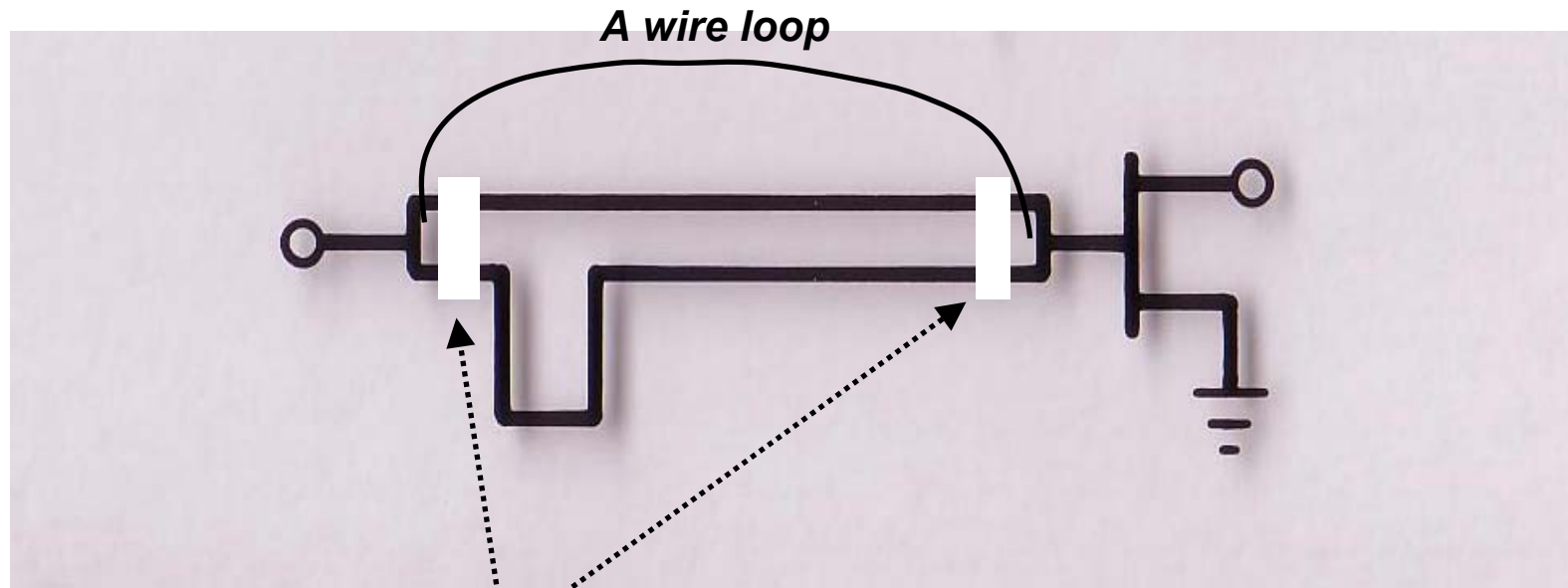
NF Spec: .7 dB

Measured: 8 dB



Finding a solution in the lab

This solution achieved a .5 db NF @ 2.4 GHz

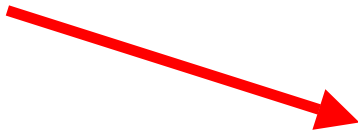


- 1- Diamond Scribe out the Input Matching Network
- 2- Solder a loop of inductive wire from FET to connector

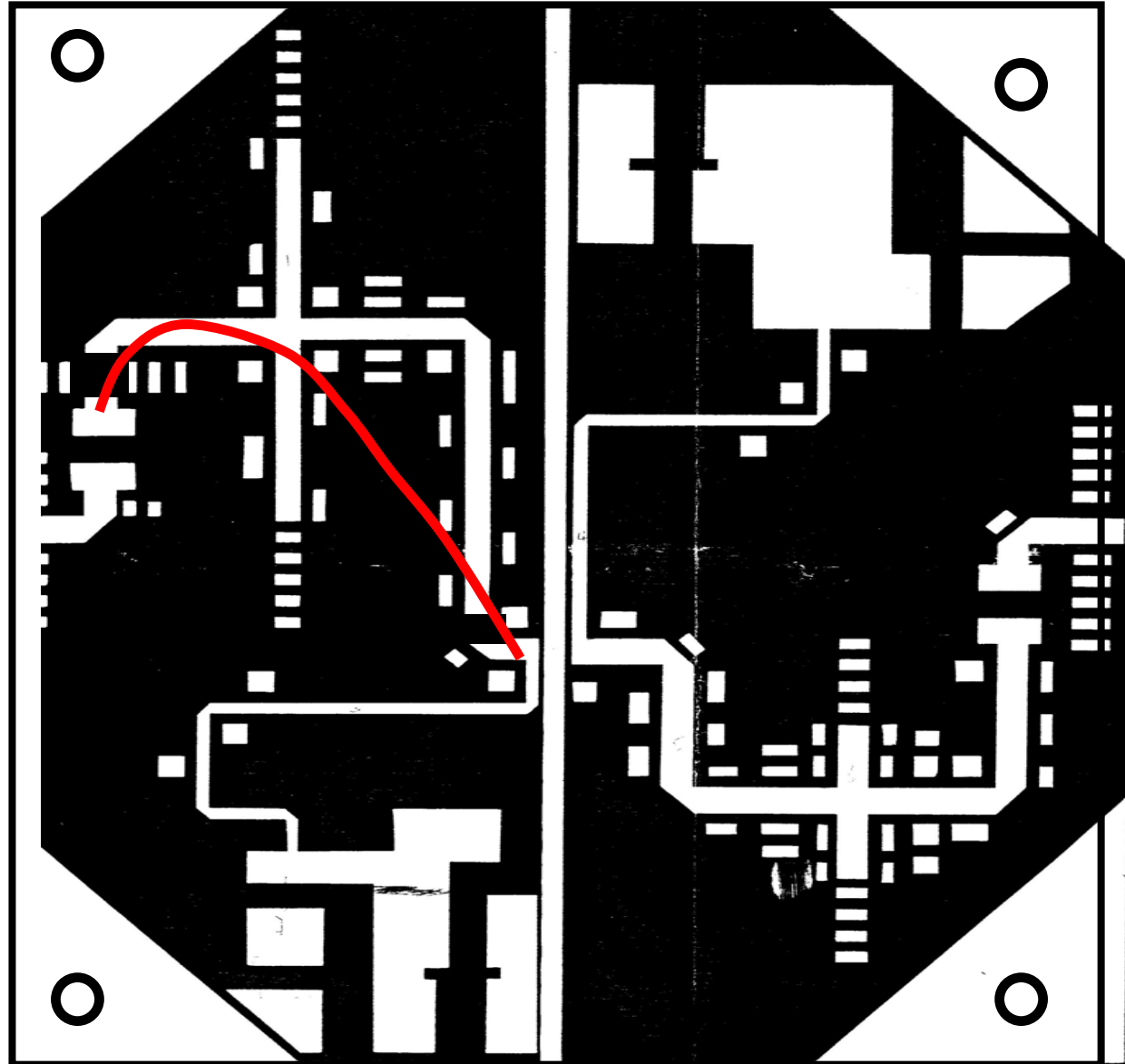


Example: Ruby Mask - 2.4 GHz LNA

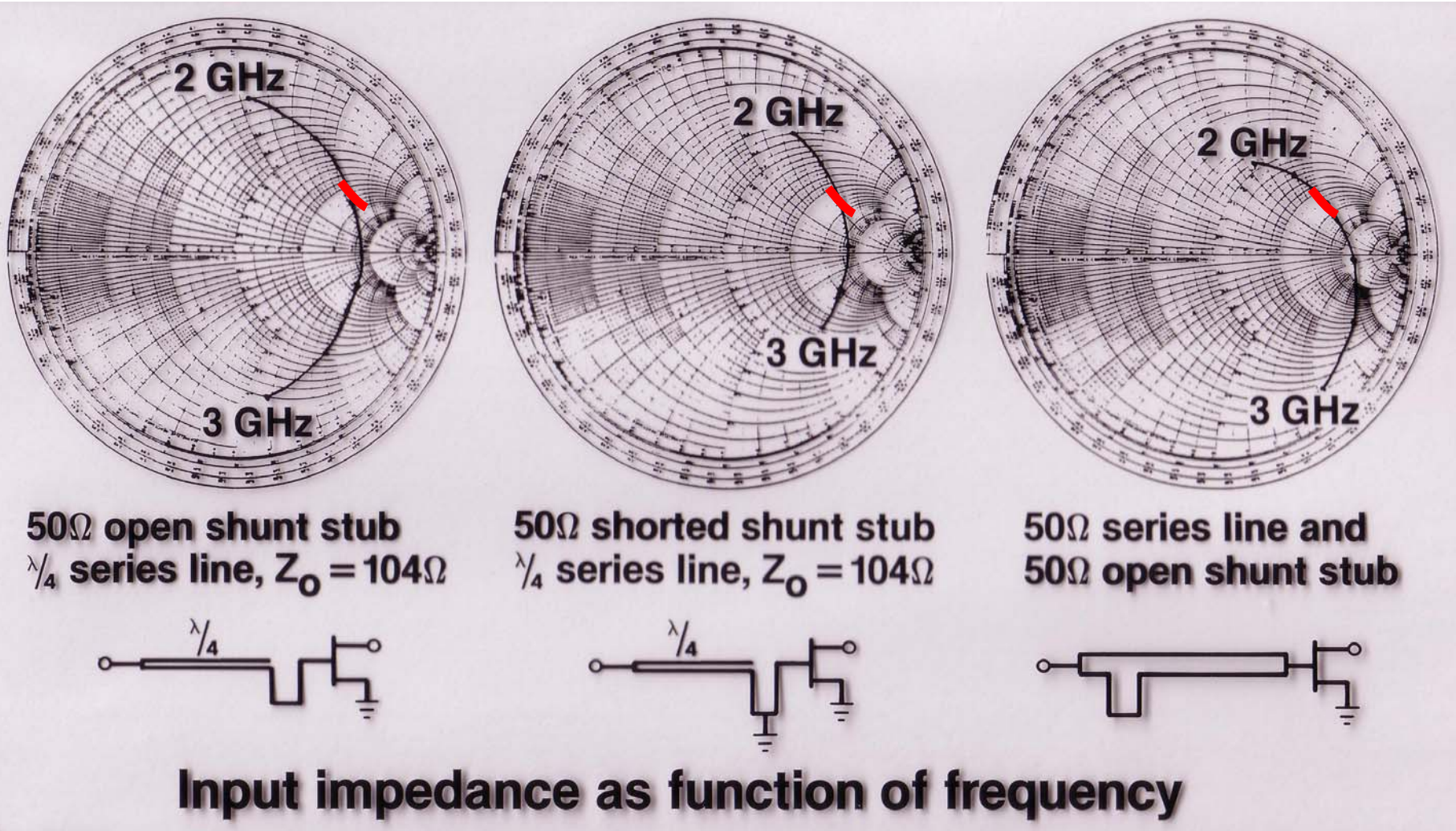
Wire loop from input
port to FET's Gate



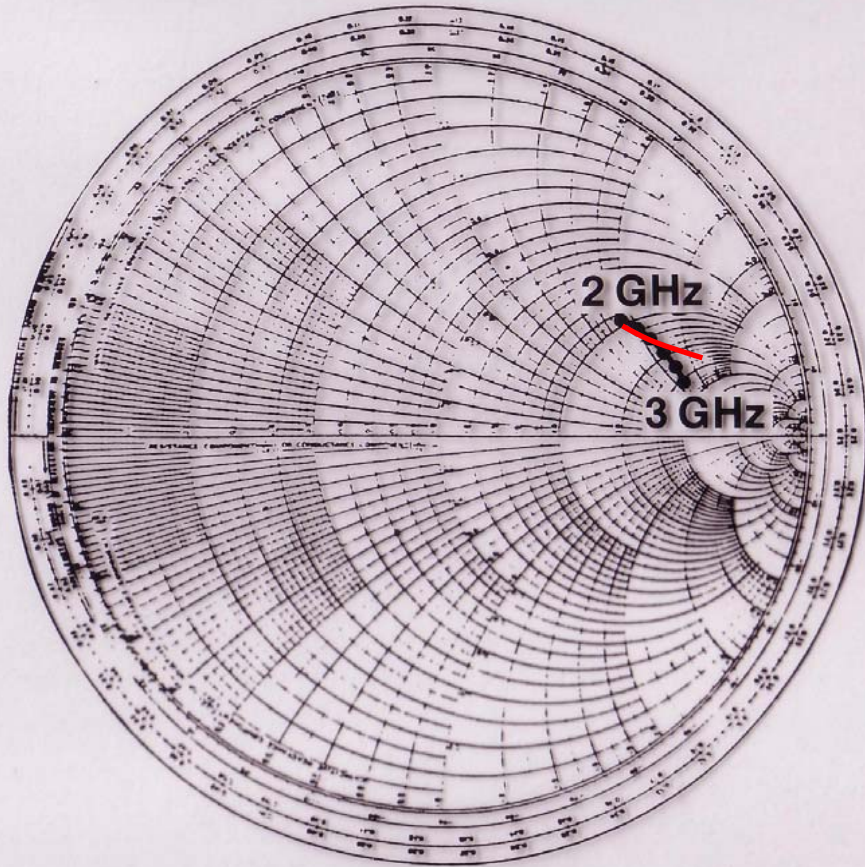
Back to the drawing
board for further
investigation



Understanding what went wrong



Single Line Matching – Low Q



Γ_S of a single line, $Z_0 = 120\Omega$

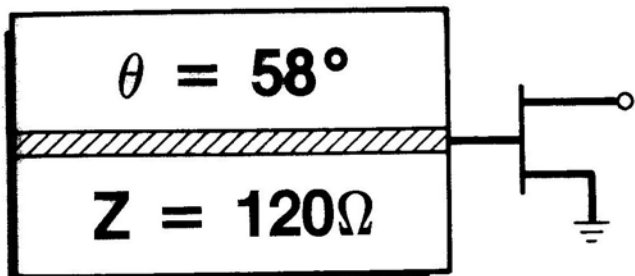


Use of high impedance, single line was the best technique for achieving robust & optimum Results, but too narrow to realize.

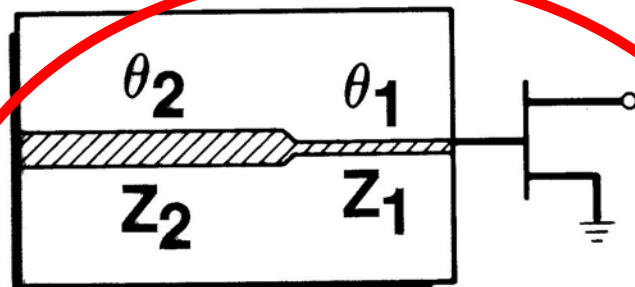
Suspended line concept was utilized to produce a realizable, wider, high impedance line with a low Q broadband network



Matching with Single Line – Low Q

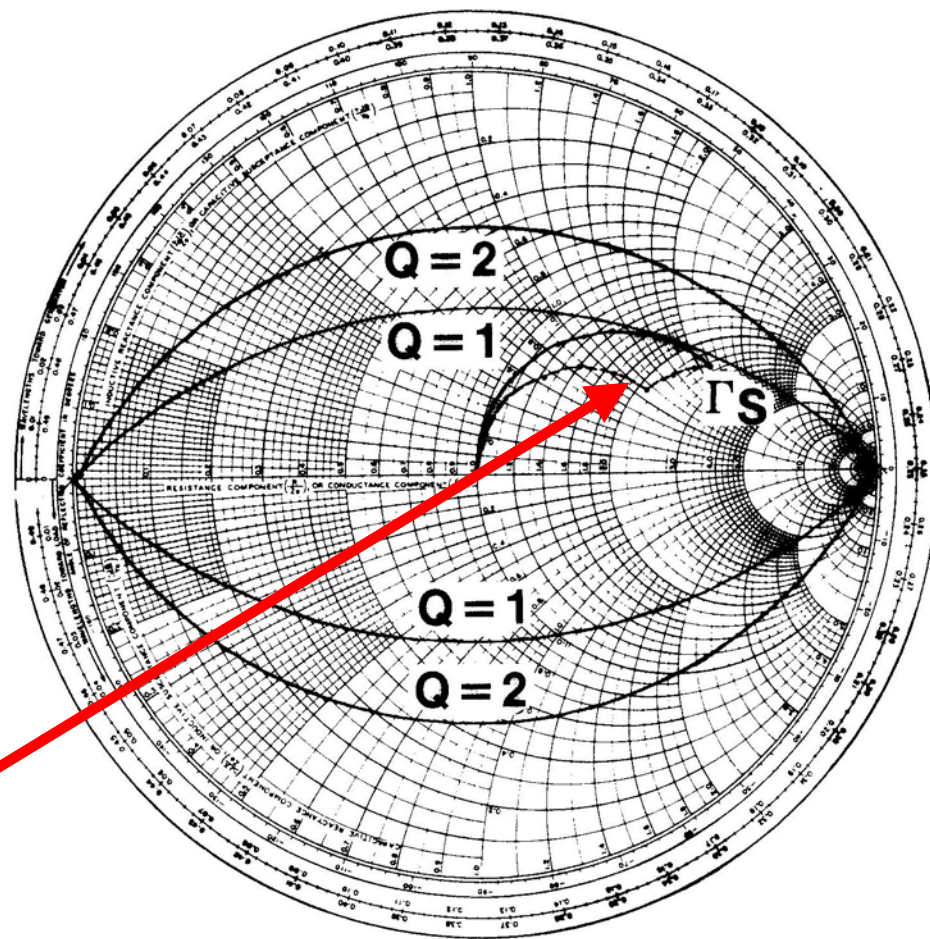


$W = 1.5$ mil on
25 mil alumina



$Z_1 = 250\Omega$ $\theta_1 = 13.5^\circ$

$Z_2 = 89\Omega$ $\theta_2 = 61^\circ$

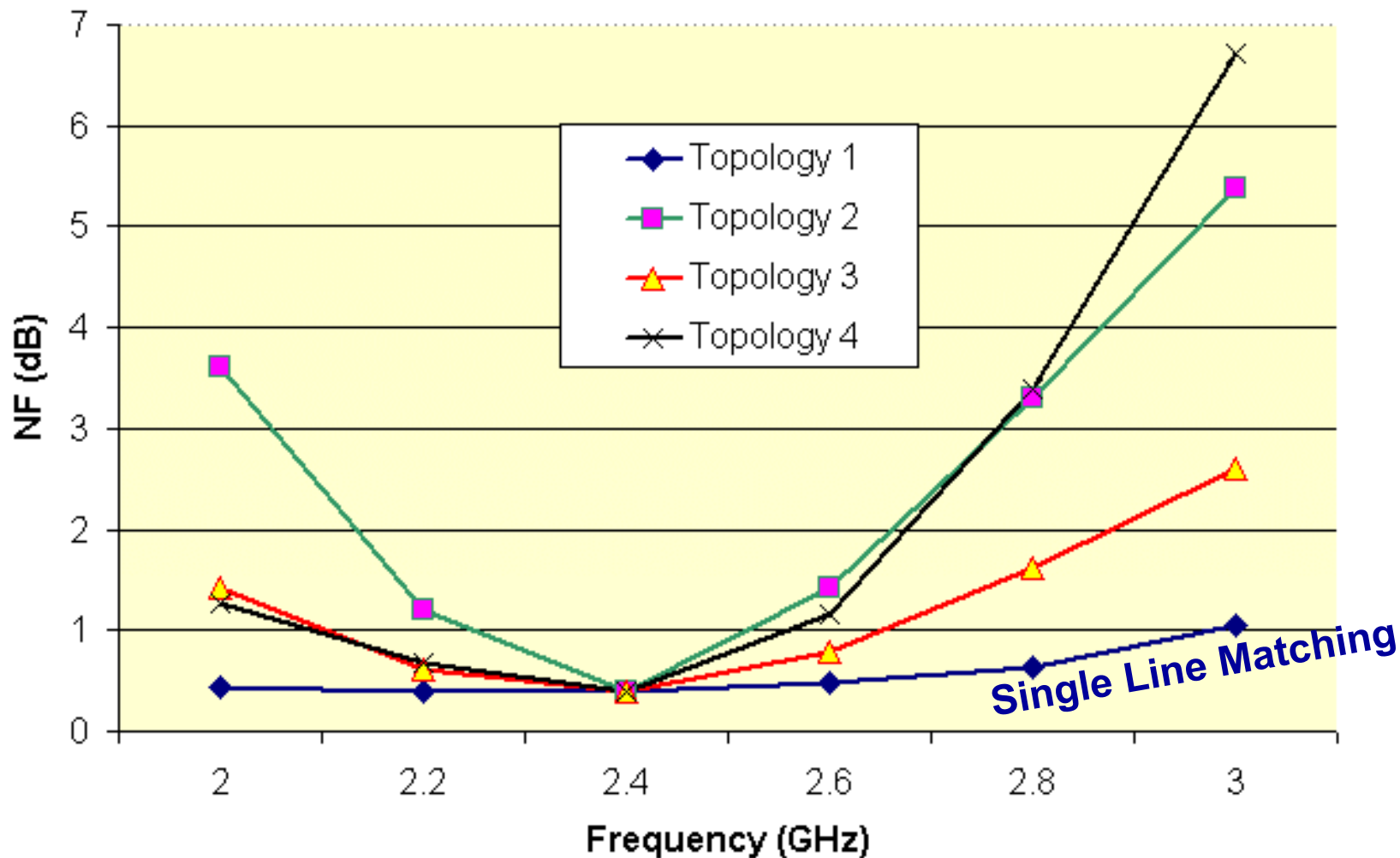


Option 2 is even more Robust, but non-realizable



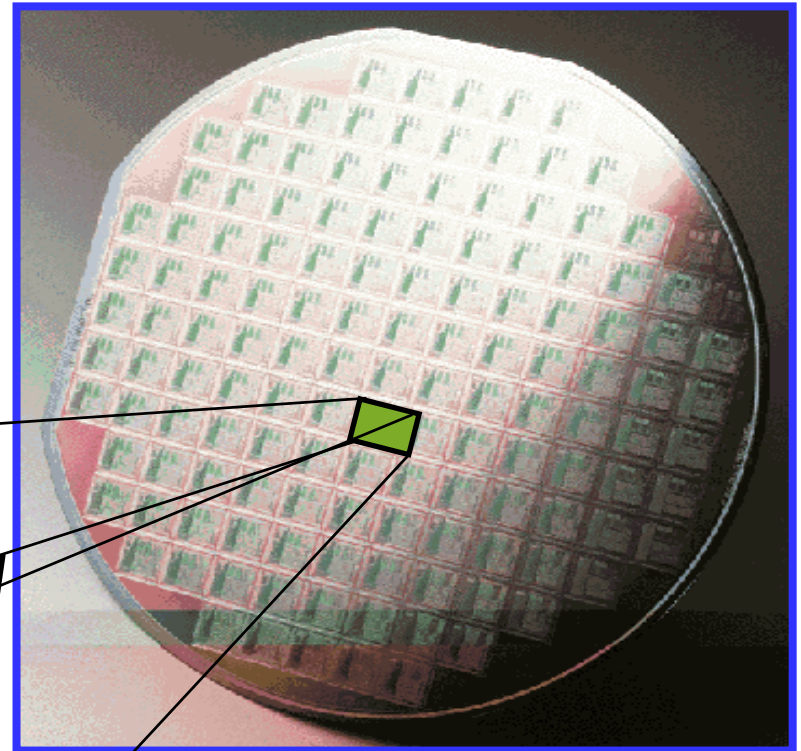
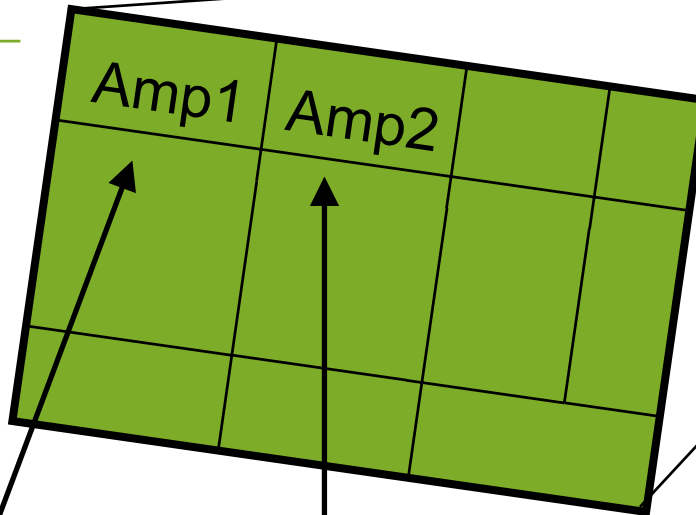
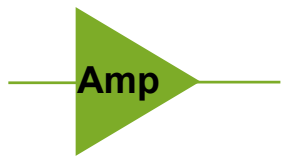
NF Simulation of the Various Matching networks

LNA Noise Figure for Four Different Noise Matching Networks



Real MMIC Designs – Fabricated on the same wafer

A Reticle contains a few circuits, stepped and repeated across the whole wafer



All designs went through the same Wafer Fab Process

1) Used a standard design technique

2) Used a DFY Based design technique



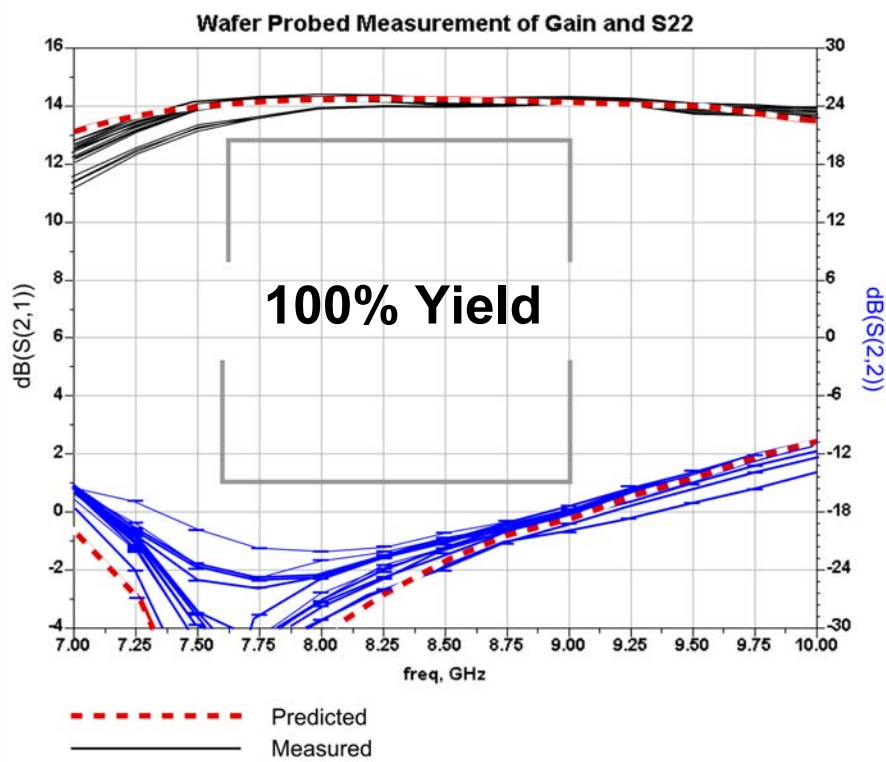
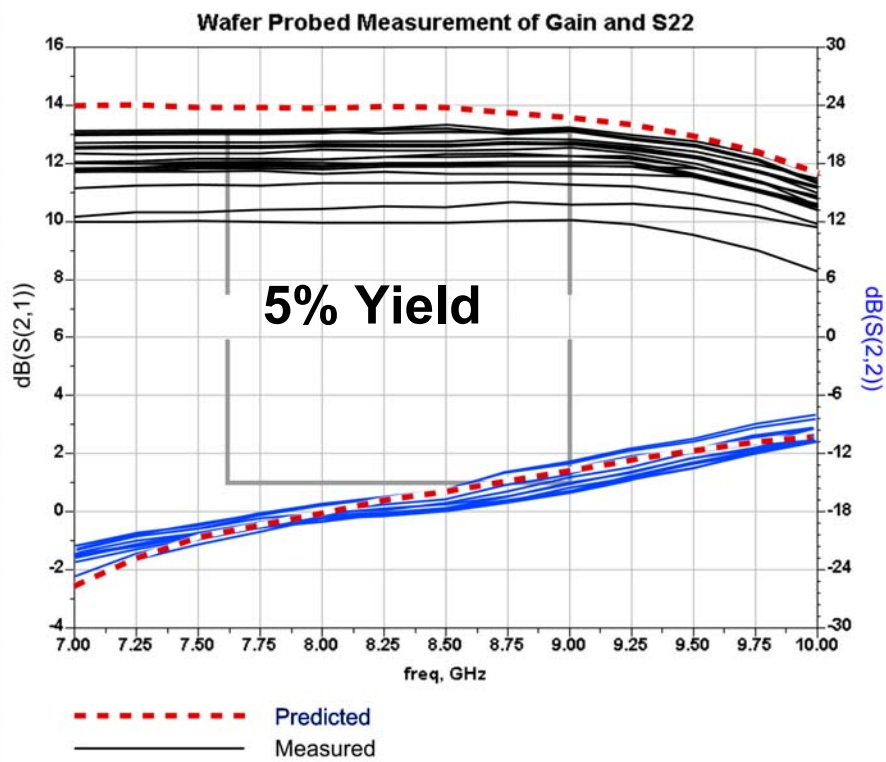
Our Goal is to Create Something like Amp2

Amp1

Amp2

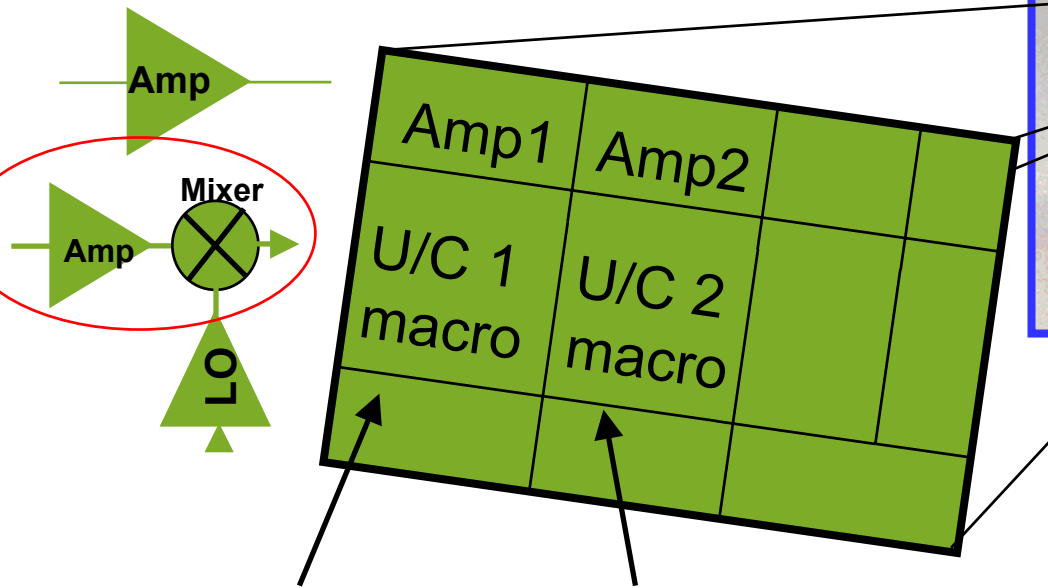
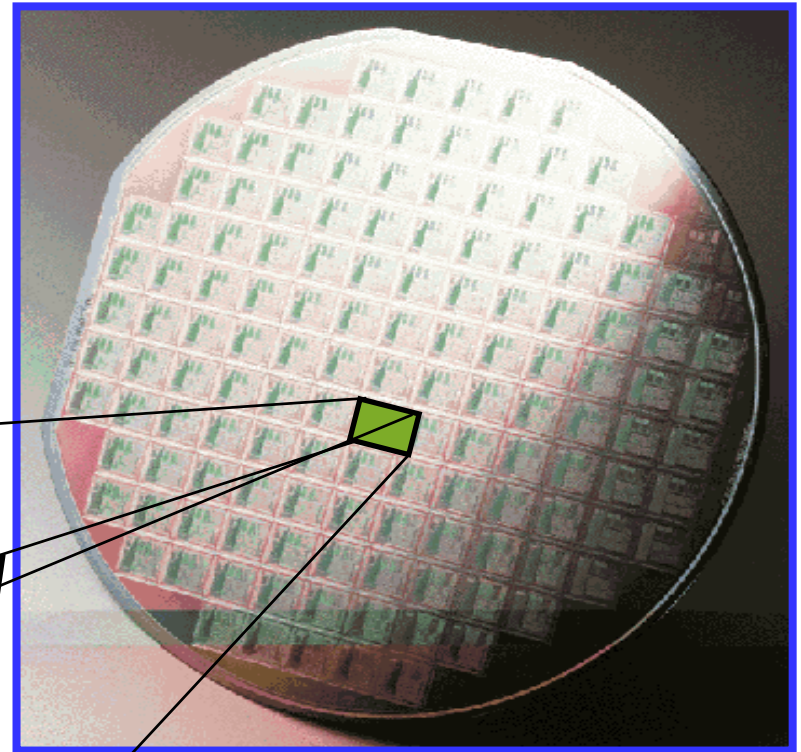
Standard Design Technique

DFY based Design Technique



Real MMIC Designs – Fabricated on the same wafer

A Reticle contains a few circuits, stepped and repeated across the whole wafer



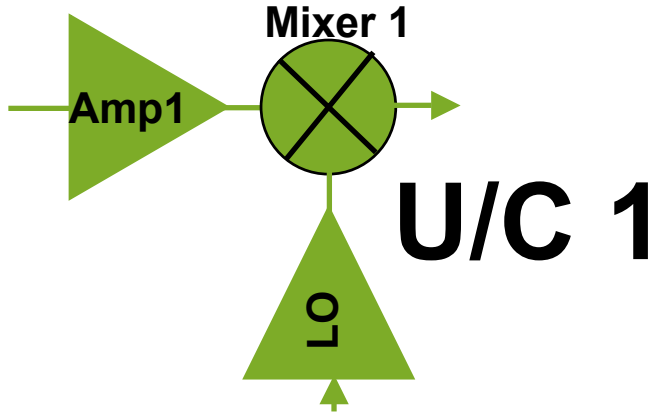
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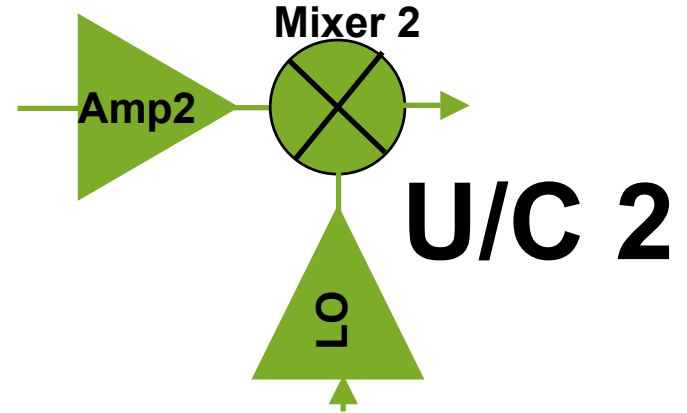


Our Goal is to Create Something like U/C 2



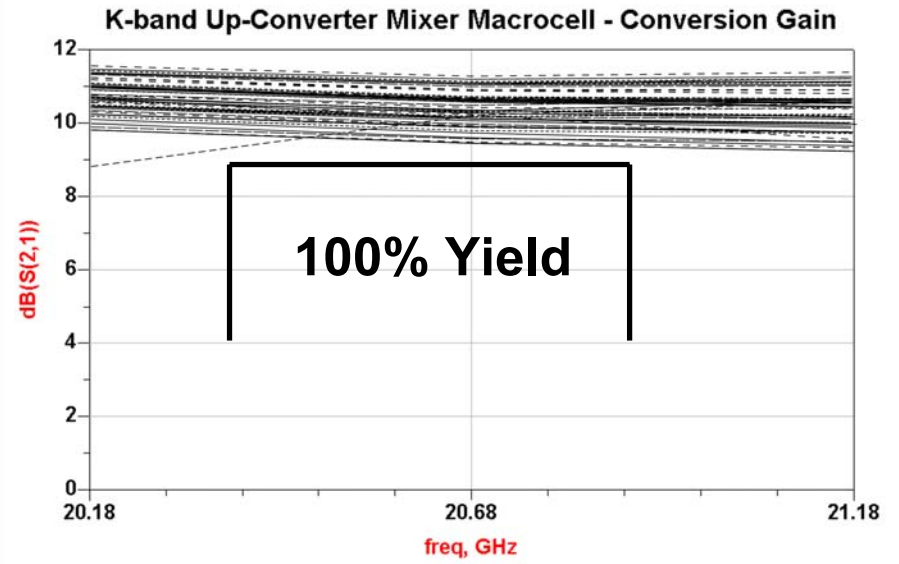
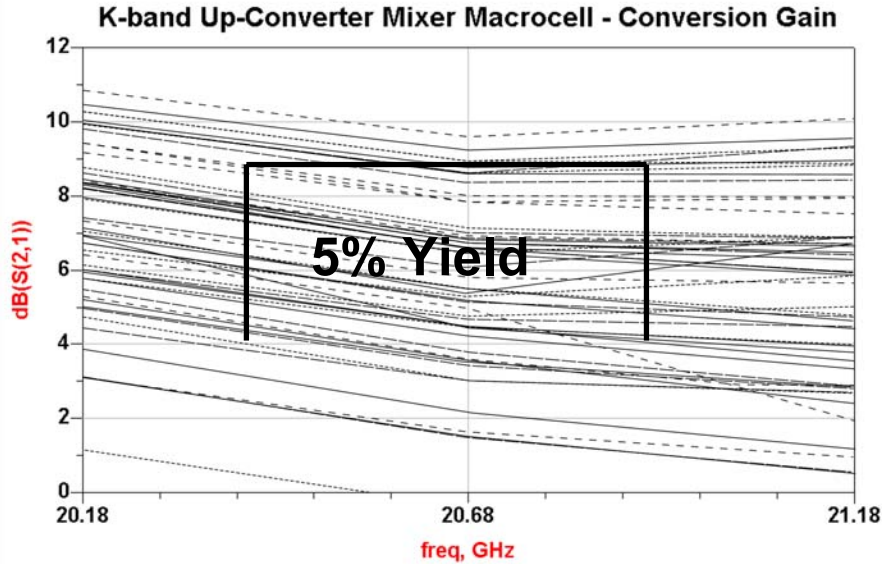
U/C 1

Standard Design Technique



U/C 2

DFY Based Design Technique



The DFY Process for MMIC

Obtain process parameters



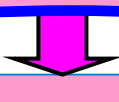
Statistical device model
or actual measured
parameters



Start nominal design



Optimize design



Monte Carlo Yield analysis

DFY Tools

Sensitivity histograms /
find sensitive network



Sensitivity analysis



Design Of Experiments
(DOE) - find sensitive
network



Fix Design



Design centering /
yield optimization

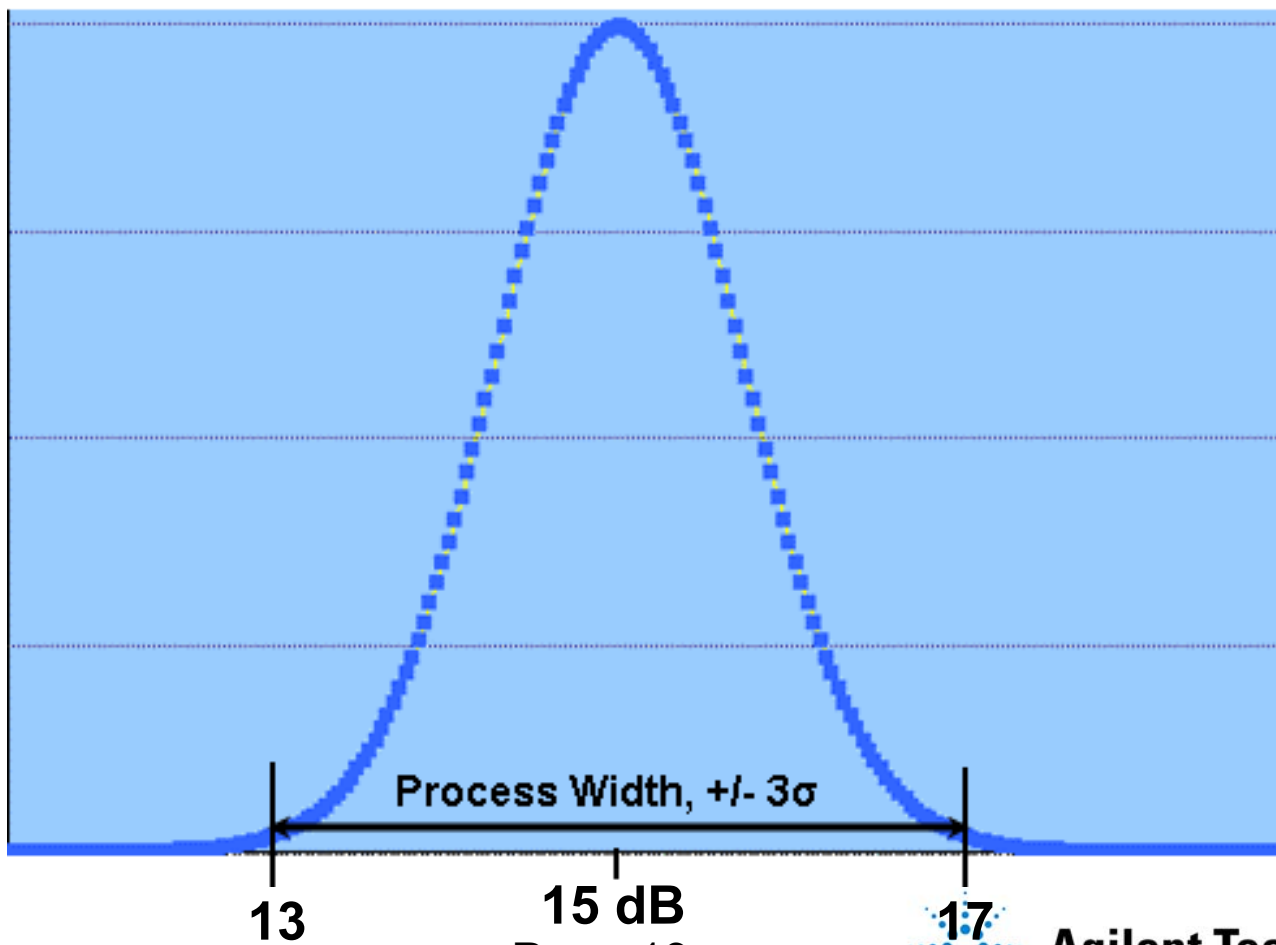


Typical Process Yield Curve

Example: Amplifier

Mean value of Gain = 15 dB

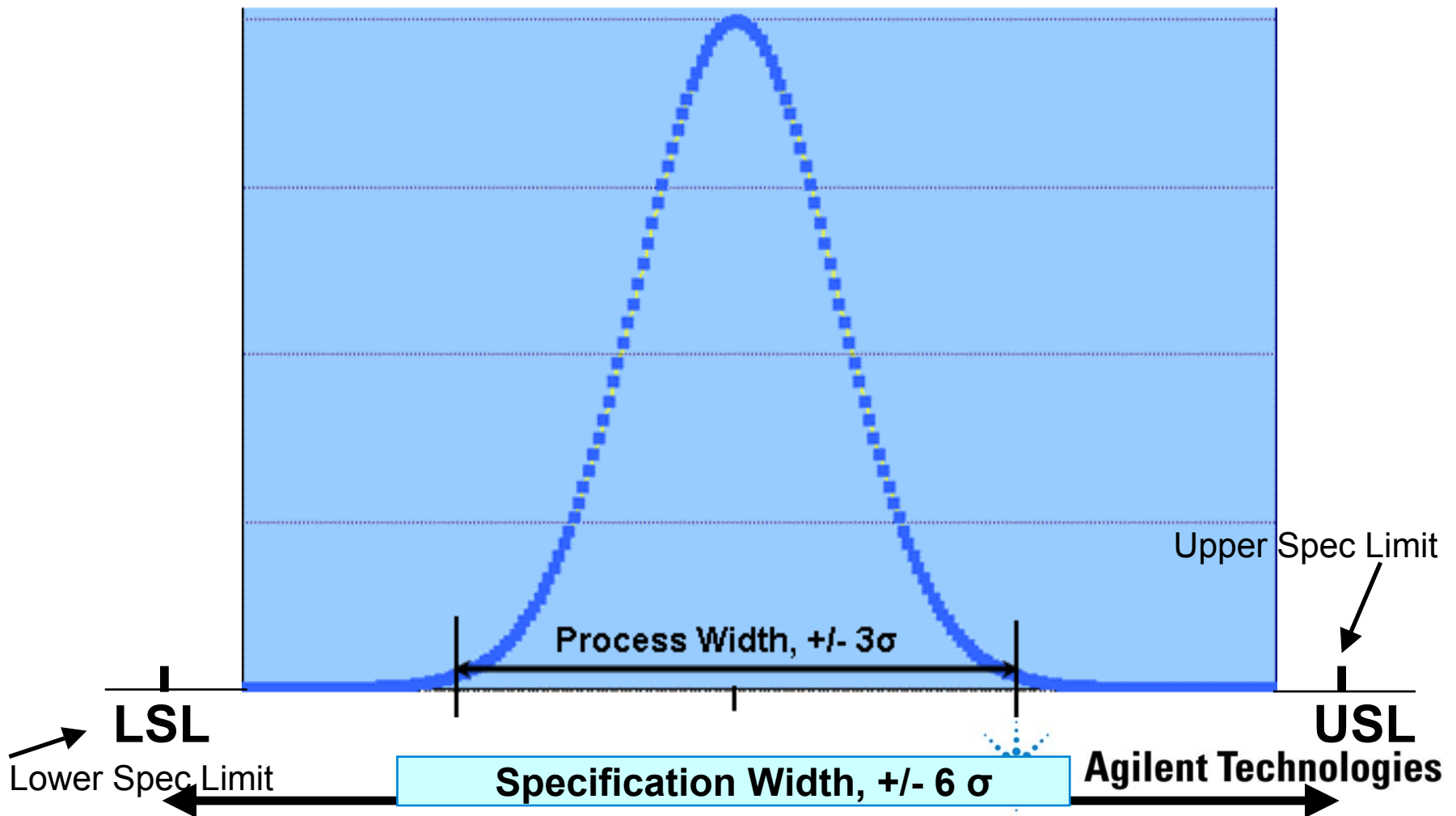
Process Variation Result in a Normal Distribution Spread



Example of a Six Sigma Robust Design

Process Width = $\pm 3\sigma$
Specs Width = $\pm 6\sigma$

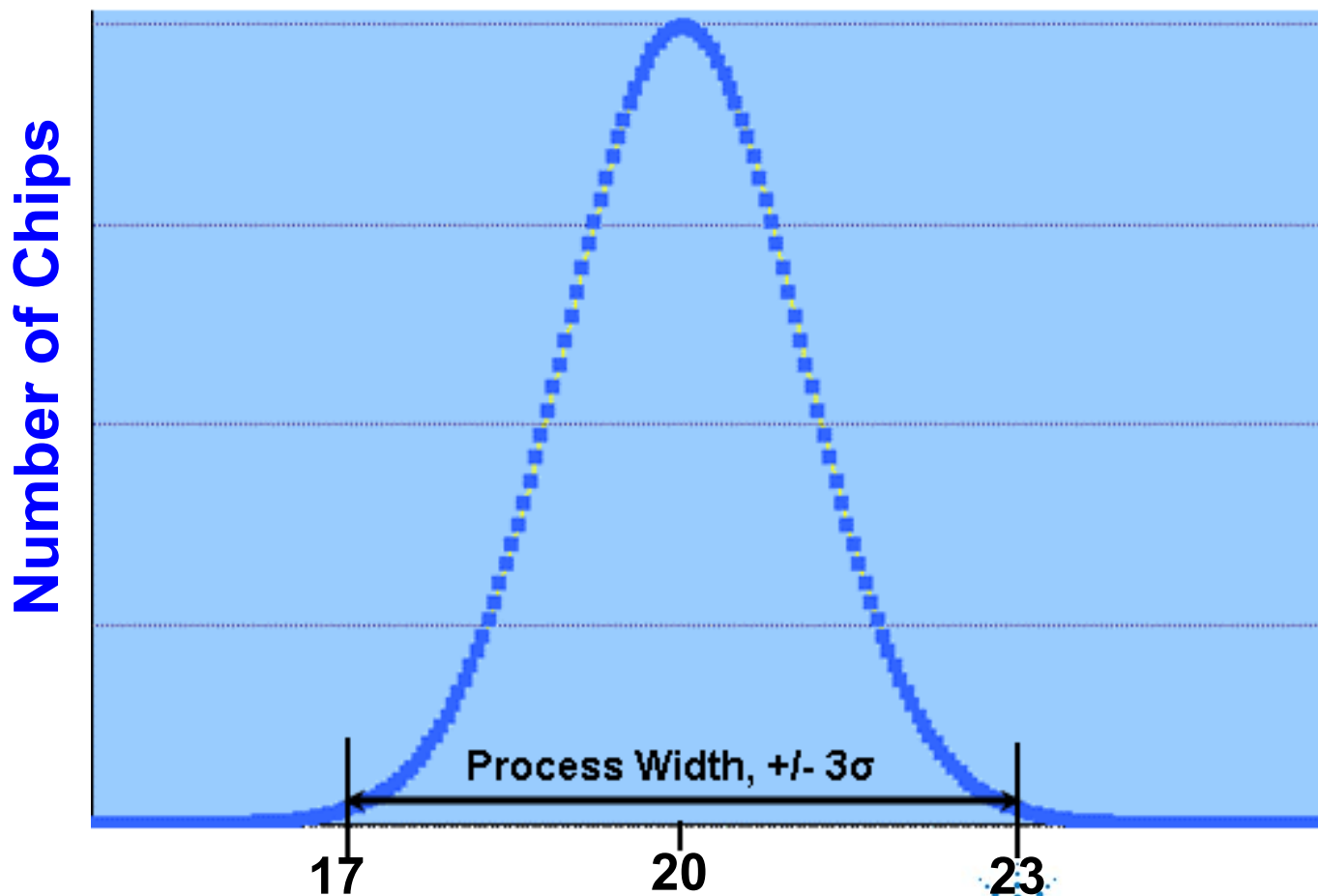
C_p = Process Capability Index
 C_p = Spec Width / Process Width
 C_p = $(USL - LSL) / \pm 3\sigma$



Example

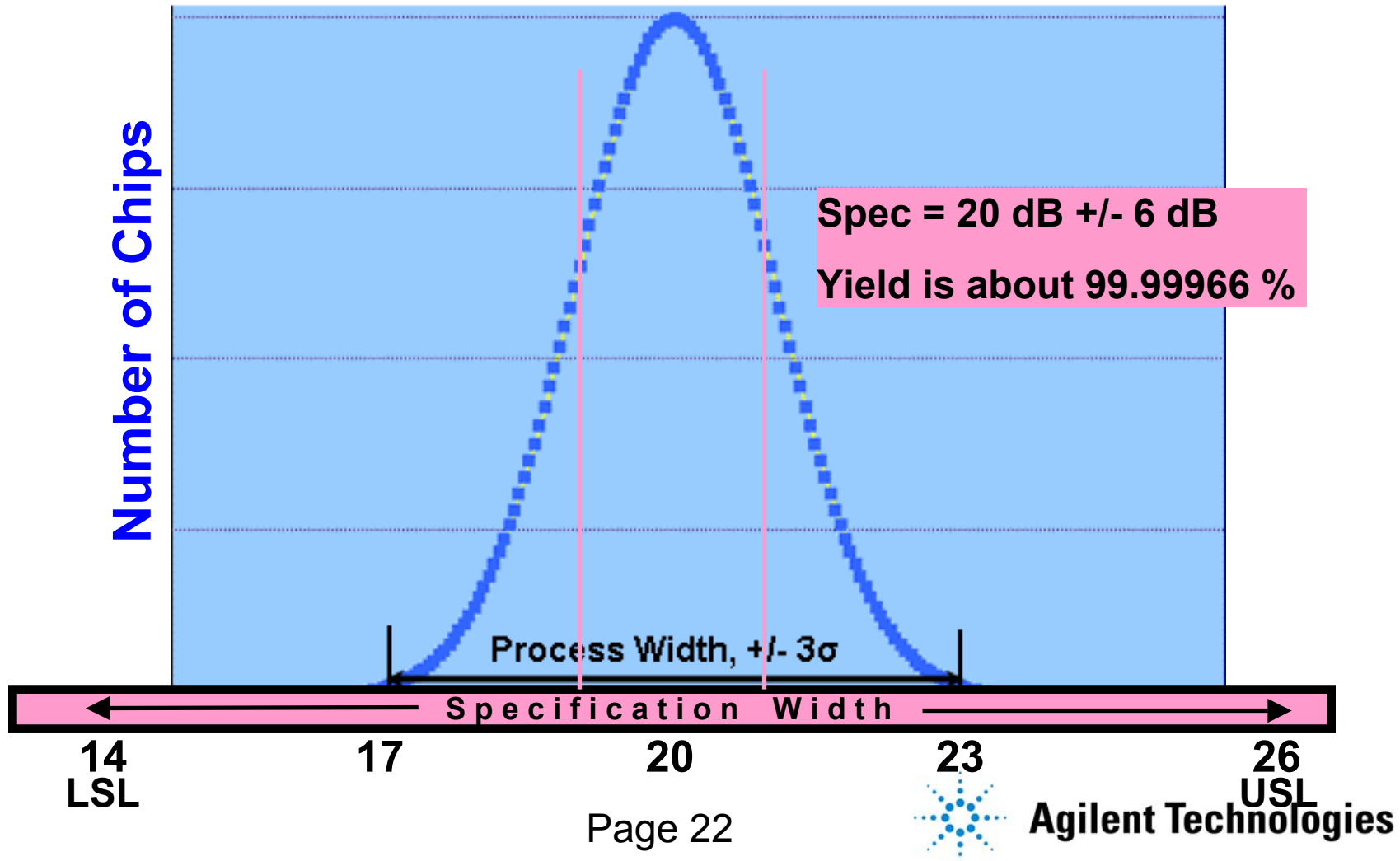
This curve could represent

a foundry's output of 100,000 Driver Amps with Gain=20 dB ($\pm 3\sigma = 6$ dB)



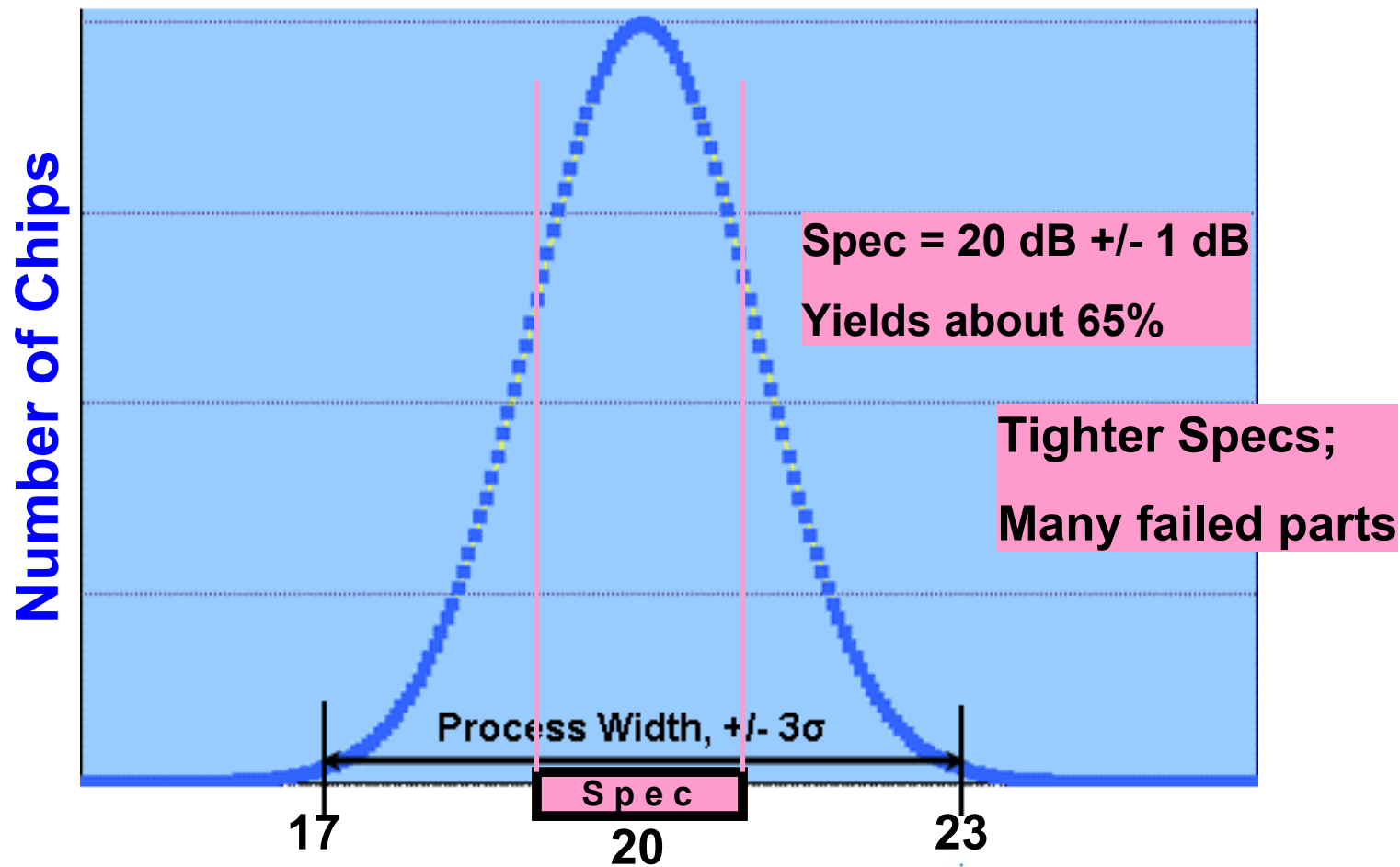
Example – Six Sigma Design

100,000 Driver Amps with Gain=20 dB ($\pm 3\sigma = 6$ dB)



Typical Process Yield Curve

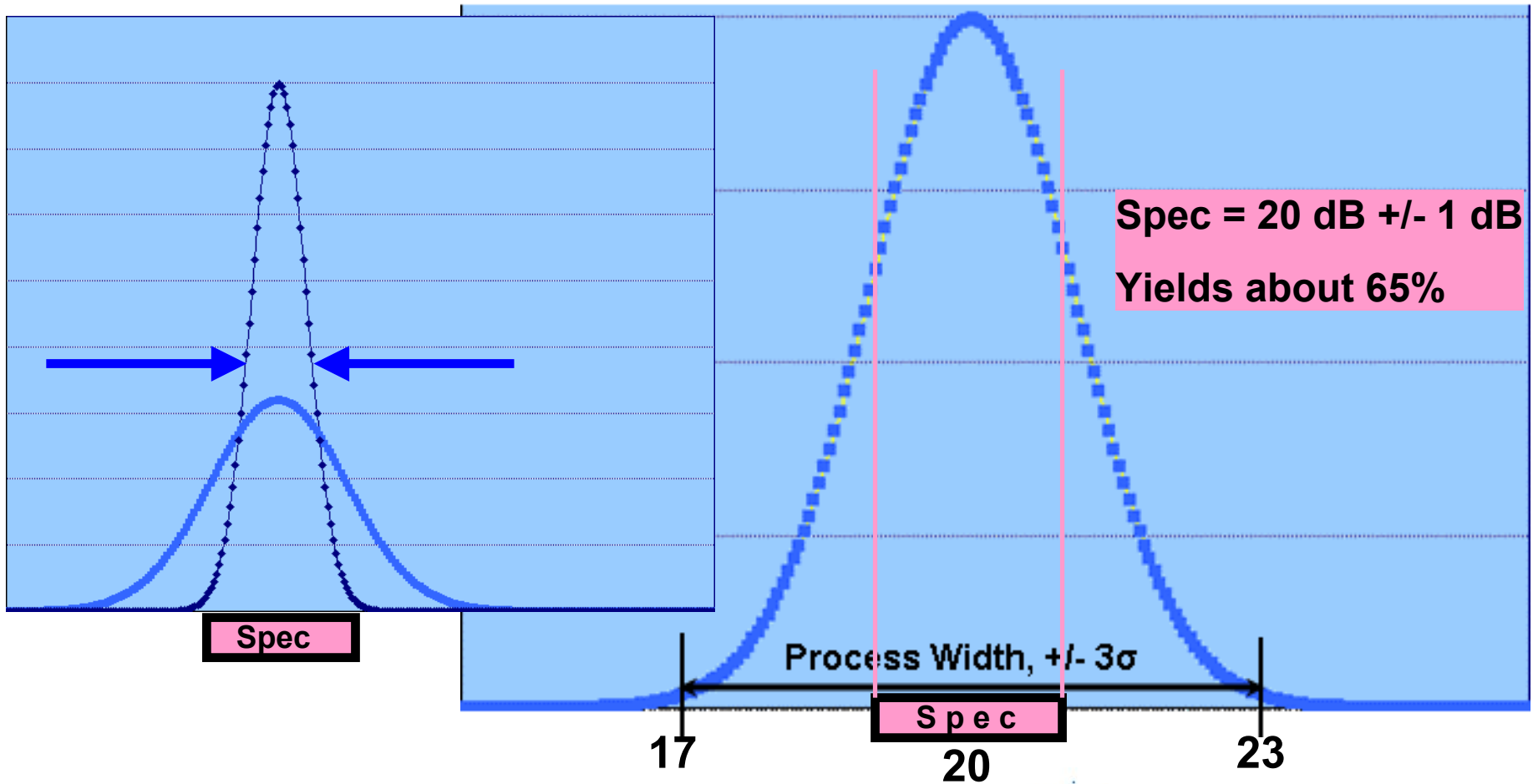
100,000 Power Amps with Gain=20 dB ($\pm 3\sigma = 6$ dB)



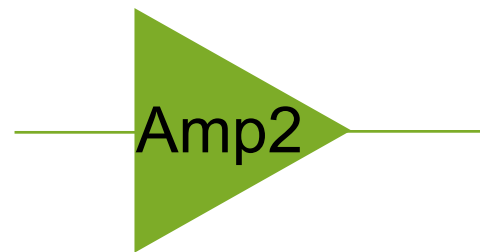
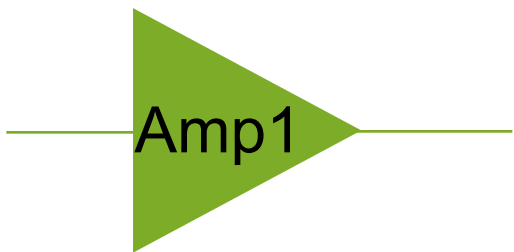
Make the Process Yield Curve Narrower

100,000 Power Amps with Gain=20 dB ($\pm 3\sigma = 6$ dB)

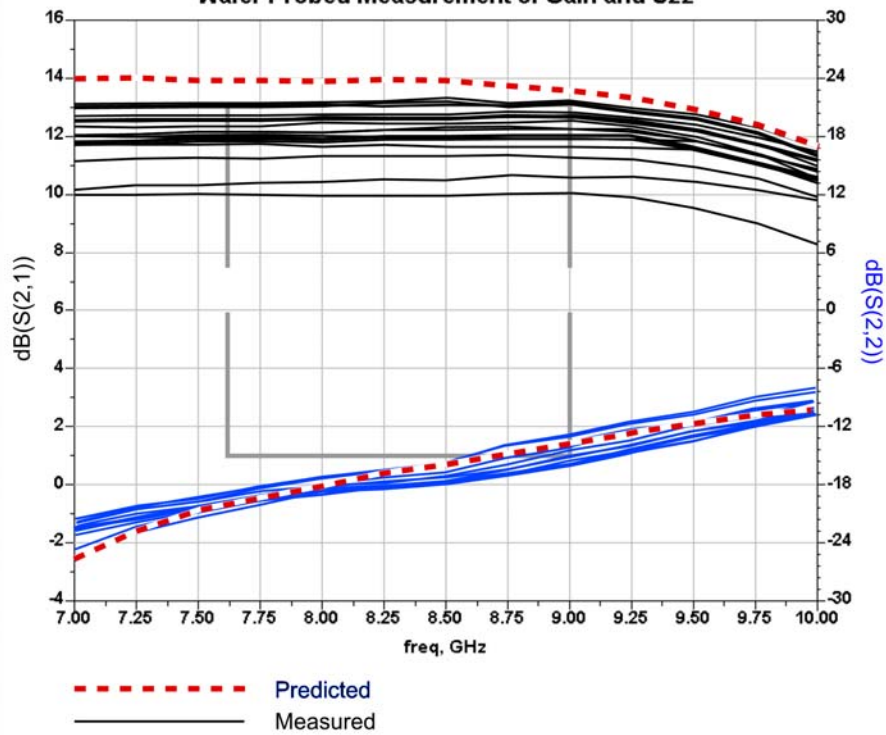
Change Design to Yield Gain=20 dB ($\pm 3\sigma = 2$ dB)



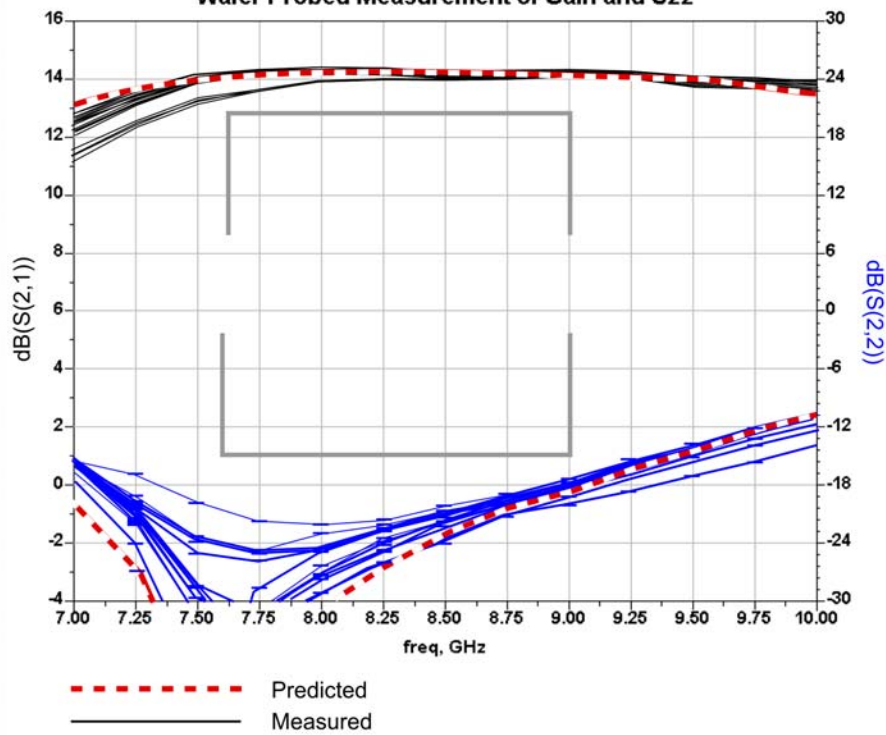
Our Goal is to Create Something like Amp2



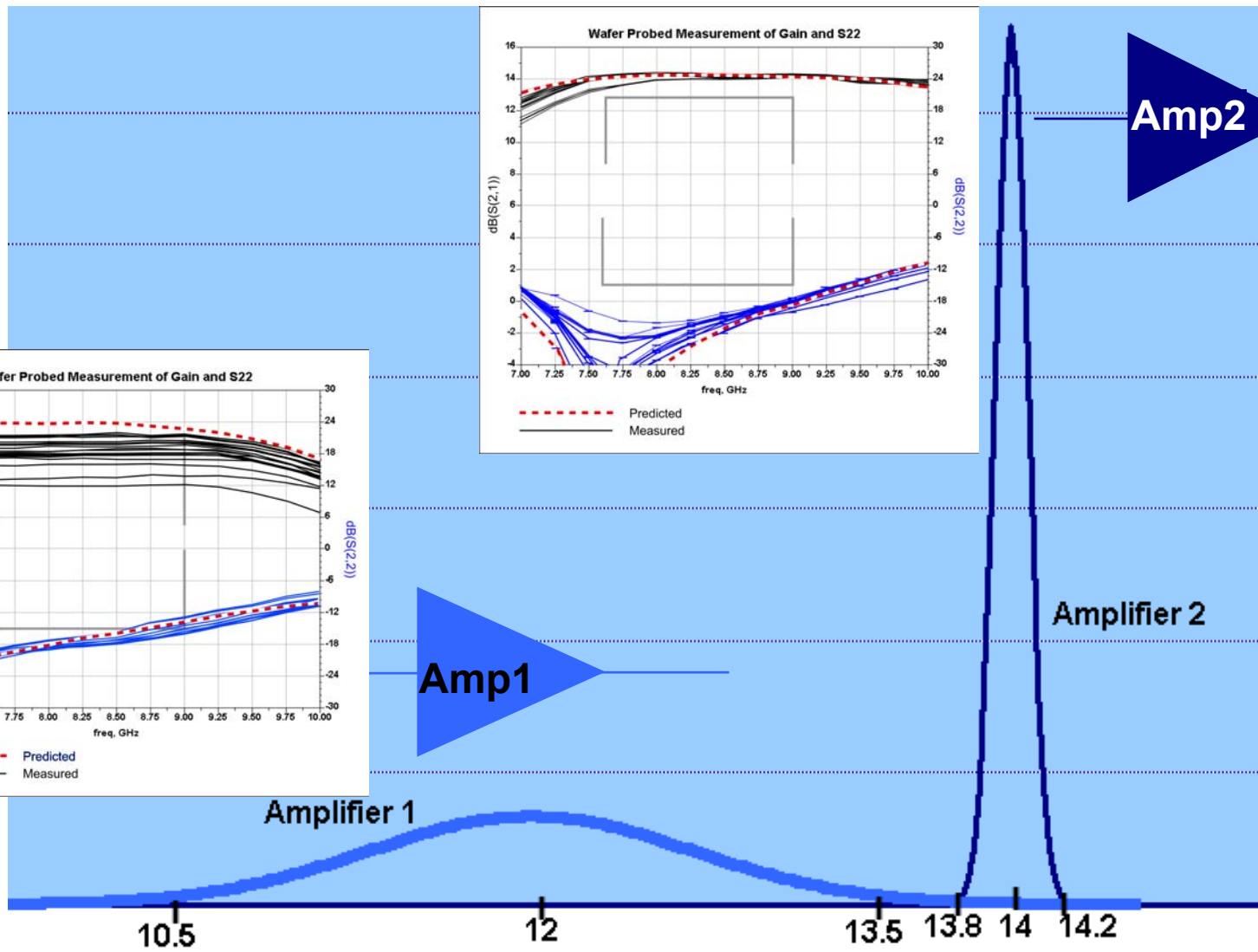
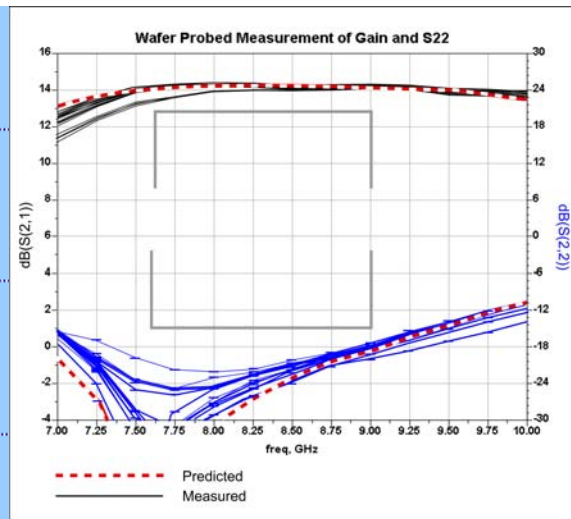
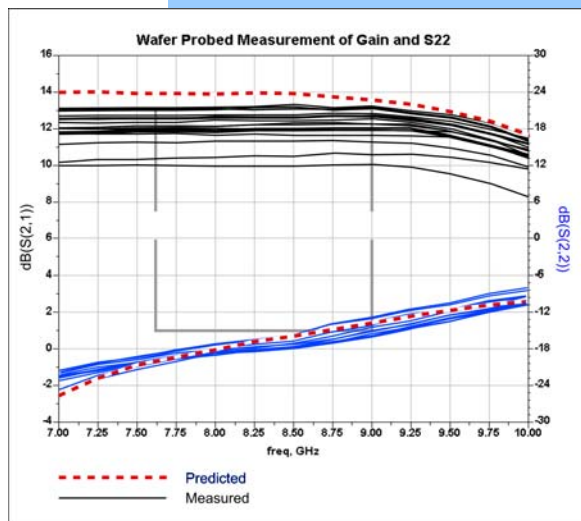
Wafer Probed Measurement of Gain and S22



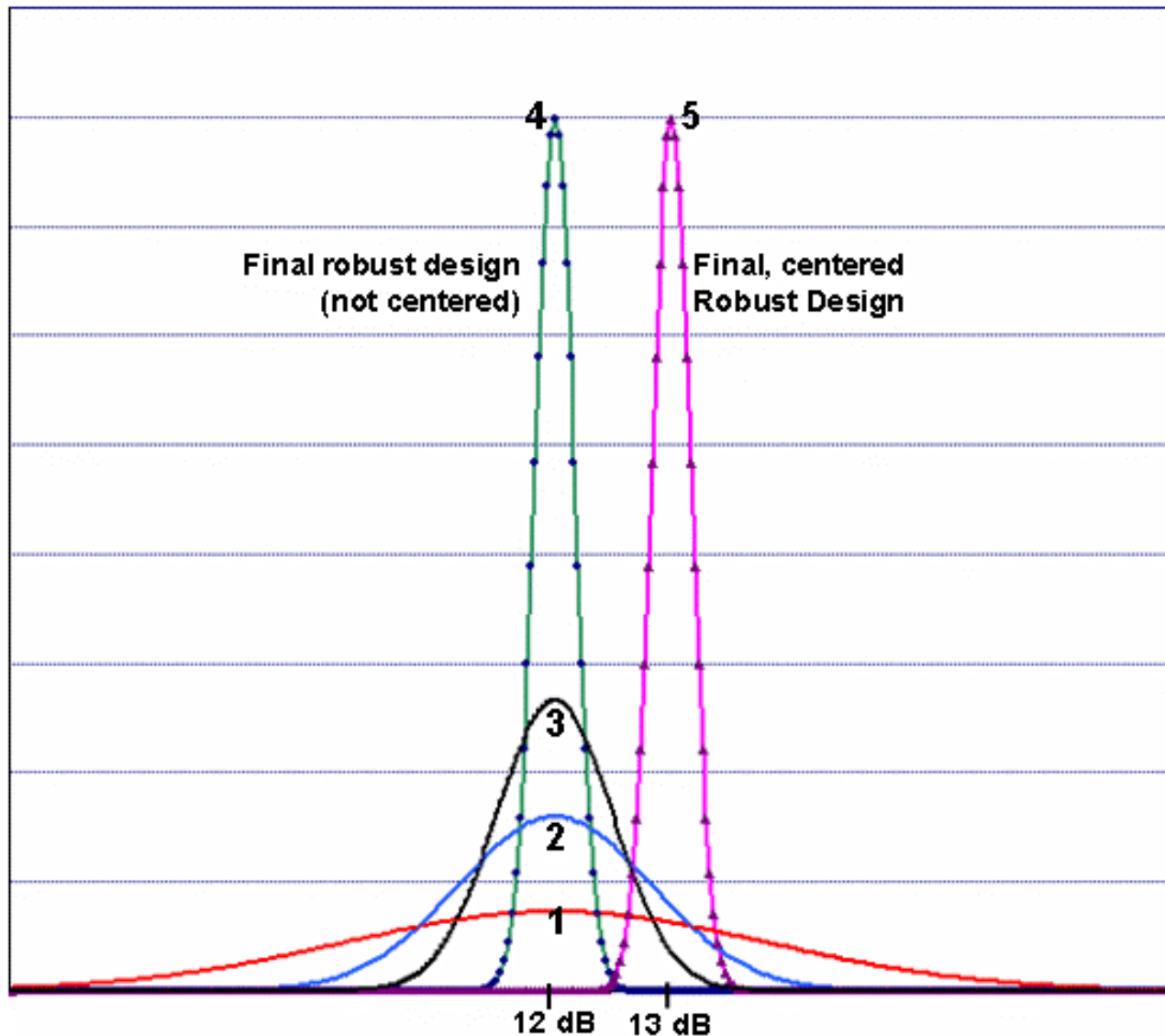
Wafer Probed Measurement of Gain and S22



Amp1 & Amp2 “Yield Distributions”



The DFY Process



Curve 1
Original Design

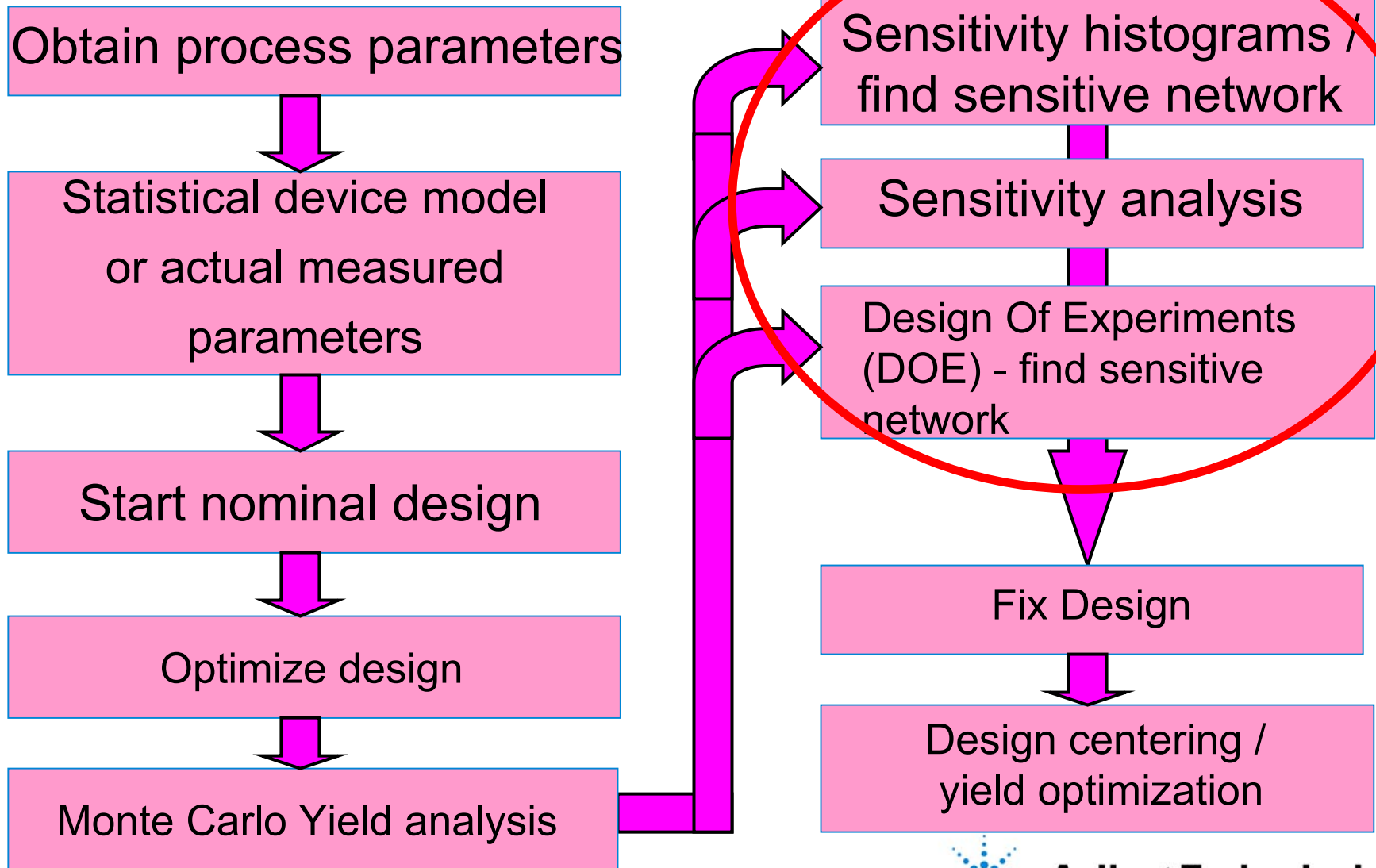
Curves 2,3
Fixing the Design to achieve Robustness

Curves 4
Further improvement towards achieving Robustness

Curve 5
Final Shift the Response by Design Centering to meet Specs.



The DFY Process for MMIC



Yield Sensitivity Histograms (YSH)

Yield analysis Data are post processed via built-in AEL Expressions to extract and display YSH results and more...

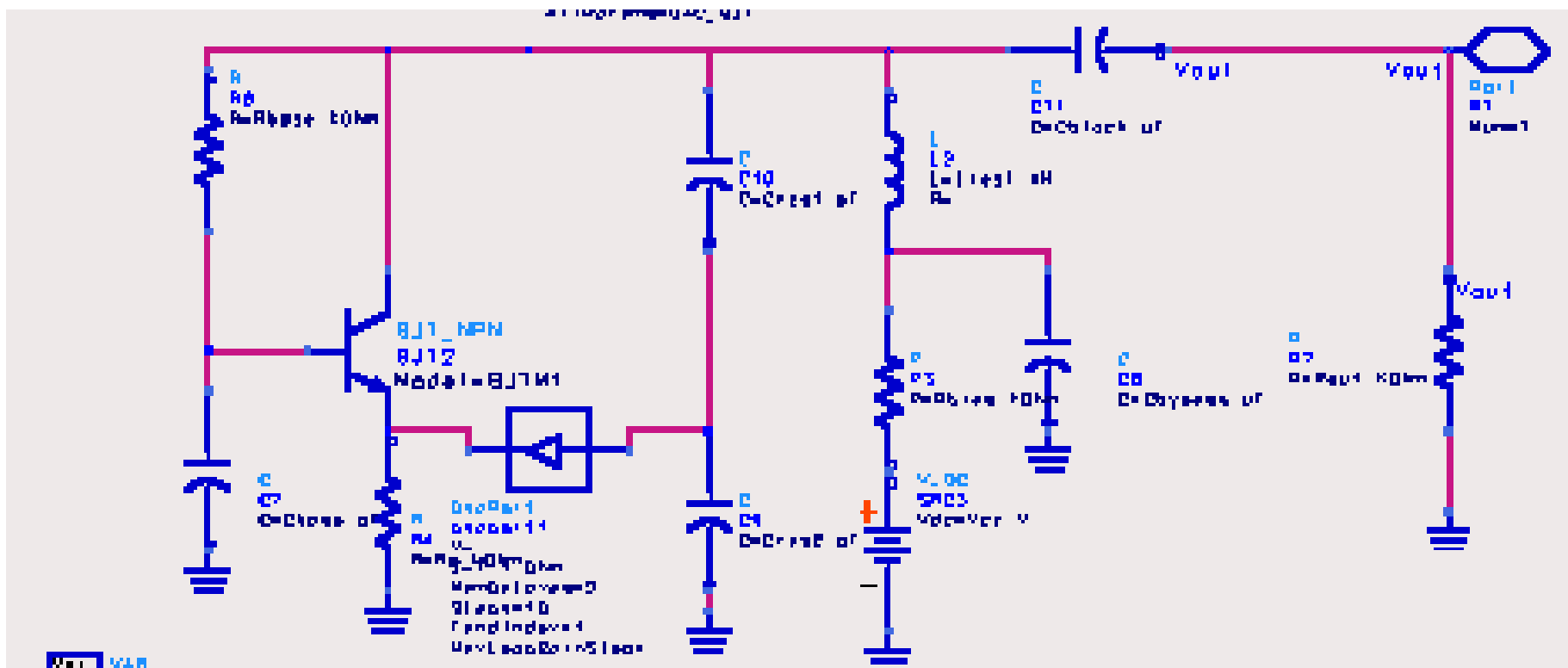
YSH display yield with respect to each element variation.

YSH provide insight to how sensitive the design is with respect to each of the design's elements.

YSH help designers to pinpoint the sensitive **RED X** parts in their designs. As a result, designers make decision to replace these parts with “tighter tolerance parts” in Board application (OR) create “less sensitive matching networks” in IC designs.



Example: VCO Design



Statistical Analysis of Oscillator Performance

- 21 measured BQ67 transistors
- 5% uniform variation in lumped component values

Specs

$P_{out} > 4\text{dBm}$

$P_{Noise} < -85\text{ dBc @ } 10\text{ KHz}$

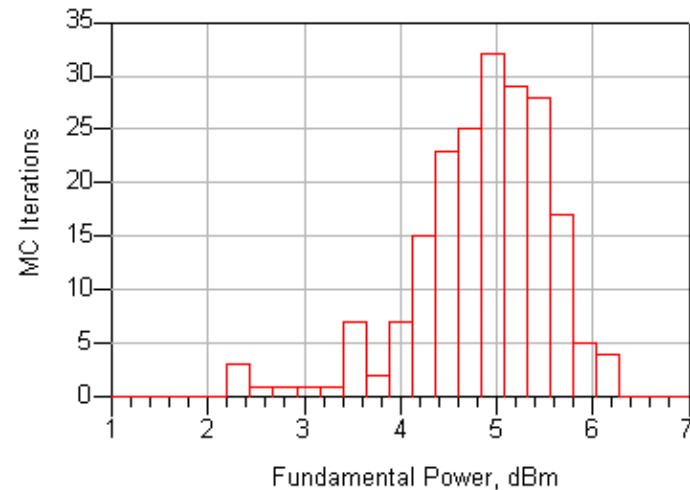
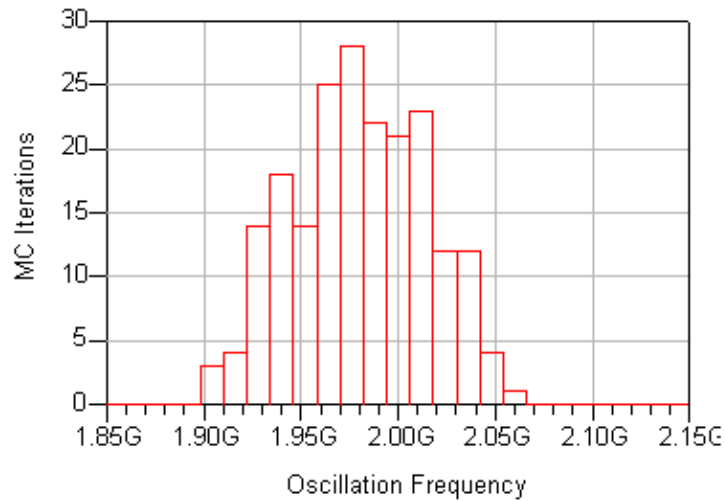
$1975\text{ MHz} < \text{Freq}_{Osc} < 2025\text{ MHz}$



VCO – Yield after Optimization – 37.5 %

Statistical Analysis of Oscillator Performance

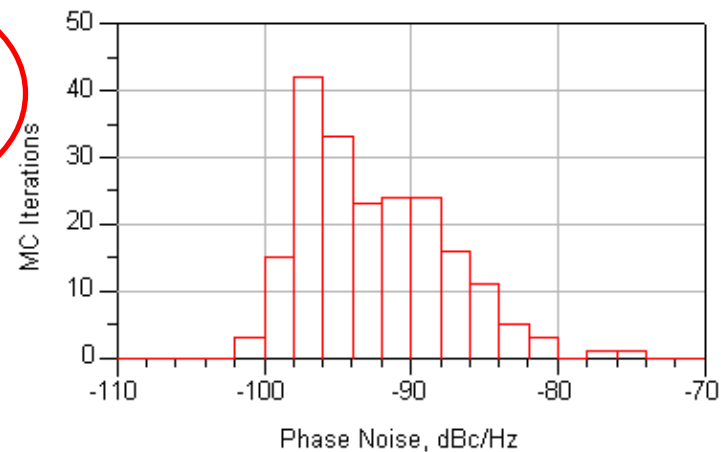
- 21 measured BFQ67 transistors
- 5% uniform variation in lumped component values



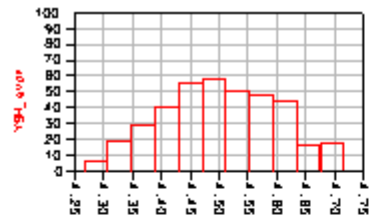
NumFail	NumPass	Yield
125.000	75.000	37.500

Number of Monte Carlo iterations that failed to produce an oscillation

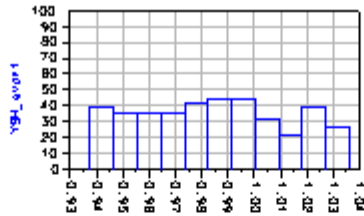
NOOSC
0



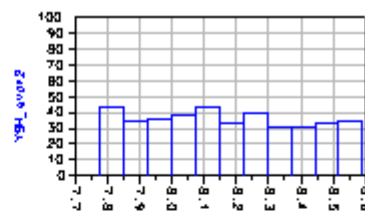
VCO – Yield Sensitivity Histograms



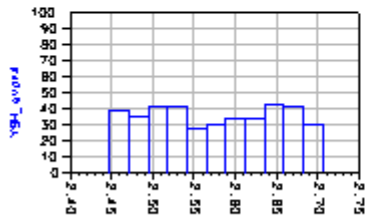
Index(YSH_ever1)
Eqn svari=Lres1



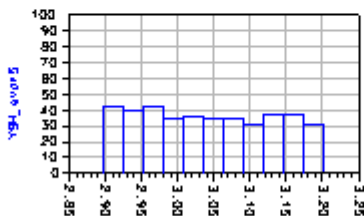
Index(YSH_ever1)
Eqn svari=Cres1



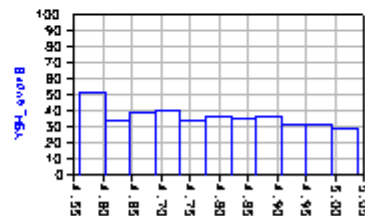
Index(YSH_ever2)
Eqn svari=Cres2



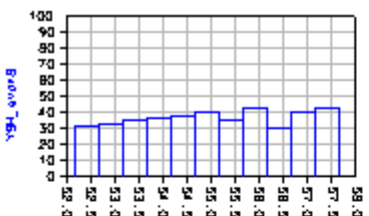
Index(YSH_ever4)
Eqn svari=Re



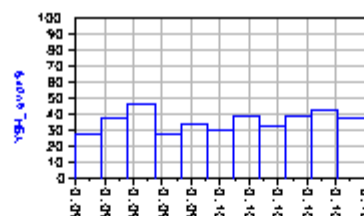
Index(YSH_ever5)
Eqn svari=Rbias



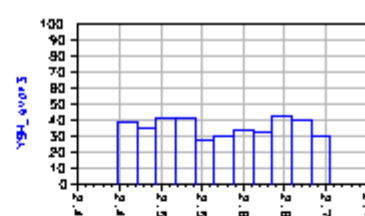
Index(YSH_ever8)
Eqn svari=Roul



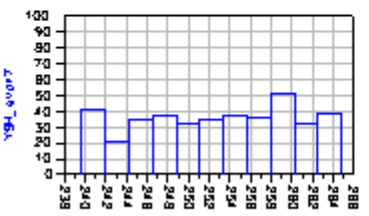
Index(YSH_ever8)
Eqn svari=Cbase



Index(YSH_ever9)
Eqn svari=Cblock



Index(YSH_ever3)
Eqn svari=Re



Index(YSH_ever7)
Eqn svari=Rbase

Eqn Spec1_spec_Min = 20

Eqn Spec1_spec_Max = 25

Eqn Spec2_spec_Min = 1975

Eqn Spec2_spec_Max=2025

Eqn Spec3_spec_Min=-200

Eqn Spec3_spec_Max=-85

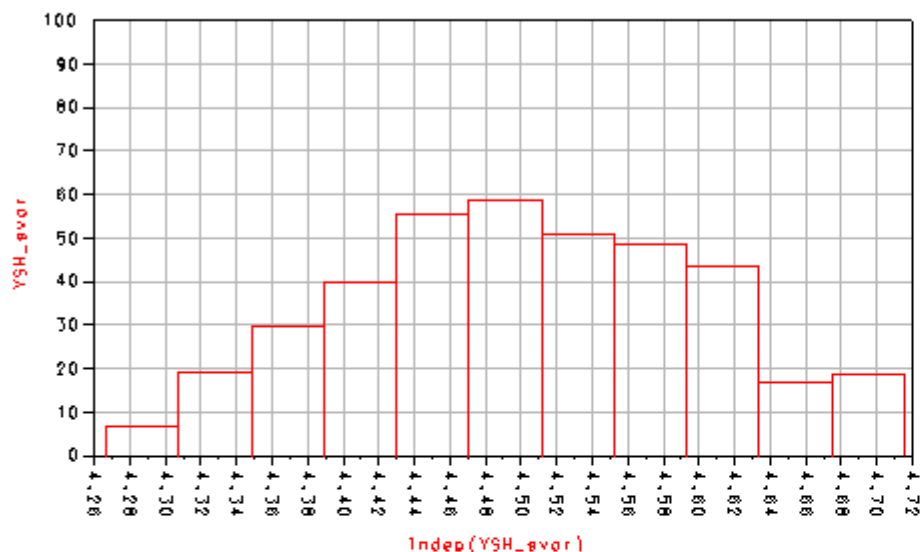


VCO – Yield Sensitivity Histogram for Lres1

```
Eqn pf_Total = pf_Spec2_svar * pf_Spec1_svar * pf_Spec3_svar
```

```
Eqn YSH_svar = yield_sens(pf_Total, 11)
```

Change "pf_Total" to "pf_Spec2_svar" if you like to see the sensitivity versus Spec2 (which is the frequency spec).



RED X component

```
Eqn svar = Lres1
```

Change the name of component to see the yield sensitivity versus the component tolerance.

```
Eqn Spec1_vs_svar=vs( mean(Spec1), svar)
```

```
Eqn pf_Spec1_svar=if ( Spec1_vs_svar > Spec1_spec_Max || Spec1_vs_svar < Spec1_spec_Min ) then 0.0 else 1.0
```

```
Eqn Spec1_spec_Min = 20      Eqn Spec1_spec_Max = 25
```

Change the specs and the yield updates automatically

```
Eqn Spec2_vs_svar = vs( mean(Spec2), svar)
```

```
Eqn pf_Spec2_svar = if ( Spec2_vs_svar > Spec2_spec_Max || Spec2_vs_svar < Spec2_spec_Min ) then 0.0 else 1.0
```

```
Eqn Spec2_spec_Min = 1975   Eqn Spec2_spec_Max=2025
```

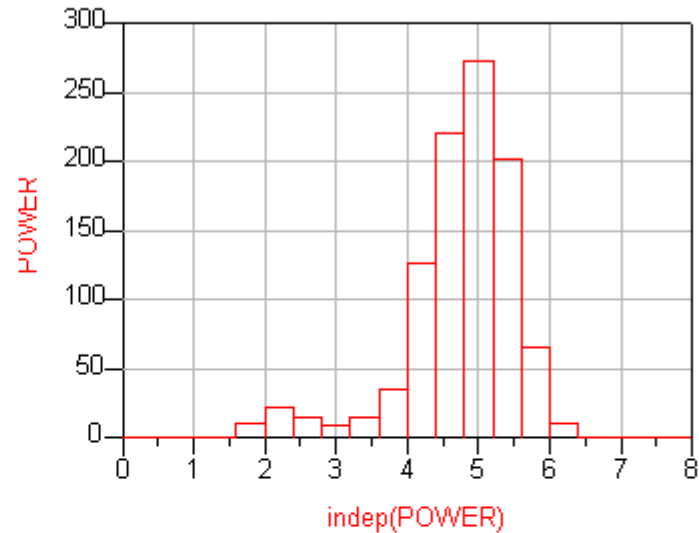
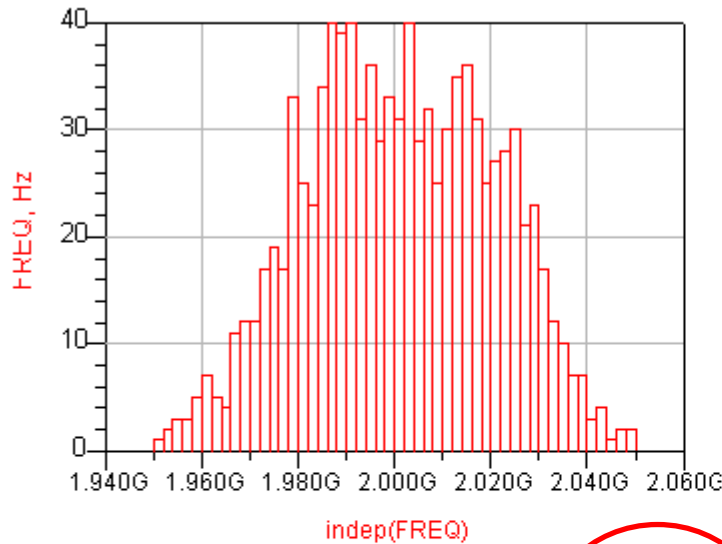
```
Eqn Spec3_vs_svar=vs( mean(Spec3), svar)
```

```
Eqn pf_Spec3_svar=if ( Spec3_vs_svar > Spec3_spec_Max || Spec3_vs_svar < Spec3_spec_Min ) then 0.0 else 1.0
```

```
Eqn Spec3_spec_Min=-200    Eqn Spec3_spec_Max=-85
```

Higher Yield by controlling Lres1 +/- 1%

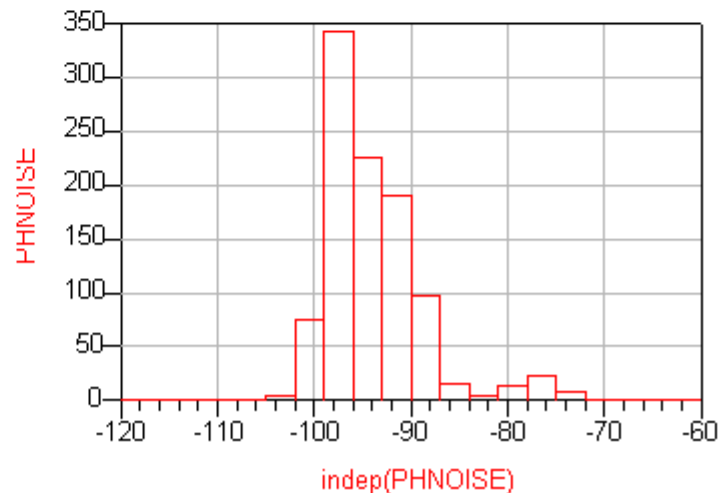
Statistical Analysis of Oscillator Performance
 - 21 measured BFQ67 transistors
 - 5% uniform variation in lumped component values



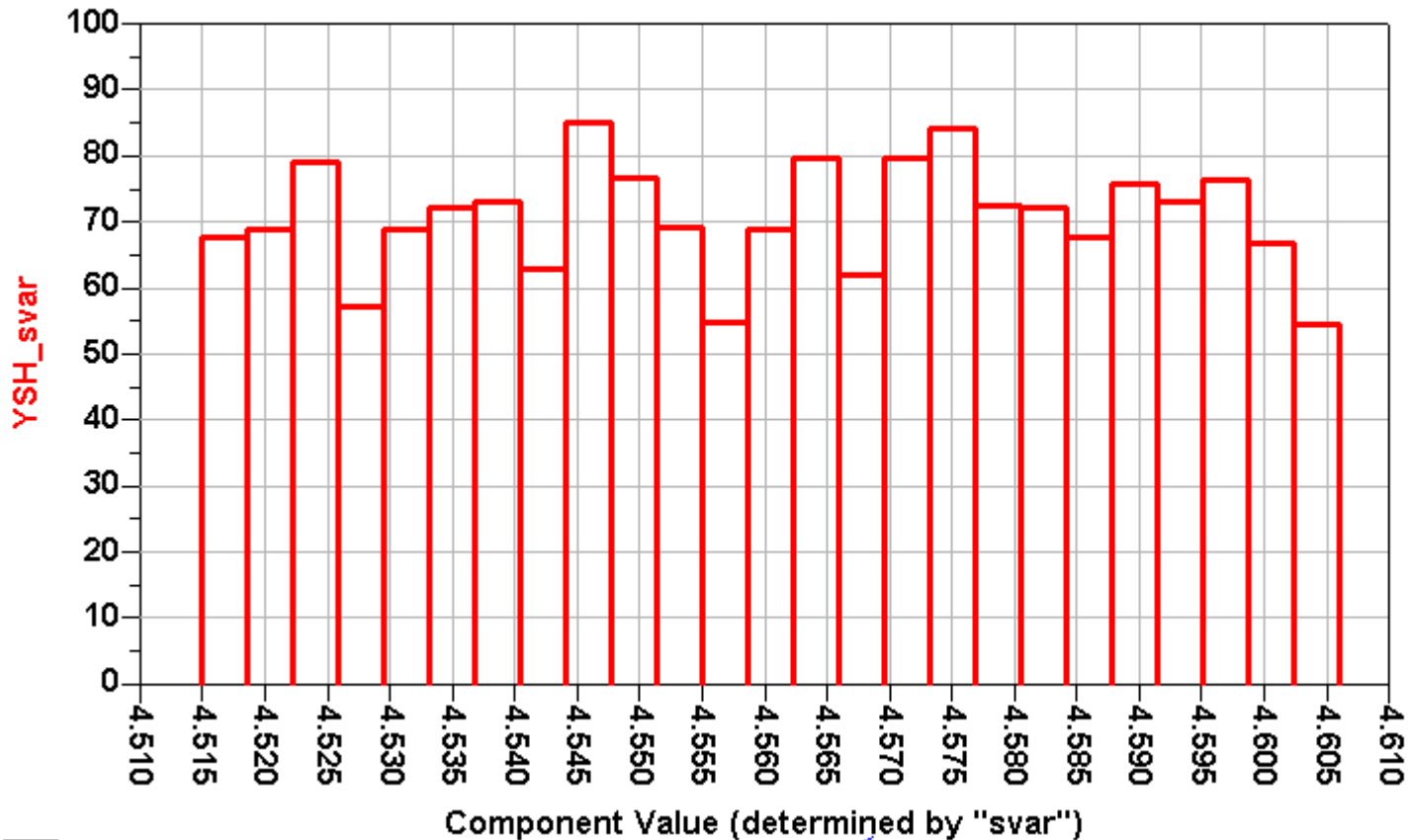
NumFail	NumPass	Yield
296.000	704.000	70.400

Number of Monte Carlo iterations that failed to produce an oscillation

...OSC
0



Yield Sensitivity Histogram of controlled "Lres1"



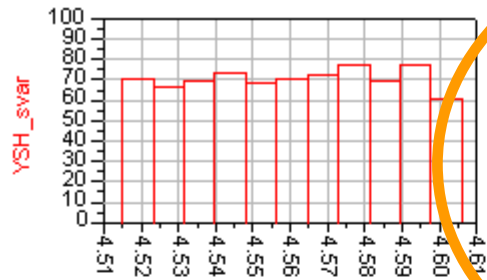
Eqn svar = Lres1

Change the name of component to see the yield sensitivity versus the component value.

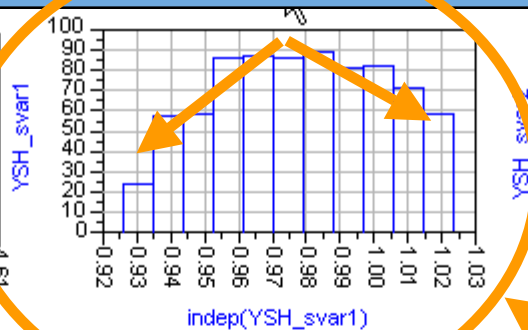
L_nom = 4.560 nh +/- 1%



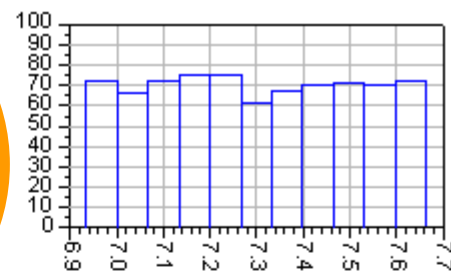
Notice now Cres1 has negative effect on Yield



indep(YSH_svar)
Eqn svar = Lres1

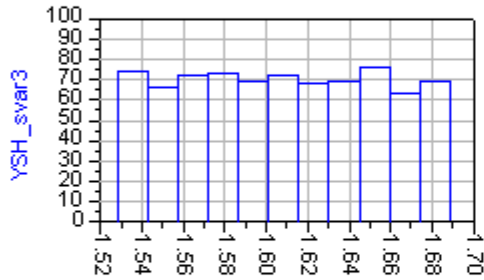


indep(YSH_svar1)
Eqn svar1=Cres1

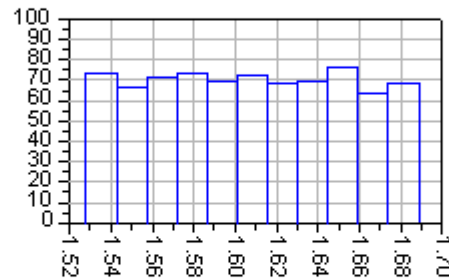


indep(YSH_svar2)
Eqn svar2=Cres2

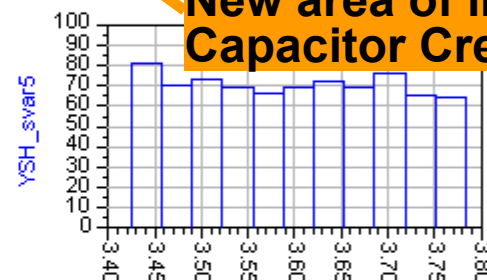
**New area of improvement
Capacitor Cres1**



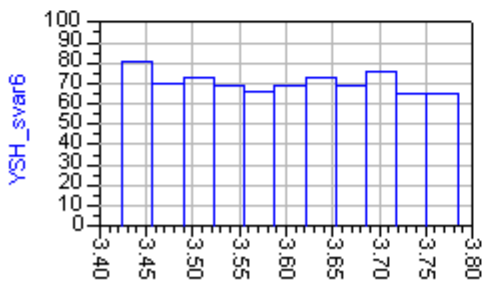
indep(YSH_svar3)
Eqn svar3=Re



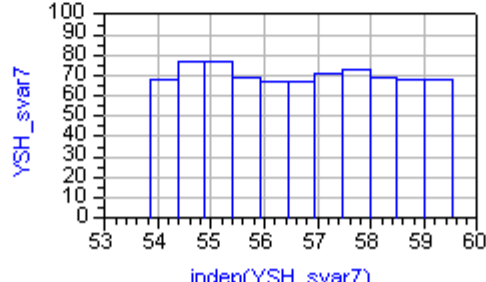
indep(YSH_svar4)
Eqn svar4=Re



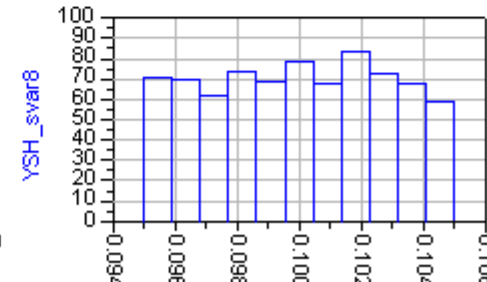
indep(YSH_svar5)
Eqn svar5=Rbias



indep(YSH_svar6)
Eqn svar6=Rbias



Eqn svar7=Cbase

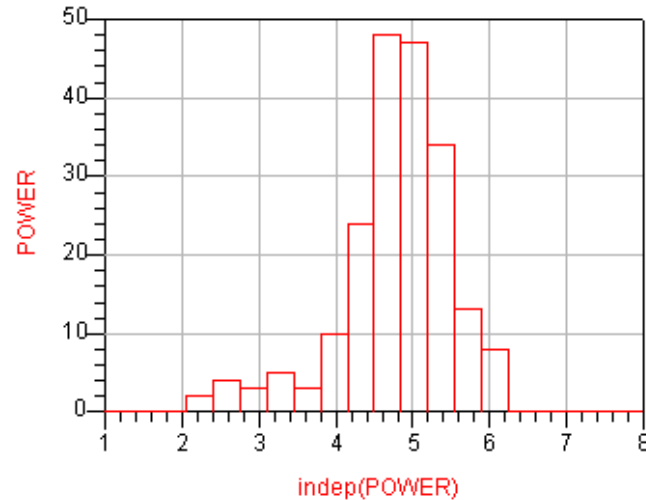
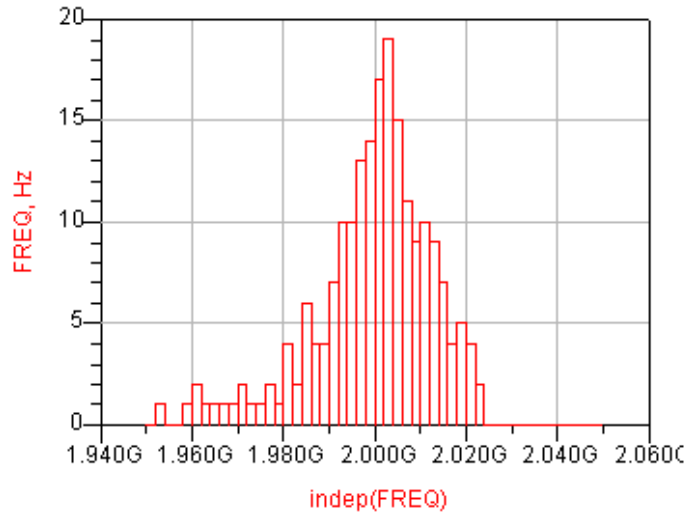


indep(YSH_svar8)
Eqn svar8=Cblock

Controlling Cres1 increase the Yield to 90%

Statistical Analysis of Oscillator Performance

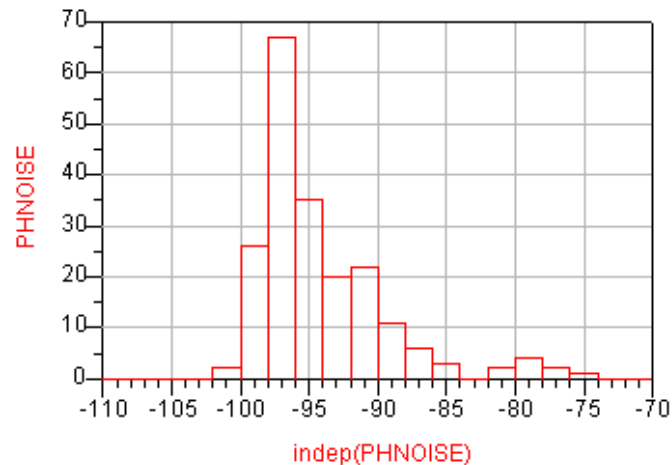
- 21 measured BFQ67 transistors
- 5% uniform variation in lumped component values



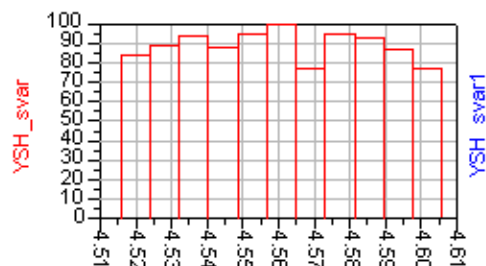
NumFail	NumPass	Yield
22.000	178.000	89.000

Number of Monte Carlo iterations that failed to produce an oscillation

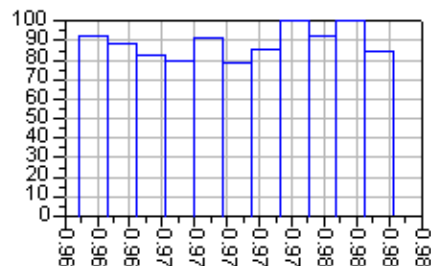
...OSC
0



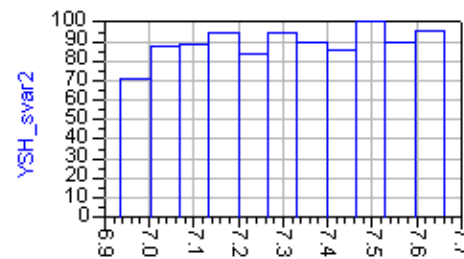
Now we don't see any more "Red X" components



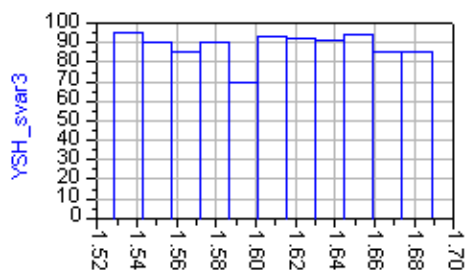
indep(YSH_svar)
Eqn svar = Lres1



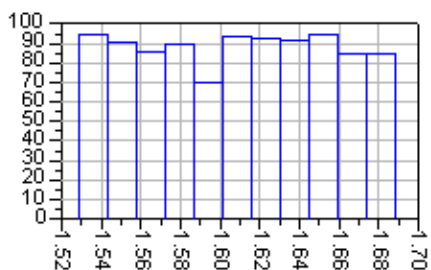
indep(YSH_svar1)
Eqn svar1=Cres1



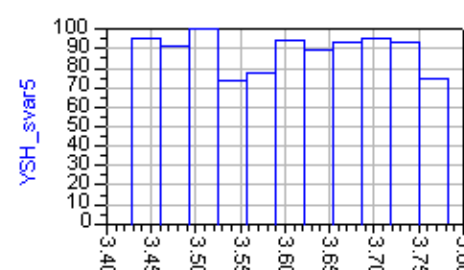
indep(YSH_svar2)
Eqn svar2=Cres2



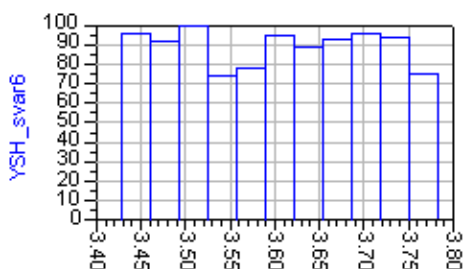
indep(YSH_svar3)
Eqn svar3=Re



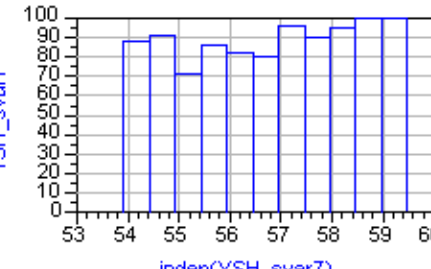
indep(YSH_svar4)
Eqn svar4=Re



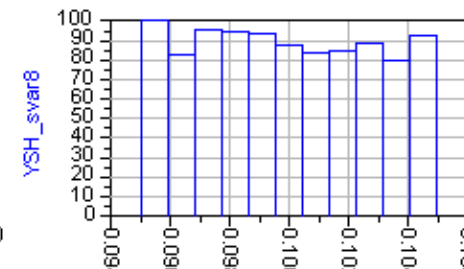
indep(YSH_svar5)
Eqn svar5=Rbias



indep(YSH_svar6)
Eqn svar6=Rbias



Eqn svar7=Cbase



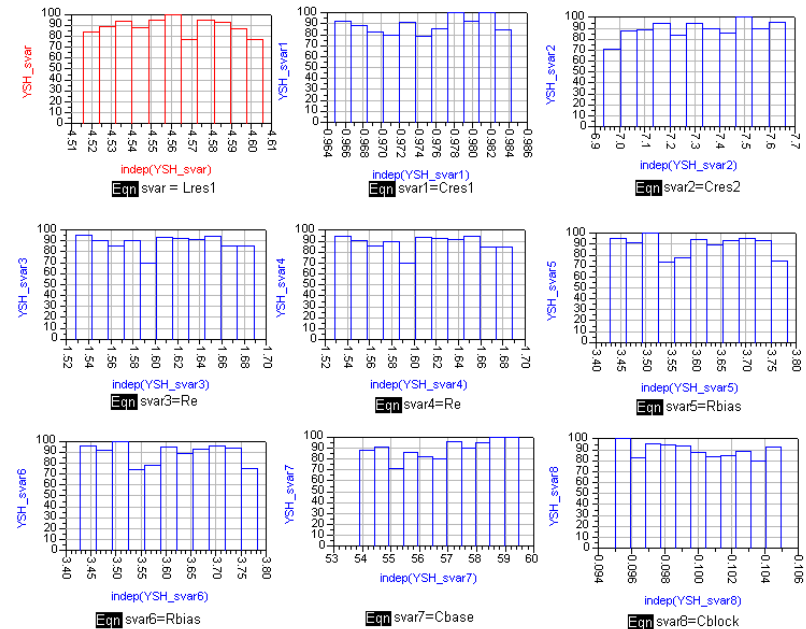
indep(YSH_svar8)
Eqn svar8=Cblock



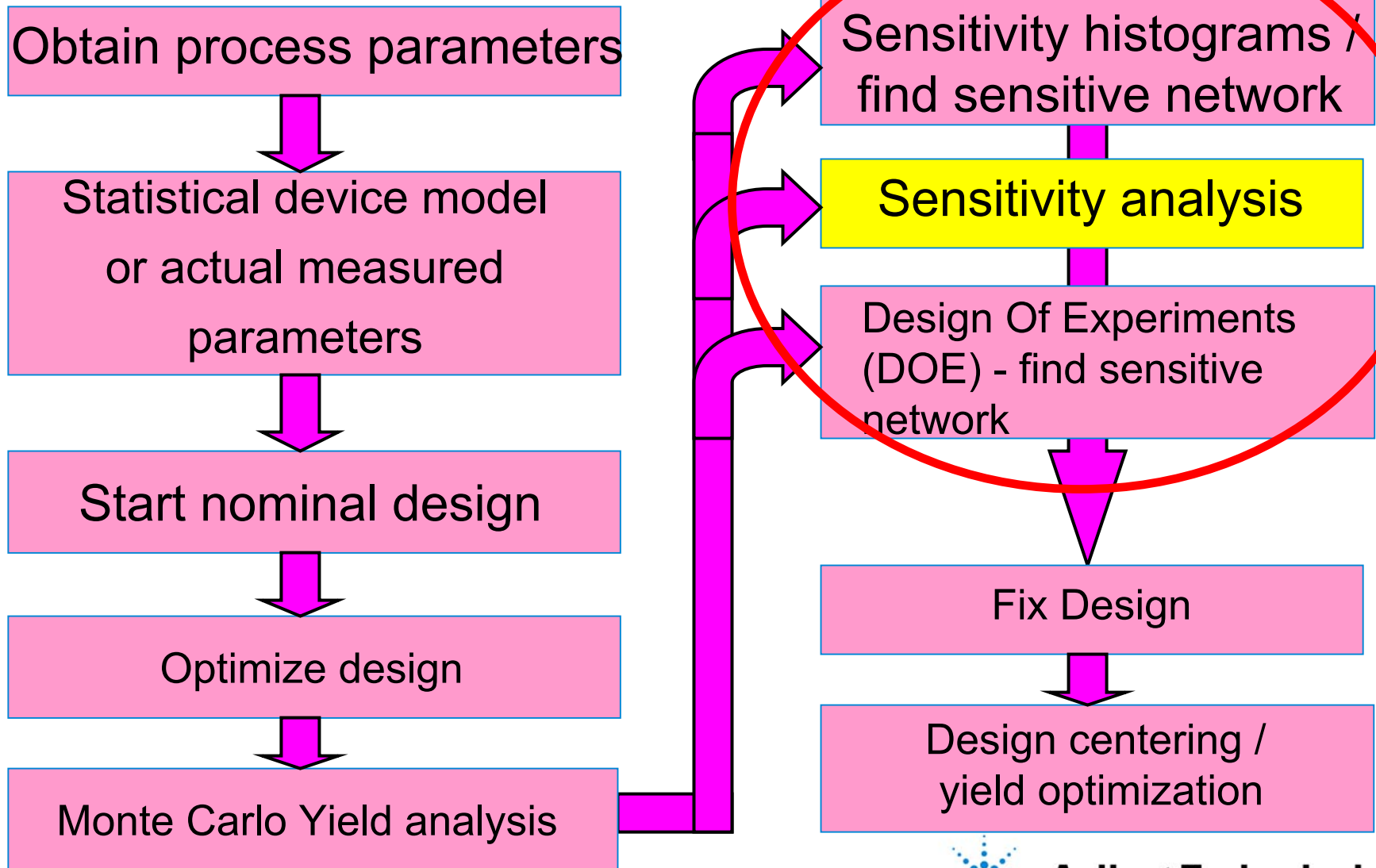
What we Learned from this VCO Example

Yield Sensitivity Histograms (YSH) helped us pinpoint the source of the yield problem in the design

YSH are generated using Post Processing of Monte Carlo Yield analysis data.

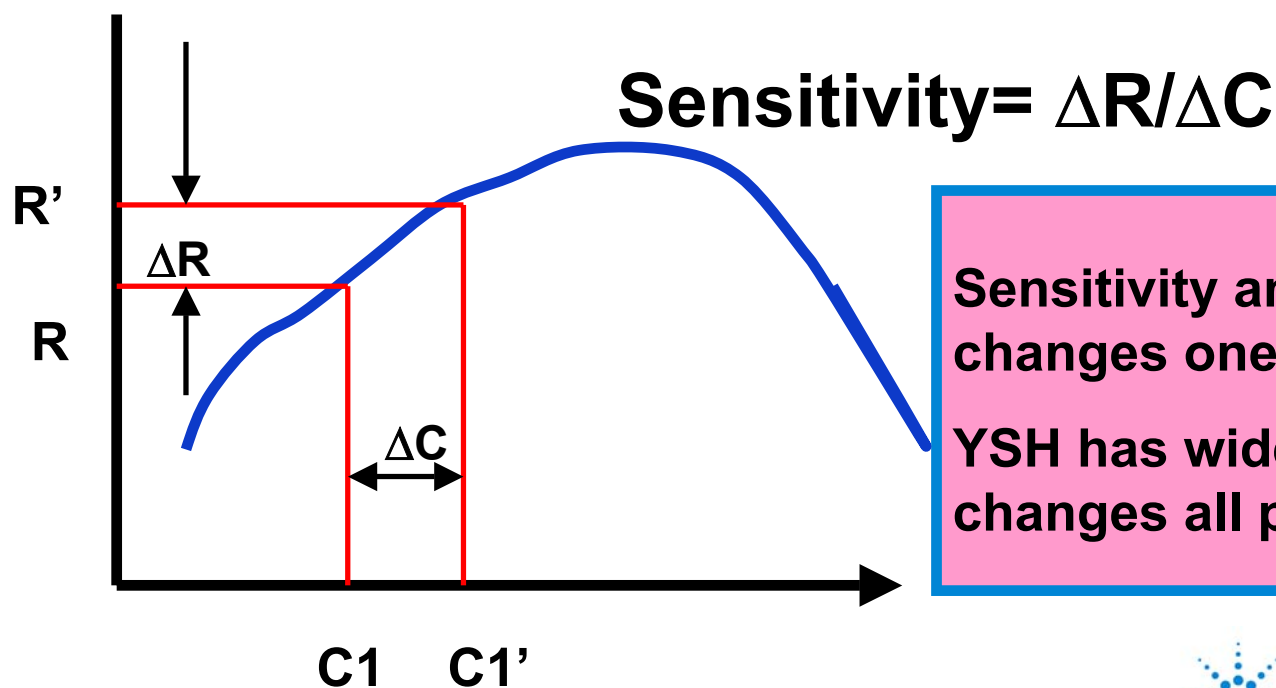


The DFY Process for MMIC



Sensitivity Analysis – How does it work?

- Change the part's nominal value by $1e-6$ and monitor the change in the response (R).
- Example for capacitor, C1 with response R
- Perturb C1 by a small delta: $C1' = C1(1+1e-6)$

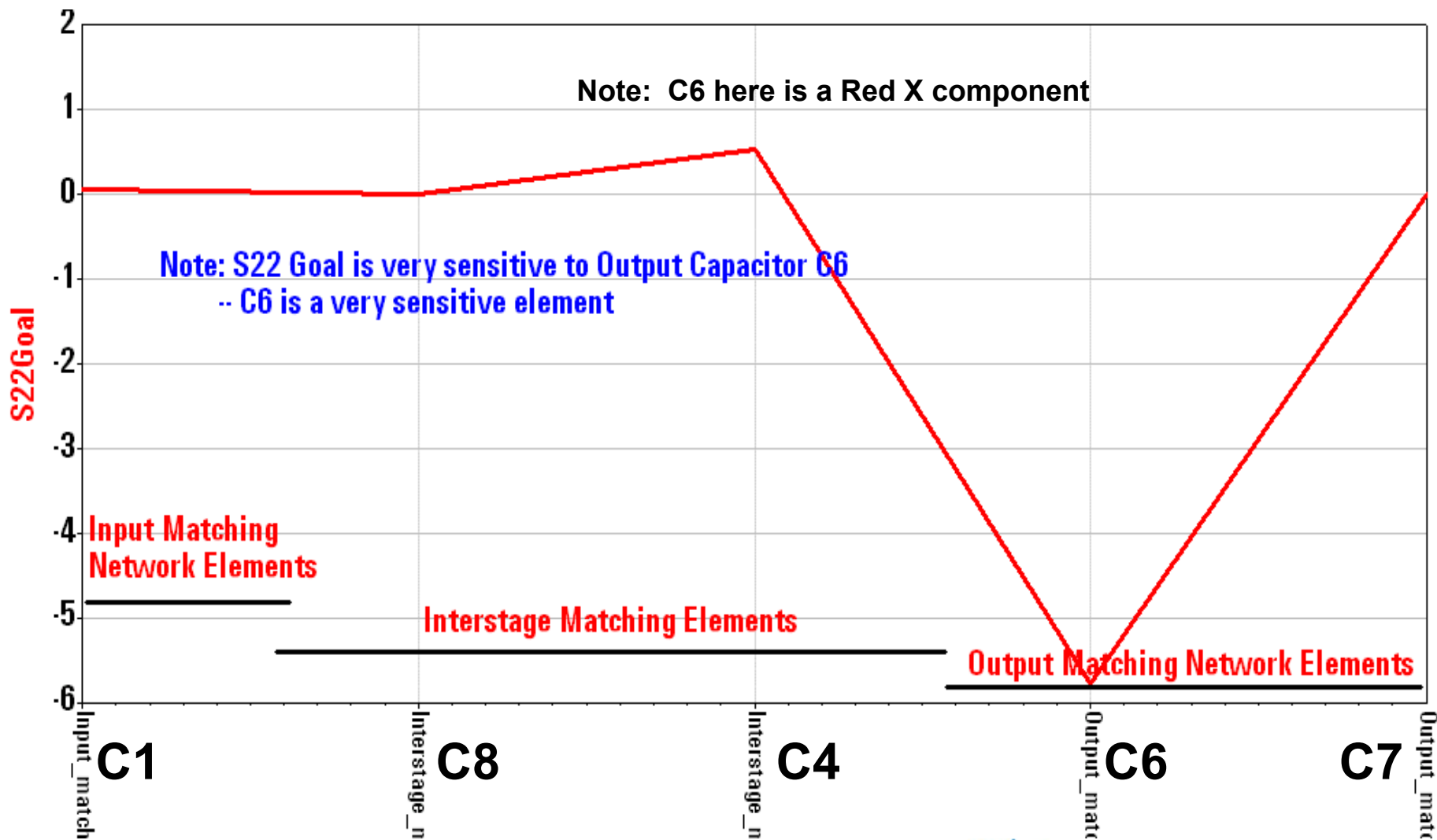


Sensitivity analysis is local. It changes one part at a time.

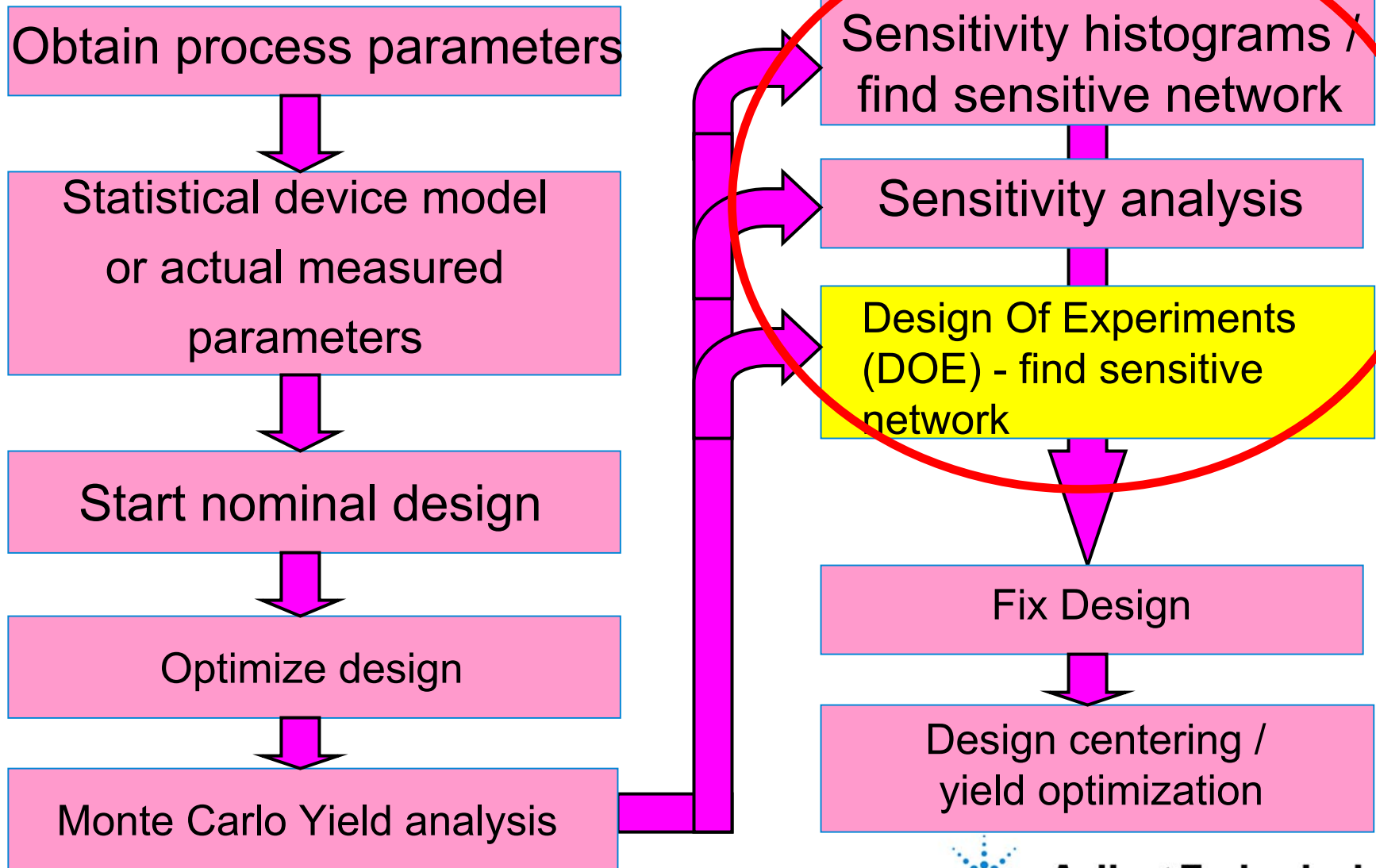
YSH has wider variation and changes all parts together.



Sensitivity of S22 to all Capacitors



The DFY Process for MMIC

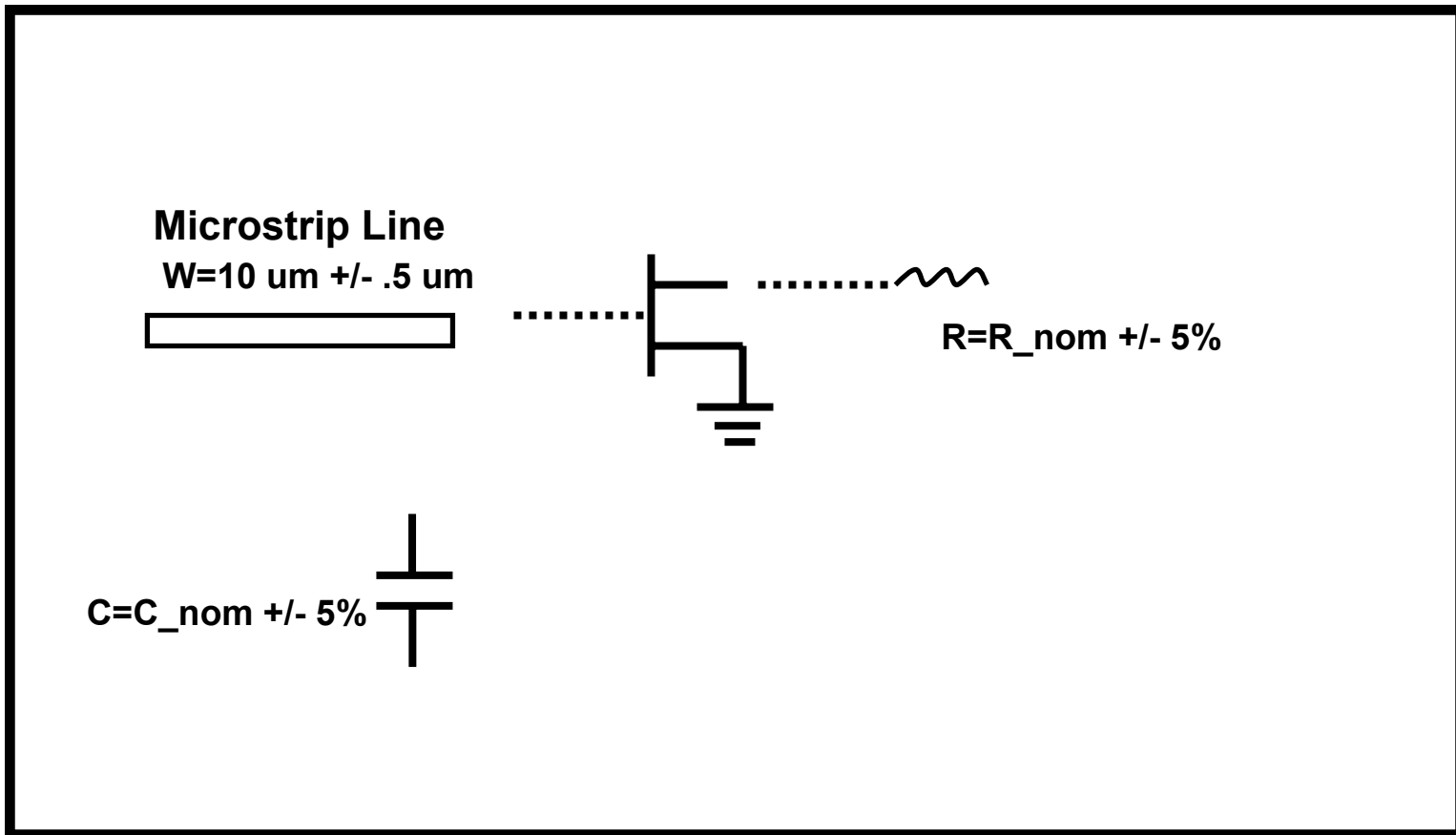




Agilent Technologies

**A Brief Tutorial on
Design of Experiments (DOE)**

DOE – A Brief Tutorial – 3 elements MMIC



DOE – A Brief Tutorial

Start by choosing variables that affect the response

Choose three variables with their +1 and -1 :

Width of lines (W)

$$W = W_{\text{nom}} \pm .5 \text{ um}$$

Resistors (R)

$$R = R_{\text{nom}} \pm 5\%$$

Capacitors (C)

$$C = C_{\text{nom}} \pm 5\%$$

Example: For a 10u wide line, $W = 10 \text{ um}$

-1 corresponds to 9.5 um

+1 corresponds to 10.5 um

0 corresponds to nominal value, 10um



Main Effect of Capacitors, C on Gain

W	R	C	Gain
-1	-1	-1	12.85
1	-1	-1	13.01
-1	1	-1	14.52
1	1	-1	14.71
-1	-1	1	12.93
1	-1	1	13.09
-1	1	1	14.61
1	1	1	14.81

Average gain for C=-1
13.7725 dB (yellow)

Average gain for C=1
13.86 dB (blue)

Slope= .044



Main Effect of Resistors, R on Gain

W	R	C	Gain
-1	-1	-1	12.85
1	-1	-1	13.01
-1	1	-1	14.52
1	1	-1	14.71
-1	-1	1	12.93
1	-1	1	13.09
-1	1	1	14.61
1	1	1	14.81

Average gain for R=-1

12.97 dB (blue)

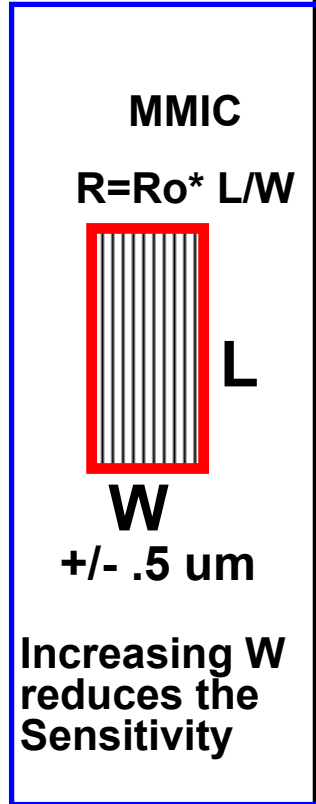
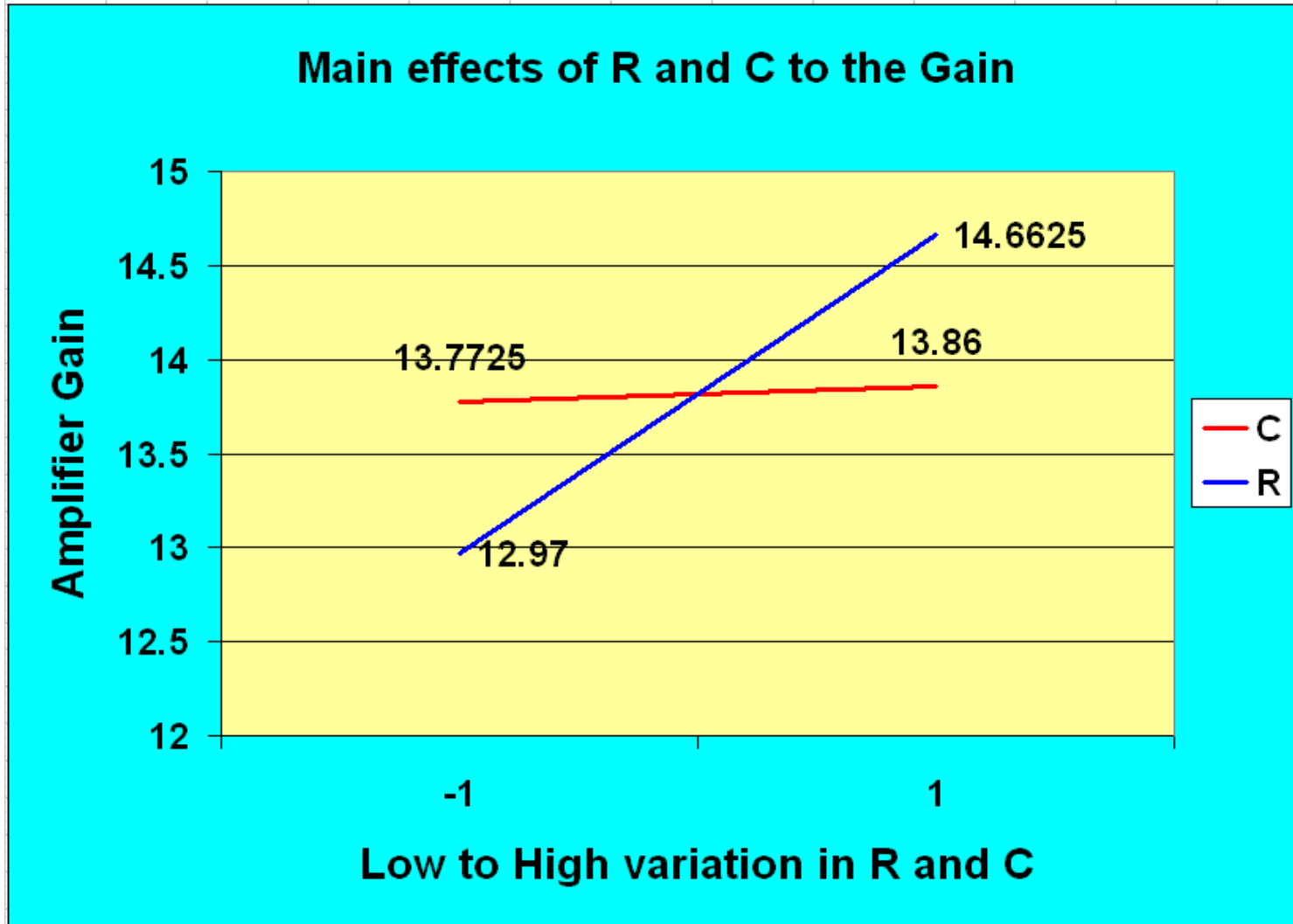
Average gain for R=1

14.6625 dB (green)

Slope = .85



Plotting Main Effects of C and R



Interaction Effect of (W and R) on Gain

W	R	C	Gain
-1	-1	-1	12.85
1	-1	-1	13.01
-1	1	-1	14.52
1	1	-1	14.71
-1	-1	1	12.93
1	-1	1	13.09
-1	1	1	14.61
1	1	1	14.81

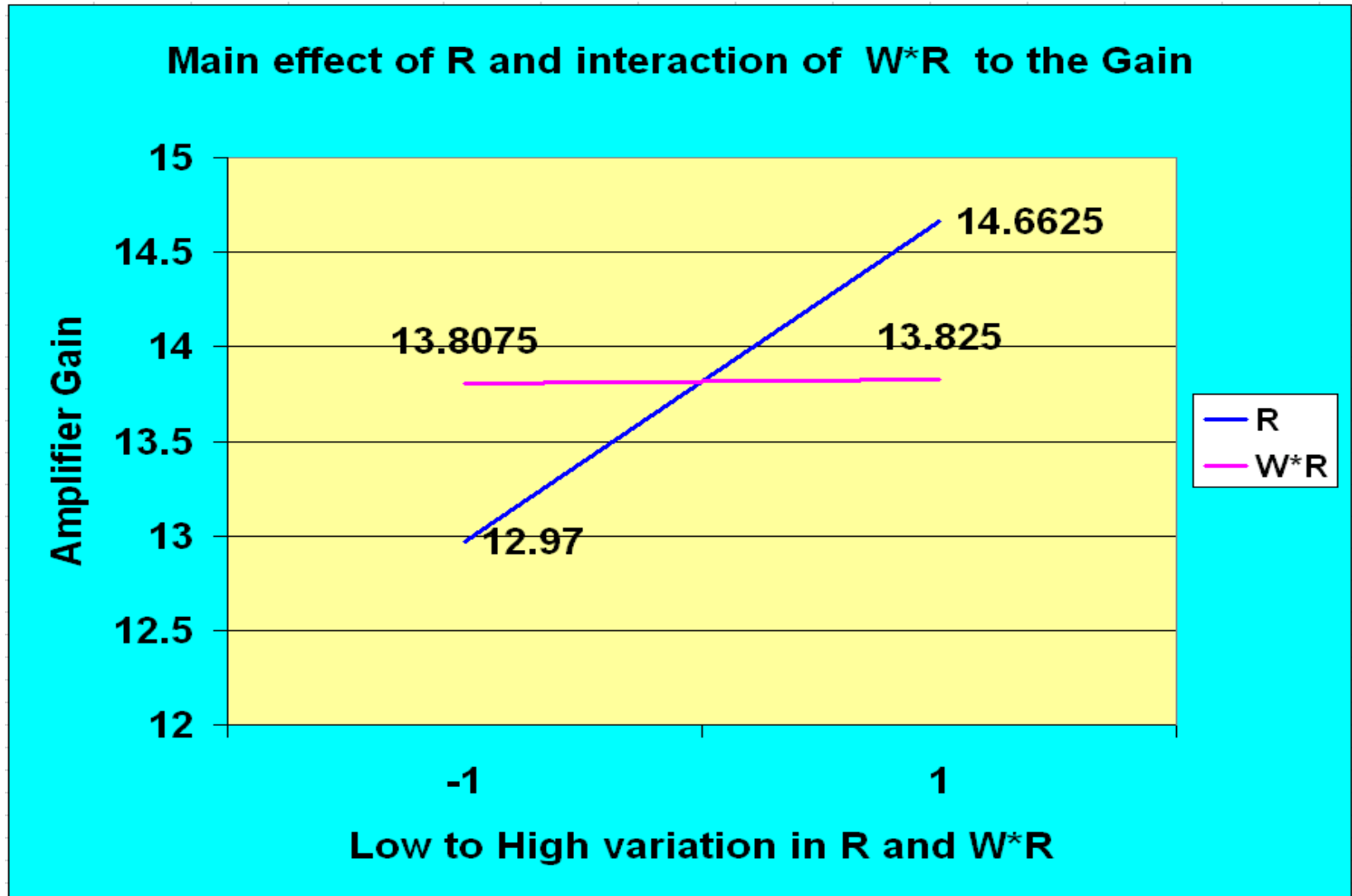
Average gain for $W \cdot R = -1$
13.8075 dB (blue)

Average gain for $W \cdot R = 1$
13.825 dB (pink)

Slope = .0088



Plotting Interaction Effects of W and R



Obtaining the Rest of the Coefficients

<u>Term</u>	<u>Coefficient</u>
Constant (nominal gain)	13.8
W	.09
R	.85
C	.044
W*R	.0088
W*C	.0013
R*C	.0050
W*R*C	0.0025

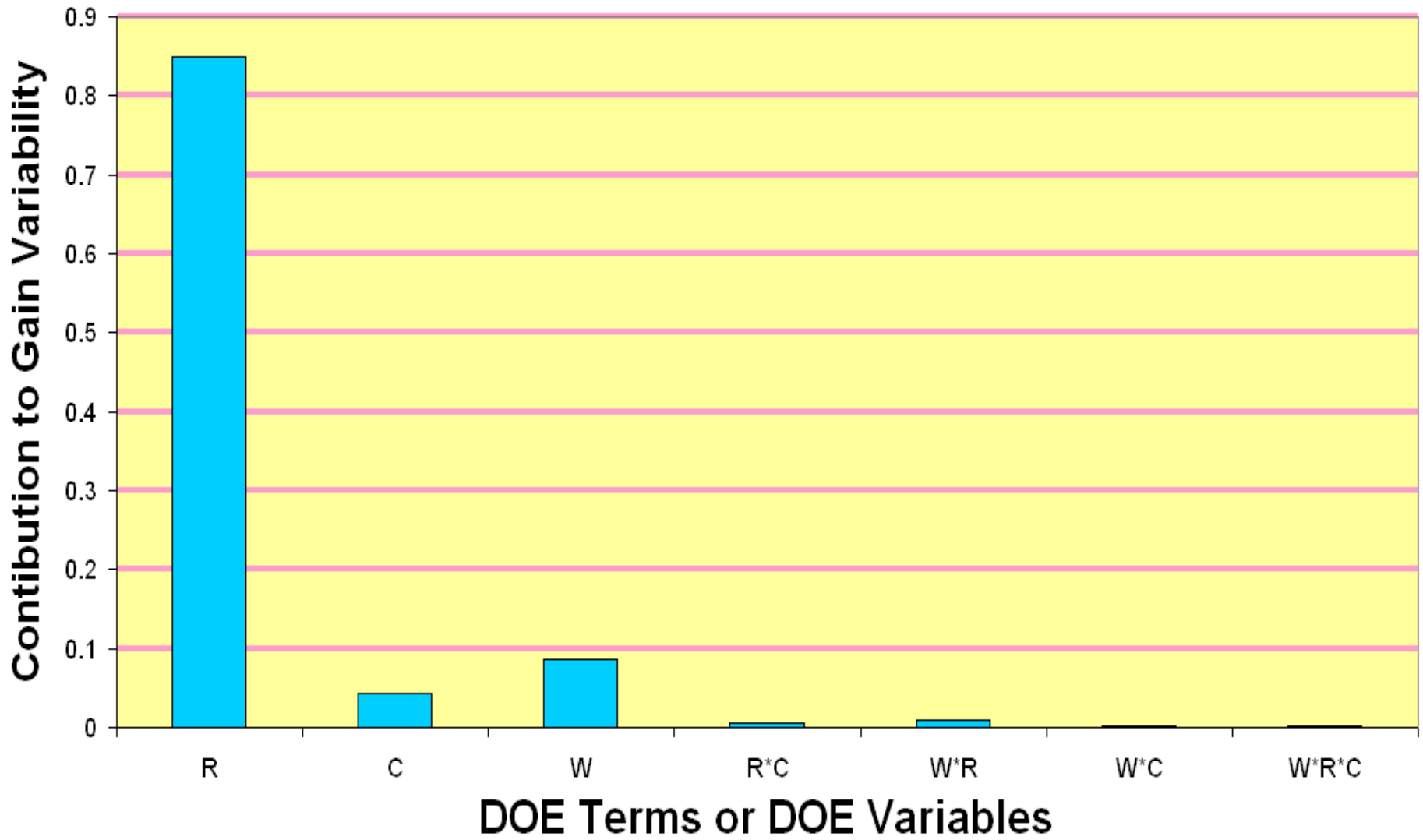
We calculated these three coefficients in the previous slides

Construct a linear equation to represent the experiment results.

$$\text{Gain} = 13.8 + .09W + .85R + .044C + .0088WR + \dots \text{etc.}$$

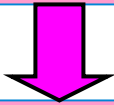


Display All Effects on a Pareto Chart



DFY tools allow designers to find the areas in the design that need to be redesigned

Obtain process parameters



Statistical device model
or actual measured
parameters



Start nominal design



Optimize design



Monte Carlo Yield analysis

DFY Tools

Sensitivity histograms /
find sensitive network

Sensitivity analysis

Design Of Experiments
(DOE) - find sensitive
network

Fix Design

Design centering /
yield optimization



DOE INTERACTIONS



Another DOE Example with 5 variables:

1. Width of lines due to process - +/- .5 microns
2. IMN_C1 (Input Matching Network) C1 +/- 5%
3. IMN_R1 (Input Matching Network) C1 +/- 5%
4. OMN_C1 (Output Matching Network) C1 +/- 5%
5. OMN_R1 (Output Matching Network) R1 +/- 5%



2

- Open the Design file:
- E_LNA_DOE2_on_five_v
ariables

• The five elements we want to run DOE on are:


- IMN_R1 IMN_C1
- Line widths
- OMN_R1 OMN_C1


• Notice the variable x that I have created. As x changes, all line widths will change +/- .5


1

I want to study the sensitivity five elements that could affect the output results: IMN C1 and R1, OMN C1 and R1, and line widths

 VAR
VAR1
w10=10*(1+x)
w15=15*(1+x)
w20=20*(1+x)
w25=25*(1+x)
w30=30*(1+x)

 VAR
VAR5
x=0 {d}

 VAR
VAR2
IMN_C1=.9 {d}
IMN_R1=8 {d}

 VAR
VAR3
OMN_C1=.26 {d}
OMN_R1=20 {d}

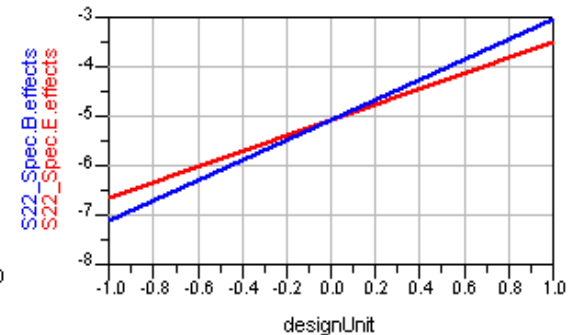
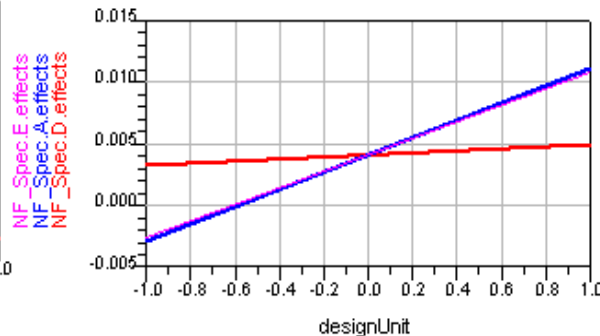
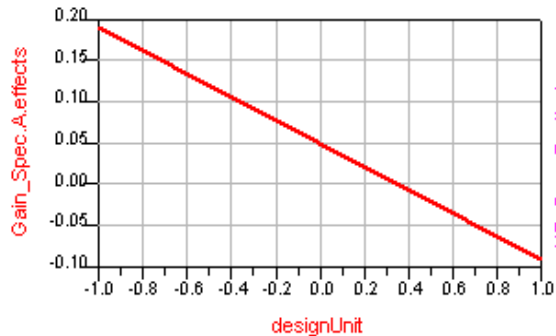
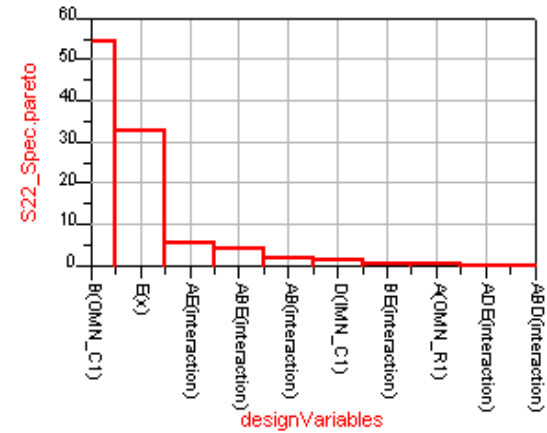
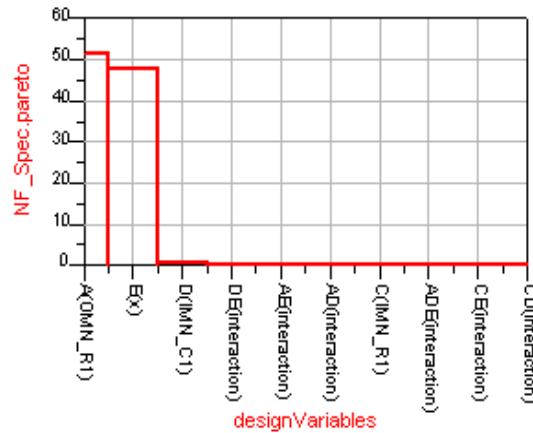
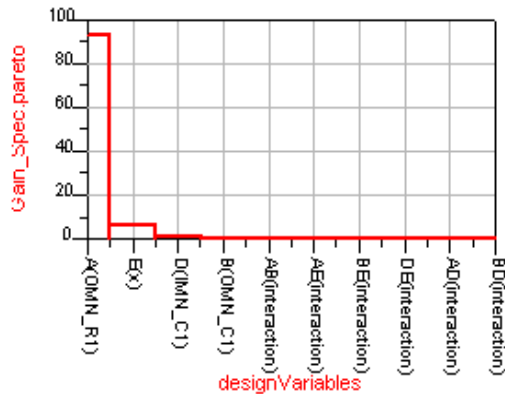
DOE Analysis

on 5 variables: line widths +/- .5 u
IMN_C1 and R1, OMN_R1 and C1 +/- 5%



DFY - DOE

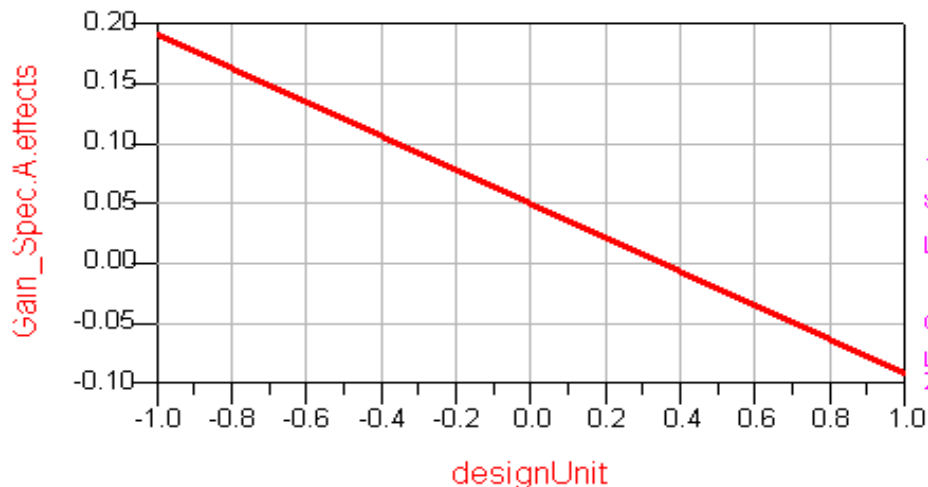
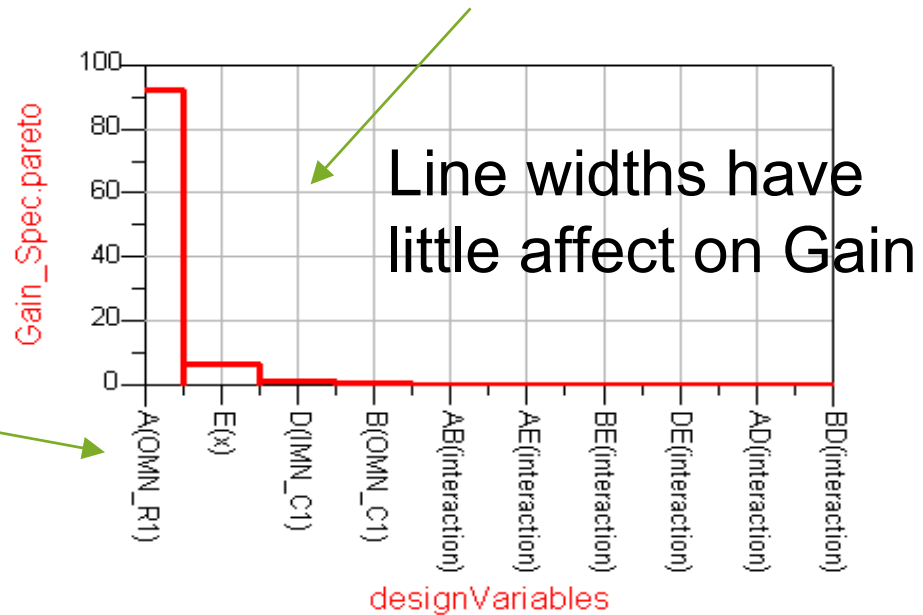
When the simulation is done, this data Display will pop automatically



DFY - DOE

Gain is mostly affected by OMN_R1

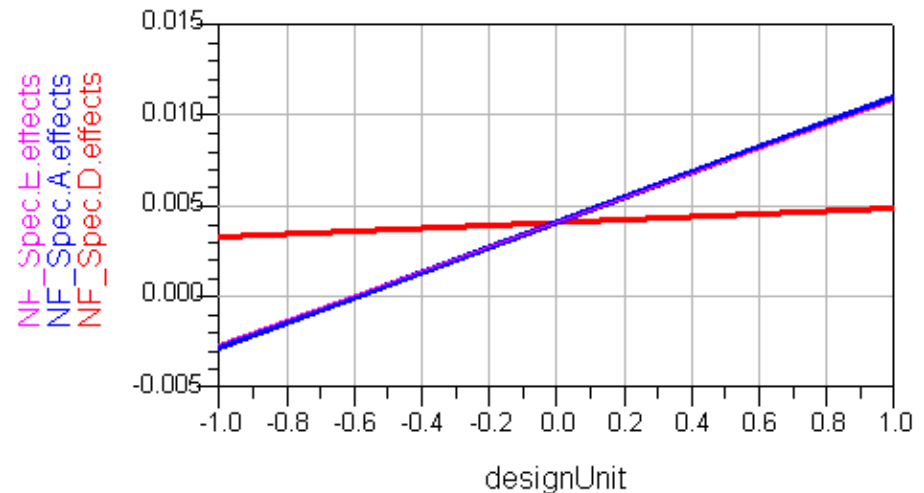
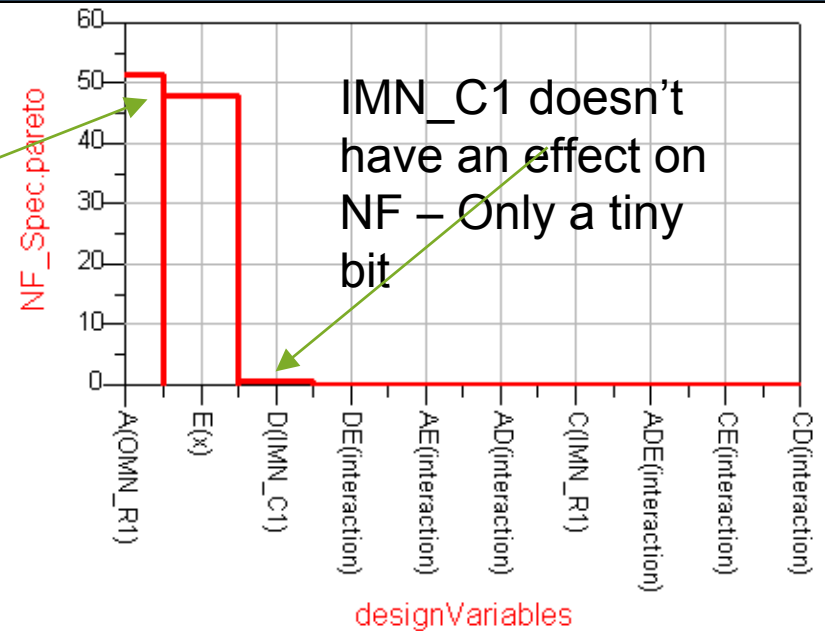
Increase OMN_R1 by 5% reduces the gain by .14 dB
Decrease OMN_R1 by 5% increases the gain by .14 dB



DFY - DOE

NF is affected by OMN_R1 and line widths (especially of the IMN)

Effect of OMN_R1 and Line widths on NF are correlated – they both have the same slope



DFY - DOE

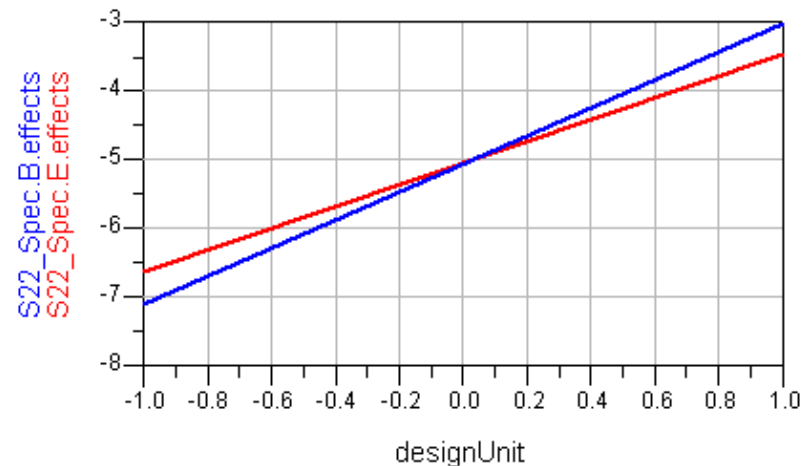
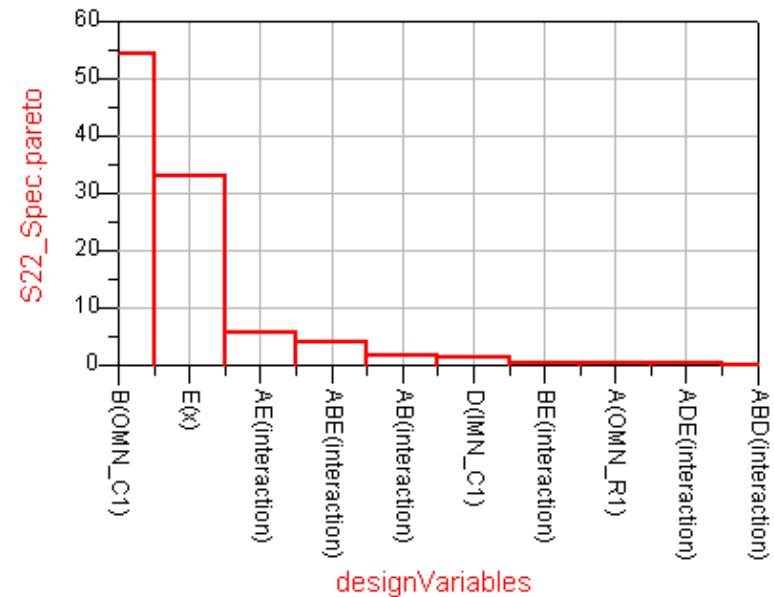
S22 is affected mostly by OMN_C1 and Line widths:

C1 adds 2 dB to S22

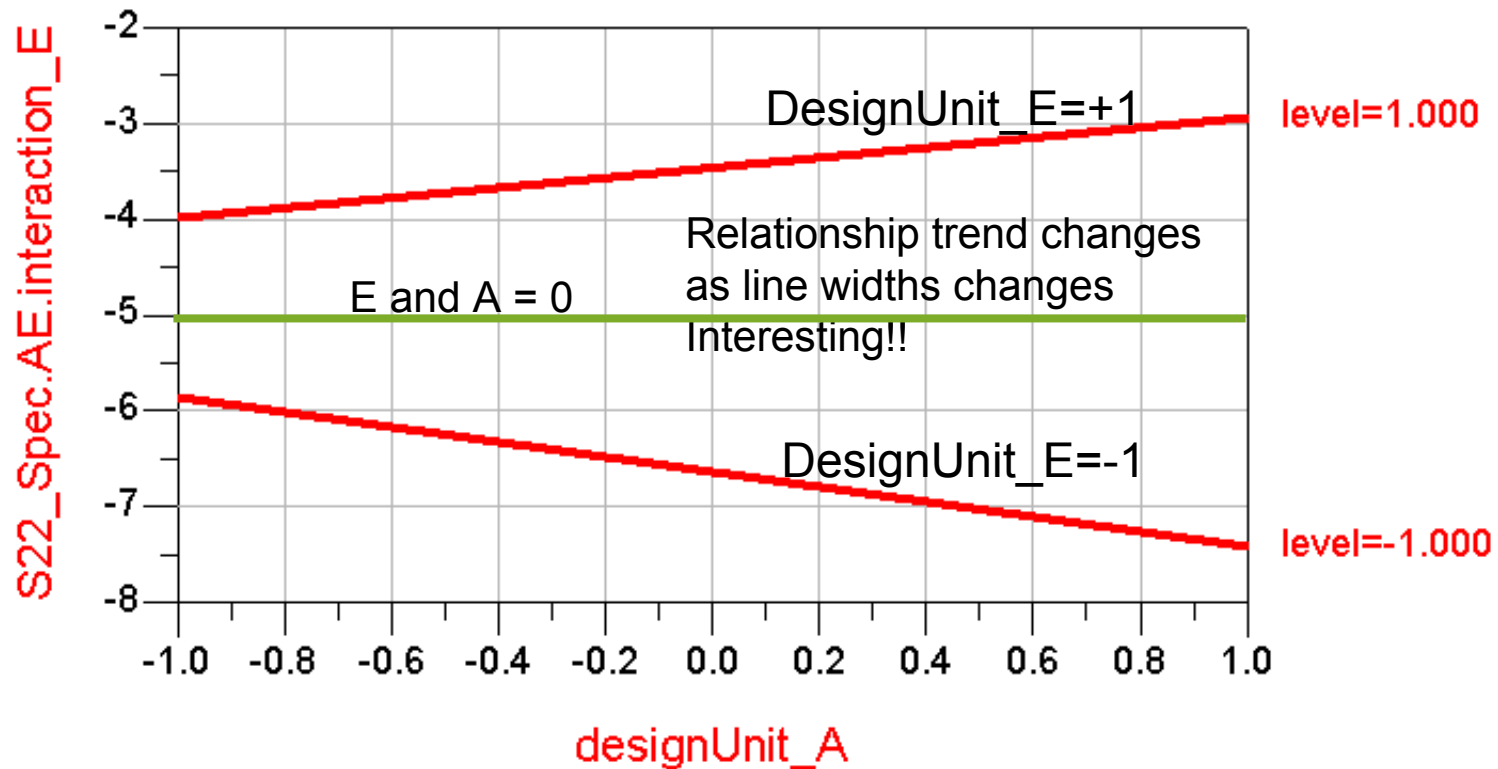
Line widths add 1.5 dB to S22

There is an interaction effects between OMN_R1 and Line widths

See next page



Interaction effects between OMN_R1 and Line widths to S22

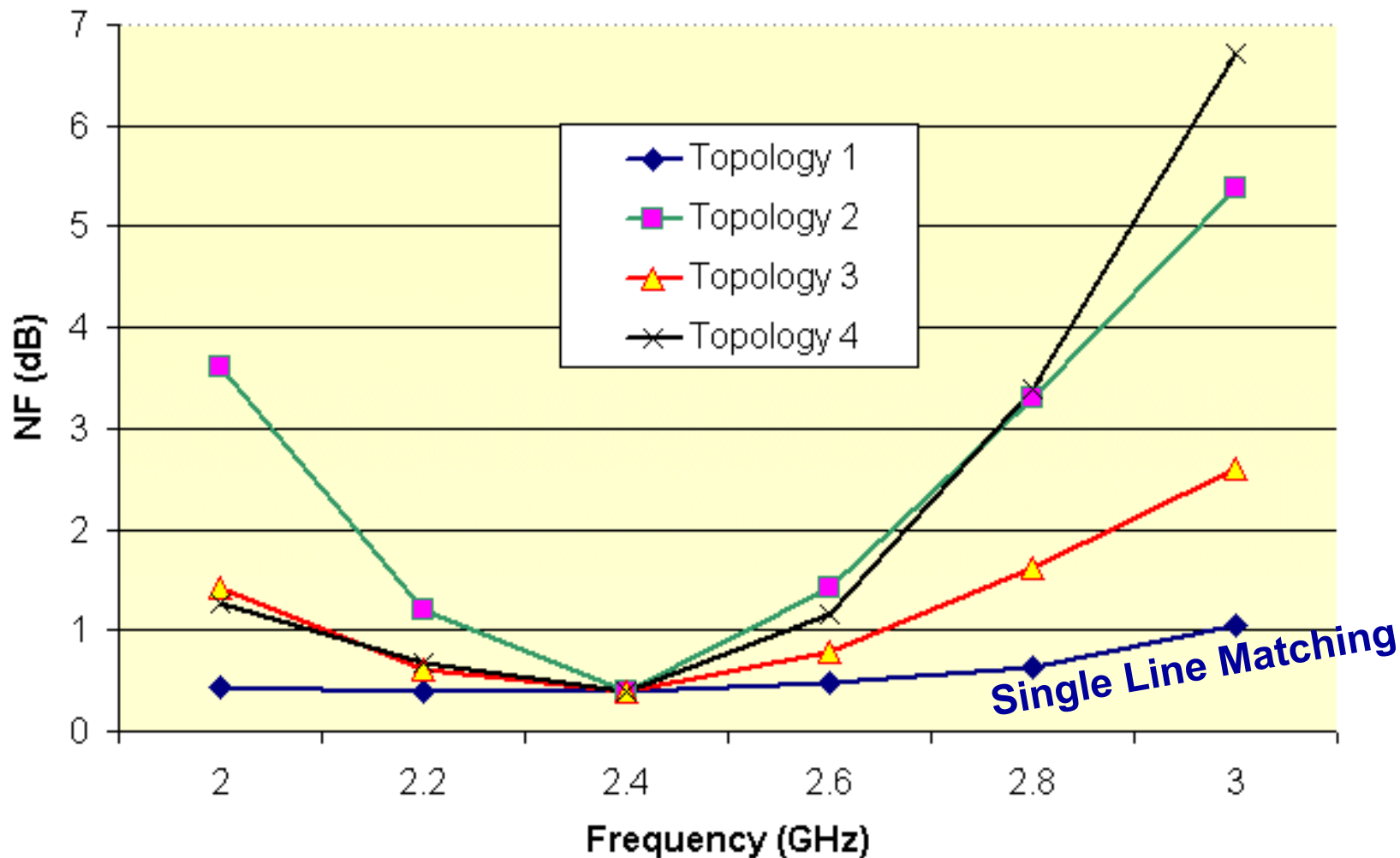


- If OMN_R1 is high and Line Widths is High, S22 gets worse by 2 dB
- If OMN_R1 is high and Line Widths is Low, S22 gets better by 2.3 dB
- If OMN_R1 is low and Line Widths is High, S22 gets worse by 1 dB
- If OMN_R1 is low and Line Widths is Low, S22 gets better by .8 dB



NF Simulation of the Various Matching networks

LNA Noise Figure for Four Different Noise Matching Networks



Re-Cap

- **Different Topologies produce different yield**
- **Selecting low Q topologies is a must.**
- **YSH help you find where the problem is coming from.**
- **DOE analysis help you find the sensitive high-Q matching networks and interactions between them**



Matching Utility Tool in ADS



ADS Matching Tool

The screenshot displays the ADS Matching Tool interface. The main window title is "[Test_Match_tool_prj] Matching_tool_study2 * (Schematic):3". The menu bar includes File, Edit, Select, View, Insert, Options, Tools, Layout, Simulate, Window, DynamicLink, Grids, Local, Power_Sim, DesignGuide, and Help. The Tools menu is open, showing options such as Electronic Notebook..., Custom Library, Digital Filter, Encode Designs..., IC-CAP Import, LineCalc, Smith Chart..., **Impedance Matching...**, Model Composer, Netlist Export, Spice Model Generator, User-Compiled Model, Check Representation..., Hierarchy..., Info..., Identify..., Component Palette Configuration..., Hot Key/Toolbar Configuration..., Data File Tool..., Connection Manager Client..., Export ADS Ptolemy Design, and Instrument Server... A mouse cursor is pointing at the "Impedance Matching..." option.

The schematic diagram shows a circuit with the following components and connections:

- Term1**: A 50 Ohm resistor connected to ground, labeled "Term1 Num=1 Z=50 Ohm".
- stage1_stability X1**: A component connected to the input of the matching network.
- DA_LCBandpassMatch2**: A matching network component, labeled "DA_LCBandpassMatch2 Matching_tool_study2".
- Term2**: A 50 Ohm resistor connected to ground, labeled "Term2 Num=2 Z=50 Ohm".
- S-PARAMETERS**: A component with the following properties:
 - S_Param
 - SP1
 - Start=3.0 GHz
 - Stop=4.0 GHz
 - Step=.1 GHz
- GCS B2P2 Include**: A component with the following properties:
 - GCS_B2P2_Include
 - Include
 - Model=VBIC
 - HBT_TEMP=25

The schematic also shows several reflection coefficient plots (MTCH) and a component labeled "SmGamma1".



ADS Matching Tool

The screenshot displays the ADS Matching Tool interface. The main window is titled "Impedance Matching Utility" and contains a menu bar (File, Tools, View, Help) and a toolbar with various icons. The "Current Schematic" is set to "[Test_Match_tool_prj]: 3" and the "SmartComponent" is "DA_LCBandpassMatch1". The "Current Design" is "Matching_tool_study2" and the "SmartComponent Capability" is "Design, Simulate, Yield, Display".

The "Overview" tab is selected, showing the "Match DesignGuide: SmartComponent Overview" with the following steps:

1. Place a SmartComponent from the "Match DG" palette (accessible from DesignGuide toolbar or menu).
2. Design SmartComponent from the "Match Assistant" or "Matching Assistant" tab.
3. Set SmartComponent simulation frequencies from the "Simulation Assistant" tab. The "Automatically Display Results" option controls automatic launching of display following simulation. The "Automatically Set Frequencies" button sets simulation frequencies based on design specifications.
4. Simulate SmartComponent from the "Simulation Assistant" tab.
5. Network sensitivity to component tolerance can be assessed using the "Yield Assistant" tab. The "Yield Assistant" can also optimize your network for maximum yield.
6. If, during any simulation, you chose not to "Automatically Display Results," you may open the display from the "Display Assistant" tab.

On the right side of the interface, a circuit diagram is shown with a resistor and a voltage source. The resistor is labeled "matching_tool_study2". The voltage source is labeled "Te Nu Z=:". A blue box highlights the text "G C S B2P2 Include" and "B2P2_Include". Below the circuit diagram, there is a note: "chstone SPAR s process was taken" and "g iconplace at we can find a matching topology".



ADS Matching Tool

The screenshot displays the ADS Matching Tool interface. The main window is titled "[MATCH_TOOL_PRJ] DA_LCBandpassMatch1_Matching_tool_study2 *(Schematic):18". The menu bar includes File, Edit, Select, View, Insert, Options, Tools, Layout, Simulate, Window, DynamicLink, Grids, Local, Power_Sim, DesignGuide, and Help.

The **Impedance Matching Utility:18** dialog box is open, showing the following details:

- of 19 networks
- Maximum Passband Error: 0.04360 dB
- Component List:
 - Input Port
 - SLC SE L=4.954724 nH C=405.877042 fF
 - CAP PG C=3.022624 pF
 - IND SE L=520.451335 pH
 - IND PG L=152.115737 pH
 - IND SE L=120.604893 pH
 - Output Port
- Buttons: Select, Optimize, Optimize All

19 matching networks choices



ADS Matching Tool

Impedance Matching Utility

File Tools View Help

Current Schematic: [Test_Match_tool_prj]: 3 SmartComponent: DA_LCBandpassMatch1

Current Design: Matching_tool_study2 SmartComponent Capability: Design, Simulate, Yield, Display

Overview | Matching Assistant | Simulation Assistant | Yield Assistant | Display Assistant

Automated SmartComponent Simulation

Simulation Frequency Sweep

Start: 3 GHz Automatically Display Results

Stop: 4 GHz Automatically Set Frequencies

Step: .1 GHz

Num. of Points: 11

Simulate Create Template Update From Template Help

Helps

"Simulate" automatically simulates selected SmartComponent

"Create Template" creates a simulation template for manual SmartComponent simulation

"Update From Template" closes the manual template and updates SmartComponent parameters

Step 1: Sir
In D
file
and
Step 2: Go
Step 3: Lib
Step 4: Pla
Step 5: Use
Step 6: Fi
Step 7: Cli
Step 8: Th

Term
Term2
Num=2
Z=50 Ohm

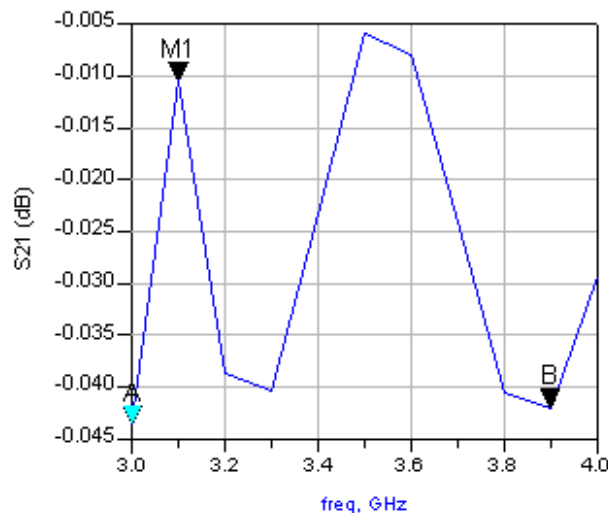
hing topology



ADS Matching Tool

Bandpass Matching Network
Display Assistant
Impedance Matching Utility

Need Help? Please see the Utility User Manual
for complete instructions on using this Display Assistant.



Input Parameters

Fp1 (GHz)	Fp2 (GHz)	Gain Change
3.000	4.000	0.000

Performance

Gain at Fp1	Gain at Fp2	Max PB Gain	Min PB Gain
-0.044	-0.029	-0.006	-0.044

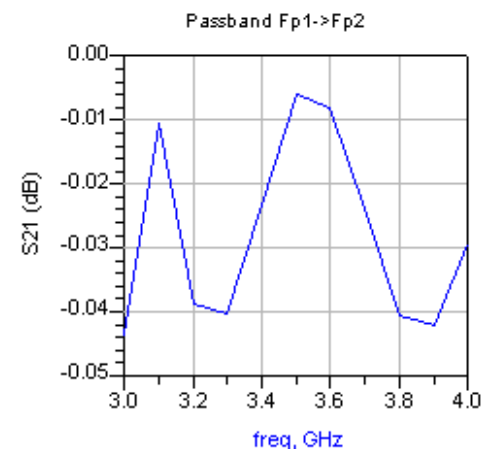
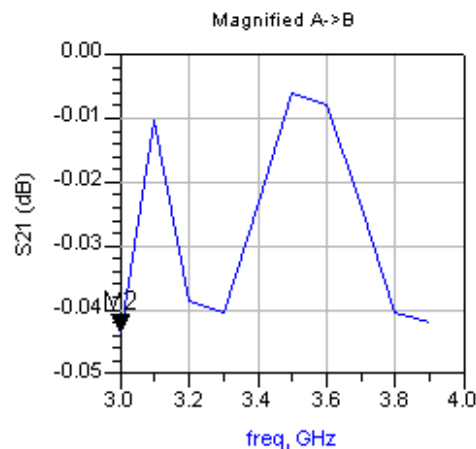
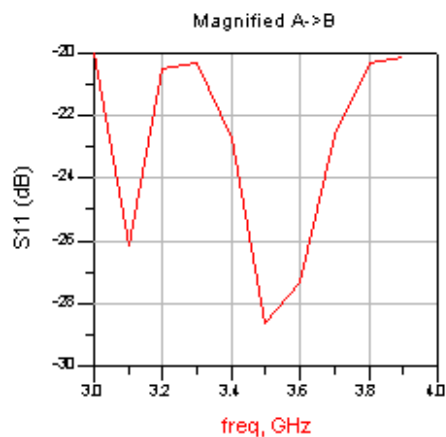
Marker M1

F (GHz)	S11 (dB)	S11 ^2	S21 (dB)
3.10	-26.18	0.00	-0.01

Marker M2

F (GHz)	S11 (dB)	S11 ^2	S21 (dB)
3.00	-20.01	0.01	-0.04

PB: Passband
Fp1: Lower Passband Edge
Fp2: Upper Passband Edge



ADS Matching Tool (Set Yield Specs and Tolerances)

Impedance Matching Utility

File Tools View Help

Current Schematic: [MATCH_TOOL_PRJ]: 18
SmartComponent: DA_LCbandpassMatch1

Current Design: Matching_tool_study2
SmartComponent Capability: Design, Simulate, Yield, Display

Overview | Matching Assistant | Simulation Assistant | **Yield Assistant** | Display Assistant

Automated SmartComponent Yield Simulation

Yield Frequency Sweep

Start: 3 GHz
Stop: 4 GHz
Step: 10 MHz
Num. of Points: 101

Statistical Components

L1
C1
C2
L2
L3

View Components

Simulations: 250 # Iterations: 10

Automatically Set Frequencies | Set Yield Spec/Goals

Automatically Display Results Yield Optimization

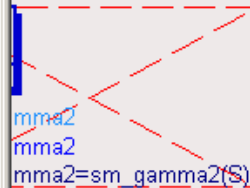
Simulate

Helps
"Simulate" or "Optimize"
"Create Template"
"Close Template"

Statistical Component Values

Component	Stat Nominal Value	Statistics	Opt Nominal Value	Optimization
L1	4.95 nH	stat{ uniform +/- 5 % }	4.95 nH	none
C1	405.88 fF	stat{ uniform +/- 5 % }	405.88 fF	none
C2	3.02 pF	stat{ uniform +/- 5 % }	3.02 pF	none
L2	520.45 pH	stat{ uniform +/- 5 % }	520.45 pH	none
L3	152.12 pH	stat{ uniform +/- 5 % }	152.12 pH	none
L4	120.6 pH	stat{ uniform +/- 5 % }	120.6 pH	none

View Statistical Components | Modify Statistics/Optimization | Close



2_Matching_tool_study2
2

ADS Matching Tool

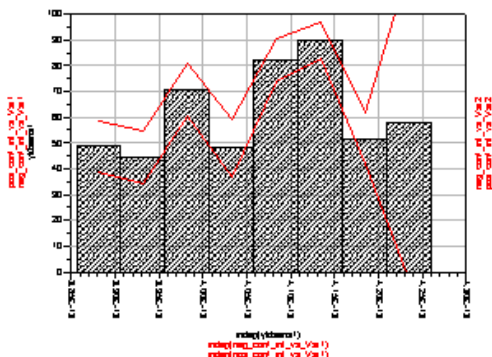


sMatch1 Matching tool study2

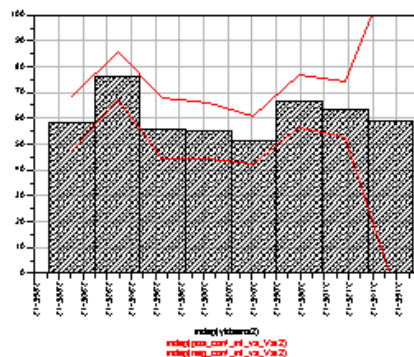
YIELD SENSITIVITY HISTOGRAMS Display Assistant DesignGuides

Need Help? Please see the appropriate DesignGuide User Manual for complete instructions on using this Display Assistant. The Display Assistant Chapter provides general-use instructions, and specifics for this Display Assistant are found in the component documentation.

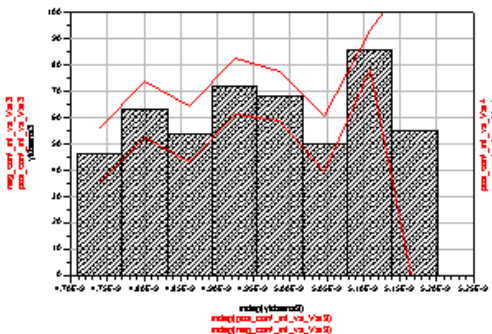
Eqn Var1=C1.C



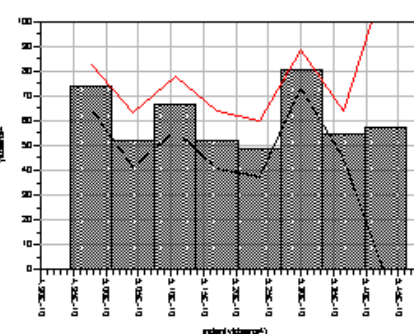
Eqn Var2=C2.C



Eqn Var3=L1.L



Eqn Var4=L2.L



Note: Type in C1 as "C1.C", L1 as "L1.L". Do the same for all component names. Must be a statistical component.

Set Goal/Spec Parameters

Eqn Sparm1=GT21 Eqn Spec1=.2 dB

Eqn LessThan1=0 Eqn F1=3 GHz

Type in the spec frequency with associated losses and spec S parameter

Example:
Sparm1=S21, LessThan1=0, Spec1=3 dB, F1=1 GHz
will set pass/fail as units of S21 greater than 3 dB loss at 1 GHz.

Note:
The filter simulation uses a data file please use GT instead of S (i.e. GT21 rather than S21)

Yield Results

Overall_Yield

22.8

Overall_Yield includes all specs from the yields in violation

Yield at F1

61

Yield_at_F1 includes only the above setspec

Between the red lines is the 80% confidence interval for the histogram.



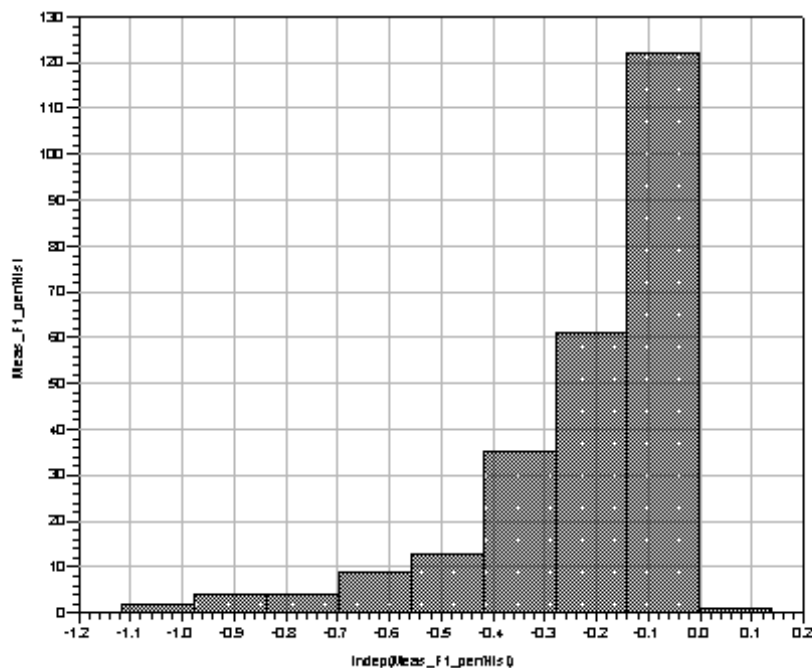
ADS Matching Tool

MEASUREMENT HISTOGRAMS Display Assistant DesignGuides

Need Help? Please see the appropriate DesignGuide User Manual for complete instructions on using this Display Assistant. The Display Assistant Chapter provides general-use instructions, and specifics for this Display Assistant are found in the component documentation.

Number of Occurrences versus Measurement Value

F1



Settable Parameters

Please use the Yield Sensitivity Histogram page in order to set desired frequency as well as associated loss and S parameter.

Yield Results

NumPass	57
NumFail	193
Yield	23

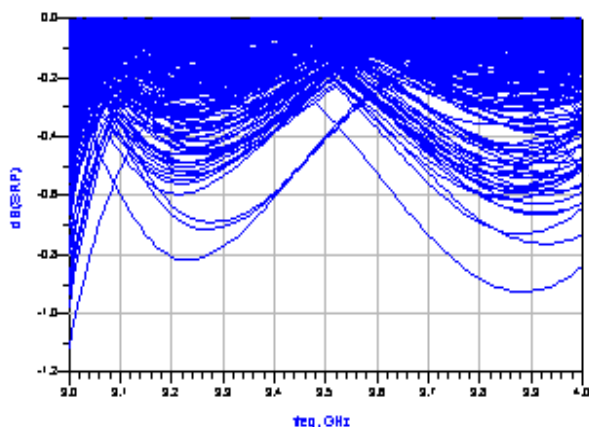


ADS Matching Tool

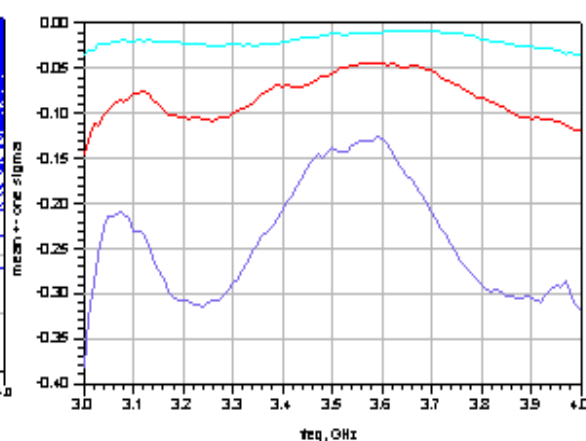
STATISTICAL RESPONSE PLOTS Display Assistant DesignGuides

Need Help? Please see the appropriate DesignGuide User Manual for complete instructions on using this Display Assistant. The Display Assistant Chapter provides general-use instructions, and specifics for this Display Assistant are found in the component documentation.

dB(SRP) vs Frequency



dB(SRP) Statistical Response Plot



In this Statistical Response plot, the center line is the average of the measurements, the top and bottom lines are, respectively, the average measurement plus and minus, one measurement standard deviation.

Settable Parameters

Please use Yield Sensitivity Histogram page to set desired frequency with associated loss.

$$\text{Eqn SRP} = \text{GT21}$$

Type in the desired frequency response

Note:
If either termination uses a data file please use GT instead of S (i.e. GT21 rather than S21)

Yield Results

freq	mean_SRP	...RP + Sd_SRP	...SRP - Sd_SRP
3.0 GHz	-0.2	-4.0E-3	-0.4
3.0 GHz	-0.2	-2.4E-3	-0.4
3.0 GHz	-0.2	-2.9E-3	-0.3
3.0 GHz	-0.1	-4.6E-3	-0.3
3.0 GHz	-0.1	-6.8E-3	-0.3
3.0 GHz	-0.1	-8.8E-3	-0.2
3.1 GHz	-0.1	-9.9E-3	-0.2
3.1 GHz	-0.1	-1.0E-2	-0.2



ADS Matching Tool

[MATCH_TOOL_PRJ] DA_LCBandpassMatch1_Matching_tool_study2 * (Schematic):18

File Edit Select View Insert Options Tools Layout Simulate Window DynamicLink Grids Local Power_Sim DesignGuide Help

Impedance Matching Utility:18

of 19 networks

Maximum Passband Error
0.03939 dB

Component List

Input Port
SLC SE L=4.980118 nH C=412.694336 fF
PLC PG L=1.306138 nH C=3.066402 pF
IND SE L=1.081204 nH
IND PG L=312.019986 pH

Output Port

Select Optimize Optimize All

LINE	STEP
LIBRARY	ADS
TEE	TEE
TAPER	

Design Assistant appropriate DesignGuide User Manual

VAR1
Parameters="3 GHz#4 GHz#0 dB#50#50 Ohm#1 nH#1 pF#(50+*50) Ohm#ZSource.s1p#S(1,1)#0#9#50 Ohm#1 nH#1 pF#(100+*100) Ohm#"

L1 L=4.980118 nH R=1e-12 Ohm
C1 C=412.694336 fF

L2 L=1.306138 nH R=1e-12 Ohm
C2 C=3.066402 pF

L3 L=1.081204 nH R=1e-12 Ohm

L4 L=312.019986 pH R=1e-12 Ohm

Port P1 Num=1

Port P2 Num=2

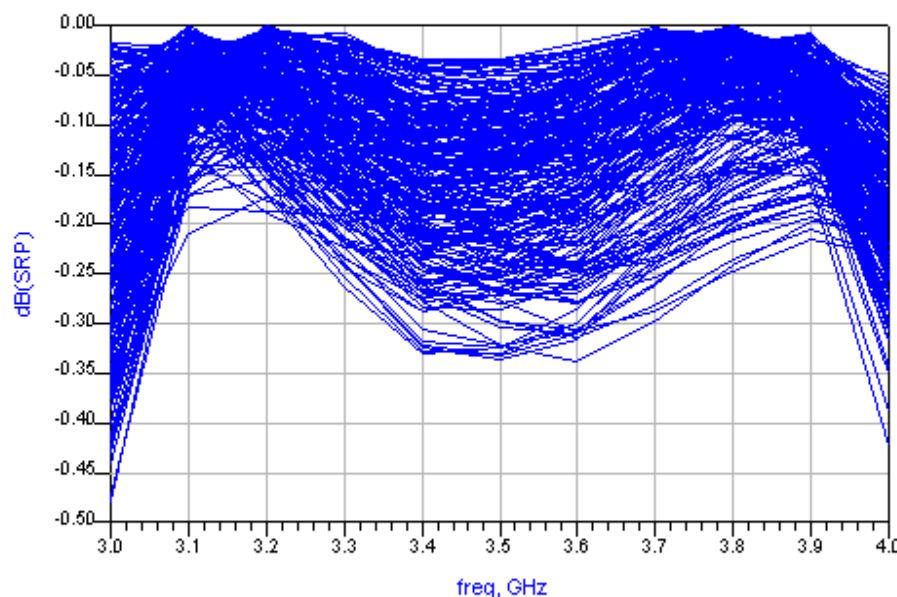


ADS Matching Tool

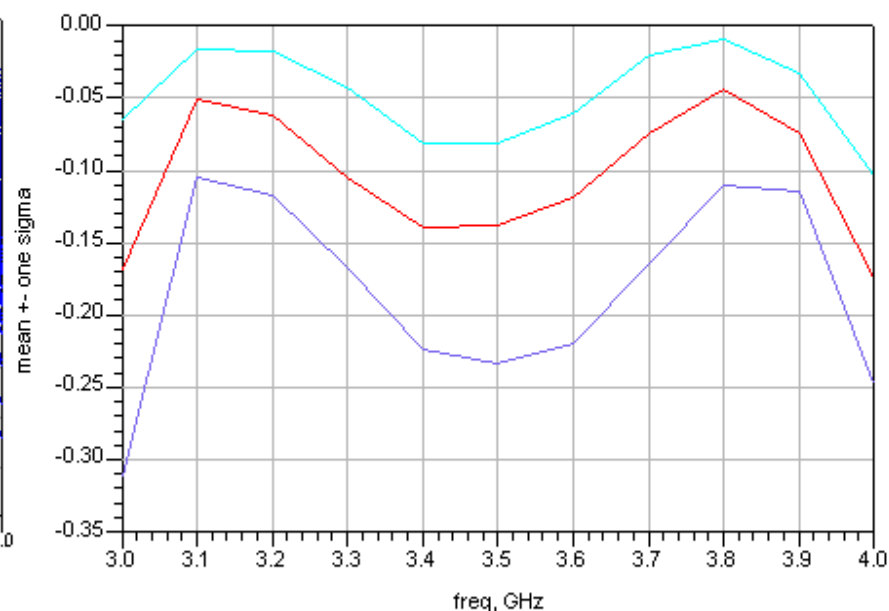
STATISTICAL RESPONSE PLOTS
Display Assistant
DesignGuides

Need Help? Please see the appropriate DesignGuide for complete instructions on using this Display Assistant Chapter provides general-use instructions for this Display Assistant are found in the compar

dB(SRP) vs Frequency



dB(SRP) Statistical Response Plot



In this Statistical Response plot, the center line is the average of the measurements, the top and bottom lines are, respectively, the average measurement plus and minus one measurement standard deviation.



ADS Matching Tool – Transform to Microstrip lines

The image displays the ADS Matching Tool interface, showing a schematic diagram and the Transformation Assistant dialog box.

Impedance Matching Utility

File Tools View Help

Current Schematic: [Test_Match_tool_prj]: 2
SmartComponent: DA_LCbandpassMatch1

Current Design: Matching_tool_study3
SmartComponent Capability: Design, Simulate, Yield, Disp

Transformation Assistant:2

Transformations:

- LC to TLine
- TLine to TLine (Kuroda)
- LC, TLine to Microstrip

Component Selection

Left-click component type to transform.

Microstrip Substrate:

h = 100 μm
Er = 12.9

Unit Element (45 deg)
Zo = 50 Ohm

Buttons: Transform, Undo, OK, Cancel, Help

Helps: Topologies shown in grey are not available for transformation

Schematic Diagram:

Lossless Bandpass Match Design Assistant
Need Help? Please see the appropriate DesignGuide User Manual

VAR1
Parameters: $f_c = 13.6 \text{ GHz}$, $C = 1.647913 \text{ pF}$, $L = 15337.431 \text{ nH}$, $L = 3624.031 \text{ nH}$, $C = 6.62396 \text{ pF}$

MSb.
MSUB
MSub1
N = 100 μm
Er = 12.9
MLN
TL1
Subst = "MSub1"
W = 57.941 μm
L = 15337.431 μm
MLSC
TL2
Subst = "MSub1"
W = 156.319 μm
L = 3624.031 μm
C1
C = 1.647913 pF
C2
C = 6.62396 pF

The DFY Process for MMIC

Obtain process parameters



Statistical device model
or actual measured
parameters



Start nominal design



Optimize design



Monte Carlo Yield analysis

DFY Tools

Sensitivity histograms /
find sensitive network



Sensitivity analysis



Design Of Experiments
(DOE) - find sensitive
network



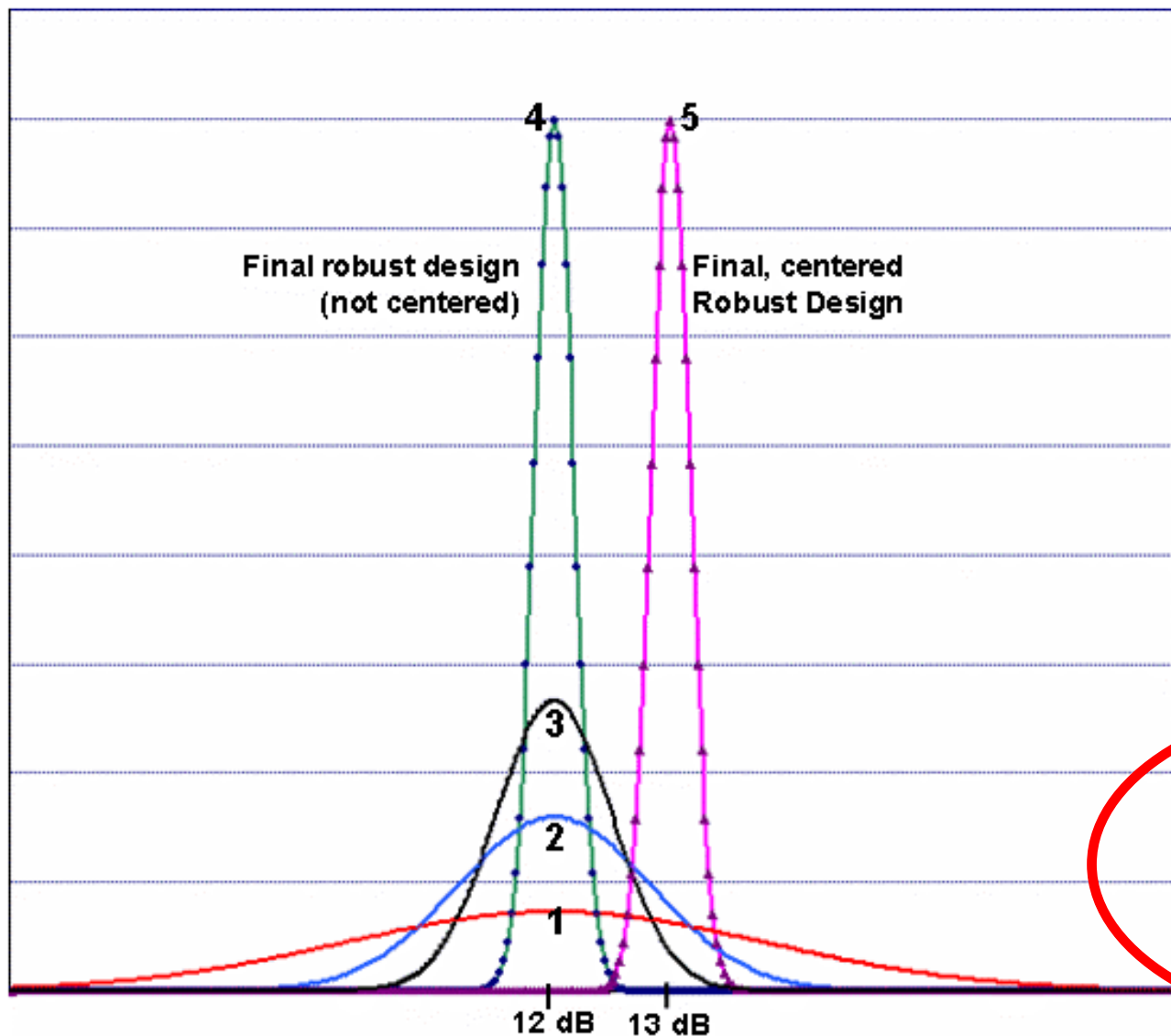
Fix Design



Design centering /
yield optimization



The DFY Process



Curve 1
Original Design

Curves 2,3
Fixing the Design to achieve Robustness

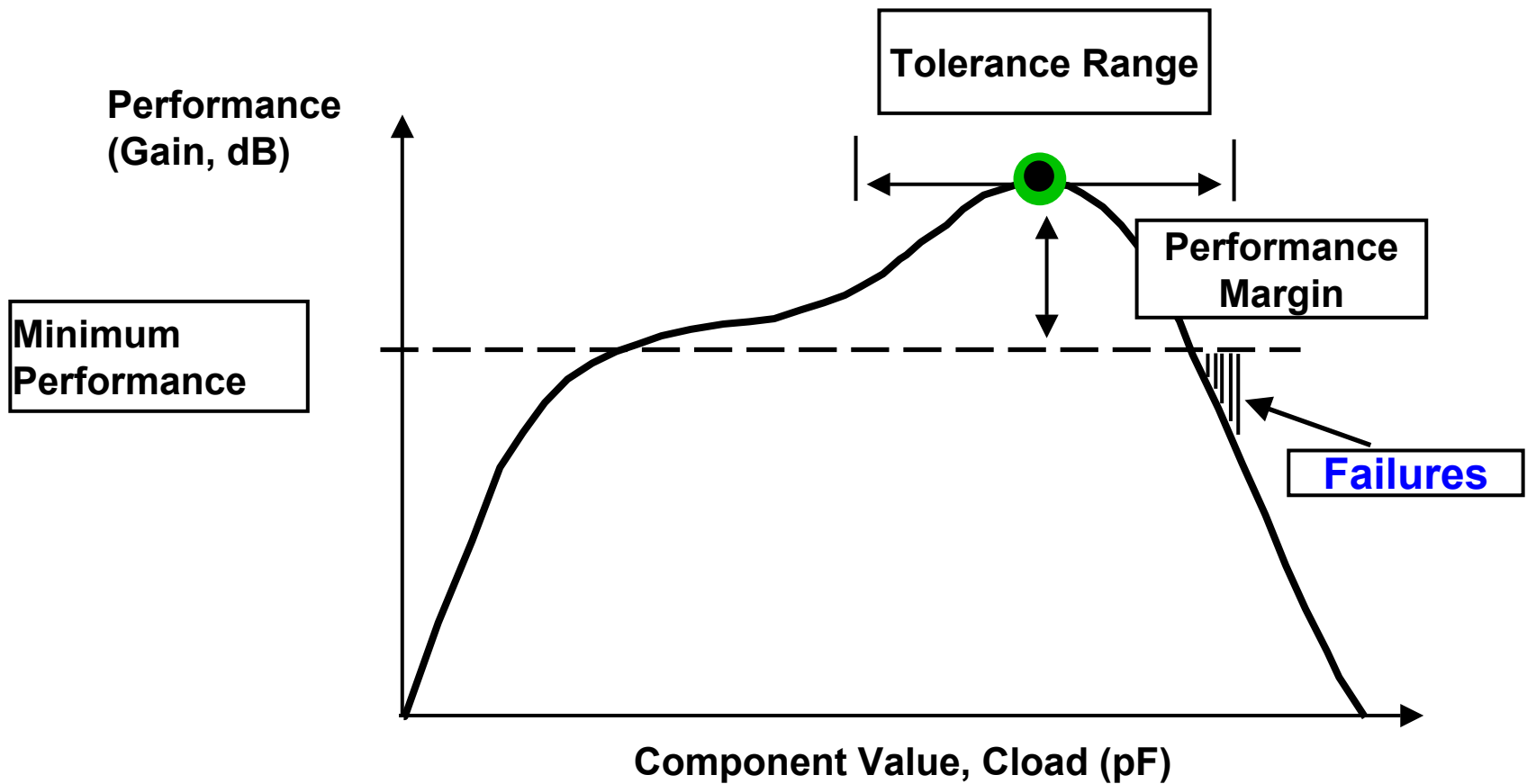
Curves 4
Further improvement towards achieving Robustness

Curve 5
Final Shift the Response by Design Centering to meet Specs.



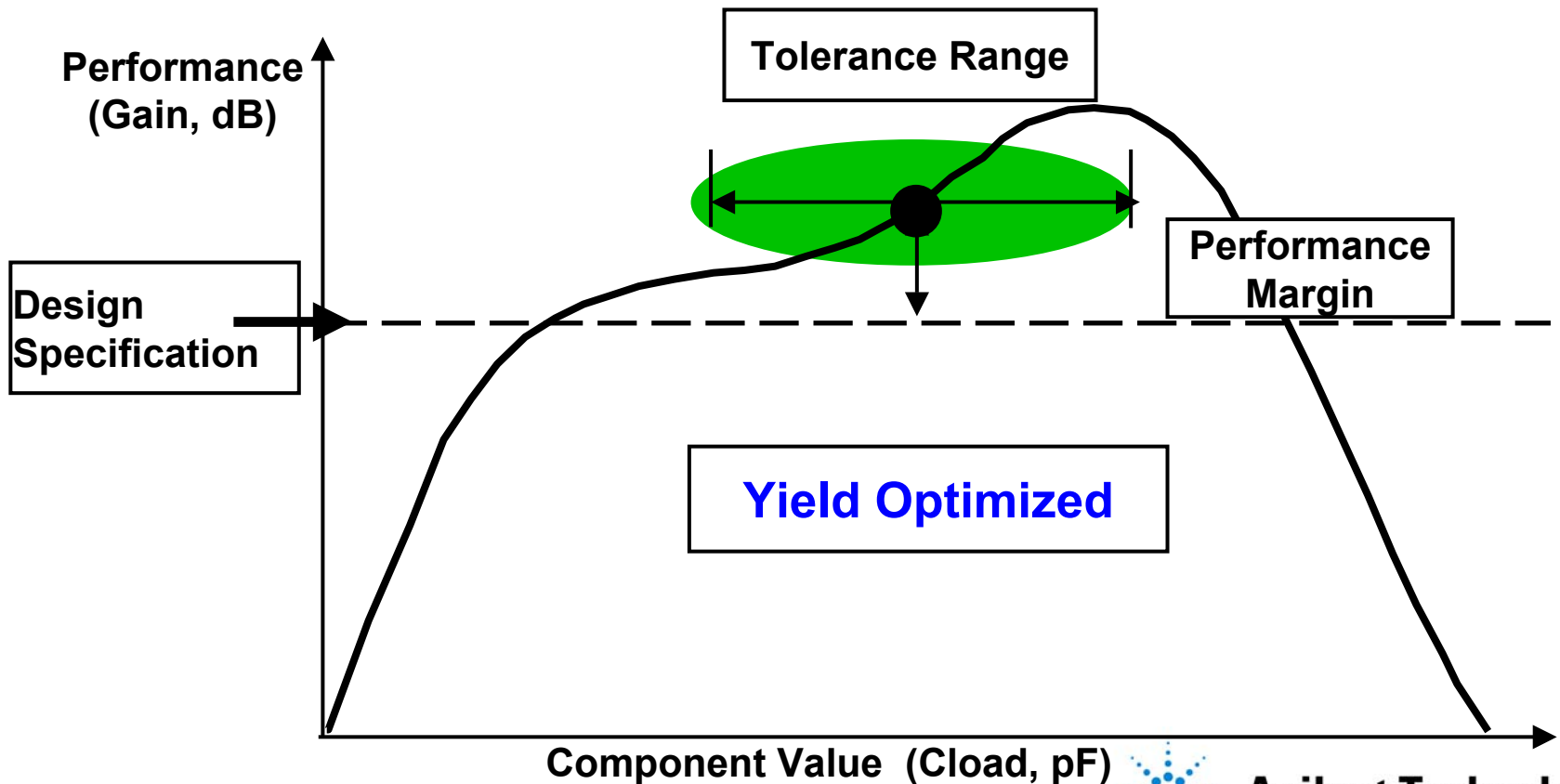
Yield Optimization (Design Centering)

Understanding the Mechanism of Design Centering



Yield Optimization (Design Centering)

Understanding the Mechanism of Design Centering



Component Value (Clod, pF)



Yield Optimization (Design Centering)

Understanding the Mechanism of Design Centering

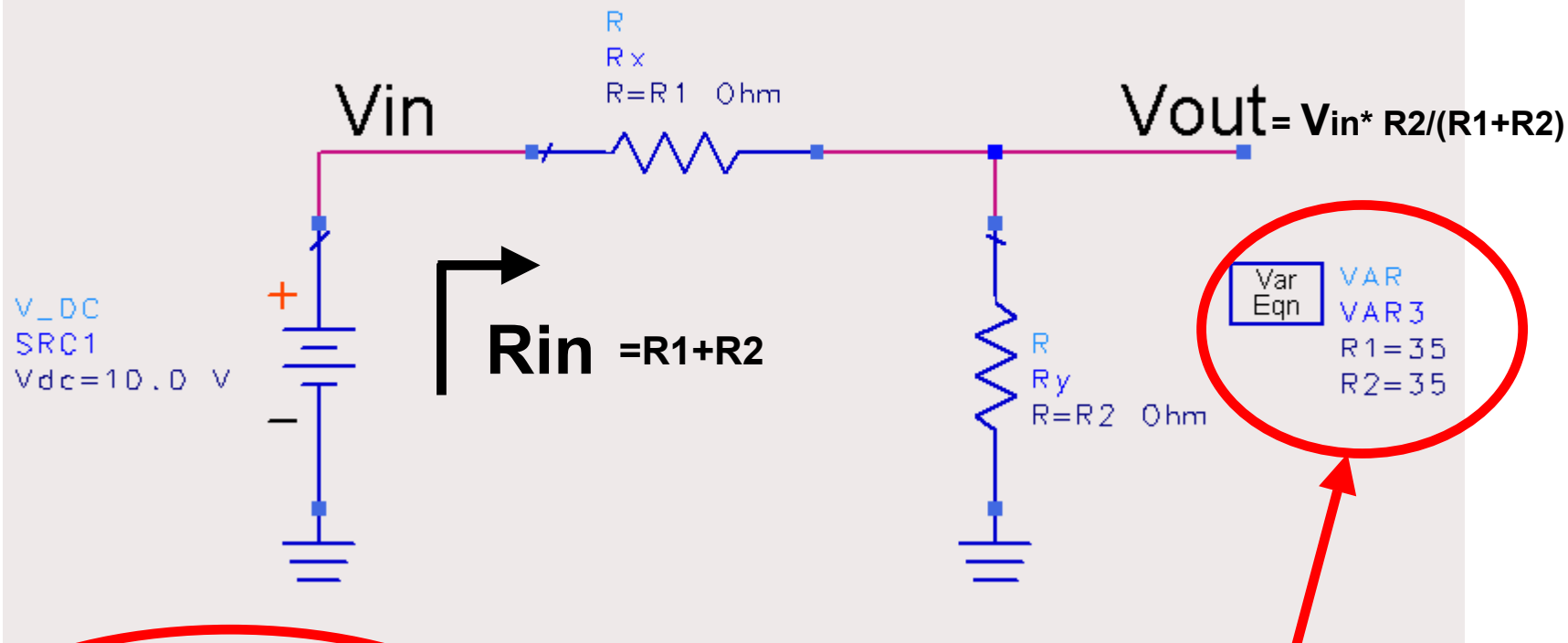
Ex. Resistive Divider

- **Design Centering**
- **Yield Sensitivity Histograms**



Yield Optimization (Design Centering) - Example

Example: "Voltage Divider"



Specifications:

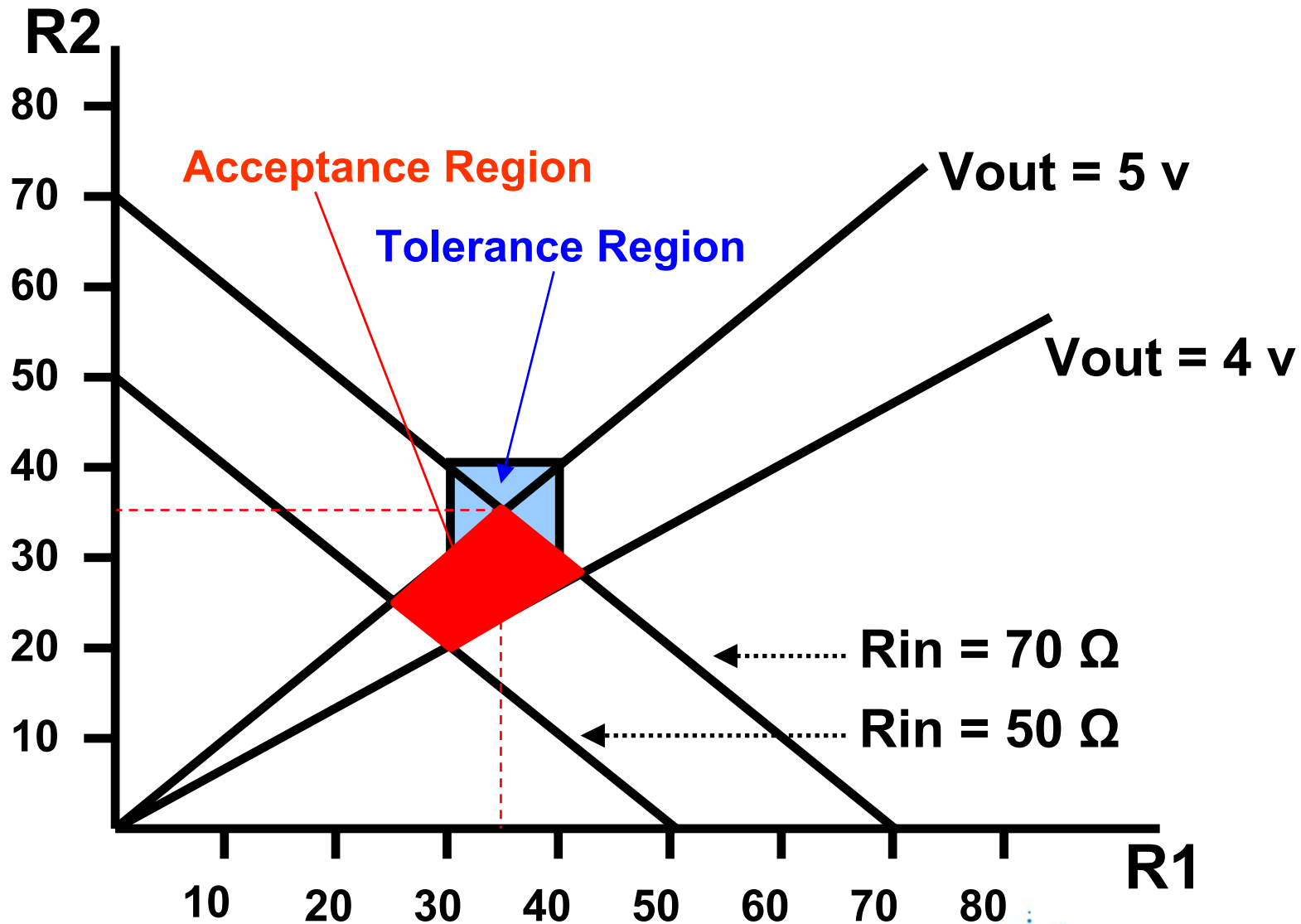
$$4 \leq V_{out} \leq 5$$

$$50 \Omega \leq R_{in} \leq 70 \Omega$$

Initial values
meet specs



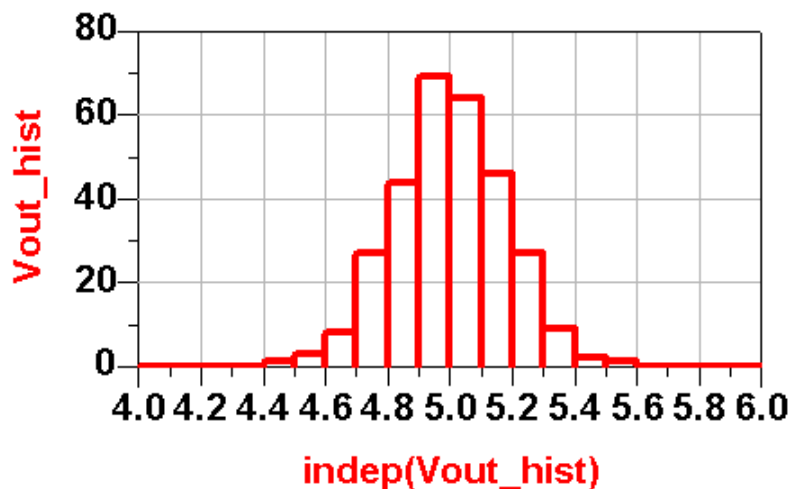
Plotting the Tolerance and Acceptance Regions



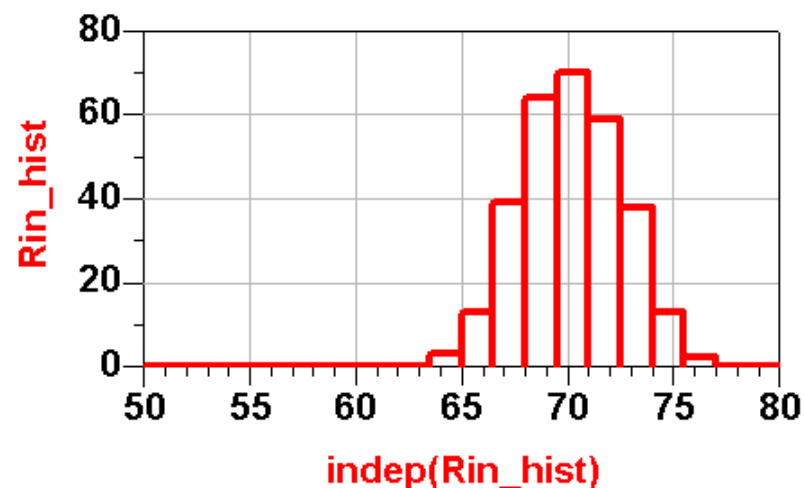
Monte Carlo Yield Simulation Results

MonteCarlo Yield Analysis on the Original Circuit

NumFail	NumPass	Yield
231.000	69.000	23.000



Eqn Vout_hist=histogram(Vout_Spec[0],20,4,6)



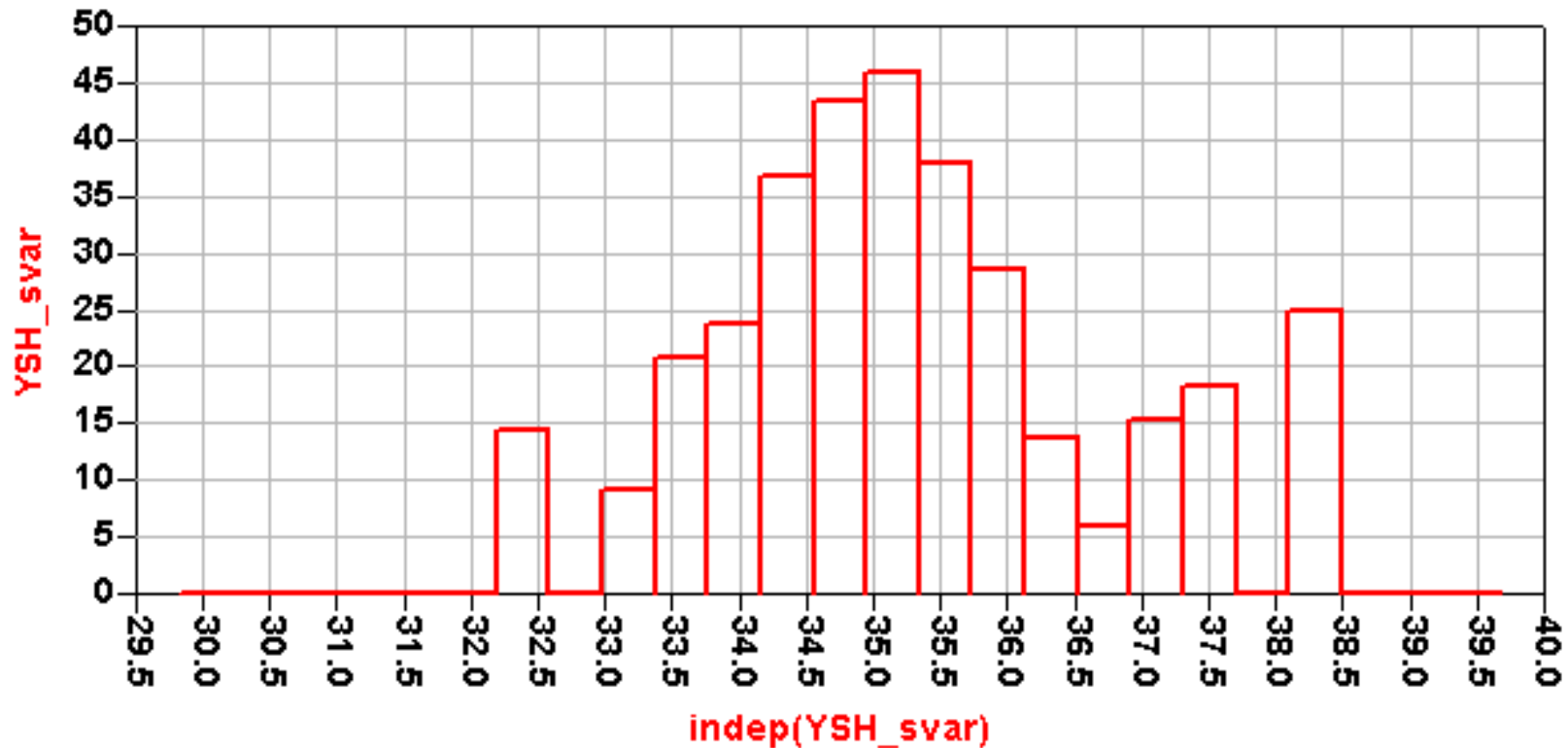
Eqn Rin_hist=histogram(Rin_Spec[0],20,50,80)



Yield Sensitivity Histograms – R1

Eqn svar = R1

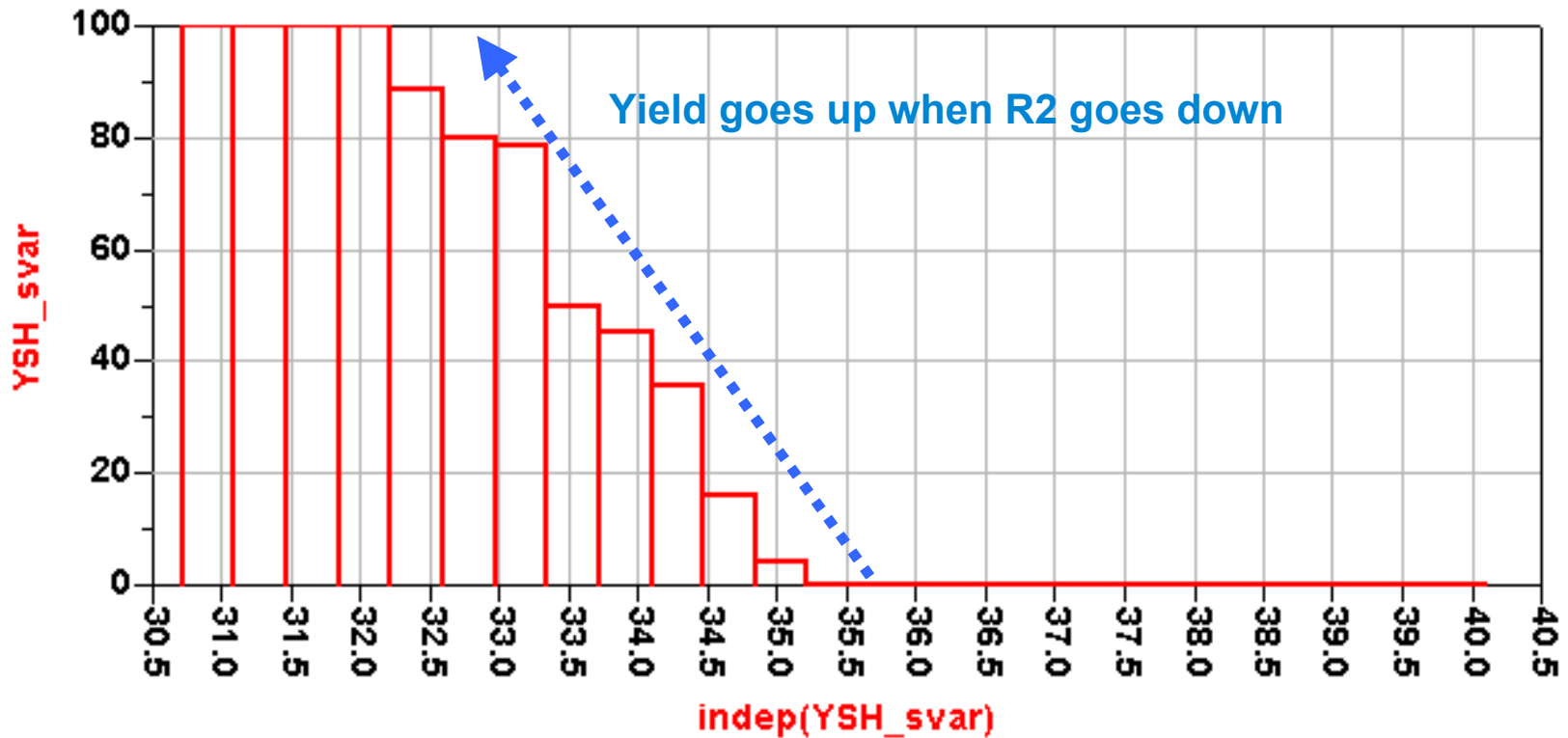
Yield Sensitivity Histogram as a function of any selected component



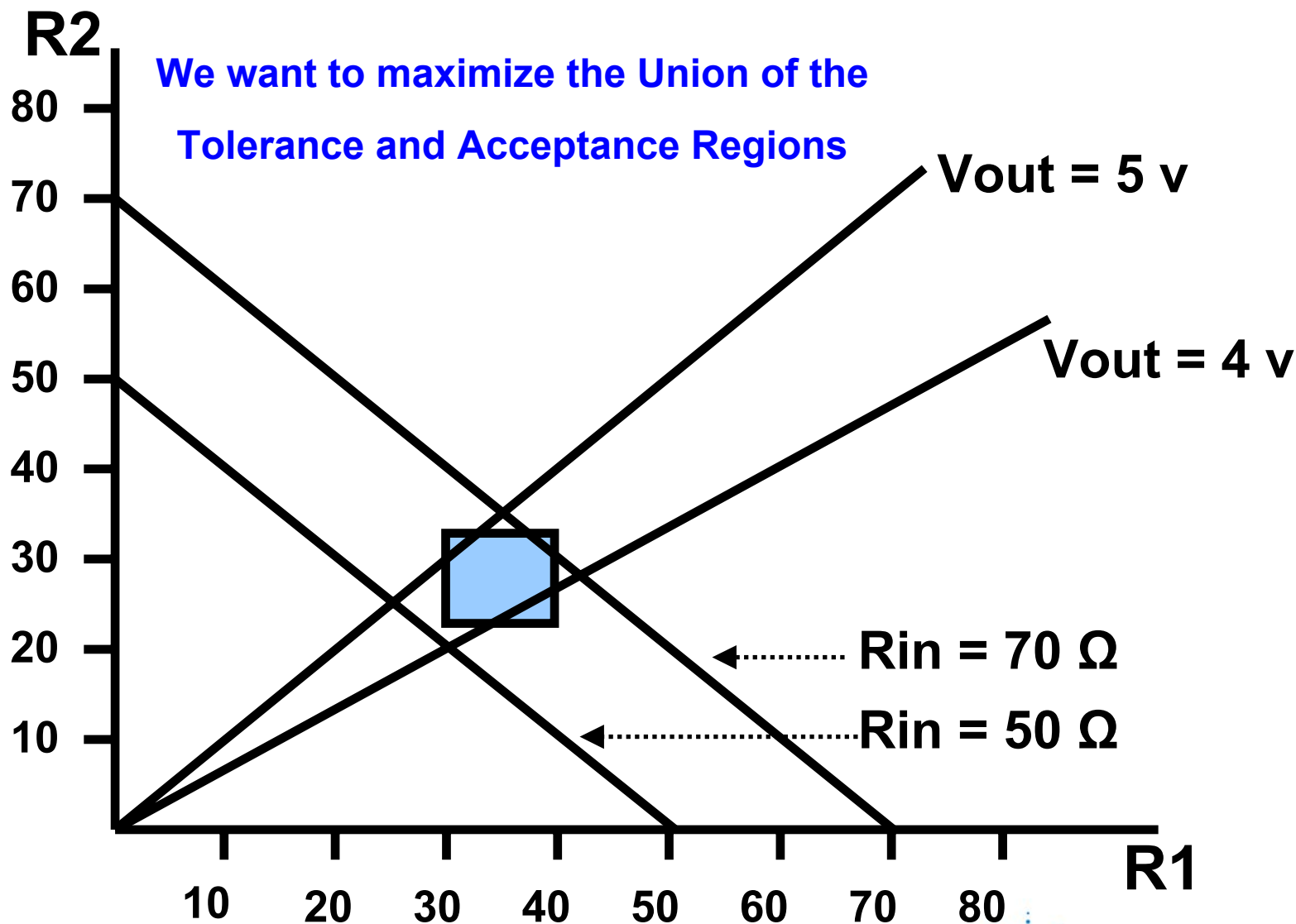
Yield Sensitivity Histograms – R2

Eqn svar = R2

Yield Sensitivity Histogram as a function of any selected component



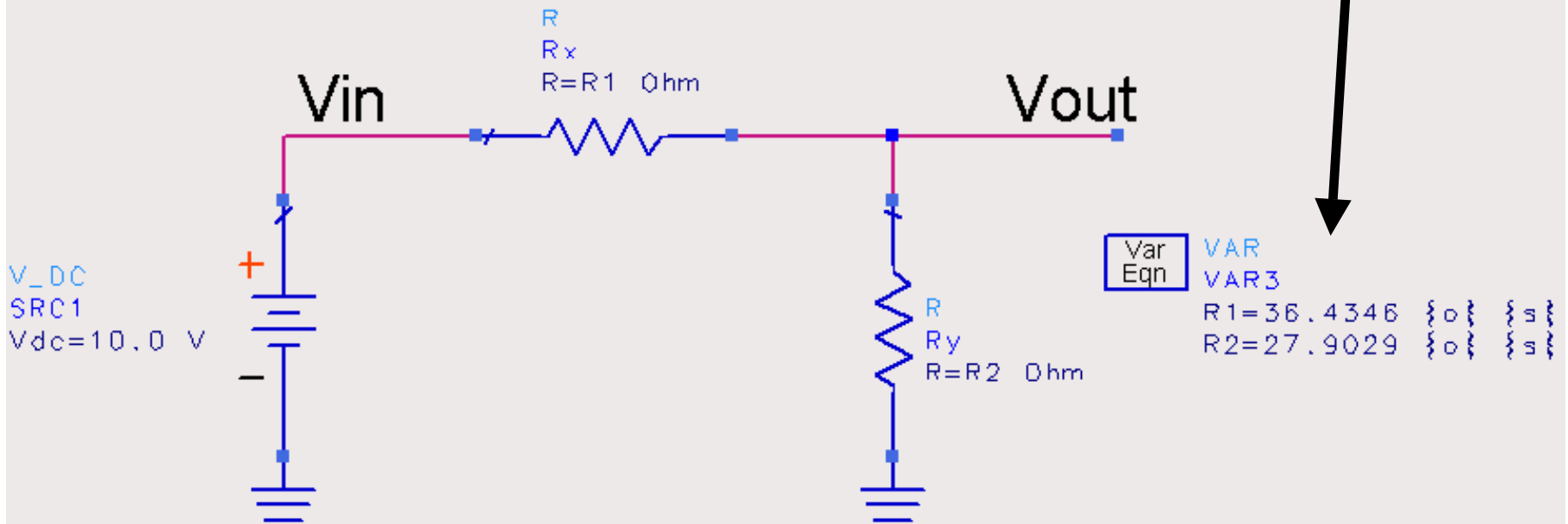
Design Centering – Maximizing the Yield



Running "Yield Optimization / Design Centering"

Design Centering Results

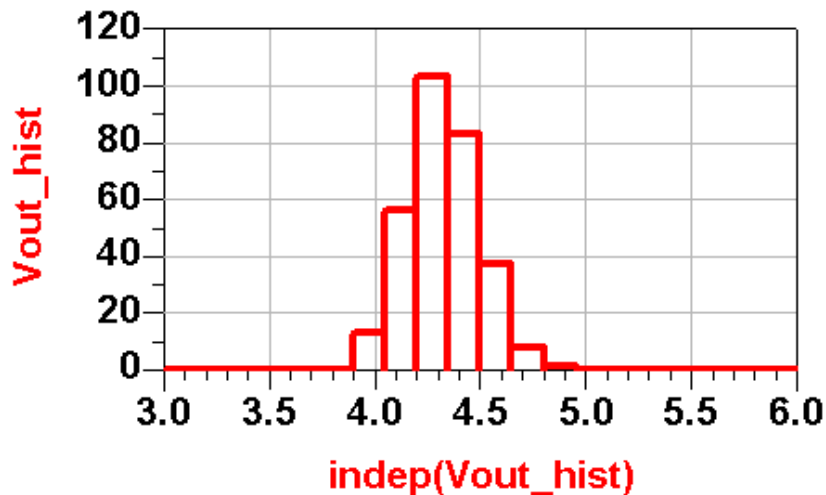
Example: "Voltage Divider"



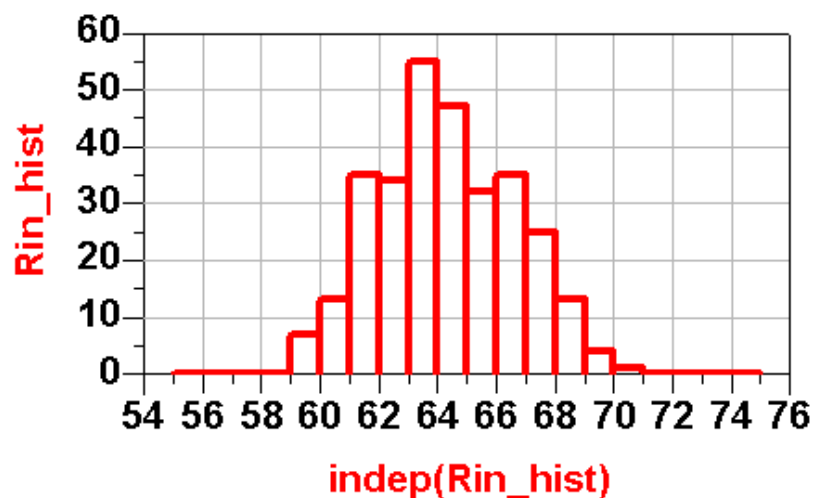
Yield Sensitivity Histograms

MonteCarlo Yield Analysis on the Centered Circuit

NumFail	NumPass	Yield
13.000	287.000	95.667



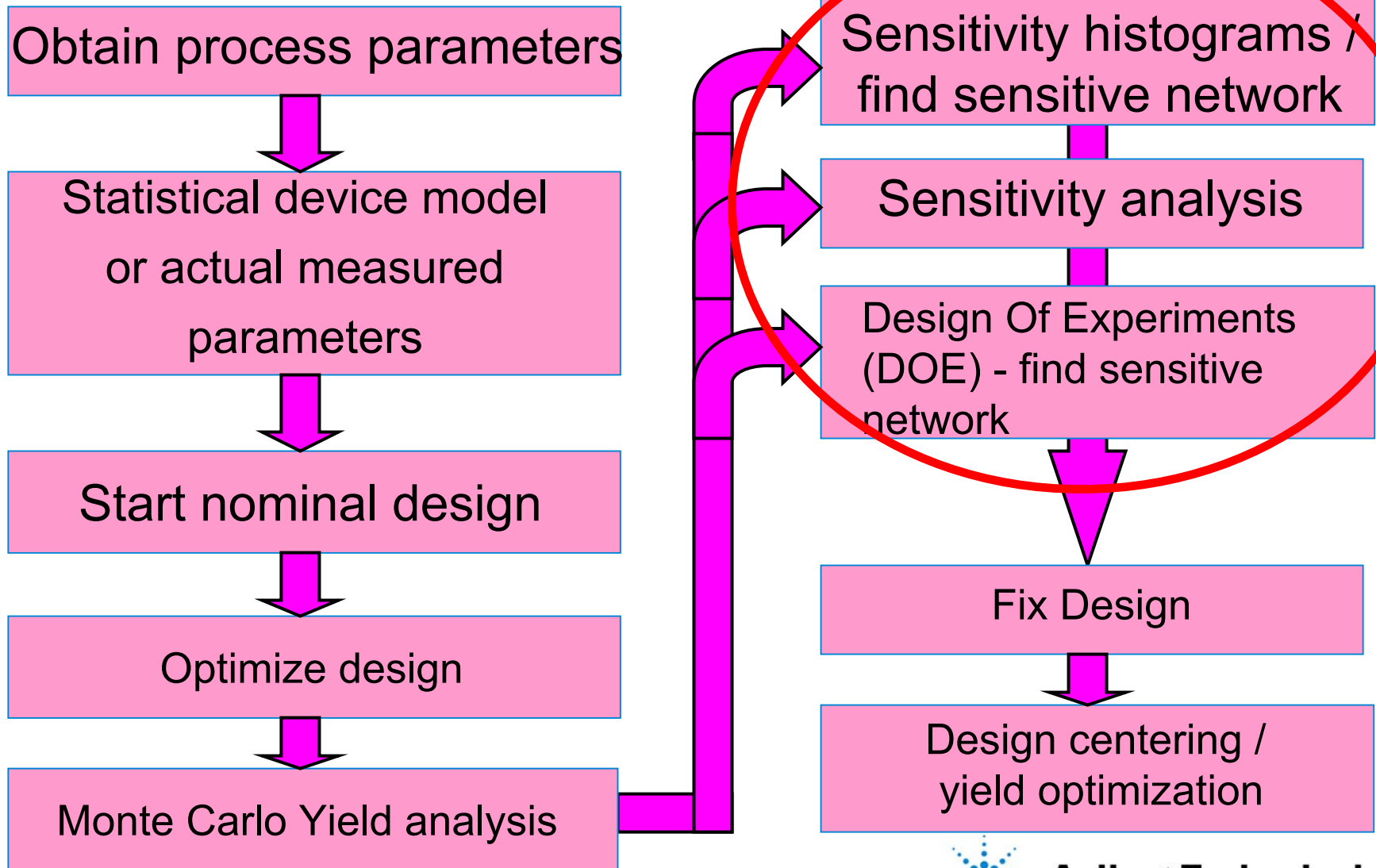
Eqn Vout_hist=histogram(Vout_Spec[0],20,3,6)



Eqn Rin_hist=histogram(Rin_Spec[0],20,55,75)



The DFY Process for MMIC



- **Design for nominal performance using performance optimization**
- **Find the yield**
- **Use YSH, Sens and/or DOE to find the problematic areas**
- **Fix them**
- **Perform Design centering**
- **Find the final yield.**
- **Fabricate – Sell – Make Tons of Money and be happy for ever!**

