# Design for Yield

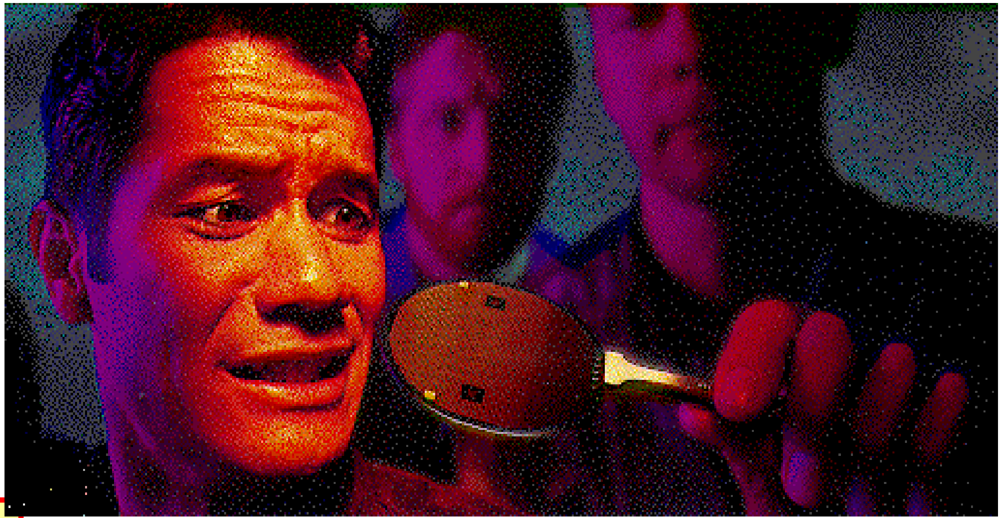
# (DFY)

## What is a Robust Design?

# A design that is less sensitive to the manufacturing process

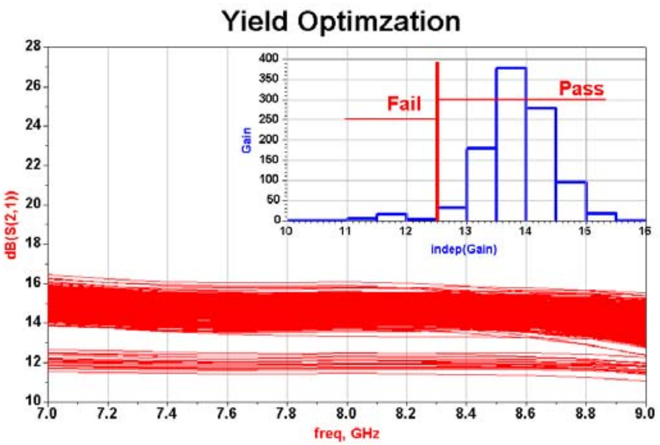
# Advanced DFY Tools

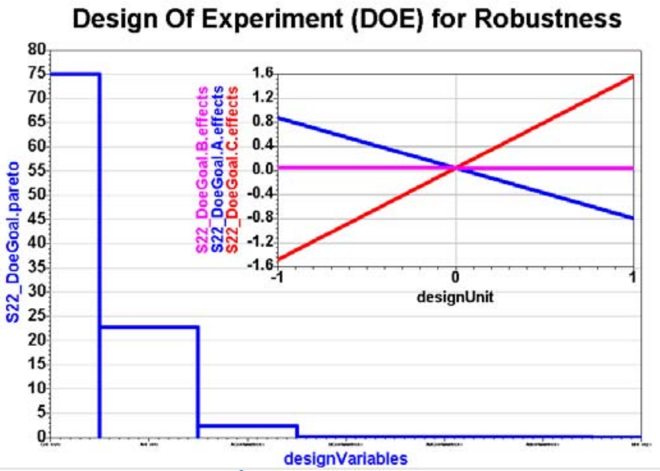
No longer designers have to worry that their circuits have to be redesigned again.



No longer managers have to be concerned for the high costs of multi wafer runs.

***ADS Advanced DFY Tools help designers achieve "First Pass Success".***



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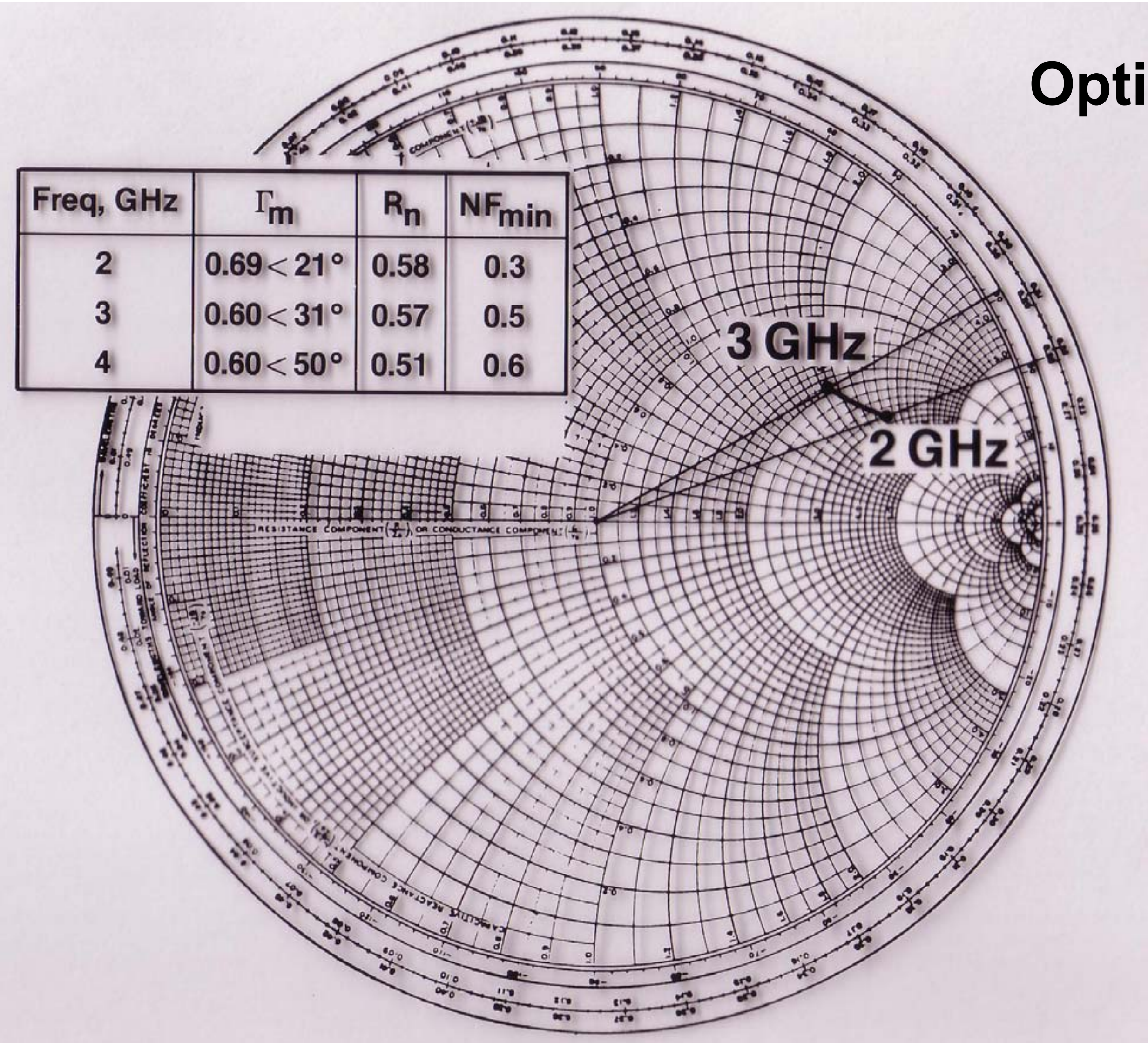
# Example: 2.4 GHz MIC LNA on Alumina Substrate

| Freq, GHz | $\Gamma_m$ | $R_n$ | $NF_{min}$ |
|---|---|---|---|
| 2 | 0.69 < 21° | 0.58 | 0.3 |
| 3 | 0.60 < 31° | 0.57 | 0.5 |
| 4 | 0.60 < 50° | 0.51 | 0.6 |




**Optimum Noise Match**

**NEC 67383 FET**

**2-3 GHz**

**Alumina Substrate**

**Er = 9.9   H=25 mils**

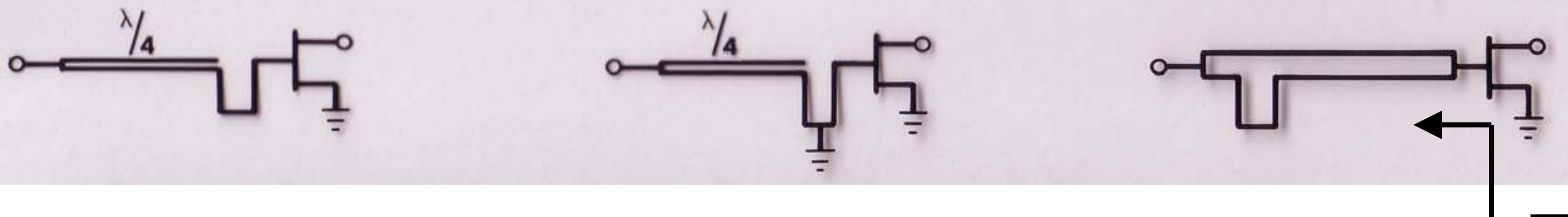
**Design Spec:**

**.7 dB NF @ 2.4 GHz**

# Example: 2.4 GHz LNA - MIC Design

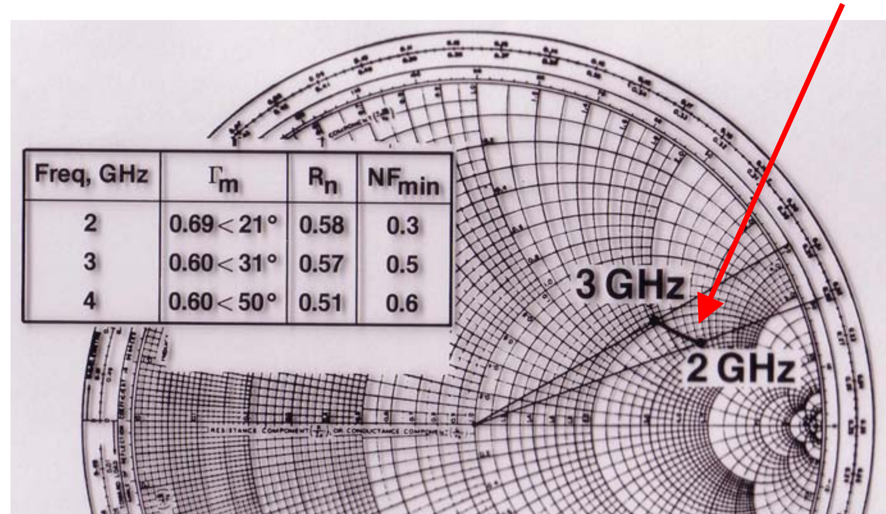
## Three of many different ways to match for optimum noise

| 50Ω open shunt stub $\lambda/4$ series line, $Z_o = 104\Omega$ | 50Ω shorted shunt stub $\lambda/4$ series line, $Z_o = 104\Omega$ | 50Ω series line and 50Ω open shunt stub |
|---|---|---|




Γm

**Goal is to have the matching network impedance coincide with the optimum noise figure impedance, Γm**




| Freq, GHz | $\Gamma_m$ | $R_n$ | $NF_{min}$ |
|---|---|---|---|
| 2 | 0.69 < 21° | 0.58 | 0.3 |
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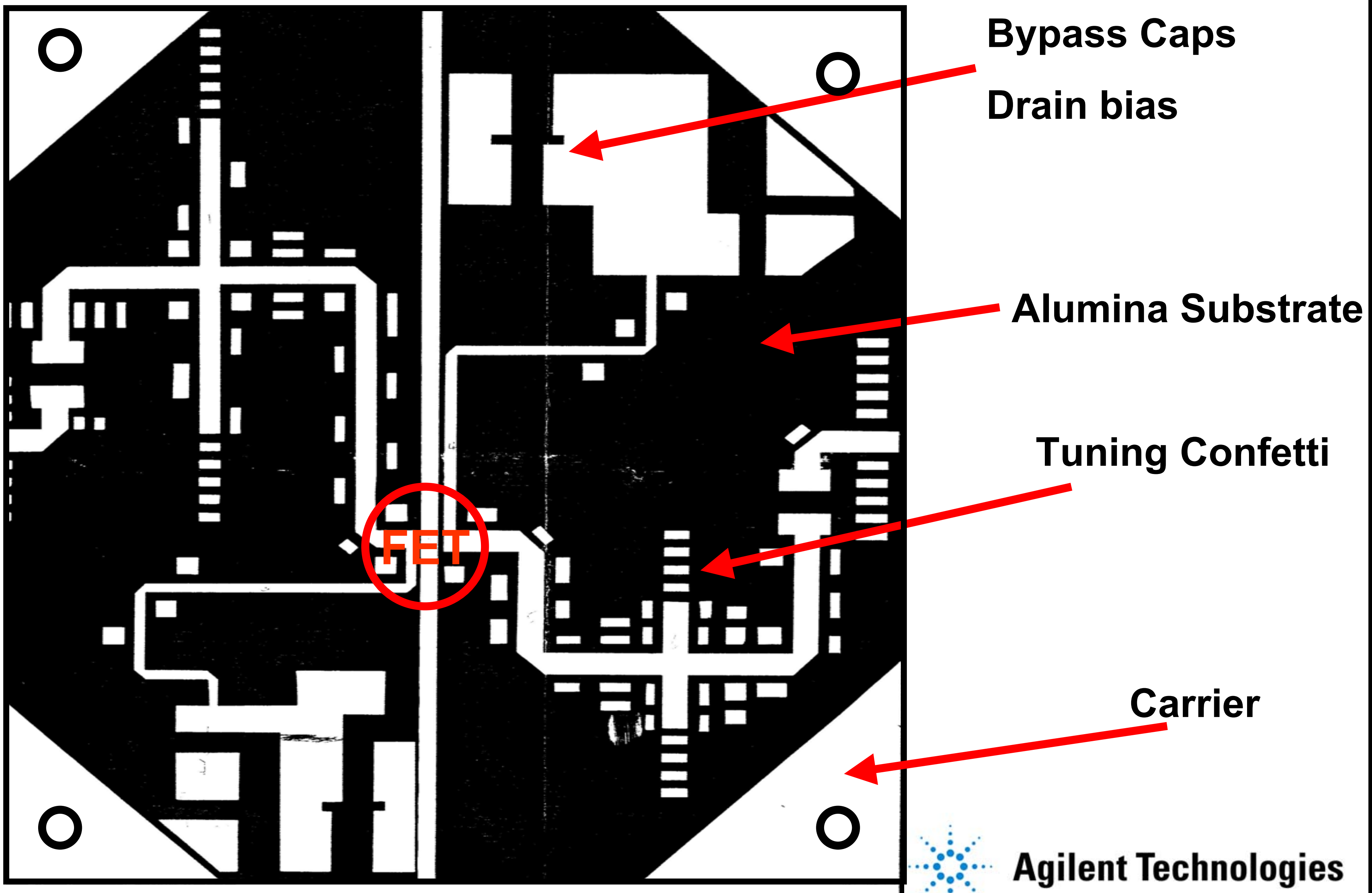
# Example: Ruby Mask - 2.4 GHz LNA

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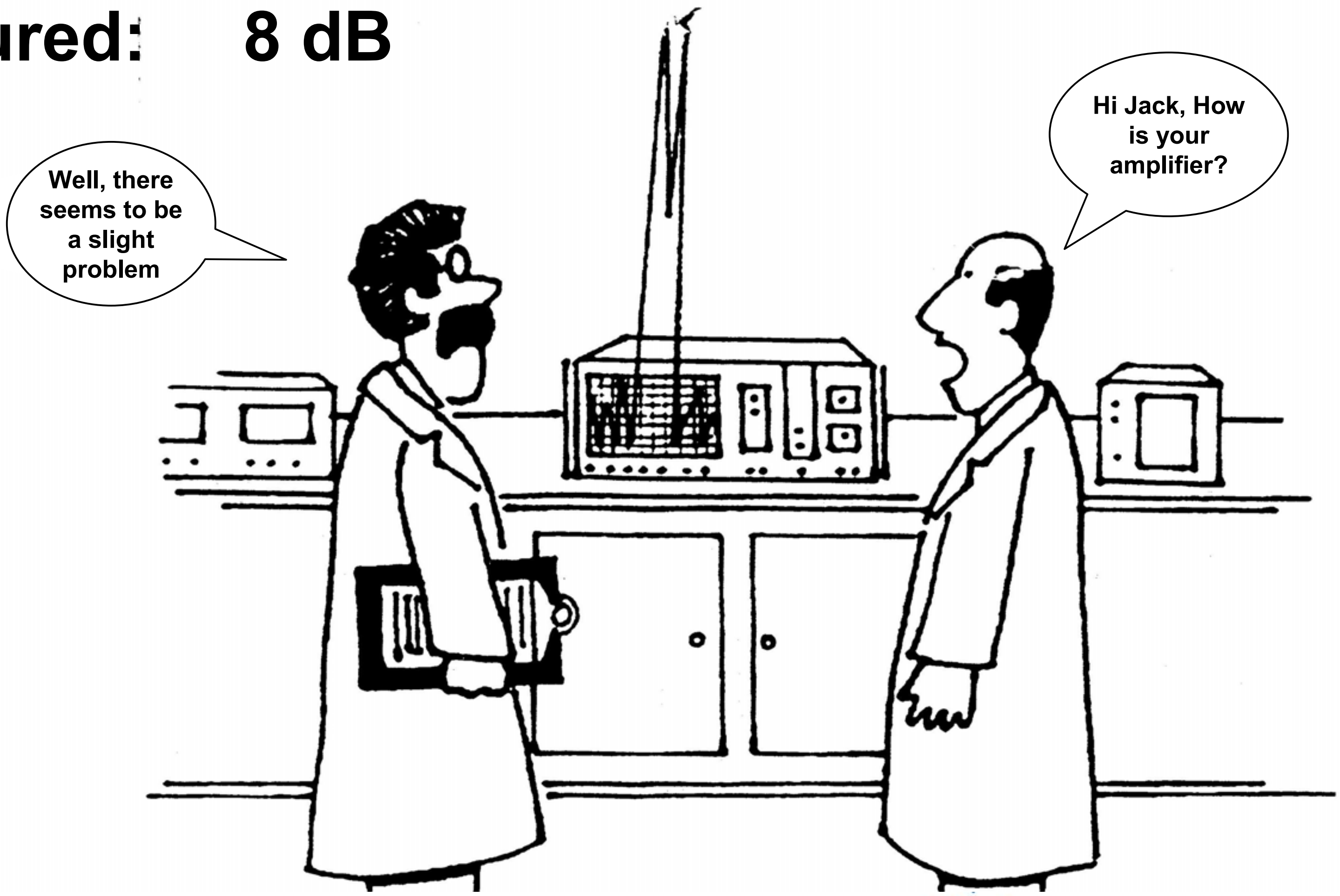
# Initial Test Results (Major Problem)

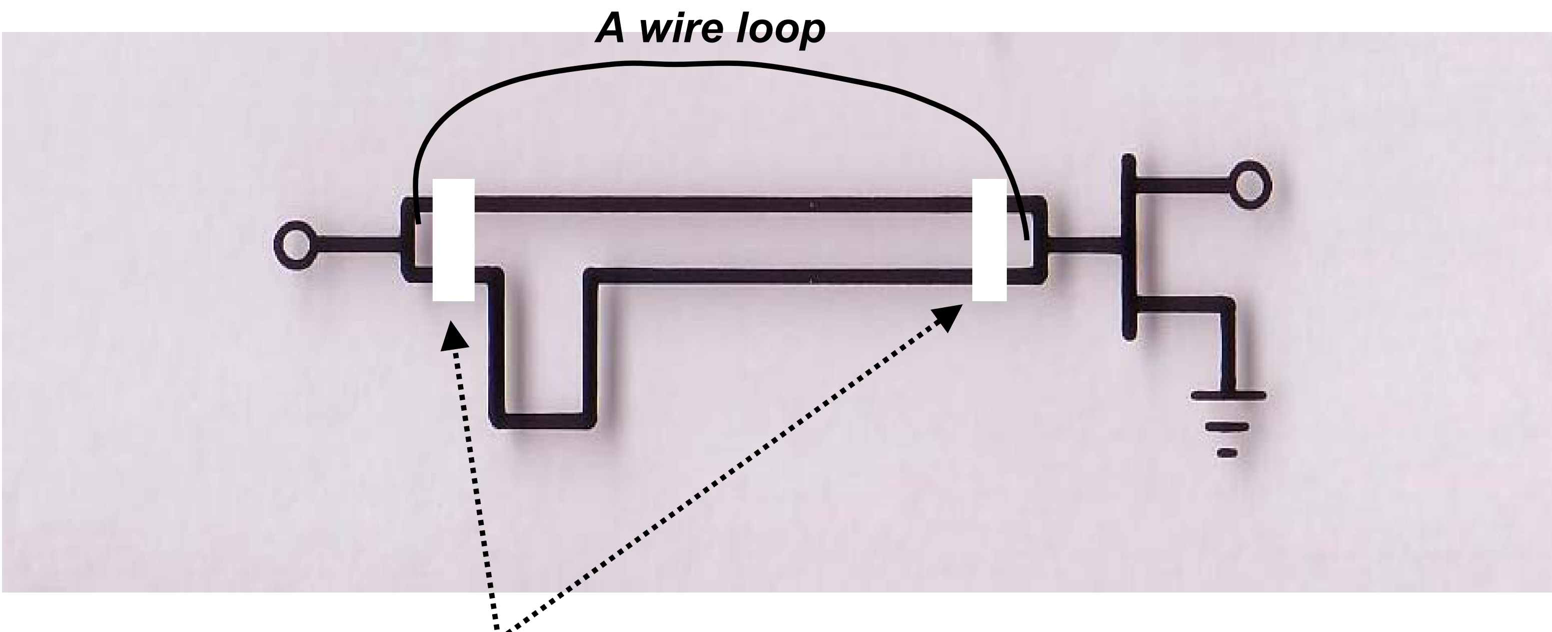
**NF Spec: .7 dB**

**Measured: 8 dB**



# Finding a solution in the lab

## This solution achieved a .5 db NF @ 2.4 GHz

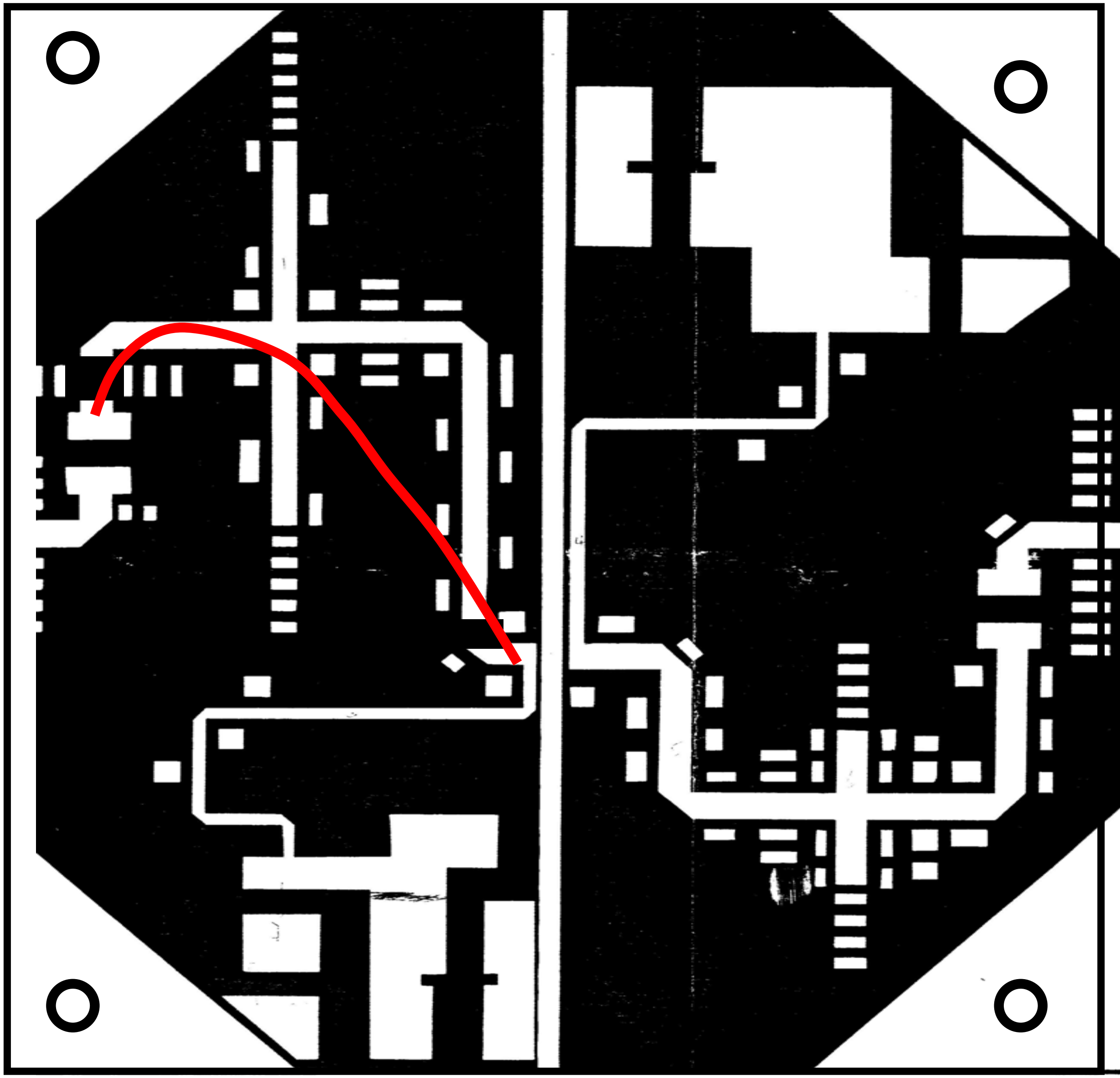



**1- Diamond Scribe out the Input Matching Network**

**2- Solder a loop of inductive wire from FET to connector**

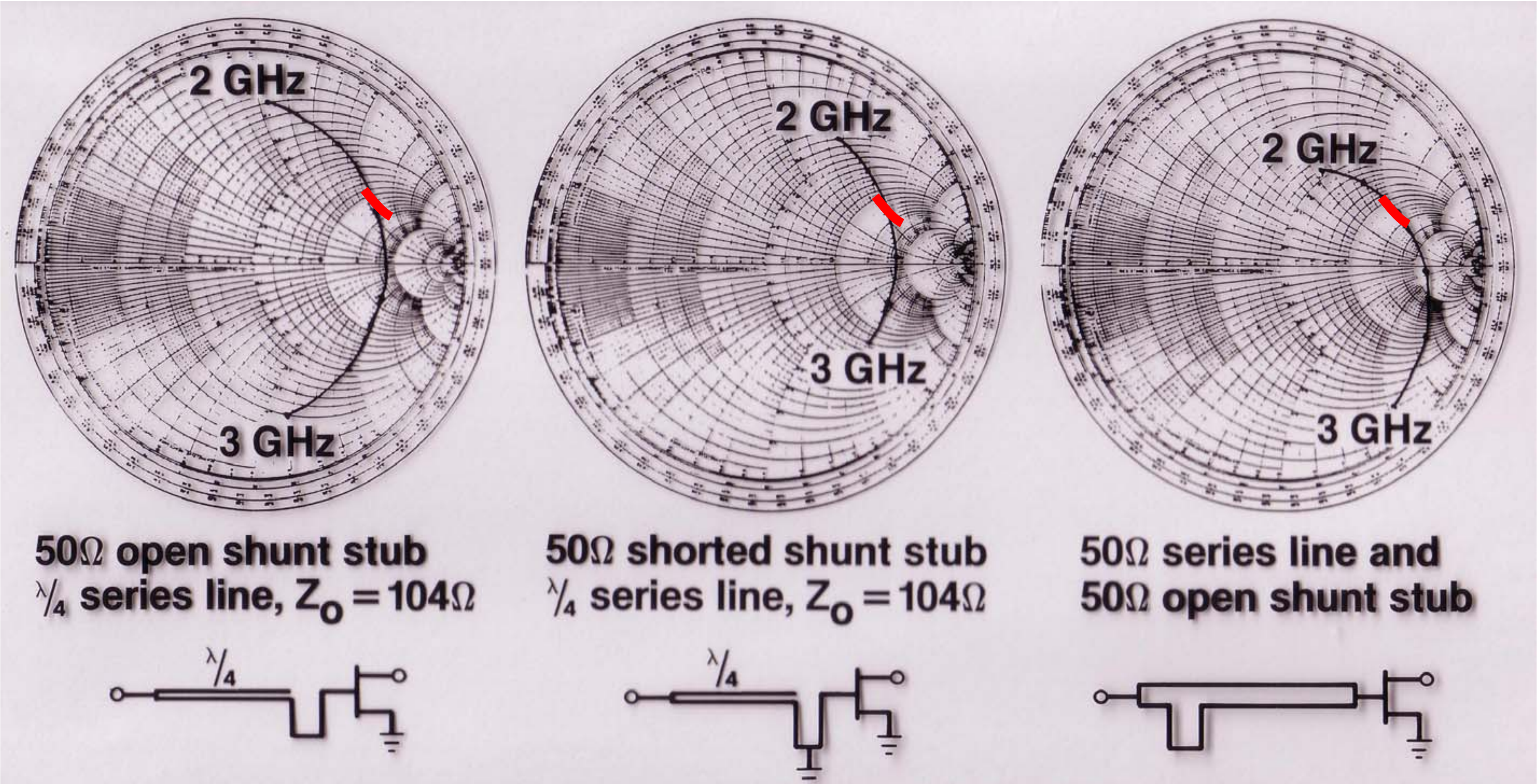
# Example: Ruby Mask - 2.4 GHz LNA

Wire loop from input port to FET's Gate



Back to the drawing board for further investigation

# Understanding what went wrong




Input impedance as function of frequency



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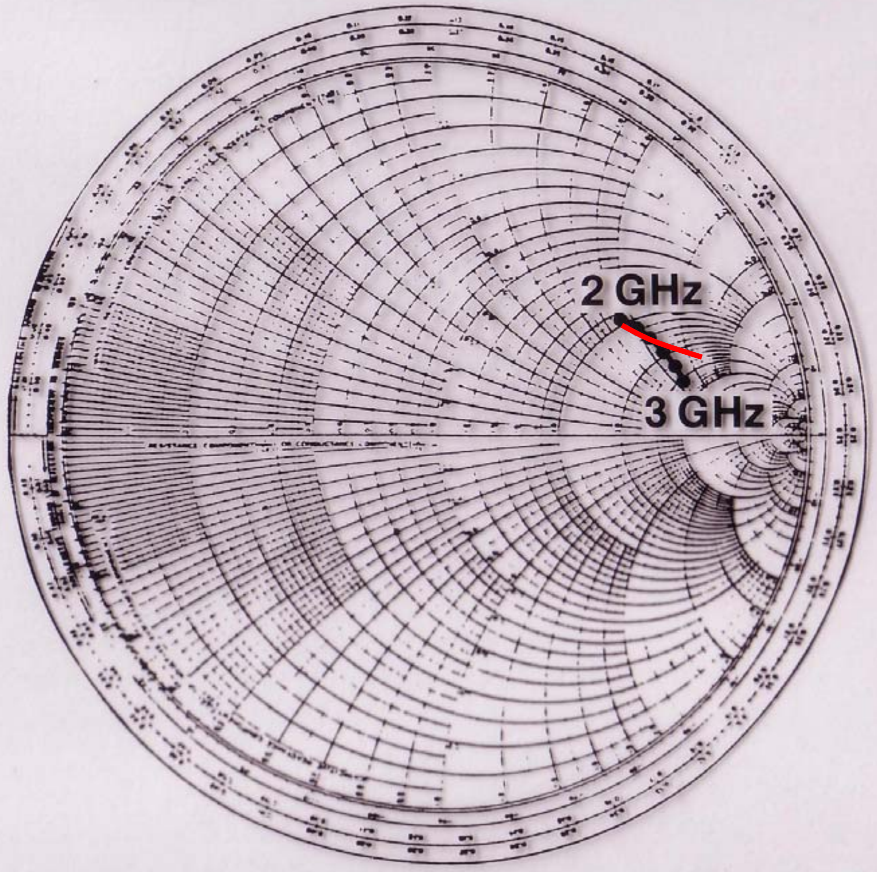
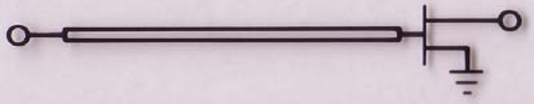
# Single Line Matching – Low Q




$\Gamma_S$ of a single line, $Z_O = 120\Omega$



Use of high impedance, single line was the best technique for achieving robust & optimum Results, <u>but too narrow to realize.</u>

Suspended line concept was utilized to produce a realizable, wider, high impedance line with a low Q broadband network



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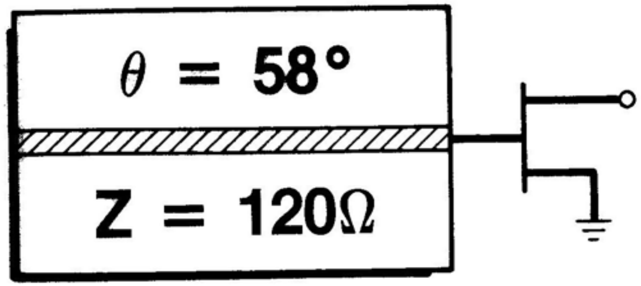
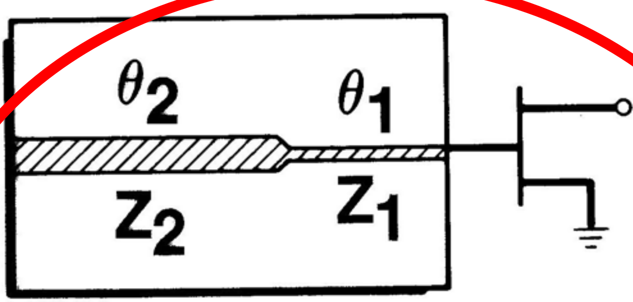
# Matching with Single Line – Low Q

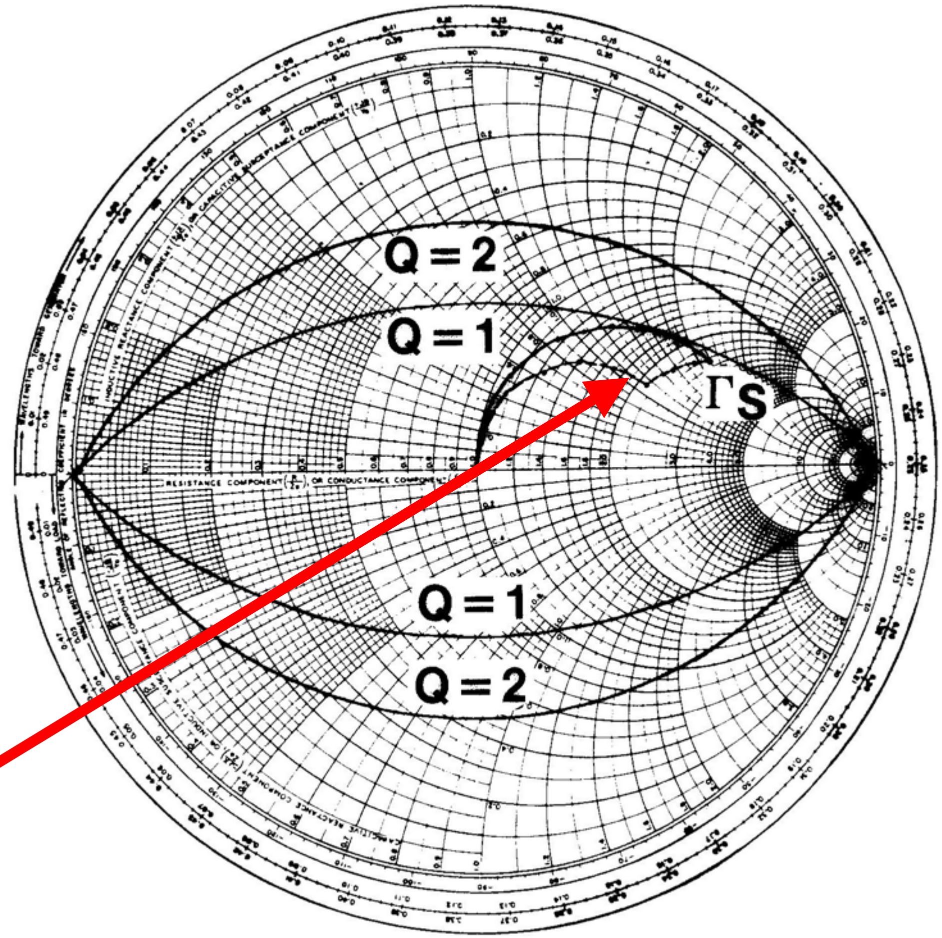



W = 1.5 mil on
25 mil alumina



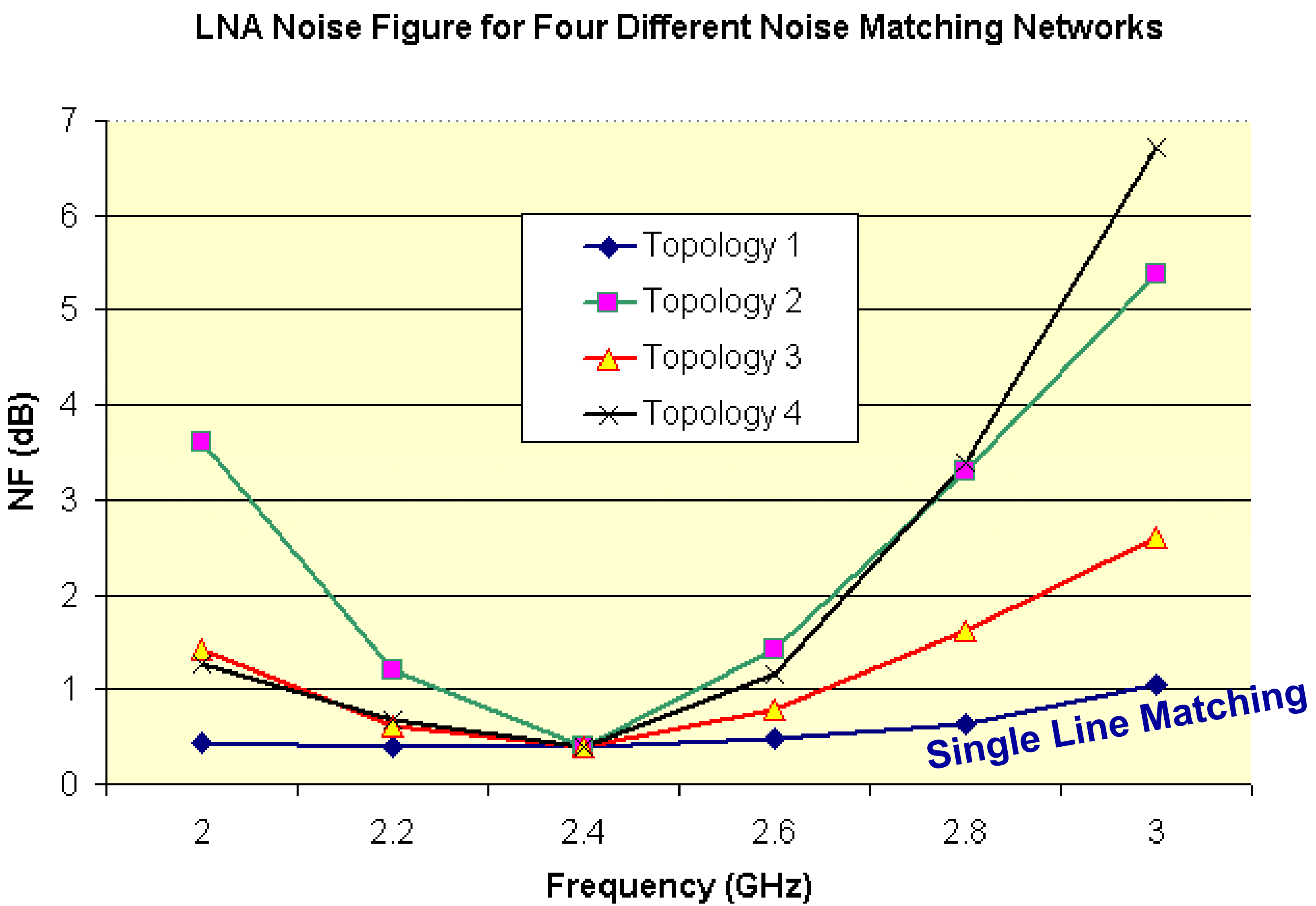

$Z_1 = 250\Omega$ $\theta_1 = 13.5°$

$Z_2 = 89\Omega$ $\theta_2 = 61°$



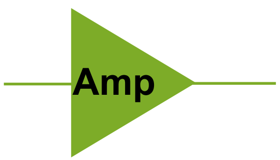

Option 2 is even more Robust, but non-realizable

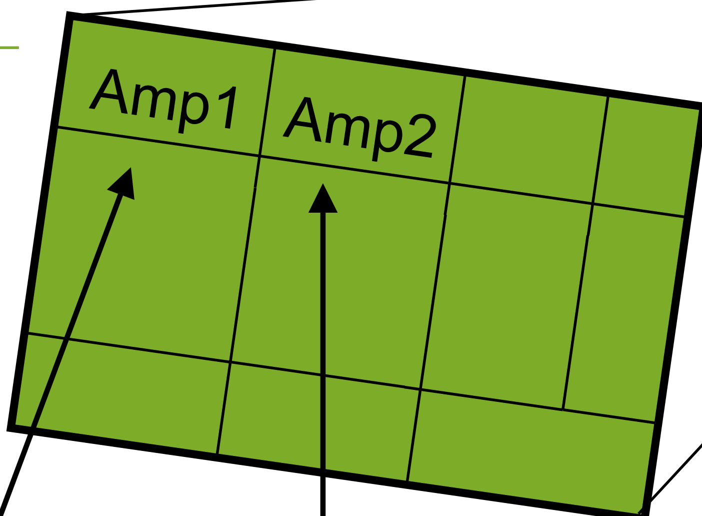
# NF Simulation of the Various Matching networks

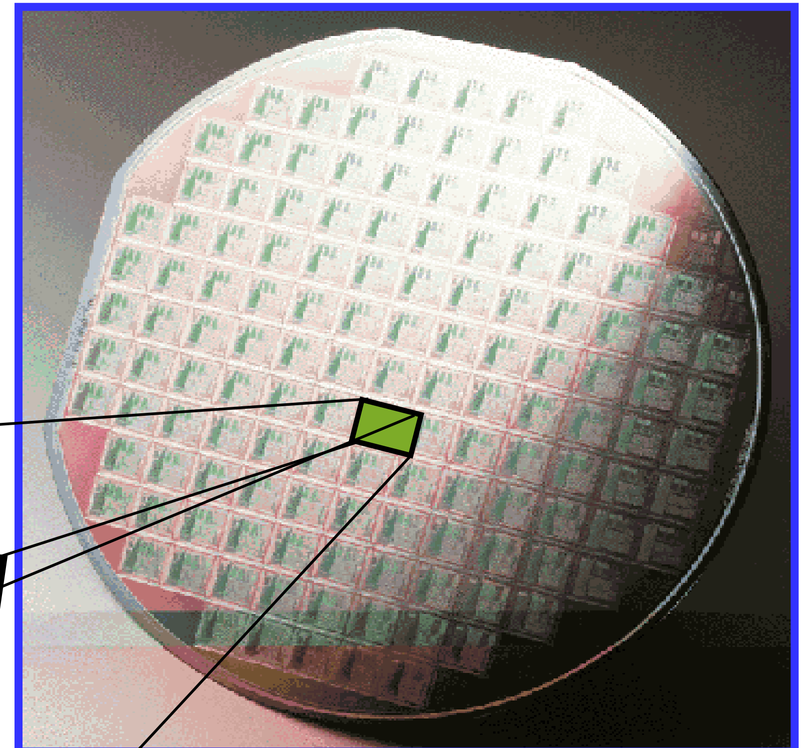


# Real MMIC Designs – Fabricated on the same wafer

**A Reticle contains a few circuits, stepped and repeated across the whole wafer**



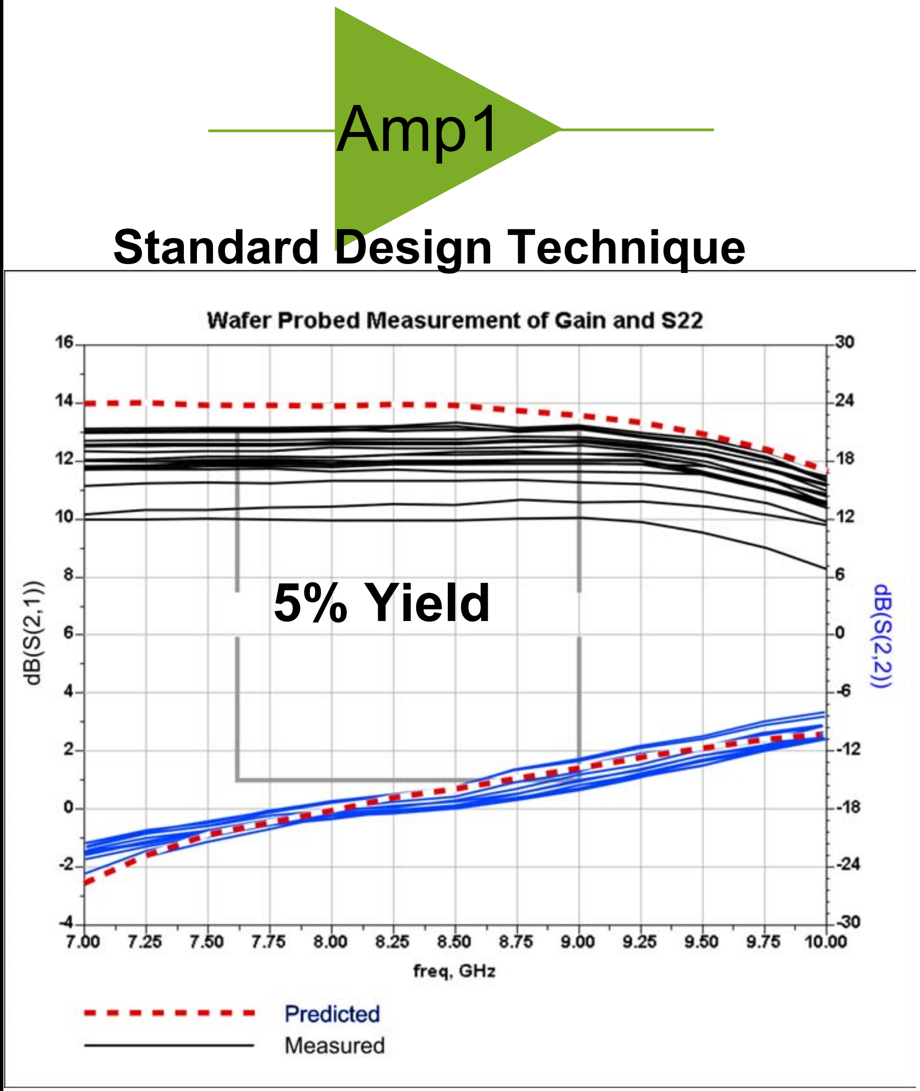



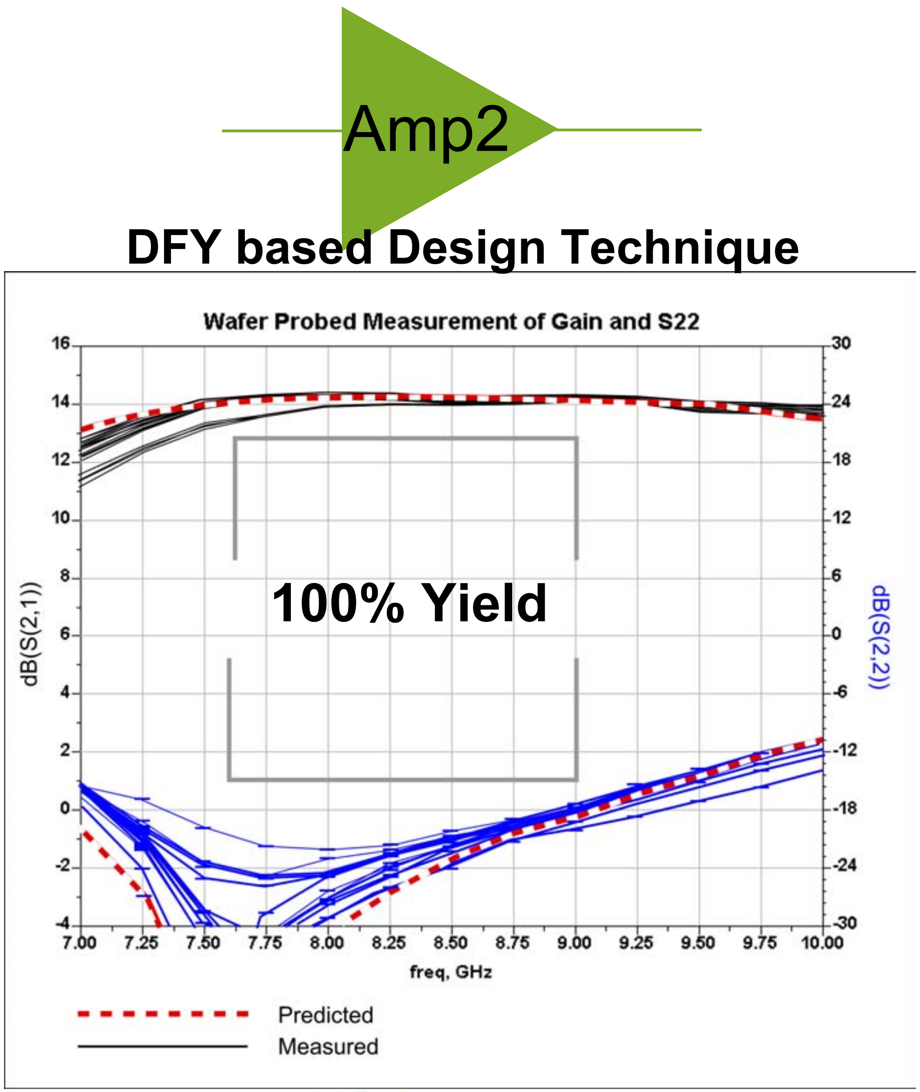
All designs went through the same Wafer Fab Process

**1) Used a standard design technique**

**2) Used a DFY Based design technique**

# Our Goal is to Create Something like Amp2



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# Real MMIC Designs – Fabricated on the same wafer

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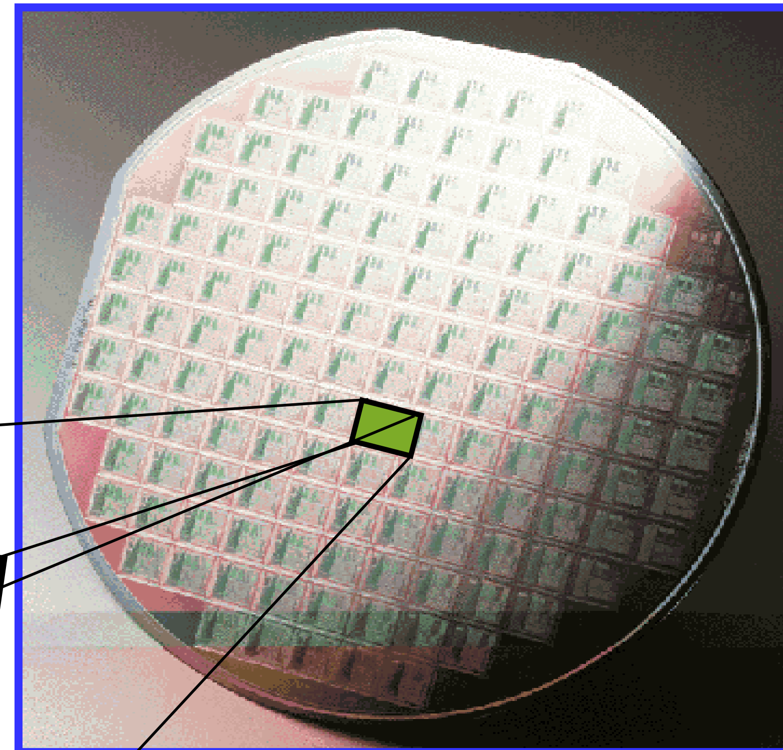
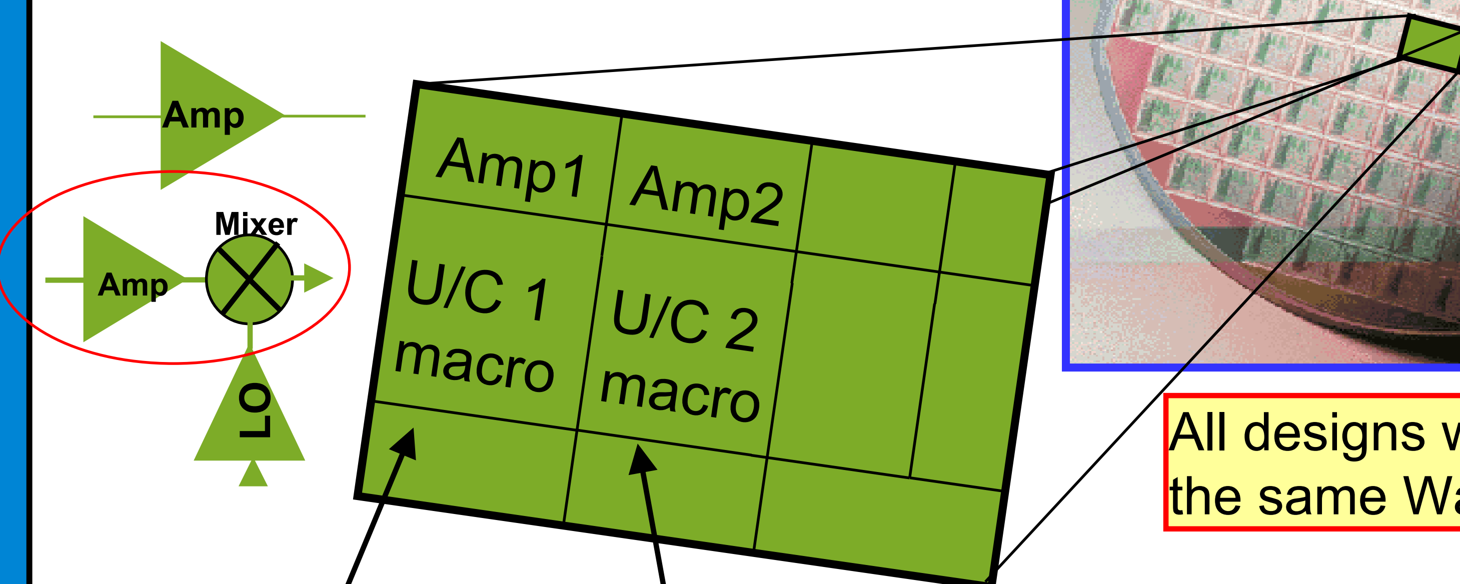




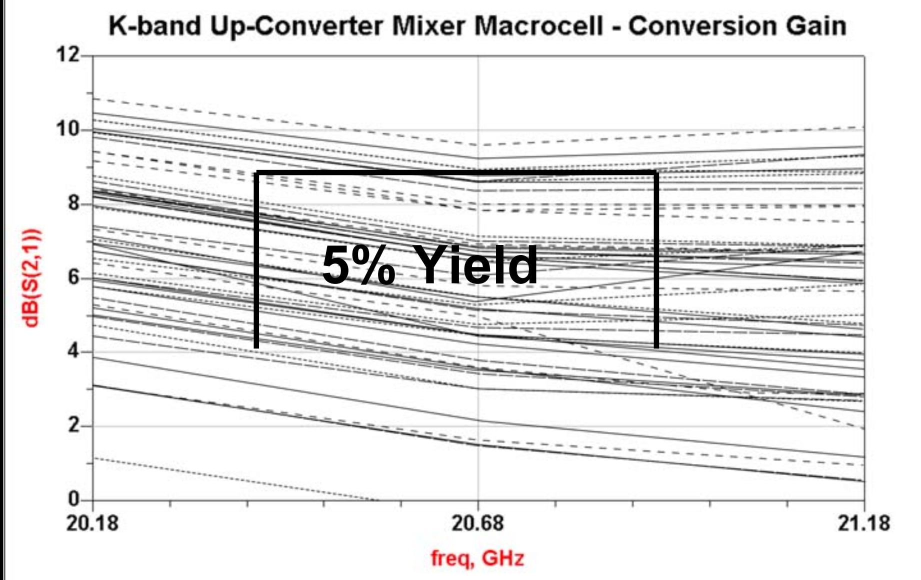

All designs went through the same Wafer Fab Process

**1) Used a standard design technique**

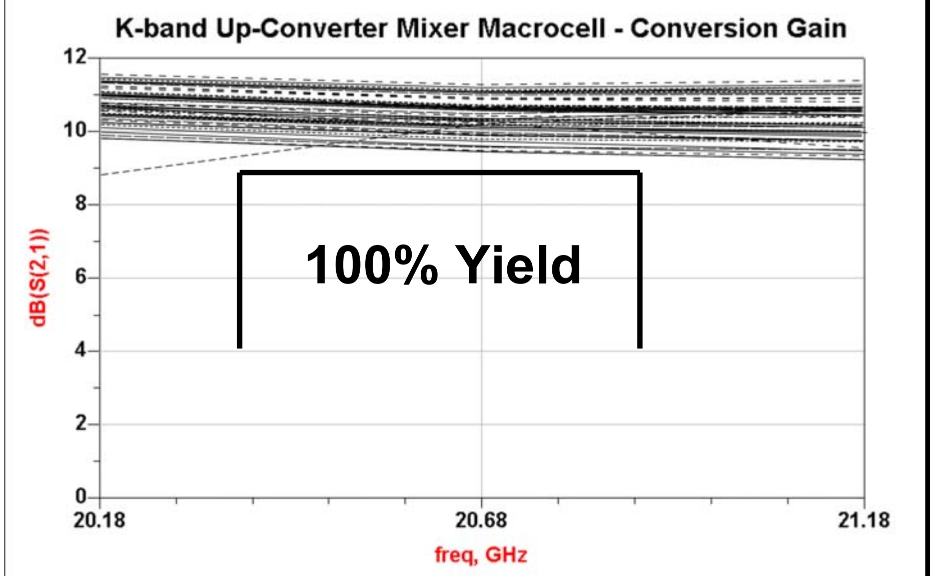
**2) Used a DFY Based design technique**

# Our Goal is to Create Something like U/C 2

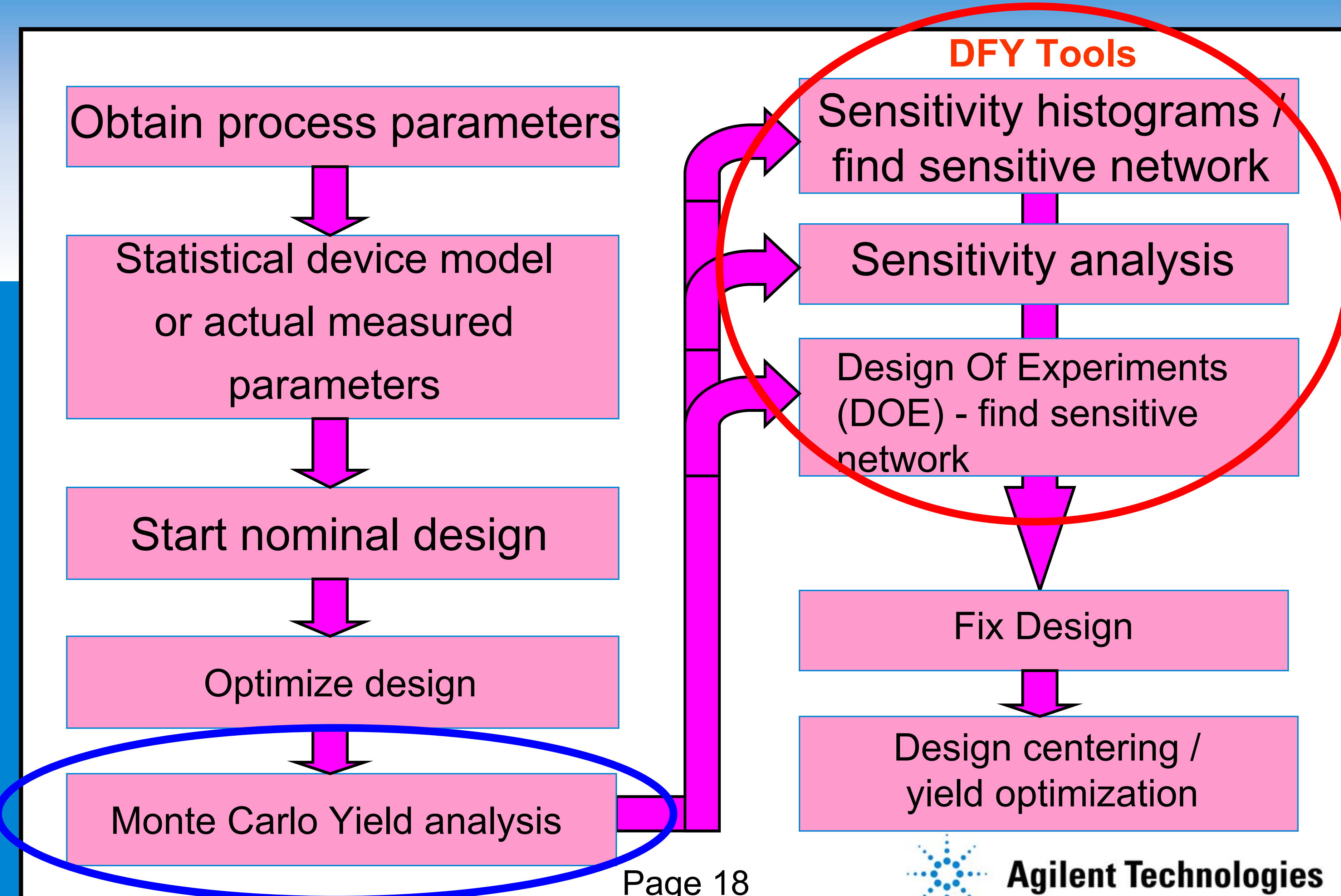

Standard Design Technique




DFY Based Design Technique



# The DFY Process for MMIC

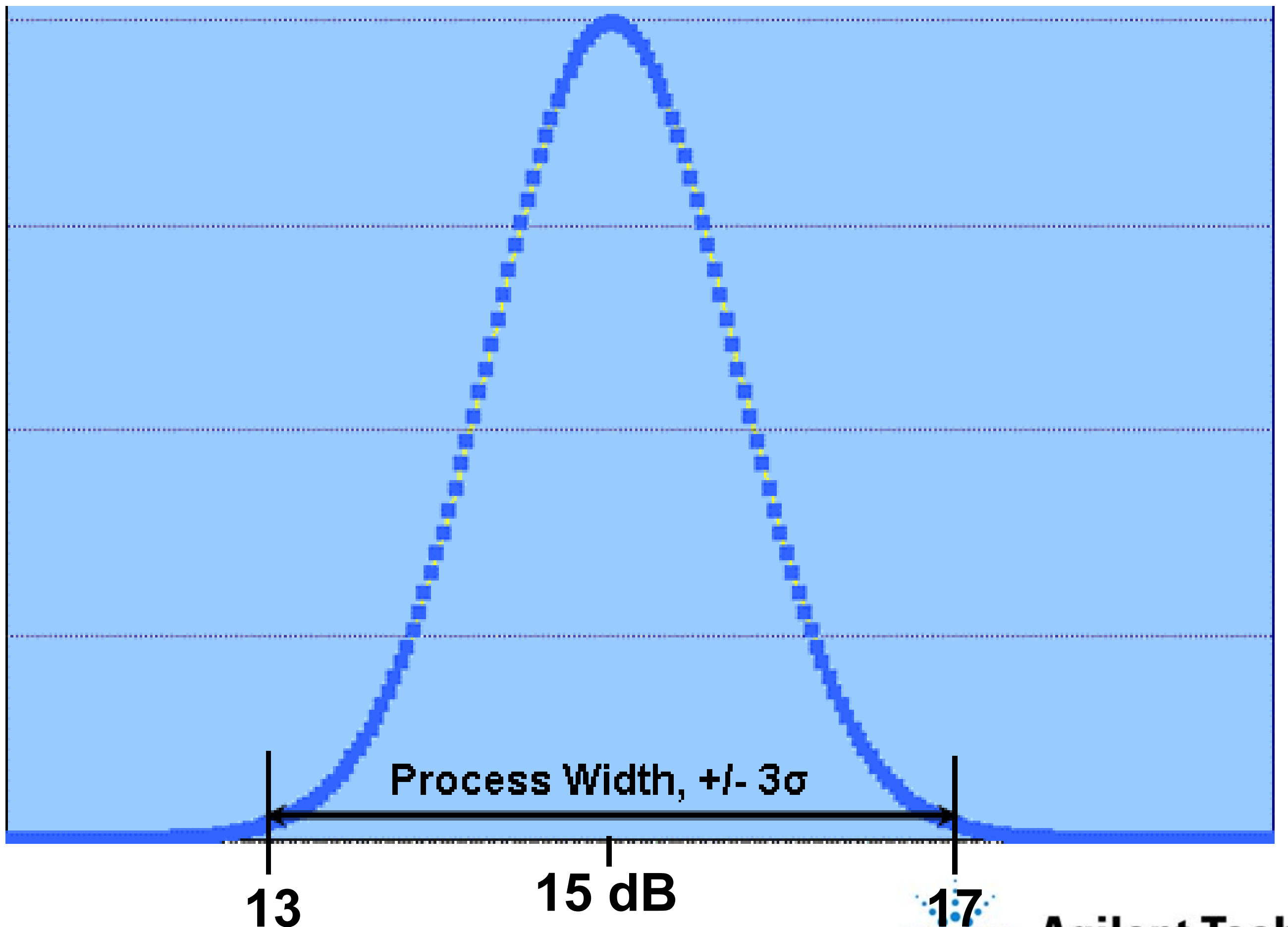


# Typical Process Yield Curve

**Example: Amplifier**

**Mean value of Gain = 15 dB**

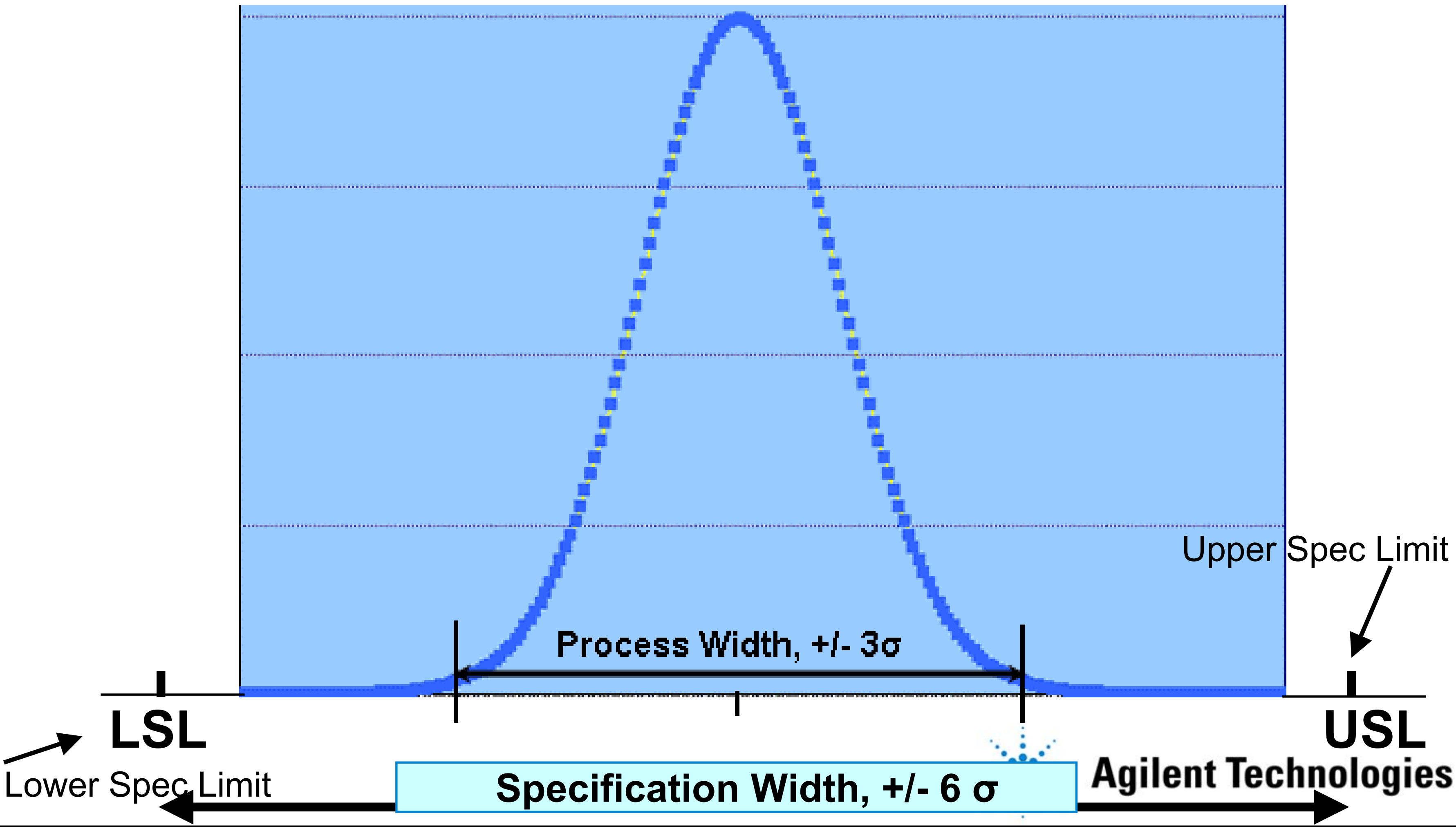
**Process Variation Result in a Normal Distribution Spread**



# Example of a Six Sigma Robust Design

Process Width = +/- 3 σ
Specs Width = +/- 6 σ

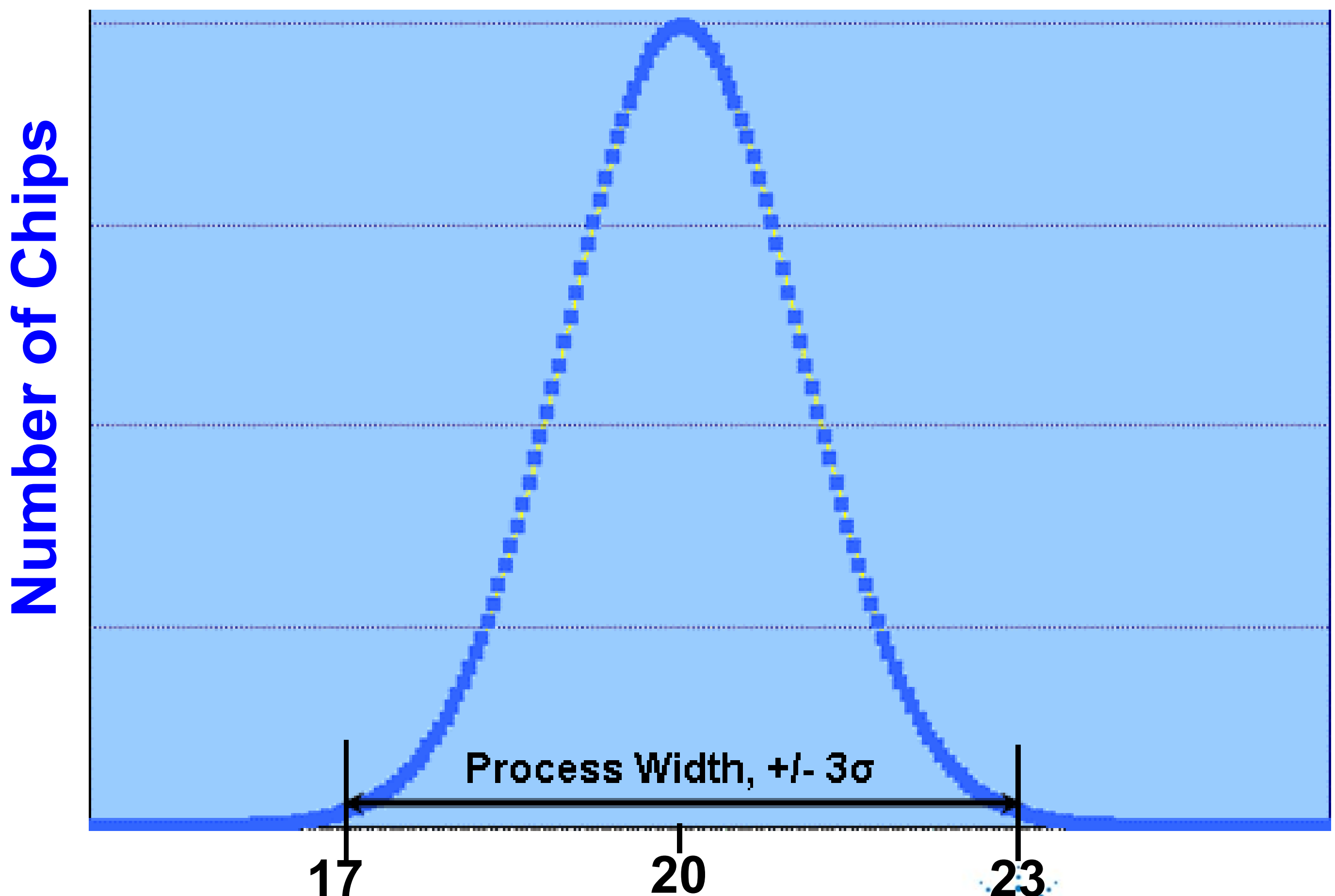
Cp= Process Capability Index
Cp= Spec Width / Process Width
Cp= (USL-LSL) / +/- 3 σ



# Example

**This curve could represent**

**a foundry's output of 100,000 Driver Amps with Gain=20 dB (+/- 3 σ = 6 dB)**



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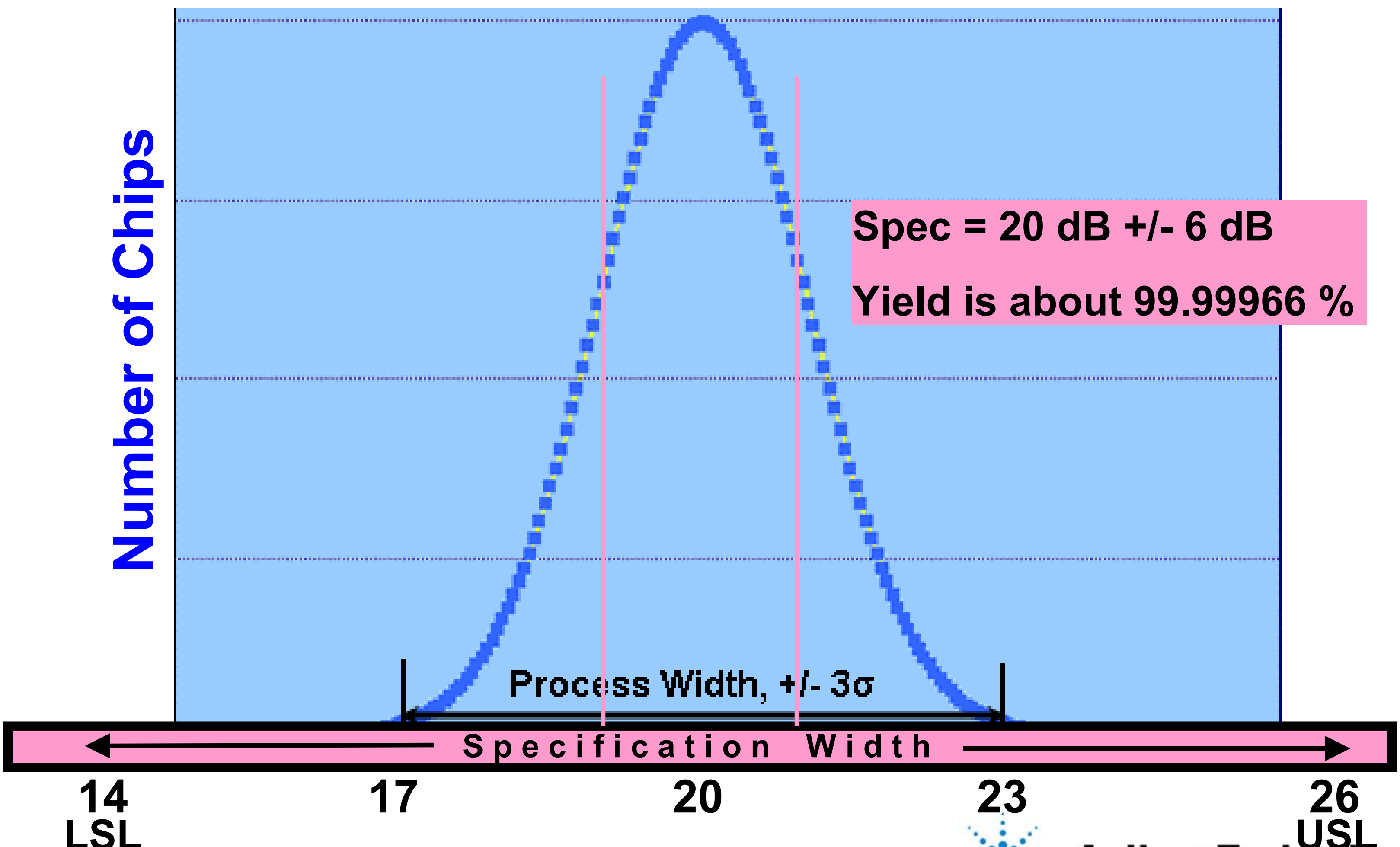
# Example – Six Sigma Design

100,000 Driver Amps with Gain=20 dB (+/- 3 σ = 6 dB)



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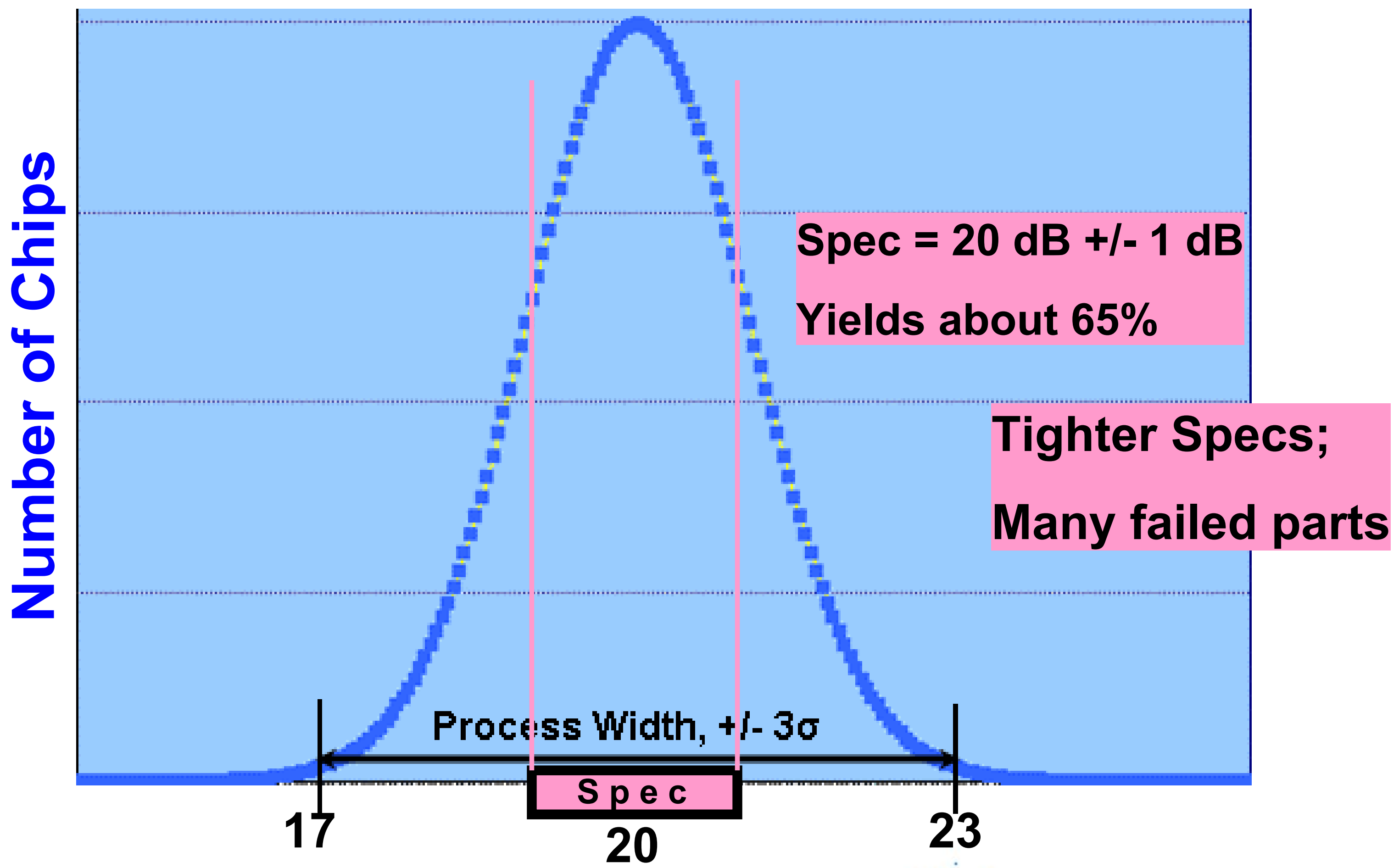
# Typical Process Yield Curve

**100,000 Power Amps with Gain=20 dB (+/- 3 σ = 6 dB)**



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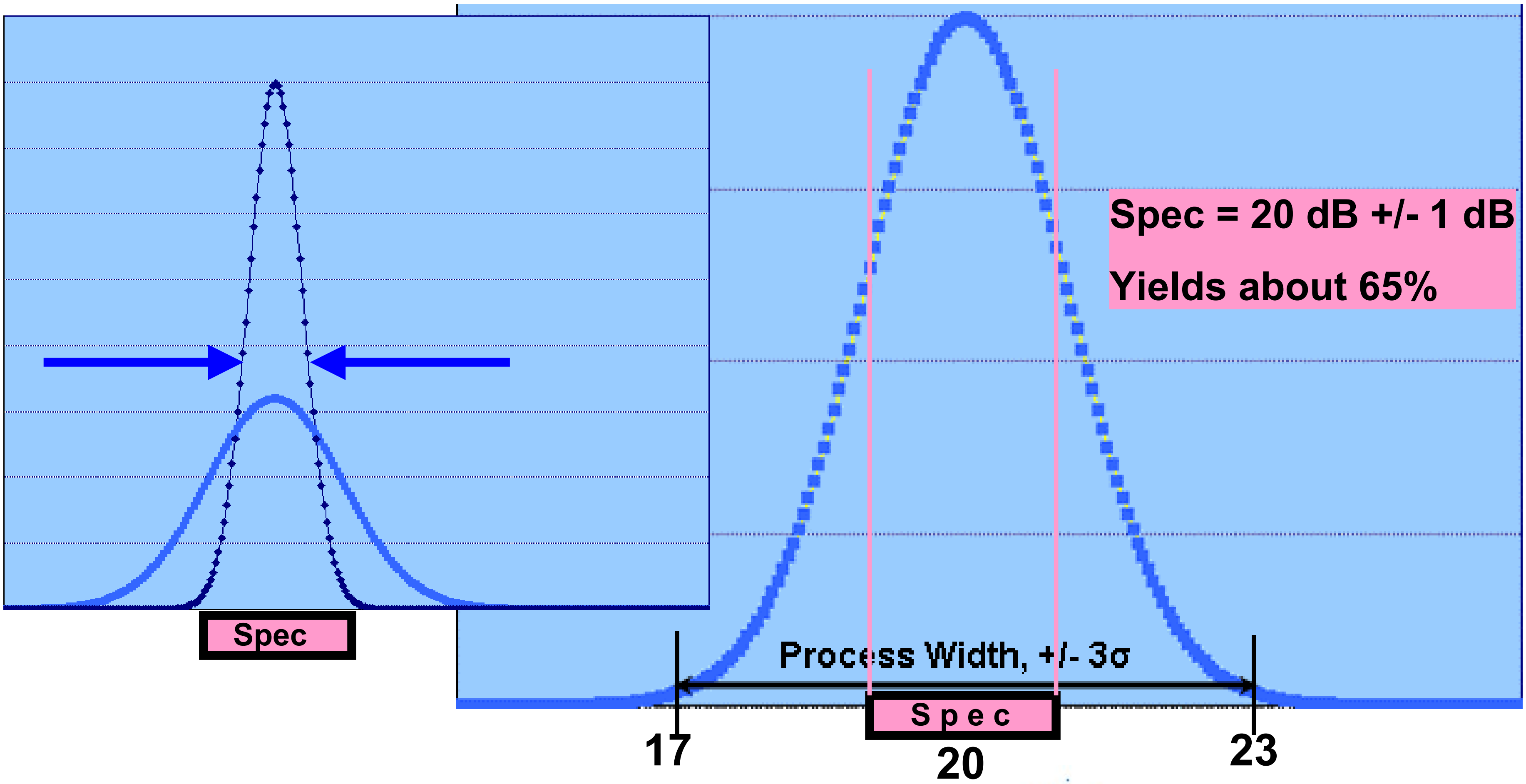
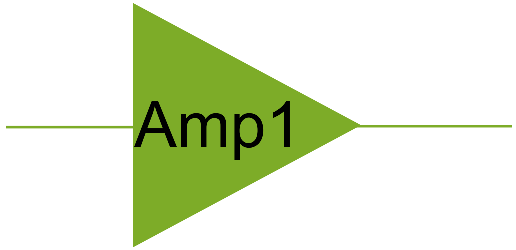
# Make the Process Yield Curve Narrower

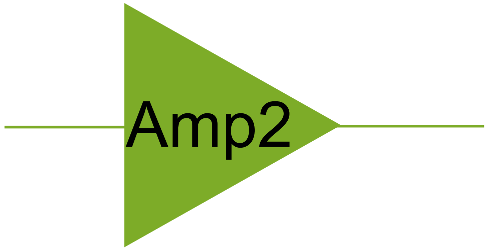
**100,000 Power Amps with Gain=20 dB (+/- 3 σ = 6 dB)**

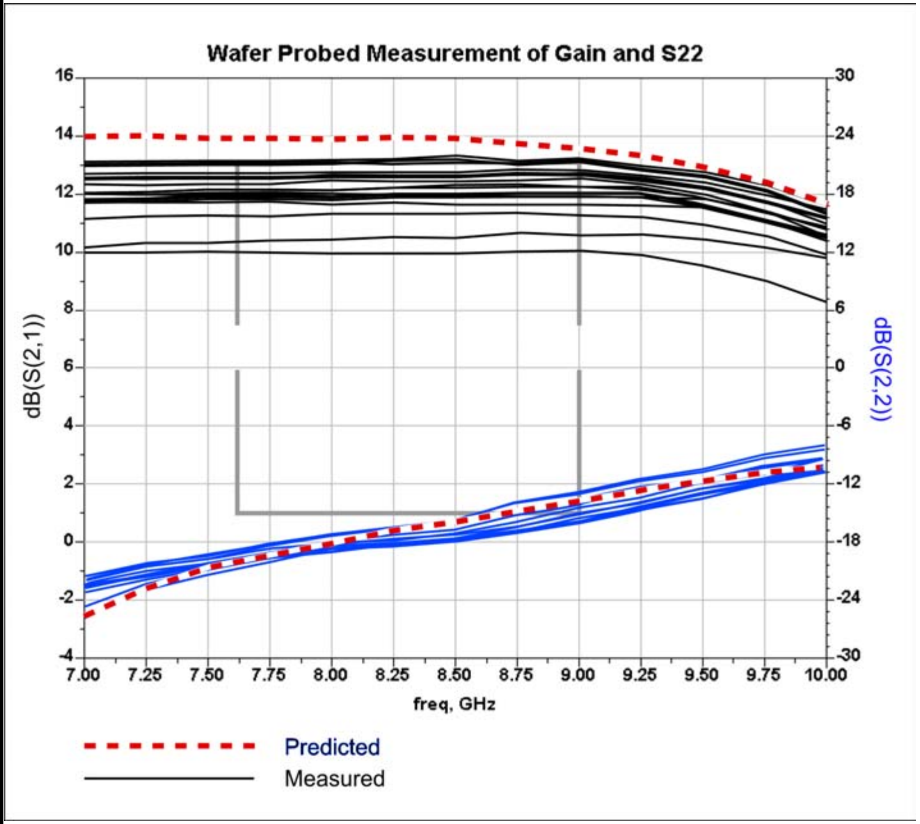
**Change Design to Yield Gain=20 dB (+/- 3 σ = 2 dB**

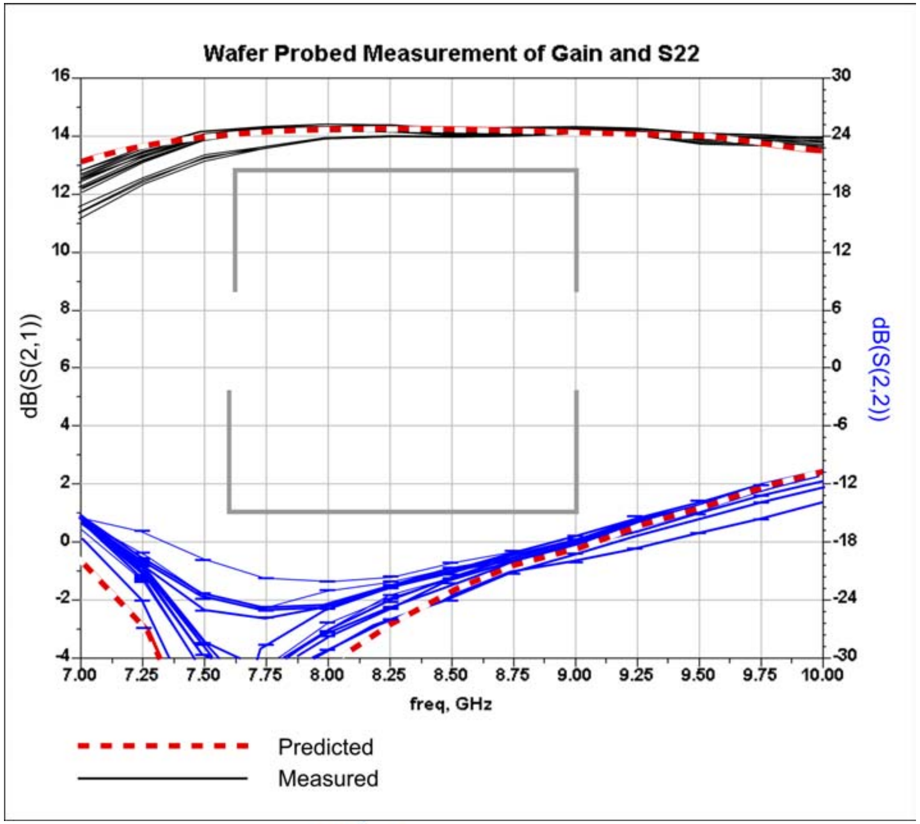


# Our Goal is to Create Something like Amp2

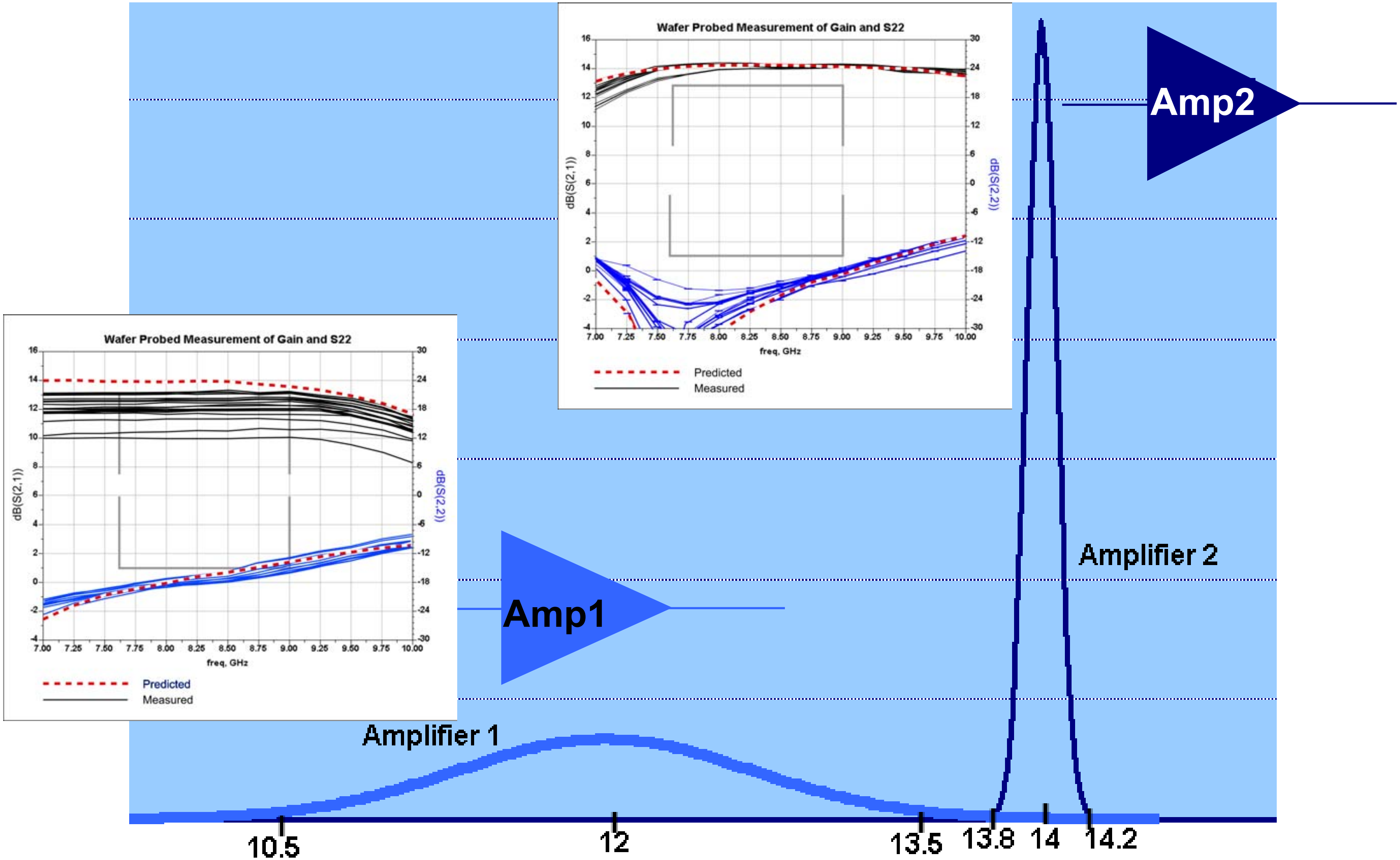


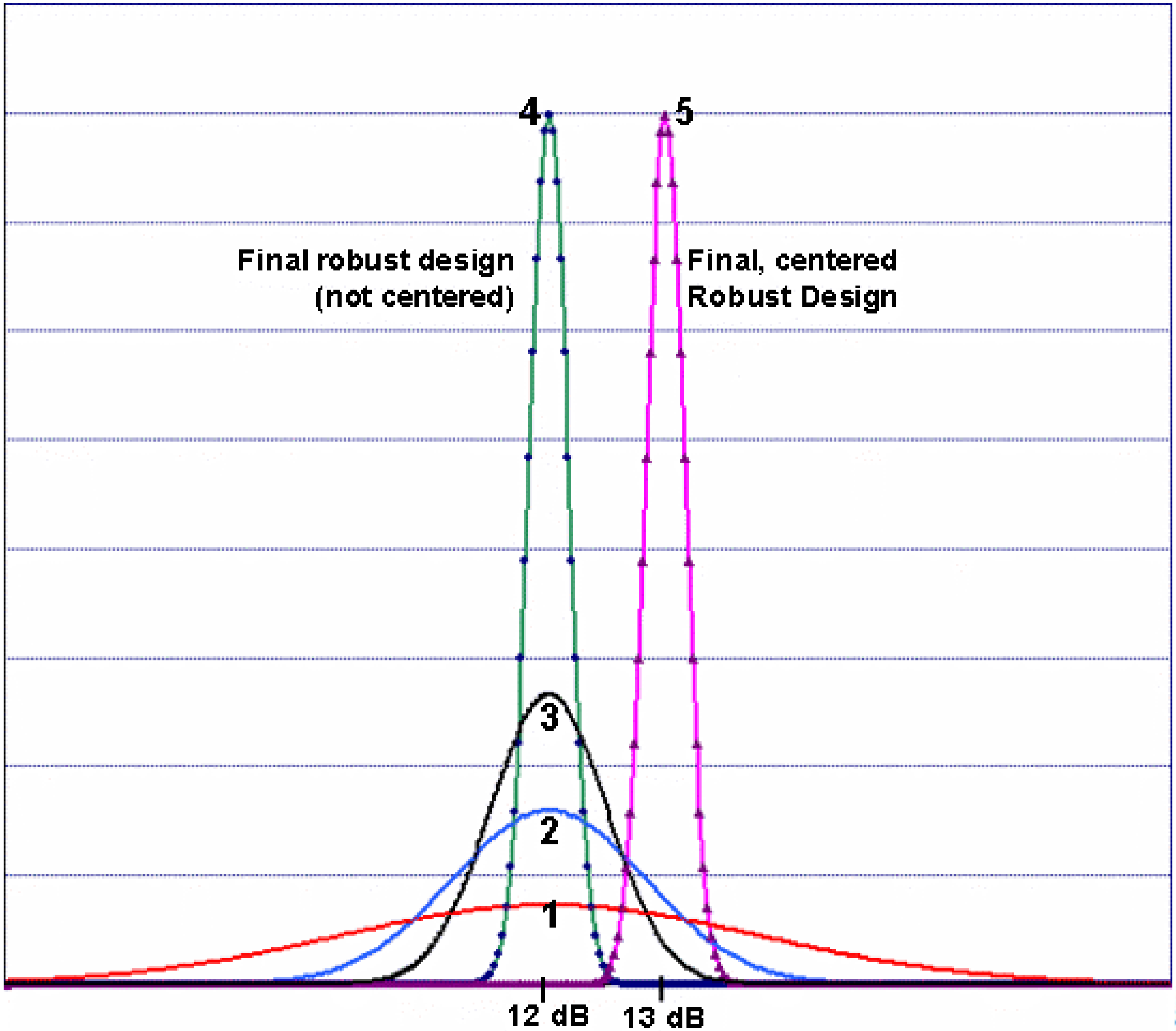



# Amp1 & Amp2 "Yield Distributions"



# The DFY Process



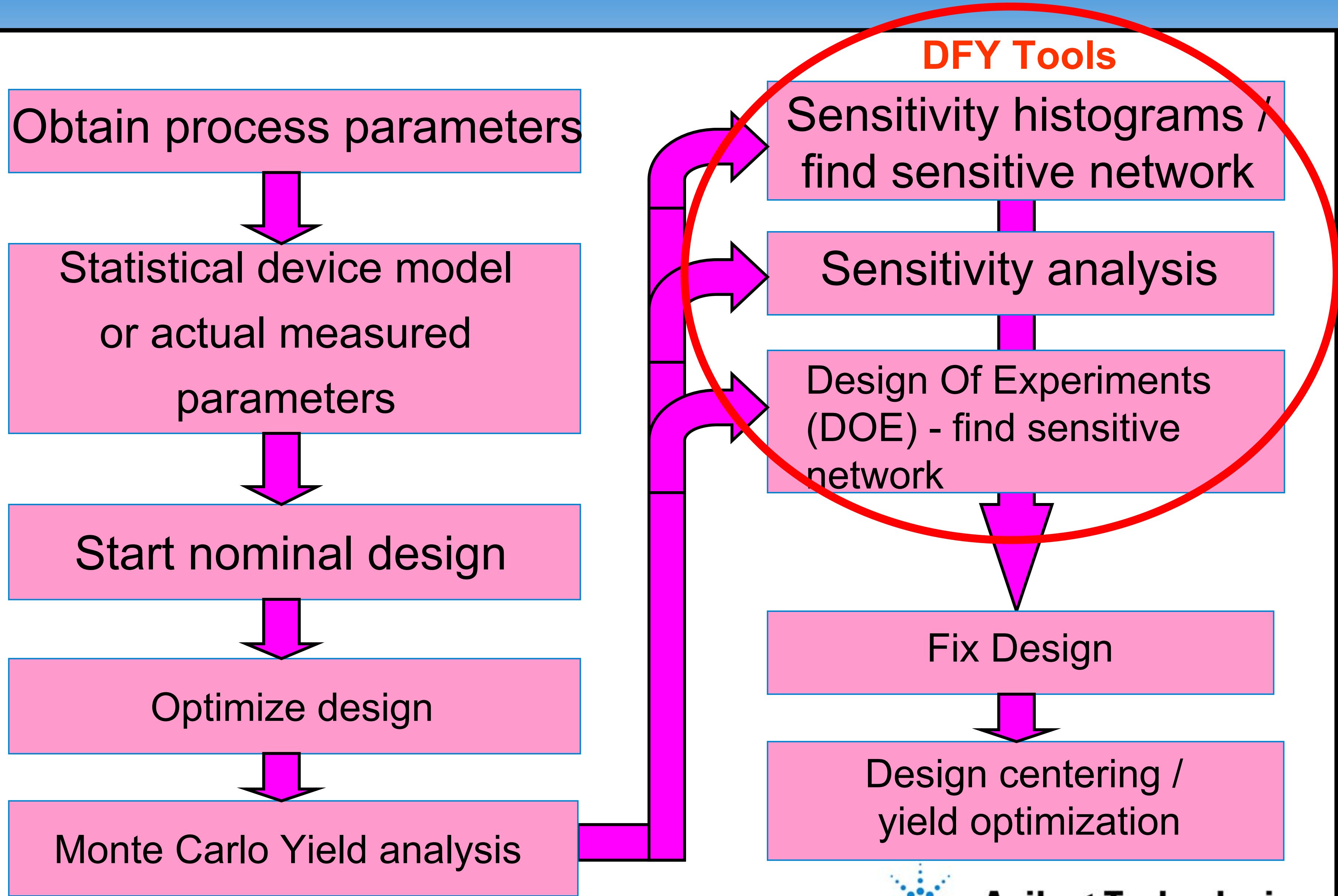

**Curve 1**
**Original Design**

**Curves 2,3**
**Fixing the Design to achieve Robustness**

**Curves 4**
**Further improvement towards achieving Robustness**

**Curve 5**
**Final Shift the Response by Design Centering to meet Specs.**

# The DFY Process for MMIC



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# Yield Sensitivity Histograms (YSH)

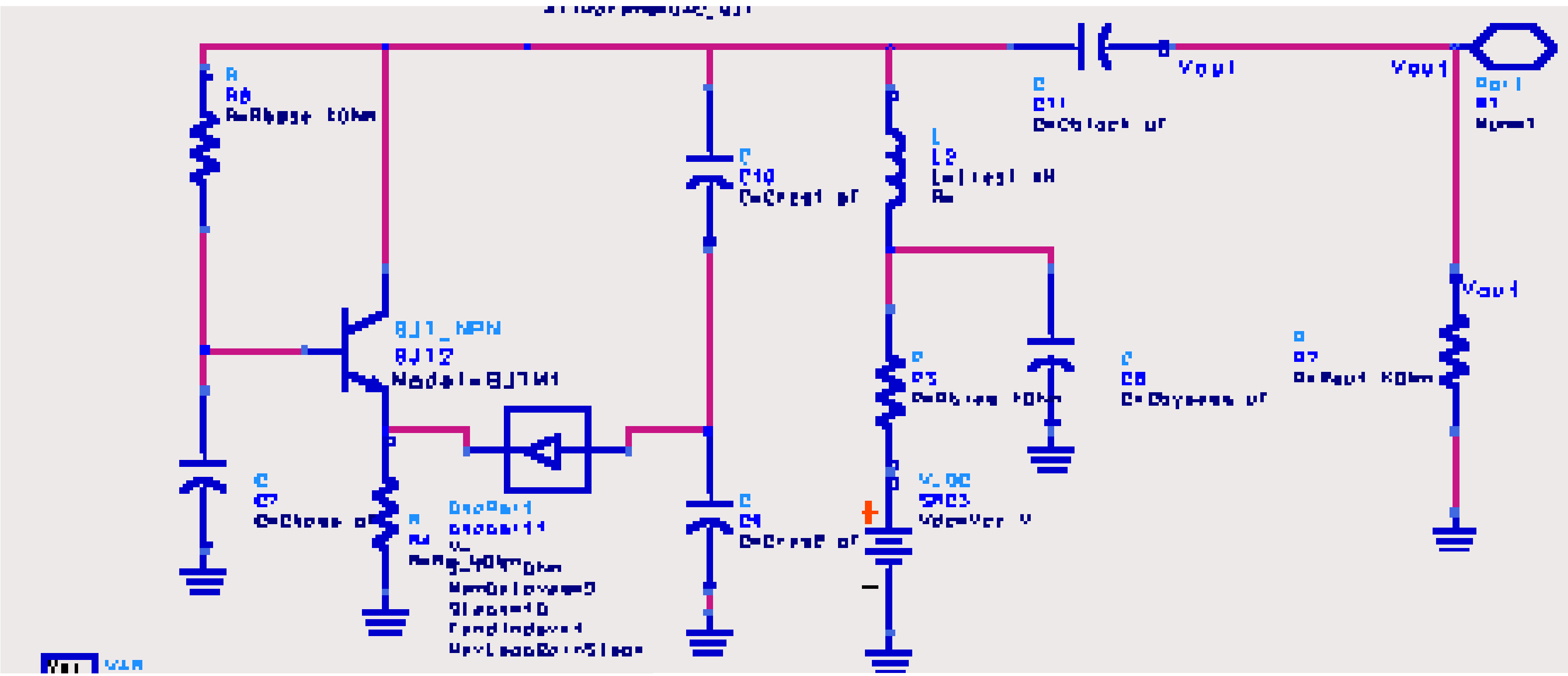
Yield analysis Data are post processed via built-in AEL Expressions to extract and display YSH results and more…

YSH display yield with respect to each element variation.

YSH provide insight to how sensitive the design is with respect to each of the design's elements.

YSH help designers to pinpoint the sensitive **RED X** parts in their designs. As a result, designers make decision to replace these parts with "tighter tolerance parts" in Board application (OR) create "less sensitive matching networks" in IC designs.

# Example: VCO Design



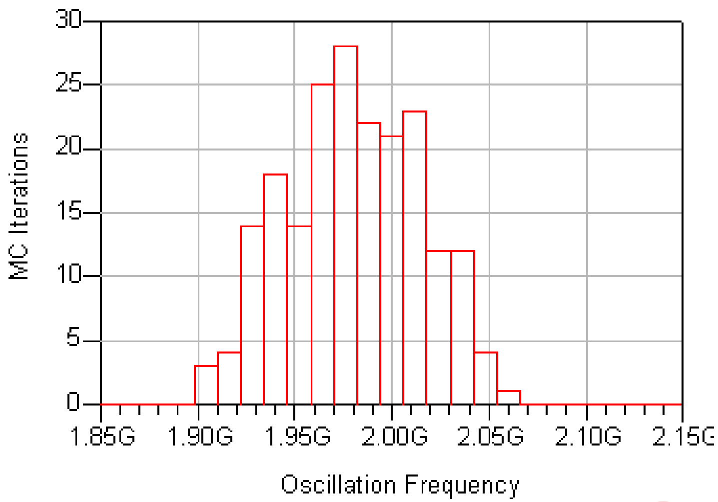

Statistical Analysis of Oscillator Performance
- 21 measured BFQ67 transistors
- 5% uniform variation in lumped component values

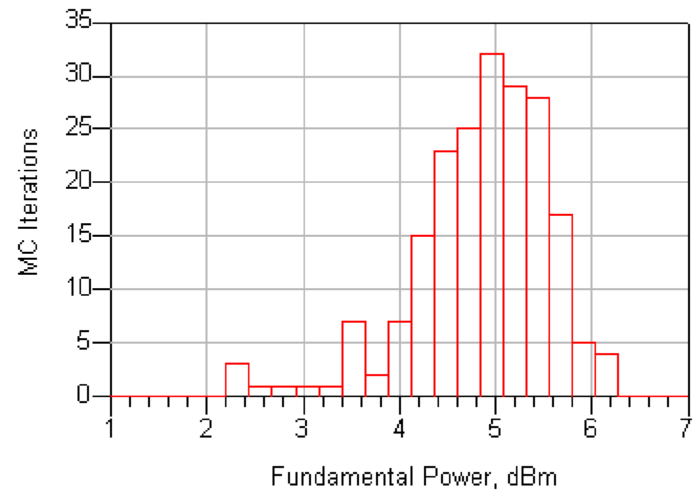
**Specs**

**Pout > 4dBm**
**P_Noise < - 85 dBc @ 10 KHz**
**1975 MHz < Freq_Osc < 2025 MHz**

# VCO – Yield after Optimization – 37.5 %

Statistical Analysis of Oscillator Performance
- 21 measured BFQ67 transistors
- 5% uniform variation in lumped component values

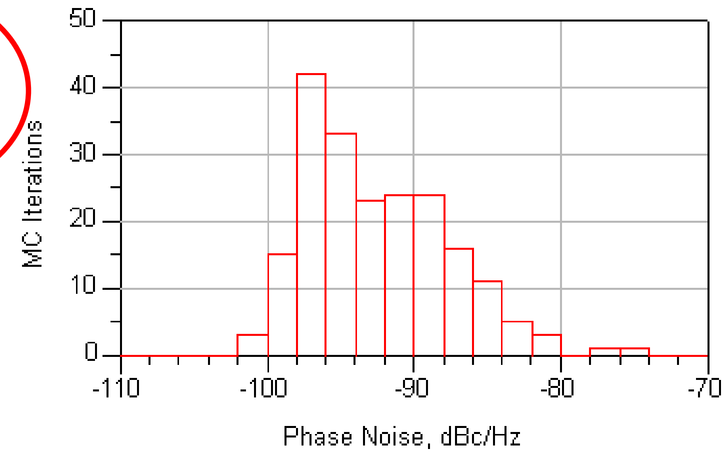


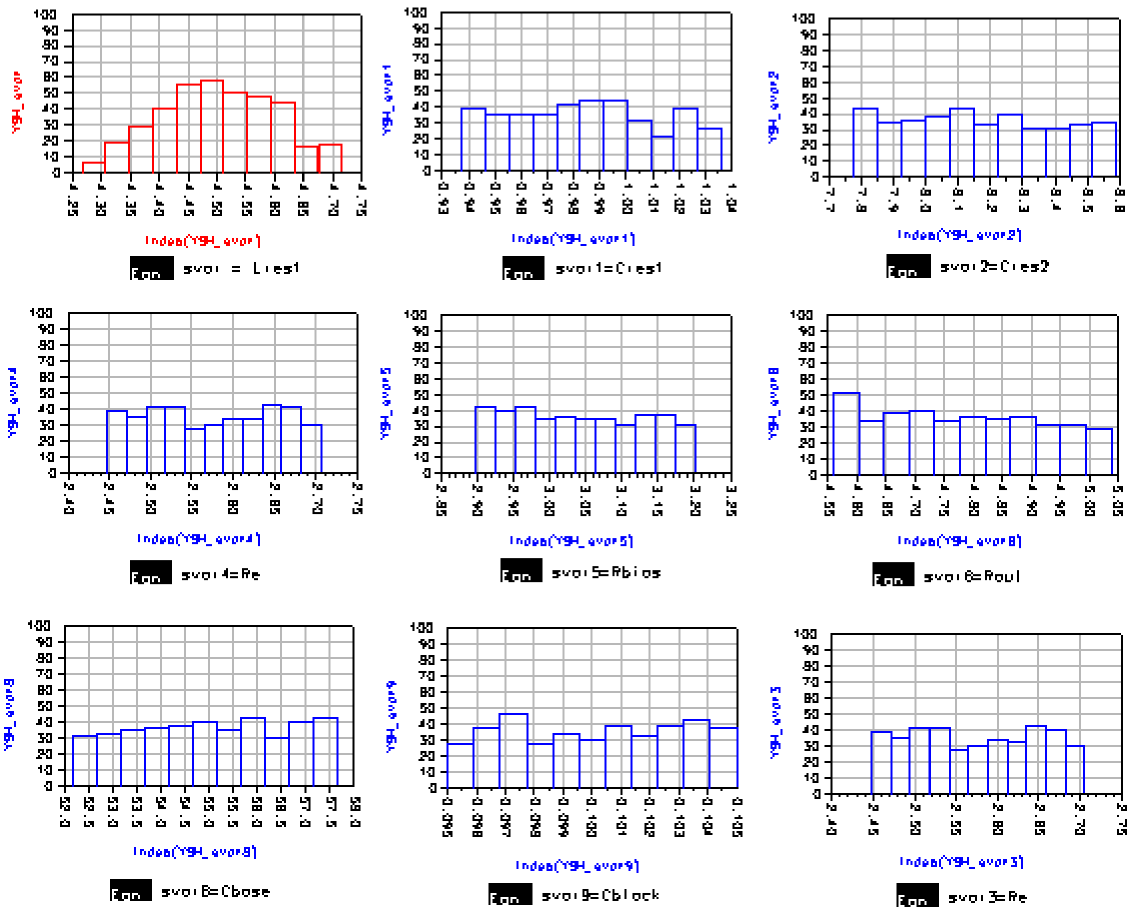

| NumFail | NumPass | Yield |
|---|---|---|
| 125.000 | 75.000 | 37.500 |

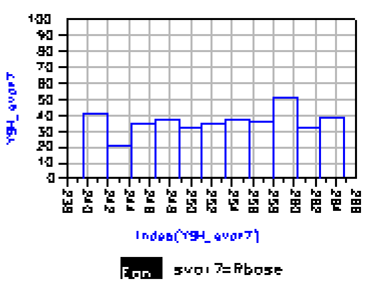
Number of Monte Carlo iterations that failed to produce an oscillation

| NOOSC |
|---|
| 0 |



# VCO – Yield Sensitivity Histograms




Eqn Spec1_spec_Min = 20

Eqn Spec1_spec_Max = 25

Eqn Spec2_spec_Min = 1975

Eqn Spec2_spec_Max=2025

Eqn Spec3_spec_Min=-200

Eqn Spec3_spec_Max=-85

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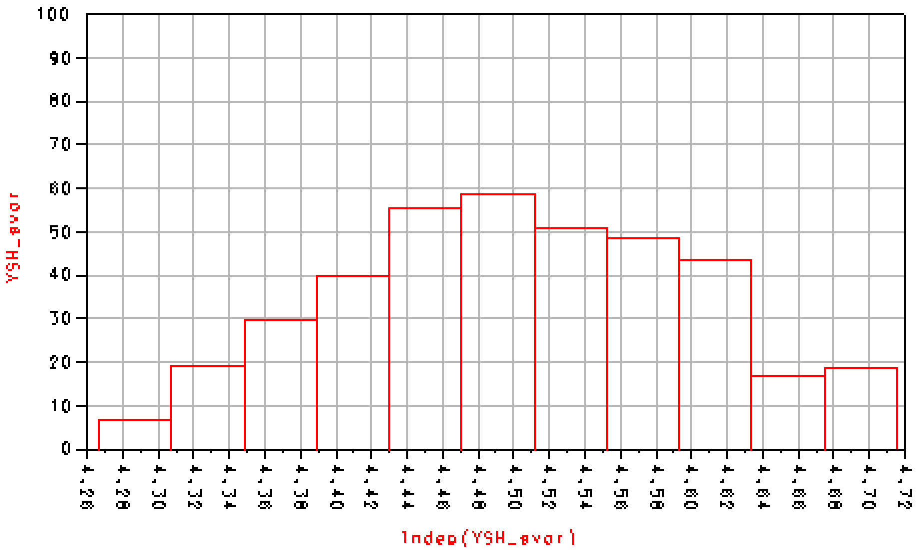
# VCO – Yield Sensitivity Histogram for Lres1

Eqn pf_Total = pf_Spec2_svar * pf_Spec1_svar * pf_Spec3_svar

Eqn YSH_svar = yield_sens(pf_Total, 11)

Change "pf_Total" to "pf_Spec2_svar" if you like to see the sensitivity versus Spec2 (which is the frequency spec).




**RED X component**

Eqn svar = Lres1

Change the name of component to see the yield sensitivity versus the component tolerance.

Eqn Spec1_vs_svar=vs( mean(Spec1), svar)

Eqn pf_Spec1_svar=if ( Spec1_vs_svar > Spec1_spec_Max || Spec1_vs_svar < Spec1_spec_Min ) then 0.0 else 1.0

Eqn Spec1_spec_Min = 20 Eqn Spec1_spec_Max = 25

Change the specs and the yield updates automatically

Eqn Spec2_vs_svar = vs( mean(Spec2), svar)

Eqn pf_Spec2_svar = if ( Spec2_vs_svar > Spec2_spec_Max || Spec2_vs_svar < Spec2_spec_Min ) then 0.0 else 1.0

Eqn Spec2_spec_Min = 1975 Eqn Spec2_spec_Max=2025

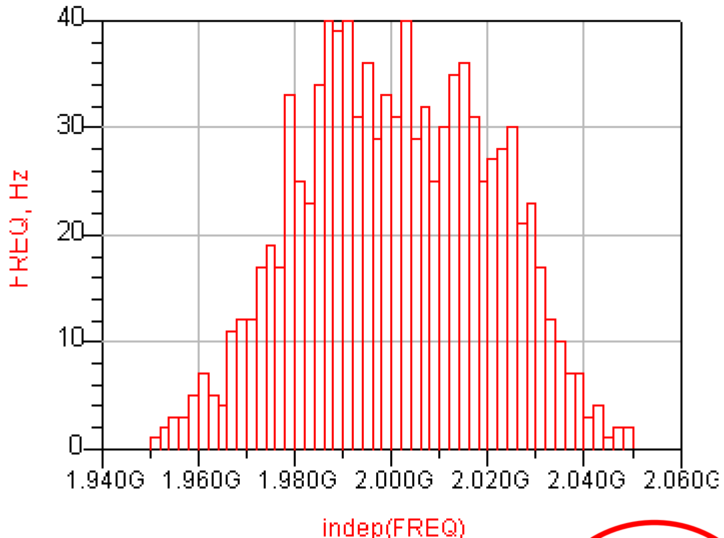
Eqn Spec3_vs_svar=vs( mean(Spec3), svar)

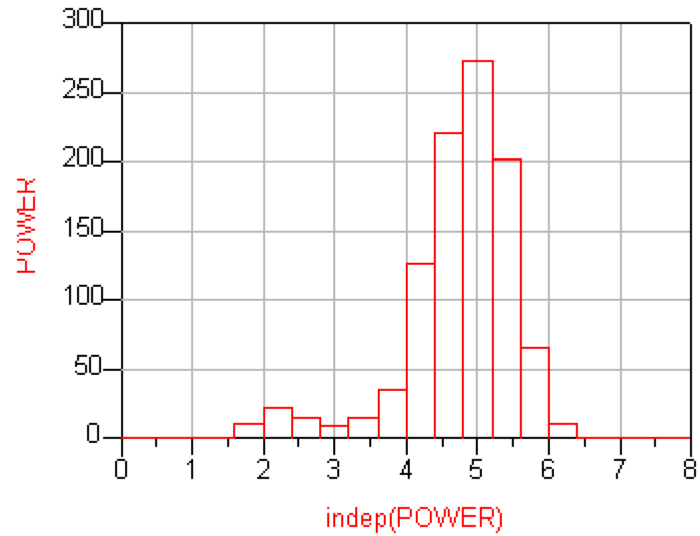
Eqn pf_Spec3_svar=if ( Spec3_vs_svar > Spec3_spec_Max || Spec3_vs_svar < Spec3_spec_Min ) then 0.0 else 1.0

Eqn Spec3_spec_Min=-200 Eqn Spec3_spec_Max=-85

# Higher Yield by controlling Lres1 +/- 1%

Statistical Analysis of Oscillator Performance
- 21 measured BFQ67 transistors
- 5% uniform variation in lumped component values

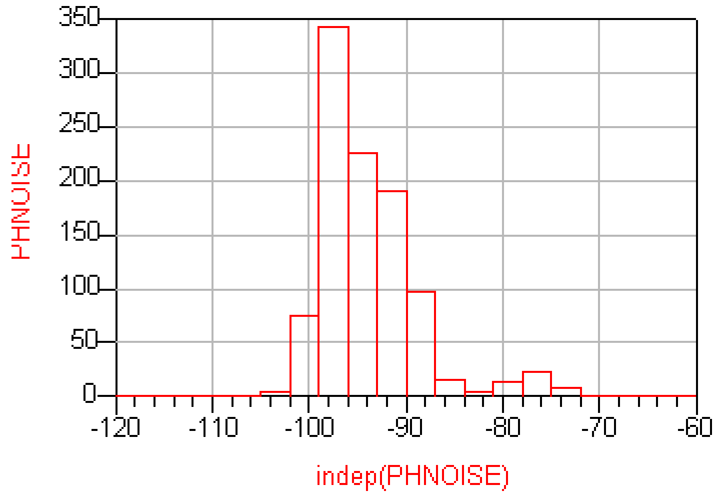


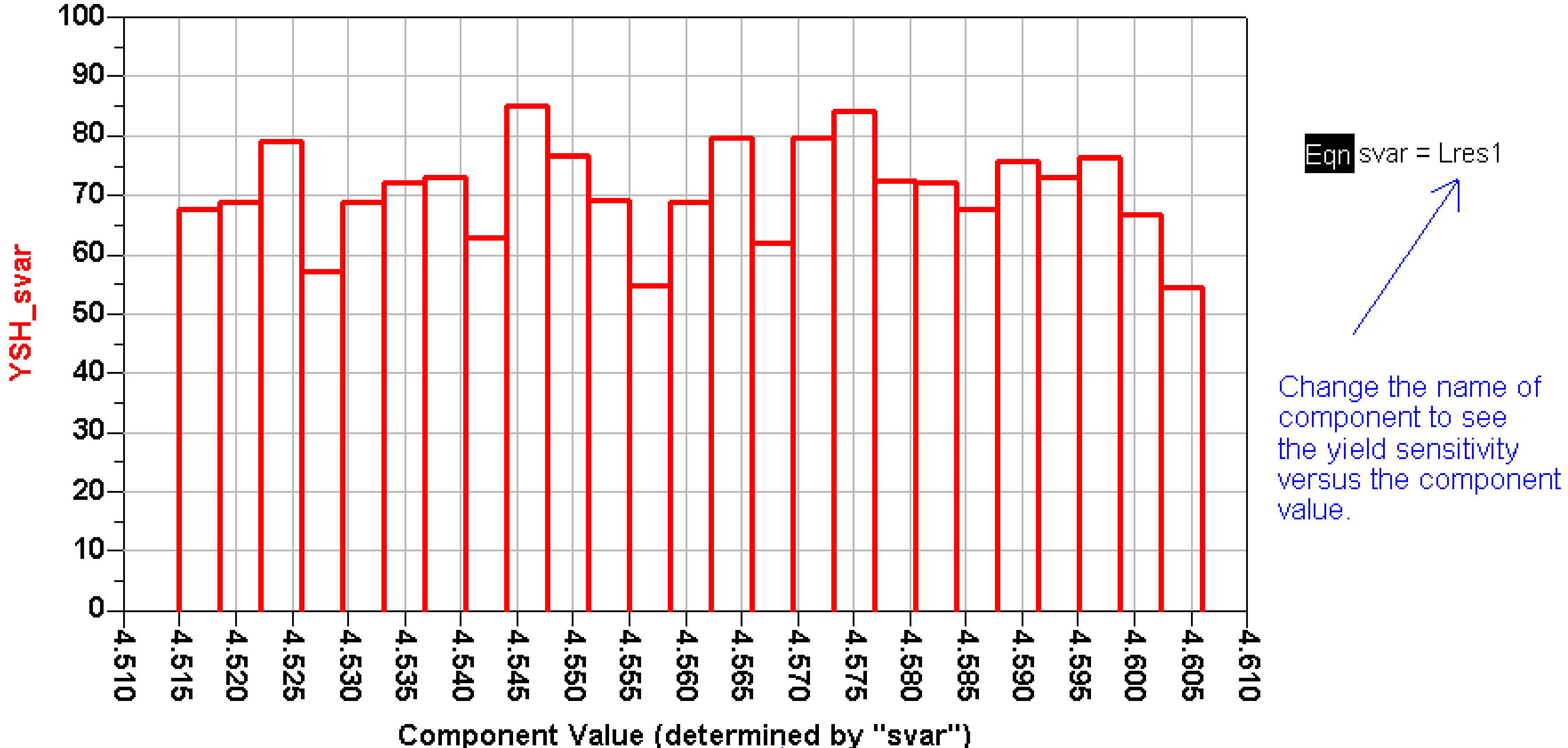

| NumFail | NumPass | Yield |
| --- | --- | --- |
| 296.000 | 704.000 | 70.400 |

Number of Monte Carlo
iterations that failed
to produce an oscillation

| ...OSC |
| --- |
| 0 |



# Yield Sensitivity Histogram of controlled “Lres1”




**L_nom = 4.560 nh +/- 1%**



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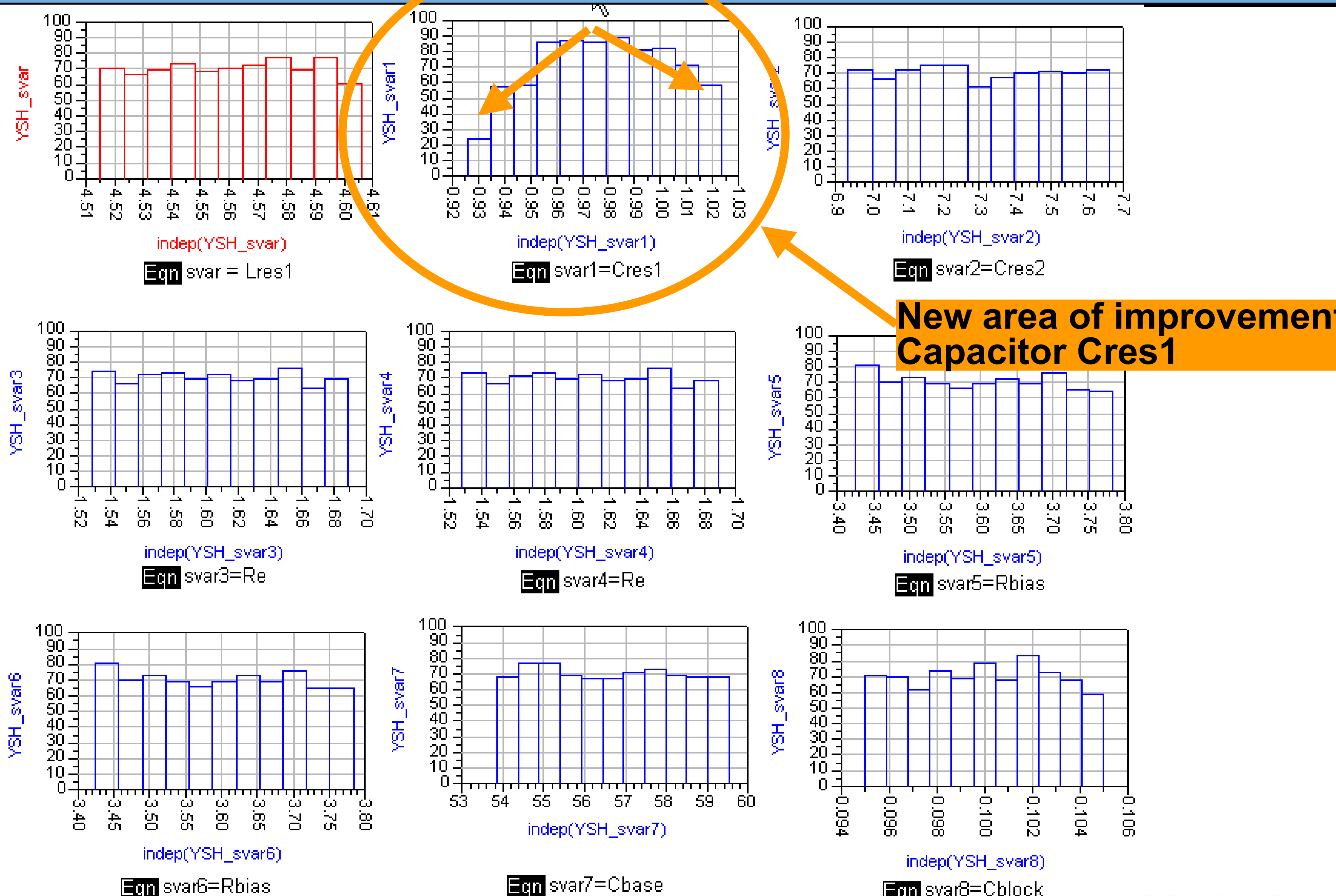
# Notice now Cres1 has negative effect on Yield



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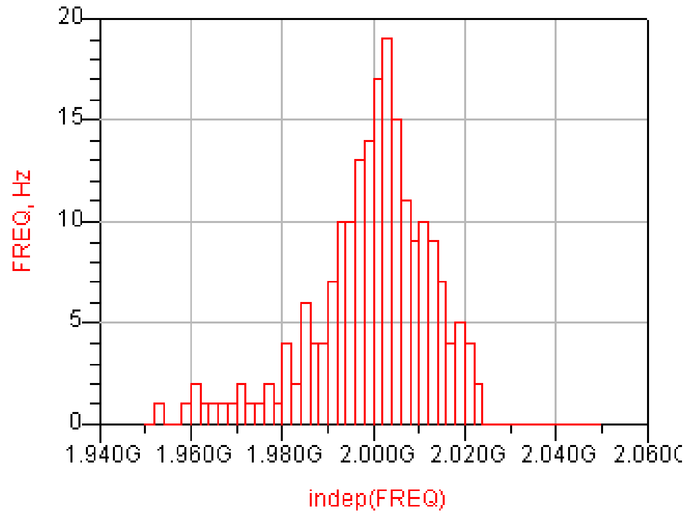
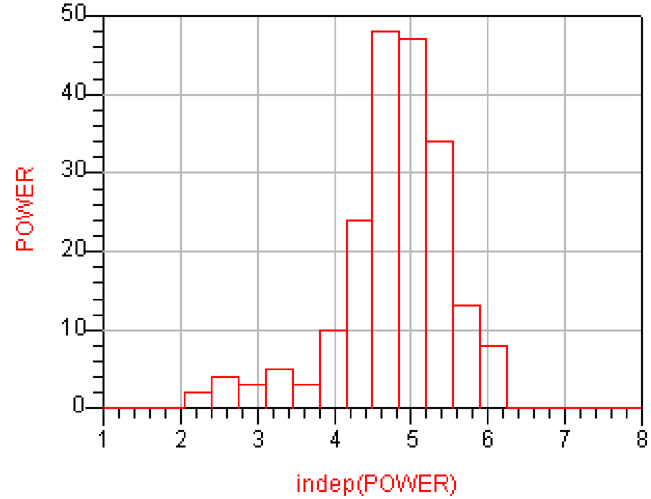
# Controlling Cres1 increase the Yield to 90%

Statistical Analysis of Oscillator Performance
- 21 measured BFQ67 transistors
- 5% uniform variation in lumped component values

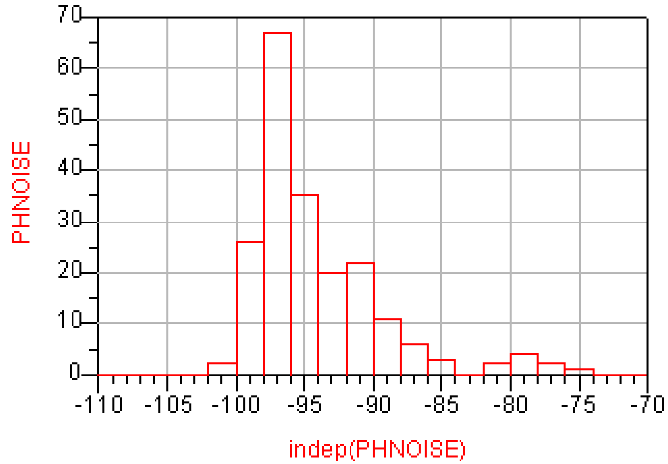


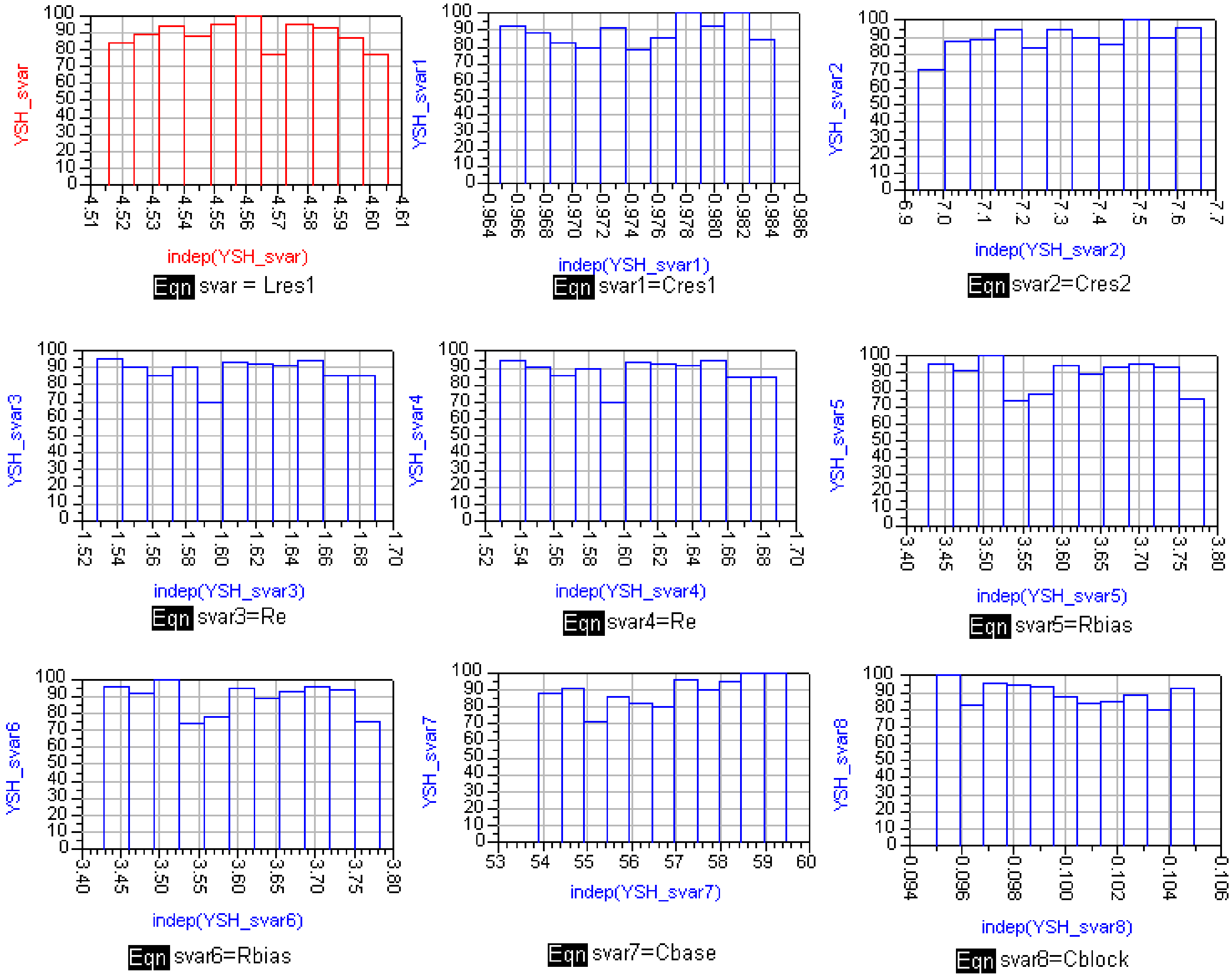

| NumFail | NumPass | Yield |
|---|---|---|
| 22.000 | 178.000 | 89.000 |

Number of Monte Carlo iterations that failed to produce an oscillation

| ...OSC |
|---|
| 0 |



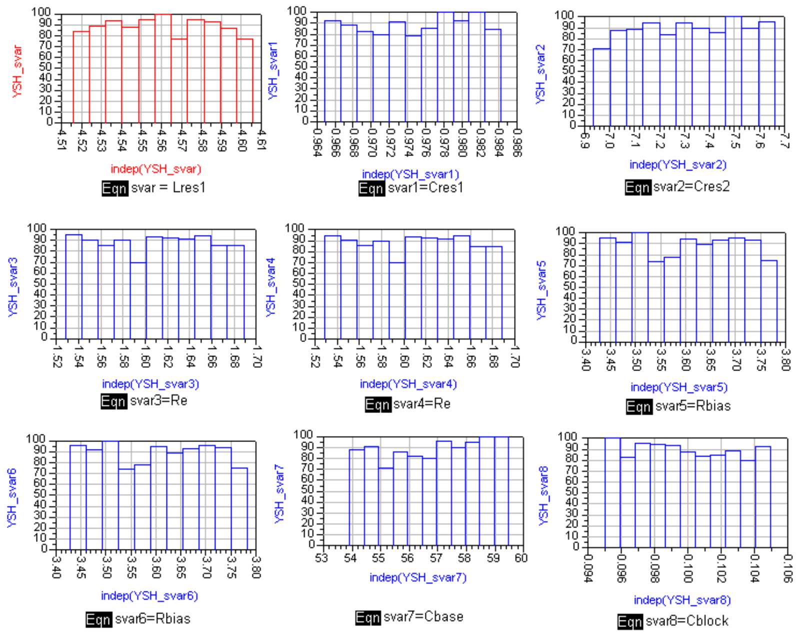
# Now we don't see any more "Red X" components



# What we Learned from this VCO Example

**Yield Sensitivity Histograms (YSH) helped us pin point the source of the yield problem in the design**

**YSH are generated using Post Processing of Monte Carlo Yield analysis data.**



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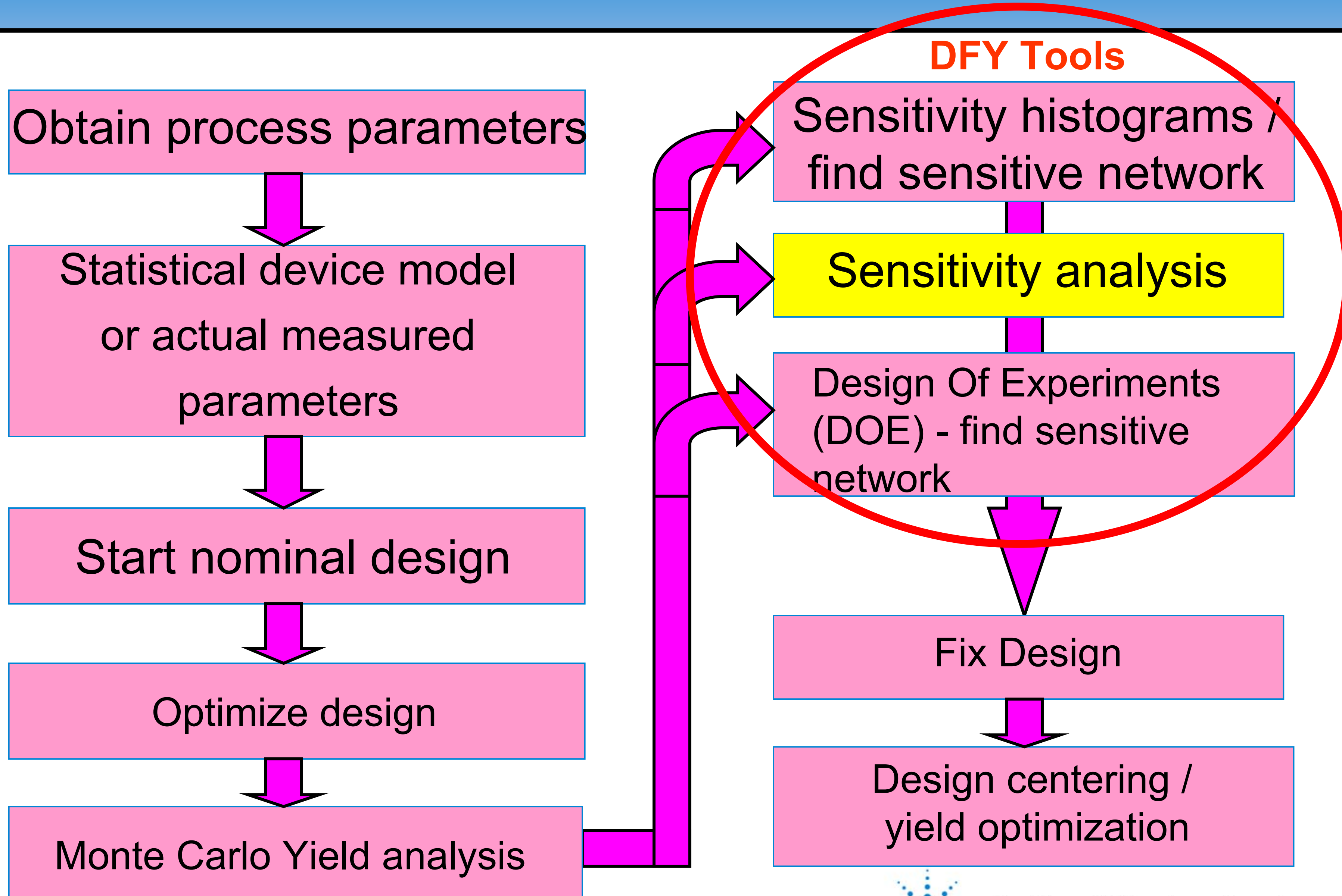
# The DFY Process for MMIC



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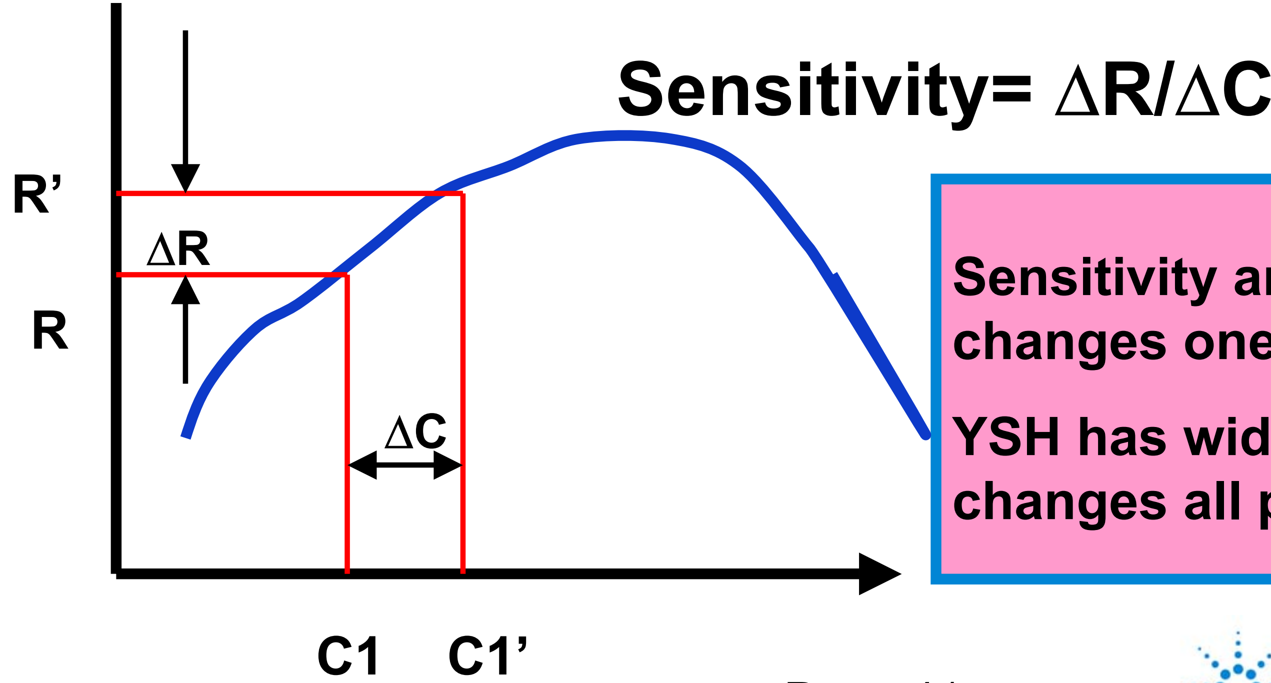
# Sensitivity Analysis – How does it work?

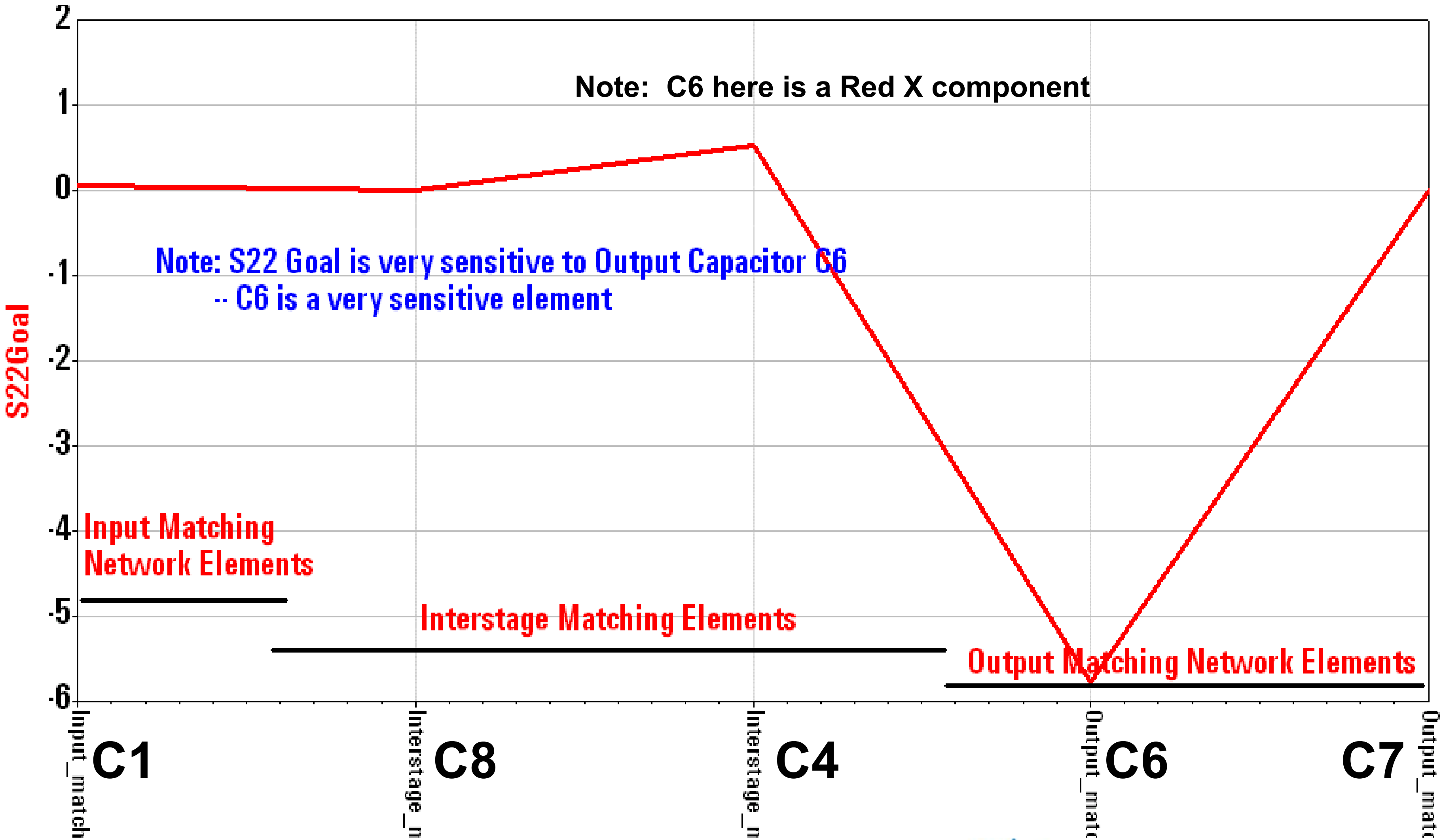
- Change the part's nominal value by 1e-6 and monitor the change in the response (R).
- Example for capacitor, C1 with response R
- Perturb C1 by a small delta:  C1' = C1(1+1e-6)



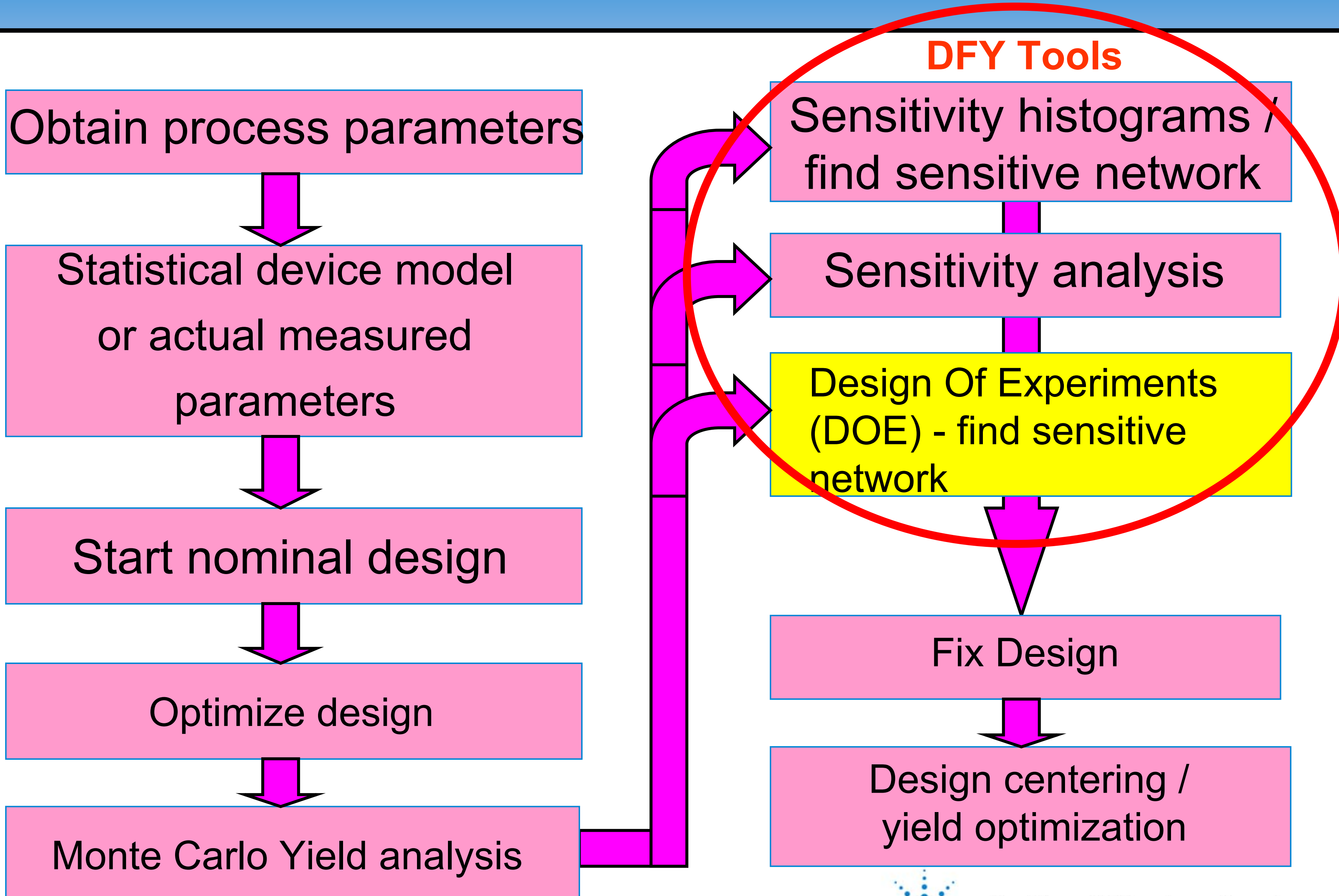

Sensitivity analysis is local.  It changes one part at a time.

YSH has wider variation and changes all parts together.

# Sensitivity of S22 to all Capacitors



# The DFY Process for MMIC



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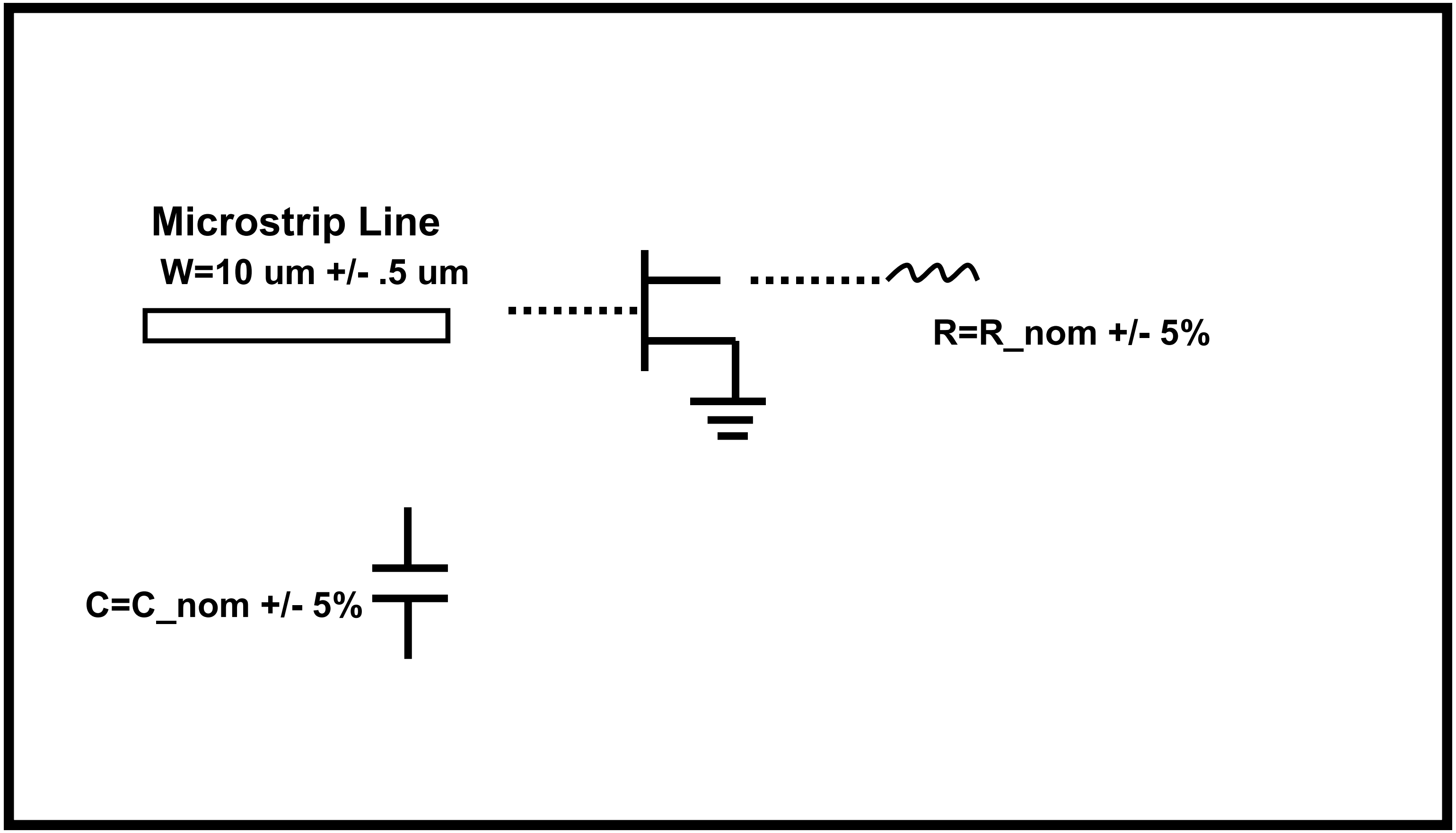
# A Brief Tutorial on Design of Experiments (DOE)

# DOE – A Brief Tutorial – 3 elements MMIC



# DOE – A Brief Tutorial

**Start by choosing variables that affect the response**

**<u>Choose three variables with their +1 and -1 :</u>**

| | |
|---|---|
| **Width of lines (W)** | **W=W_nom ± .5 um** |
| **Resistors (R)** | **R= R_nom ± 5%** |
| **Capacitors (C)** | **C= C_nom ± 5%** |

**Example: For a 10u wide line, W=10 um**

**-1 corresponds to 9.5 um**

**+1 corresponds to 10.5 um**

**0 corresponds to nominal value, 10um**

# Main Effect of Capacitors, C on Gain

| W | R | C | Gain |
|---|---|---|---|
| | | | |
| -1 | -1 | -1 | 12.85 |
| 1 | -1 | -1 | 13.01 |
| -1 | 1 | -1 | 14.52 |
| 1 | 1 | -1 | 14.71 |
| -1 | -1 | 1 | 12.93 |
| 1 | -1 | 1 | 13.09 |
| -1 | 1 | 1 | 14.61 |
| 1 | 1 | 1 | 14.81 |

**Average gain for C=-1**

**13.7725 dB (yellow)**

**Average gain for C=1**

**13.86 dB (blue)**

**Slope= .044**

# Main Effect of Resistors, R on Gain

| W | R | C | Gain |
|---|---|---|---|
| | | | |
| -1 | -1 | -1 | 12.85 |
| 1 | -1 | -1 | 13.01 |
| -1 | 1 | -1 | 14.52 |
| 1 | 1 | -1 | 14.71 |
| -1 | -1 | 1 | 12.93 |
| 1 | -1 | 1 | 13.09 |
| -1 | 1 | 1 | 14.61 |
| 1 | 1 | 1 | 14.81 |

**Average gain for R=-1**

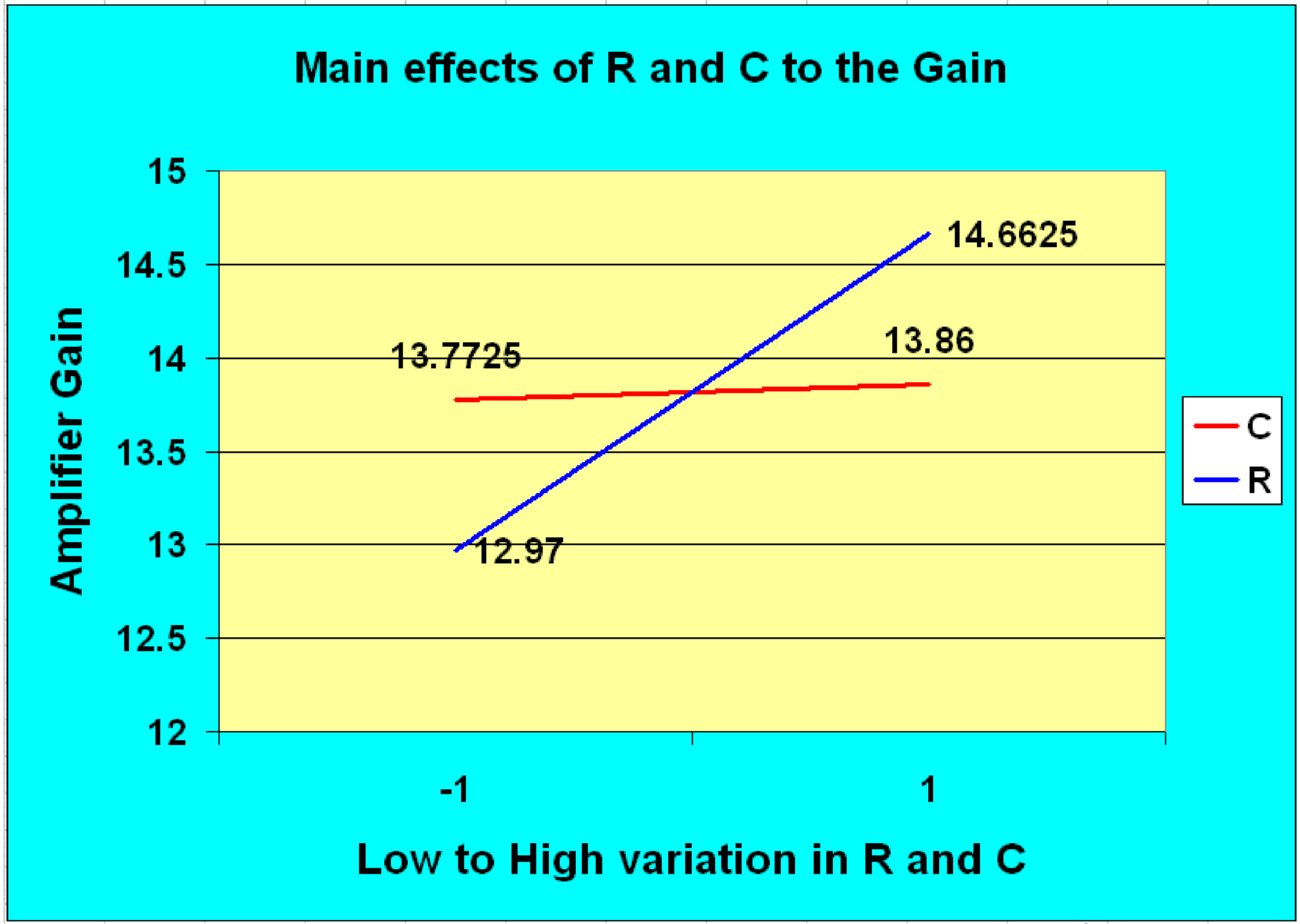
**12.97 dB (blue)**

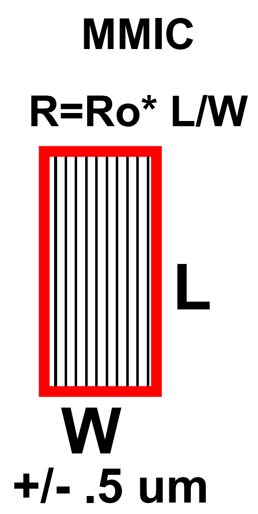
**Average gain for R=1**

**14.6625 dB (green)**

**Slope = .85**

# Plotting Main Effects of C and R




Increasing W reduces the Sensitivity



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# Interaction Effect of (W and R) on Gain

| W | R | C | Gain |
|---|---|---|---|
| | | | |
| -1 | -1 | -1 | 12.85 |
| 1 | -1 | -1 | 13.01 |
| -1 | 1 | -1 | 14.52 |
| 1 | 1 | -1 | 14.71 |
| -1 | -1 | 1 | 12.93 |
| 1 | -1 | 1 | 13.09 |
| -1 | 1 | 1 | 14.61 |
| 1 | 1 | 1 | 14.81 |

**Average gain for W*R=-1**

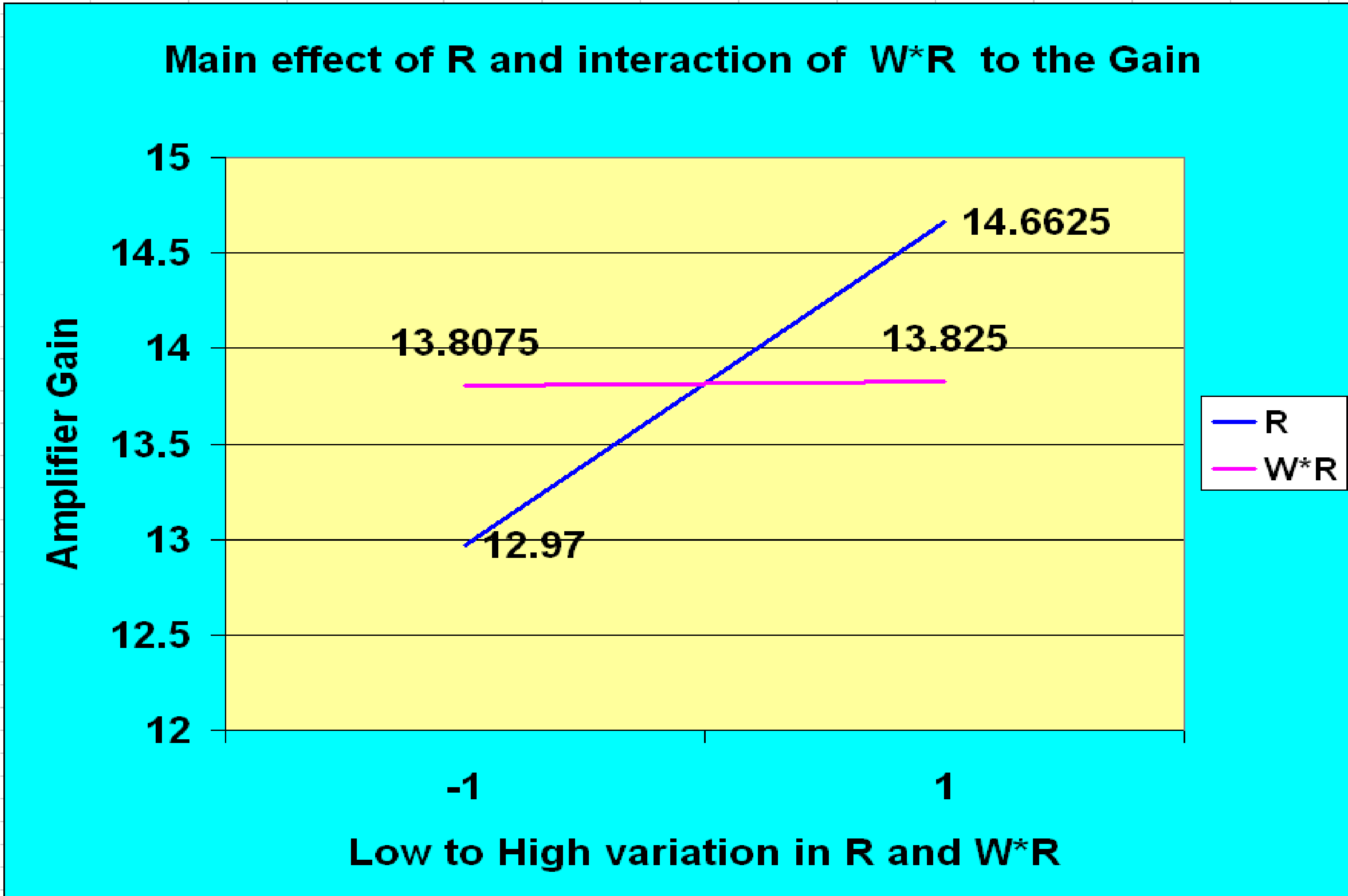
**13.8075 dB (blue)**

**Average gain for W*R=1**

**13.825 dB (pink)**

**Slope = .0088**

# Plotting Interaction Effects of W and R



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# Obtaining the Rest of the Coefficients

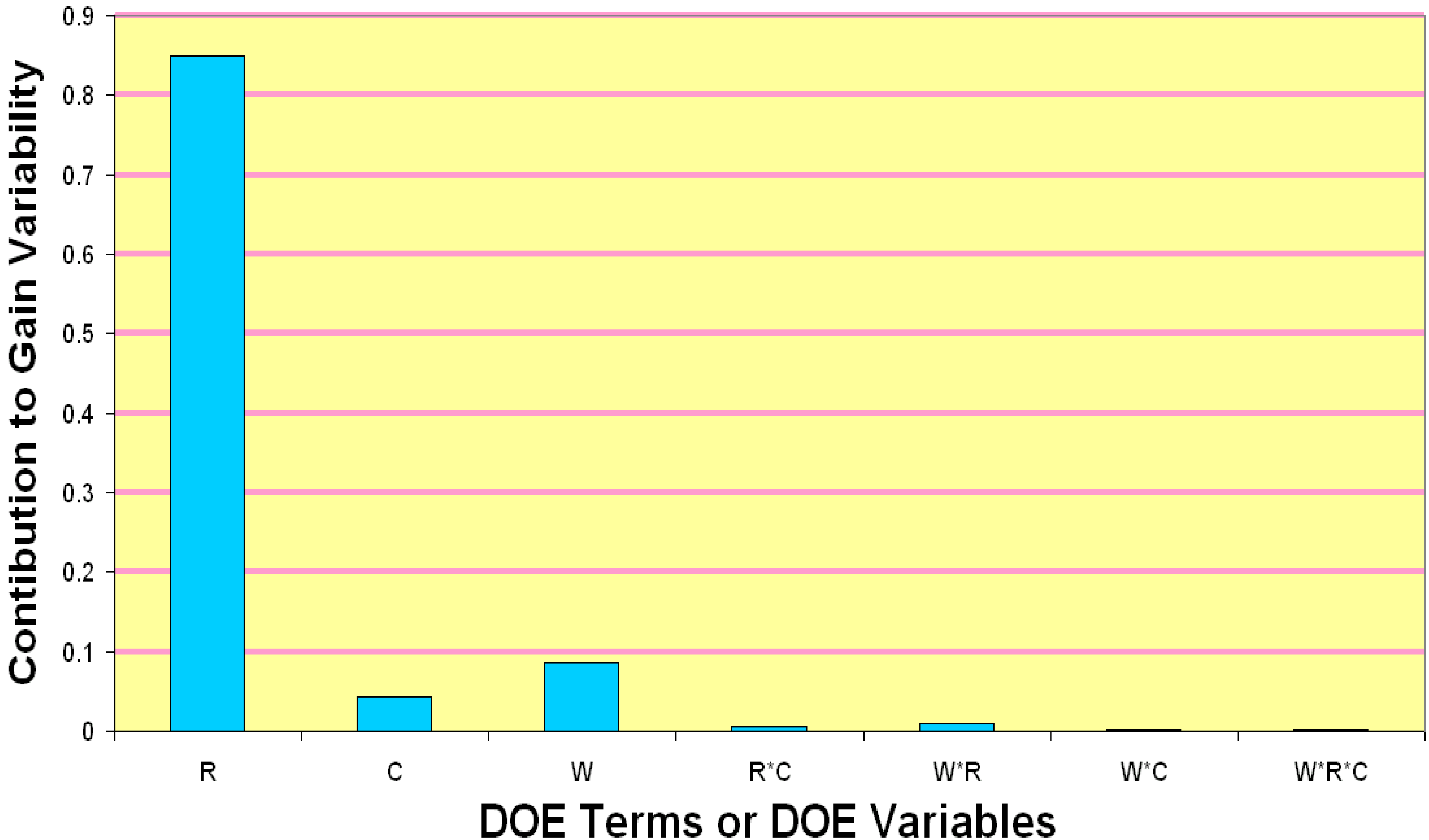
| Term | Coefficient |
|---|---|
| Constant (nominal gain) | 13.8 |
| W | .09 |
| R | .85 |
| C | .044 |
| W*R | .0088 |
| W*C | .0013 |
| R*C | .0050 |
| W*R*C | 0.0025 |

We calculated these three coefficients in the previous slides

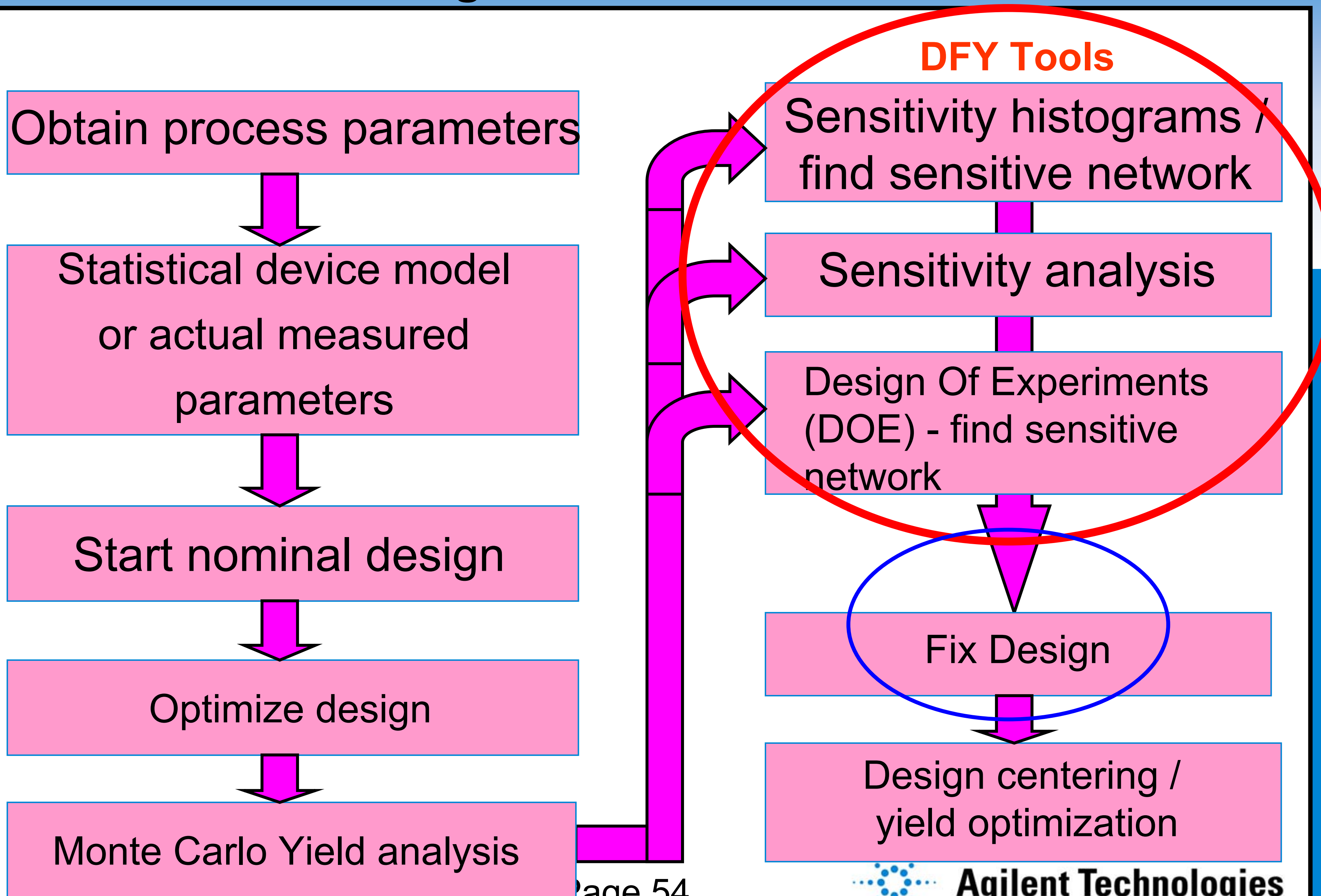
**Construct a linear equation to represent the experiment results.**

**Gain=13.8+.09W+.85R+.044C+.0088WR+…..etc.**

# Display All Effects on a Pareto Chart



# DFY tools allow designers to find the areas in the design that need to be redesigned



# DOE INTERACTIONS

## *Another DOE Example with 5 variables:*

1. Width of lines due to process - +/- .5 microns
2. IMN_C1 (Input Matching Network) C1 +/- 5%
3. IMN_R1 (Input Matching Network) C1 +/- 5%
4. OMN_C1 (Output Matching Network) C1 +/- 5%
5. OMN_R1 (Output Matching Network) R1 +/- 5%

# DFY- DOE

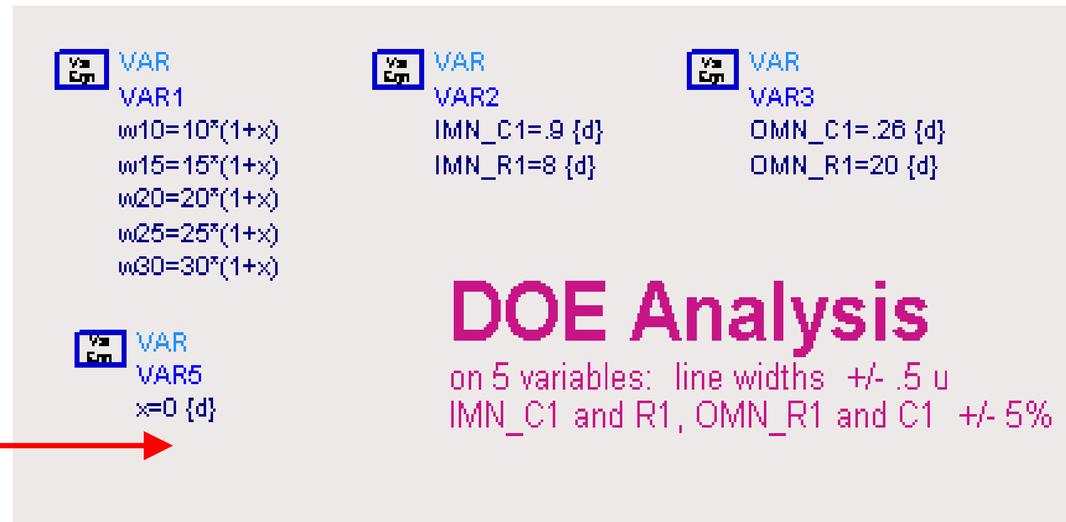
2

- Open the Design file:
- E_LNA_DOE2_on_five_variables

1

*I want to study the sensitivity five elements that could affect the output results: IMN C1 and R1, OMN C1 and R1, and line widths*

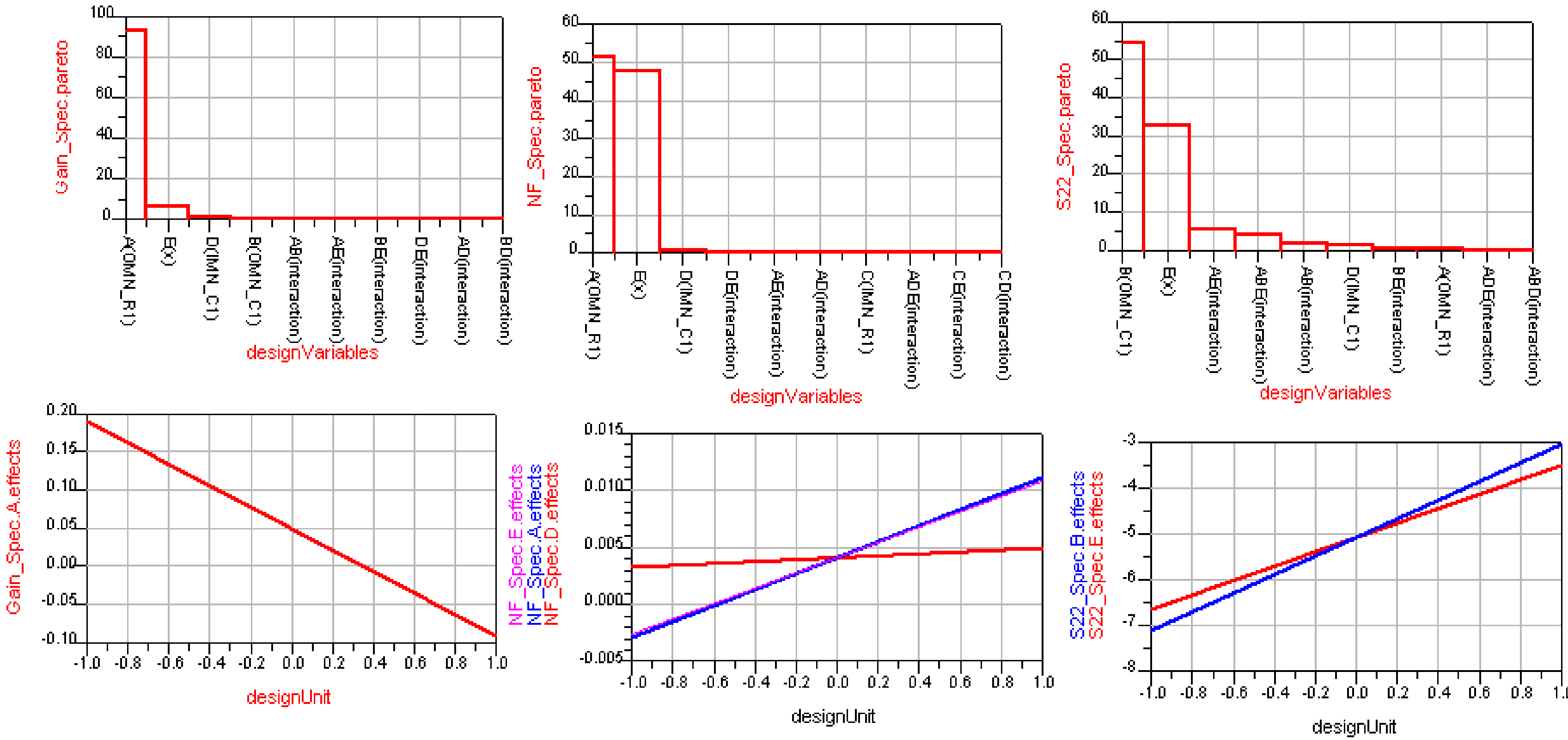
- The <u>five elements</u> we want to run DOE on are:
- IMN_R1 IMN_C1
- Line widths
- OMN_R1 OMN_C1




- Notice the variable x that I have created. As x changes, all line widths will change +/- .5

# DFY - DOE

When the simulation is done, this data Display will pop automatically



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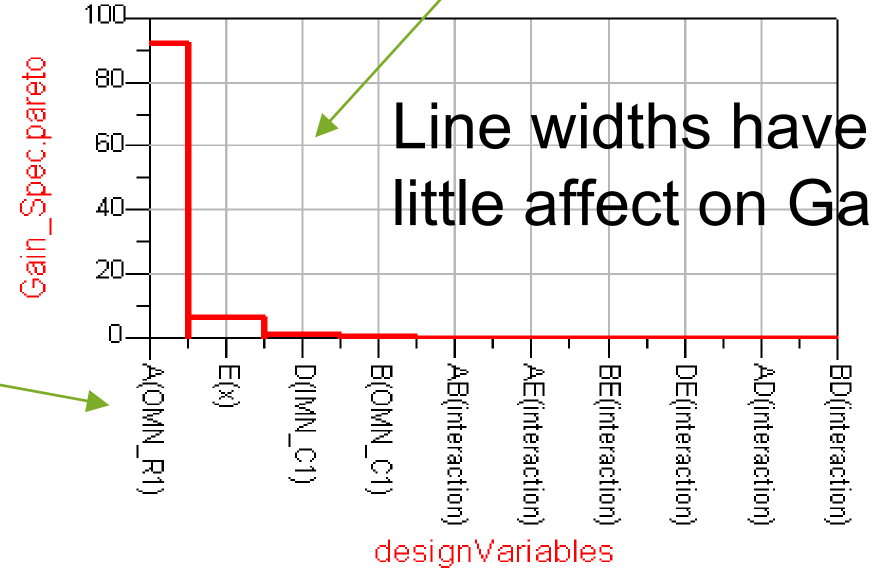
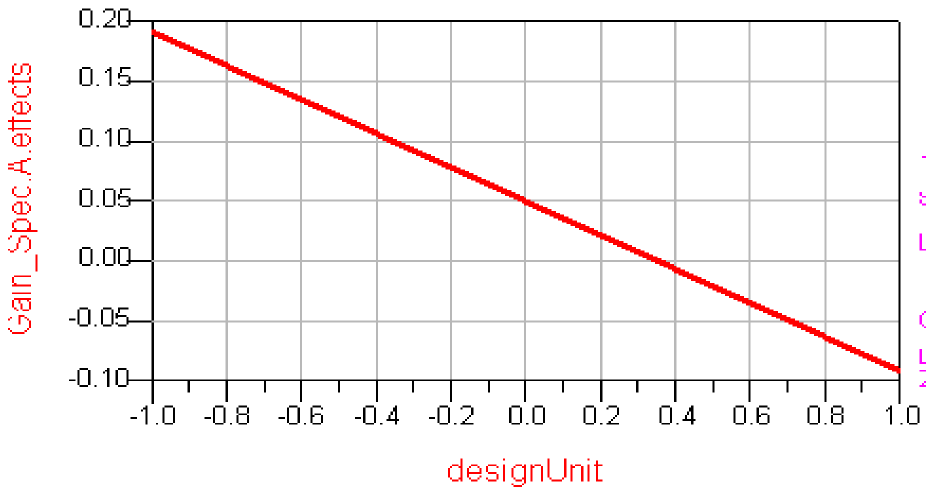
# DFY - DOE

Gain is mostly affected by OMN_R1




Line widths have little affect on Gain

Increase OMN_R1 by 5% reduces the gain by .14 dB
Decrease OMN_R1 by 5% increases the gain by .14 dB



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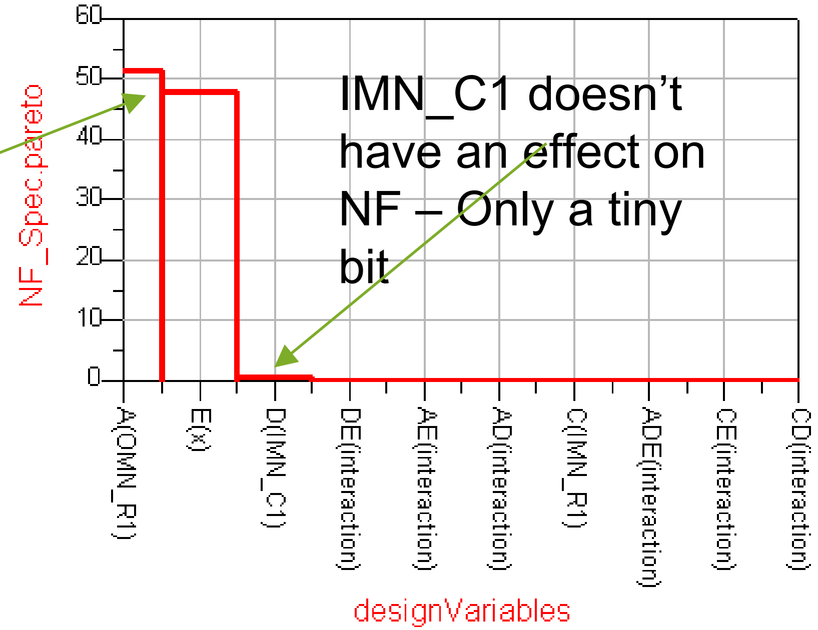
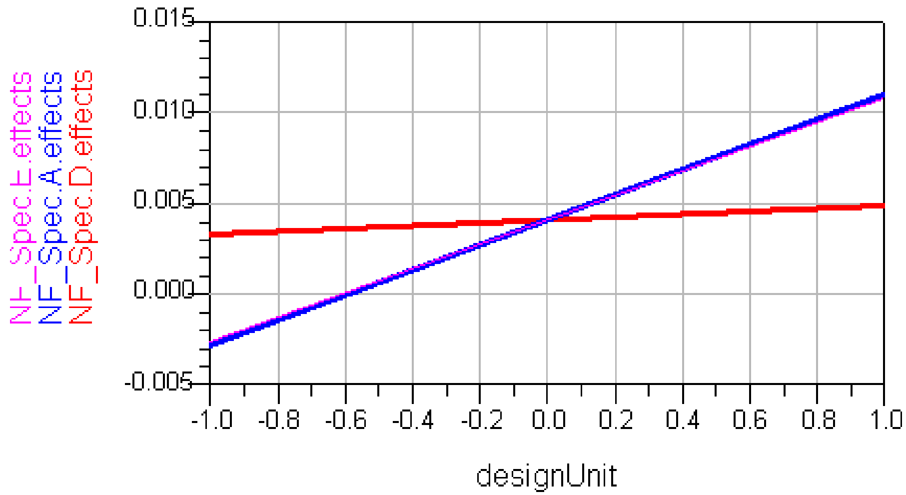
# DFY - DOE

NF is affected by OMN_R1 and line widths (especially of the IMN)




IMN_C1 doesn't have an effect on NF – Only a tiny bit

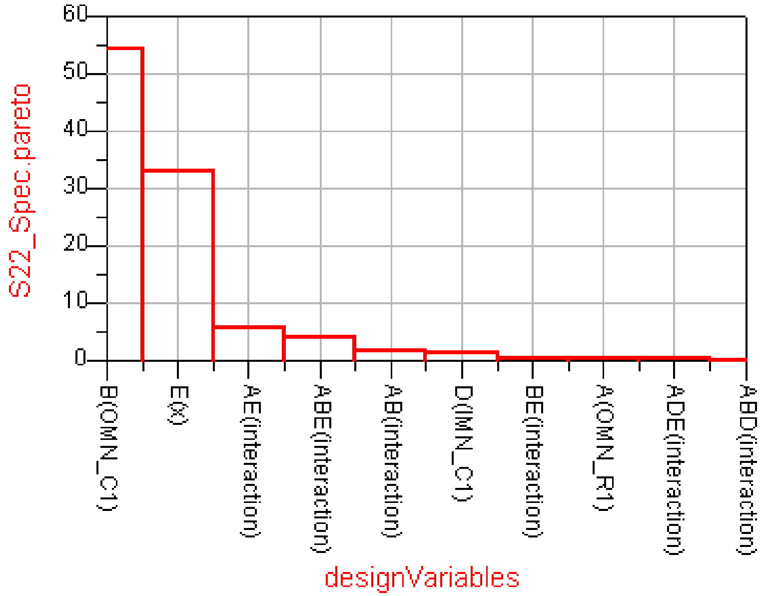
Effect of OMN_R1 and Line widths on NF are correlated – they both have the same slope



# DFY - DOE

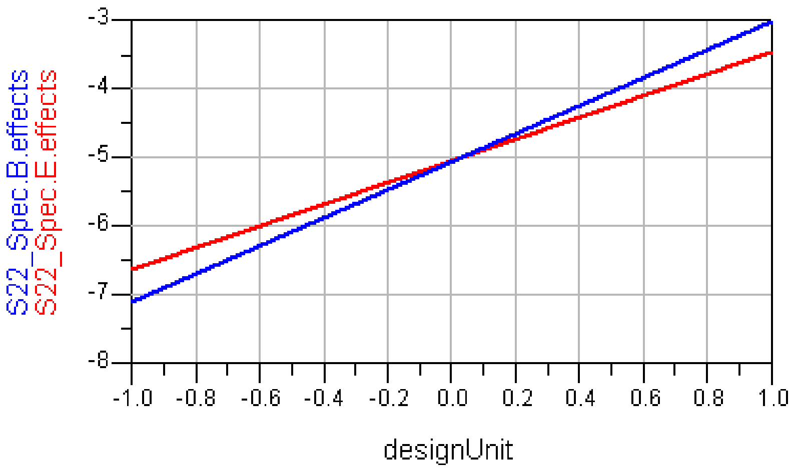
S22 is affected mostly by OMN_C1 and Line widths:

C1 adds 2 dB to S22
Line widths add 1.5 dB to S22




There is an interaction effects between OMN_R1 and Line widths

See next page



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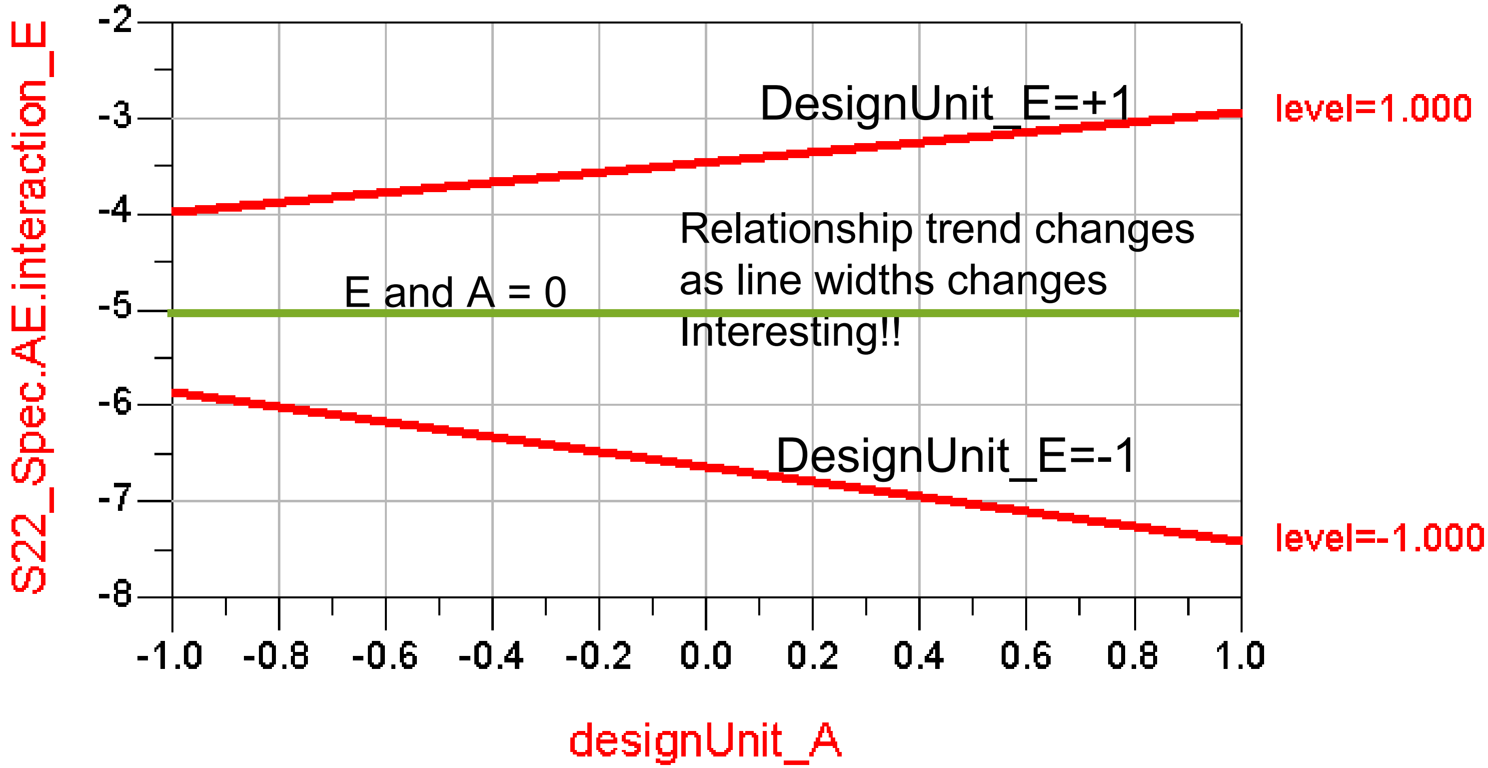
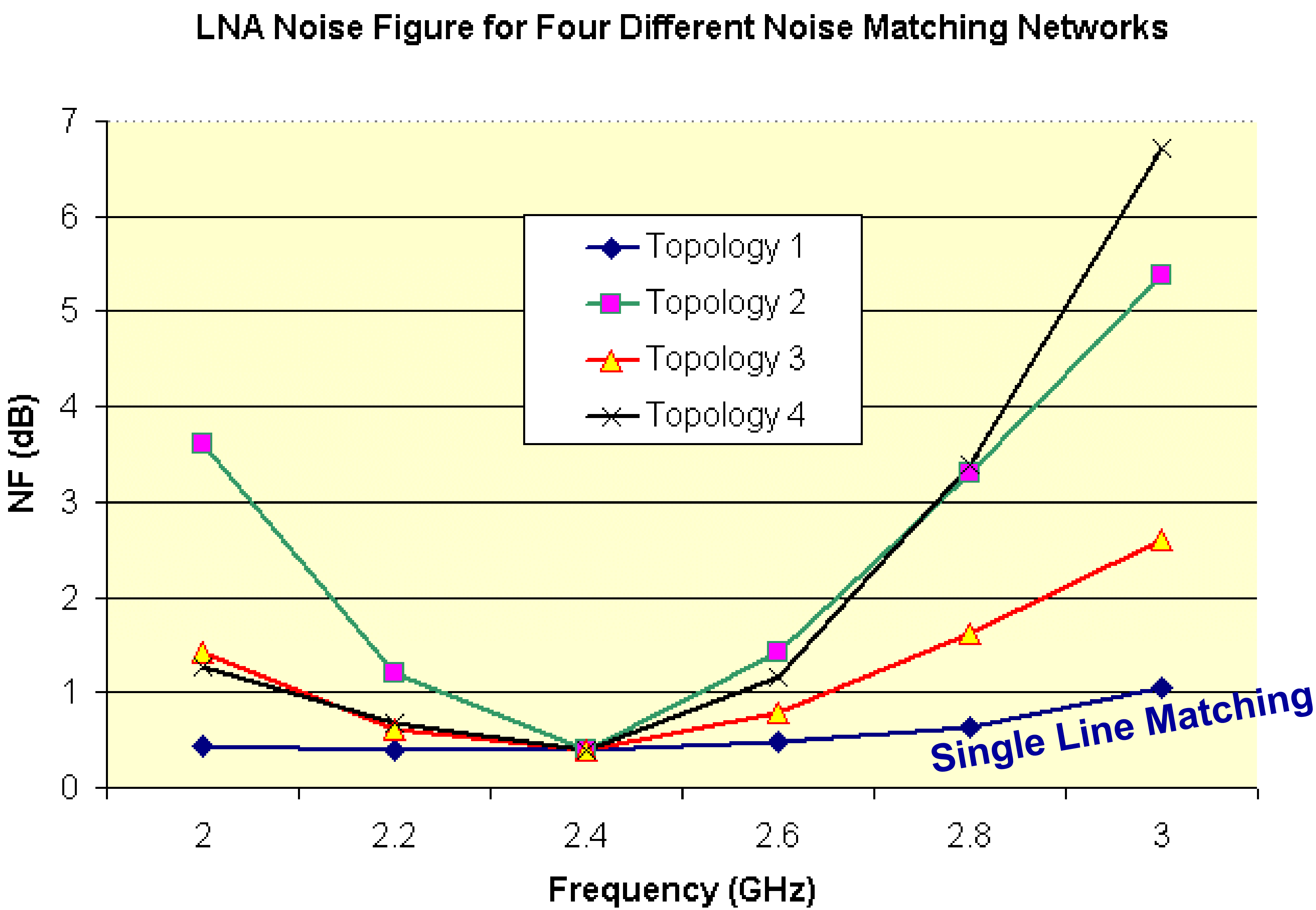
# Interaction effects between OMN_R1 and Line widths to S22




If OMN_R1 is high and Line Widths is High, S22 gets worse by 2 dB
If OMN_R1 is high and Line Widths is Low, S22 gets better by 2.3 dB
If OMN_R1 is low and Line Widths is High, S22 gets worse by 1 dB
If OMN_R1 is low and Line Widths is Low, S22 gets better by .8 dB

# NF Simulation of the Various Matching networks

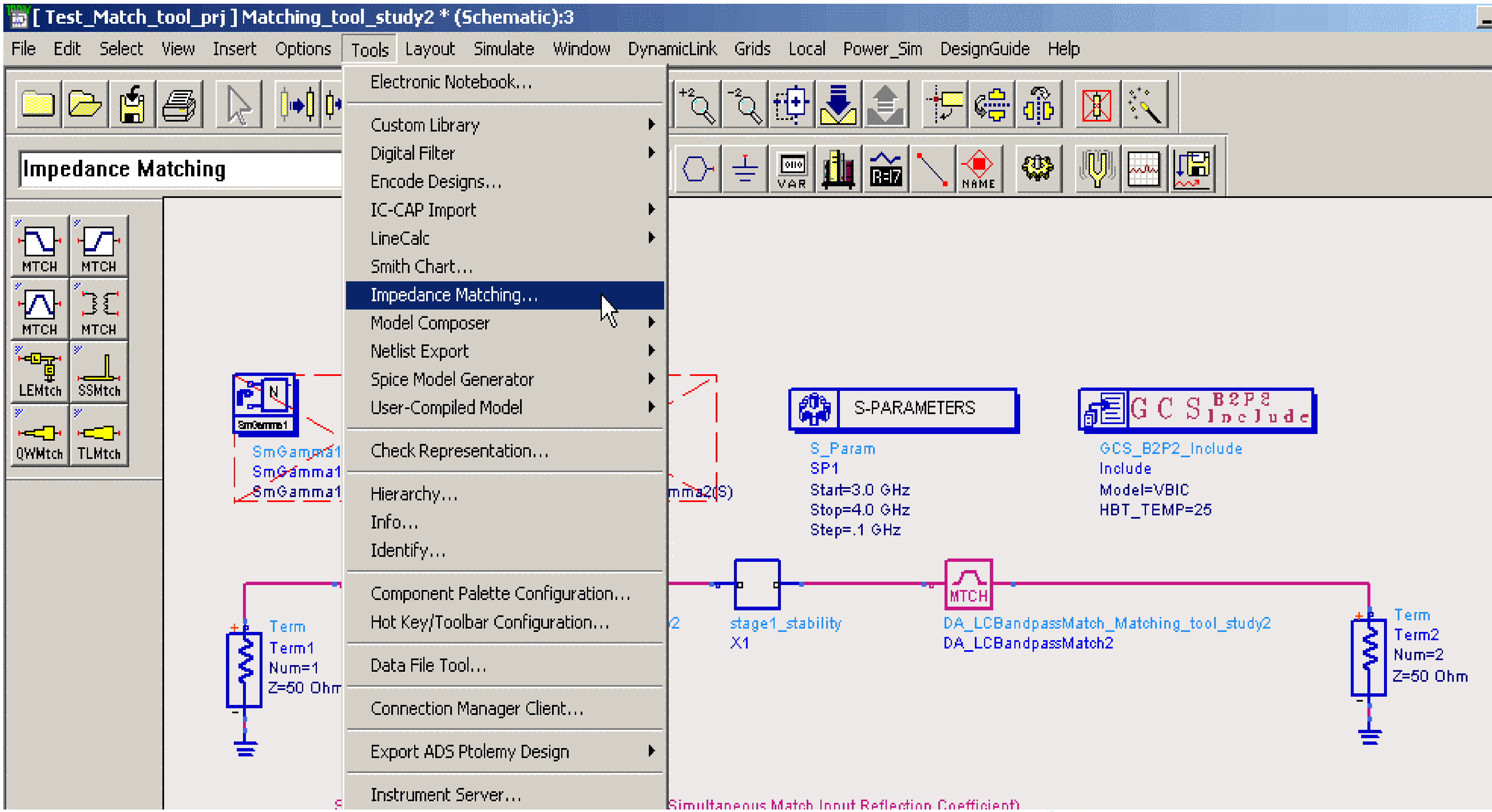


# Re-Cap

- Different Topologies produce different yield
- Selecting low Q topologies is a must.
- YSH help you find where the problem is coming from.
- DOE analysis help you find the sensitive high-Q matching networks and interactions between them

# Matching Utility Tool in ADS

# ADS Matching Tool



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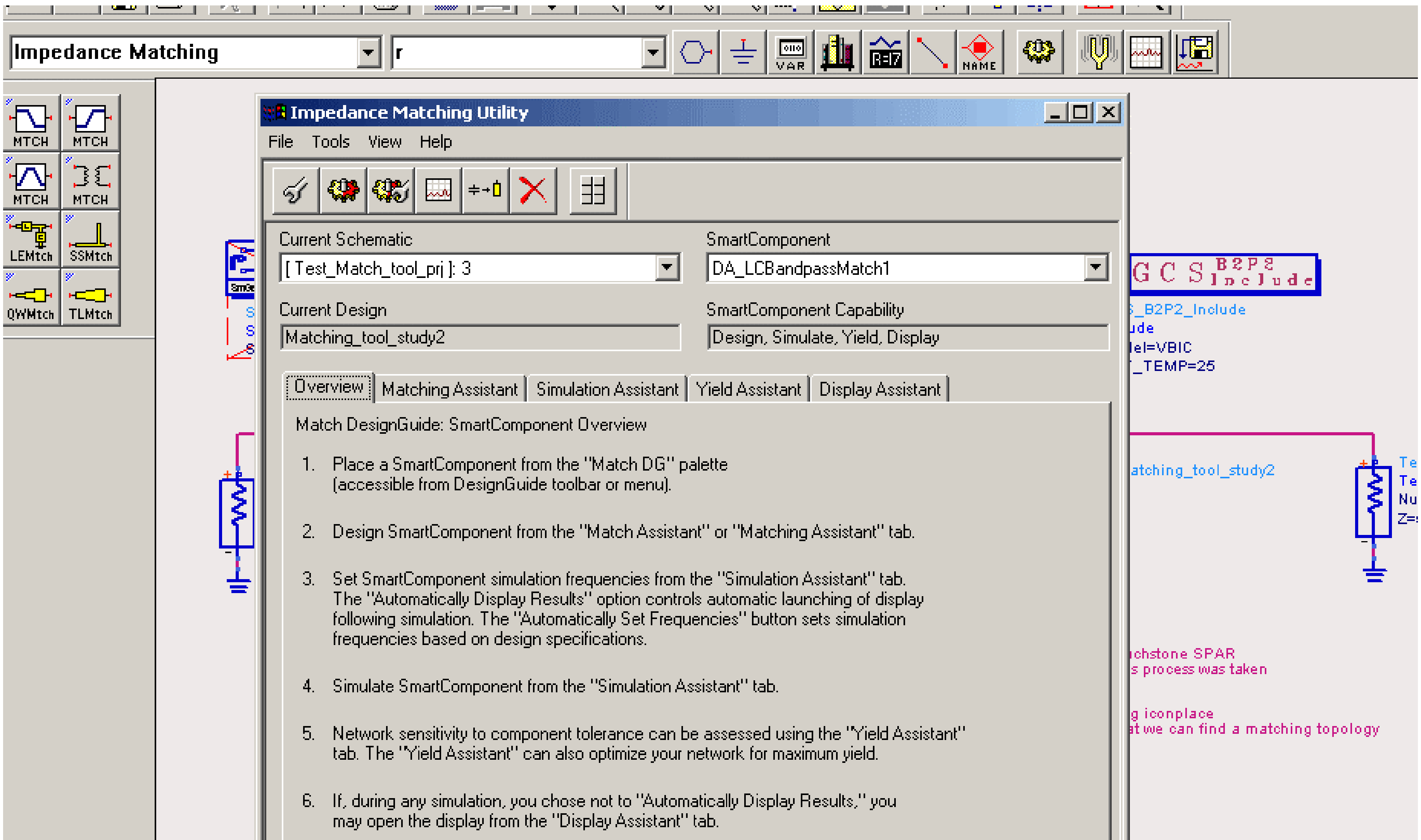
# ADS Matching Tool



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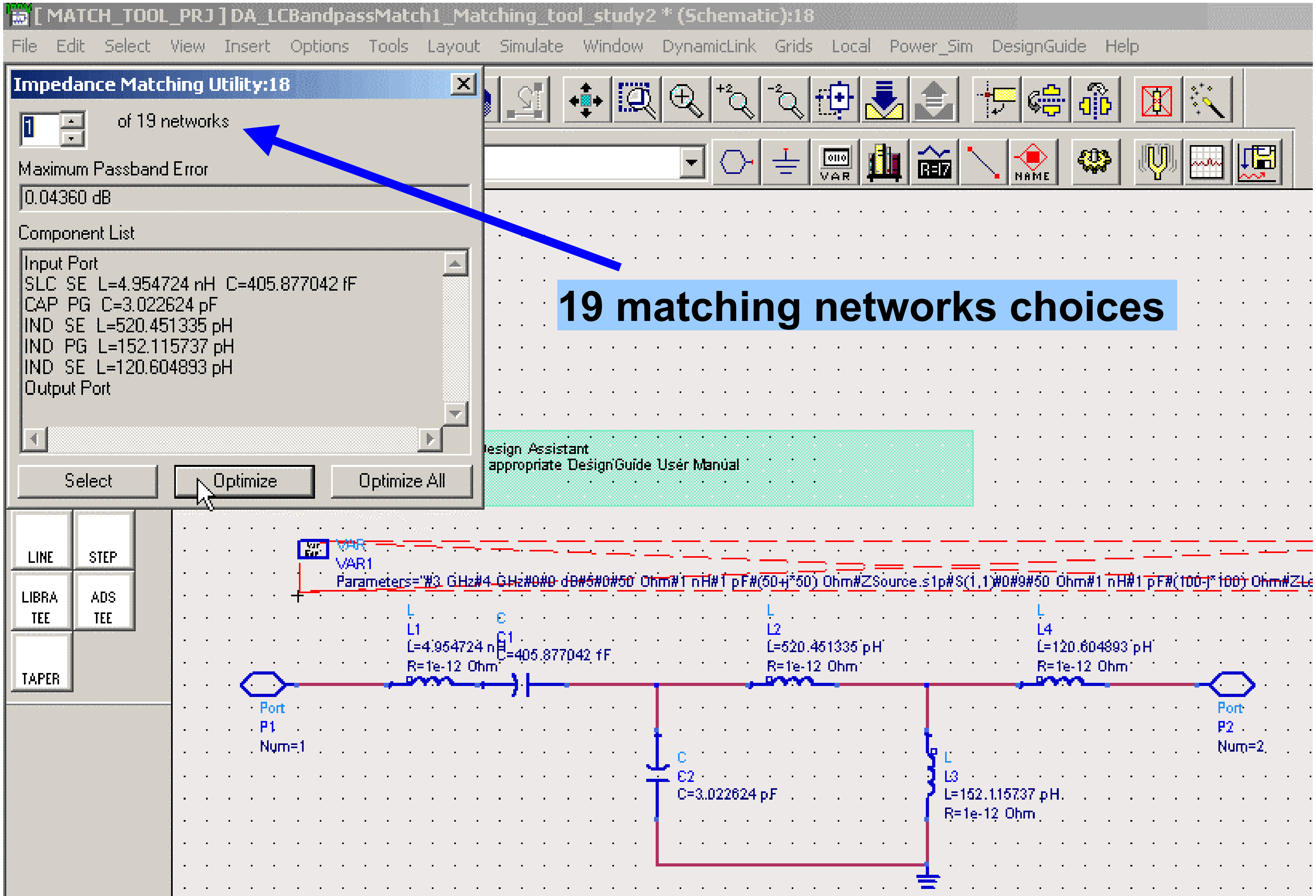
# ADS Matching Tool



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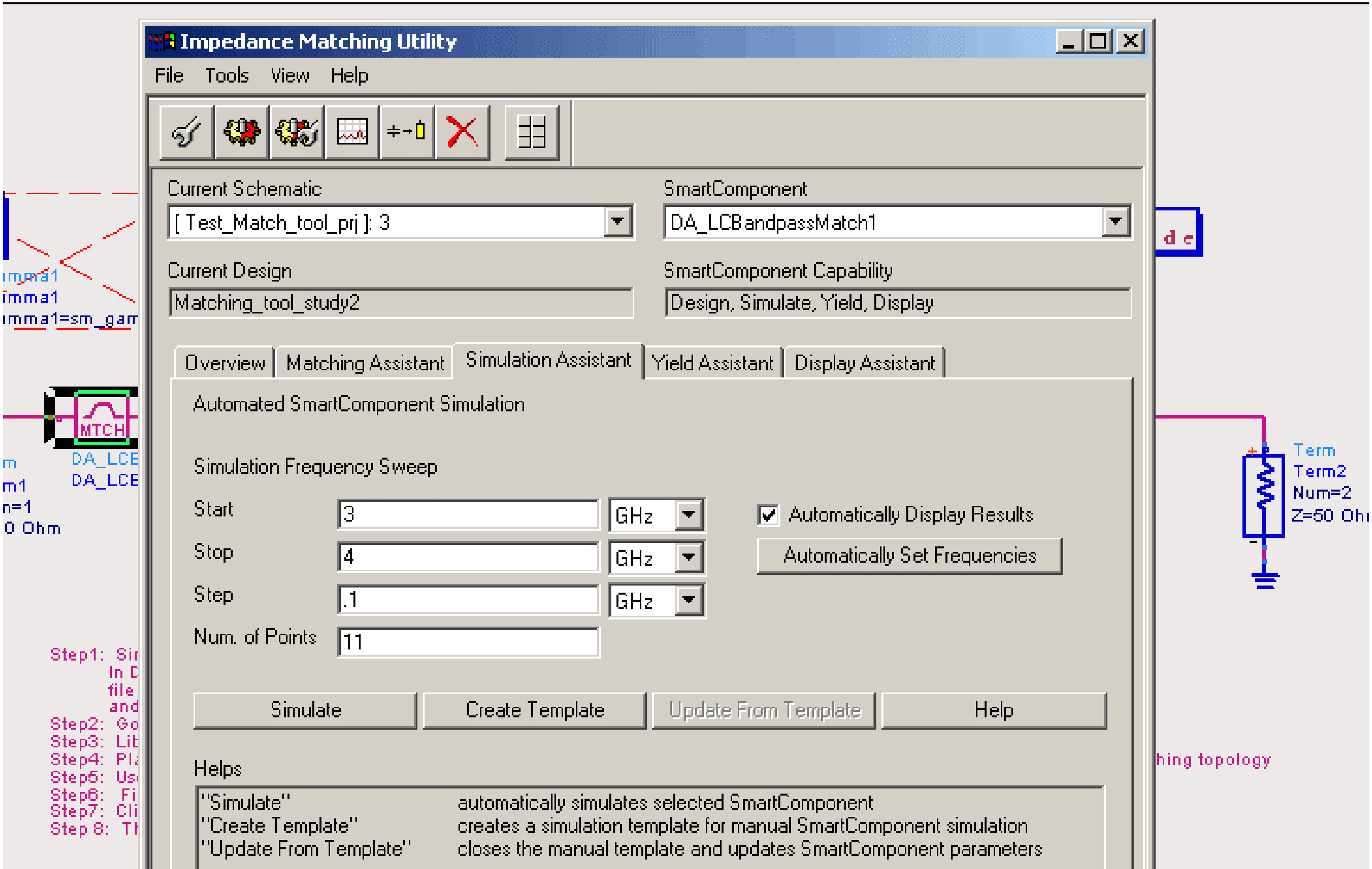
# ADS Matching Tool



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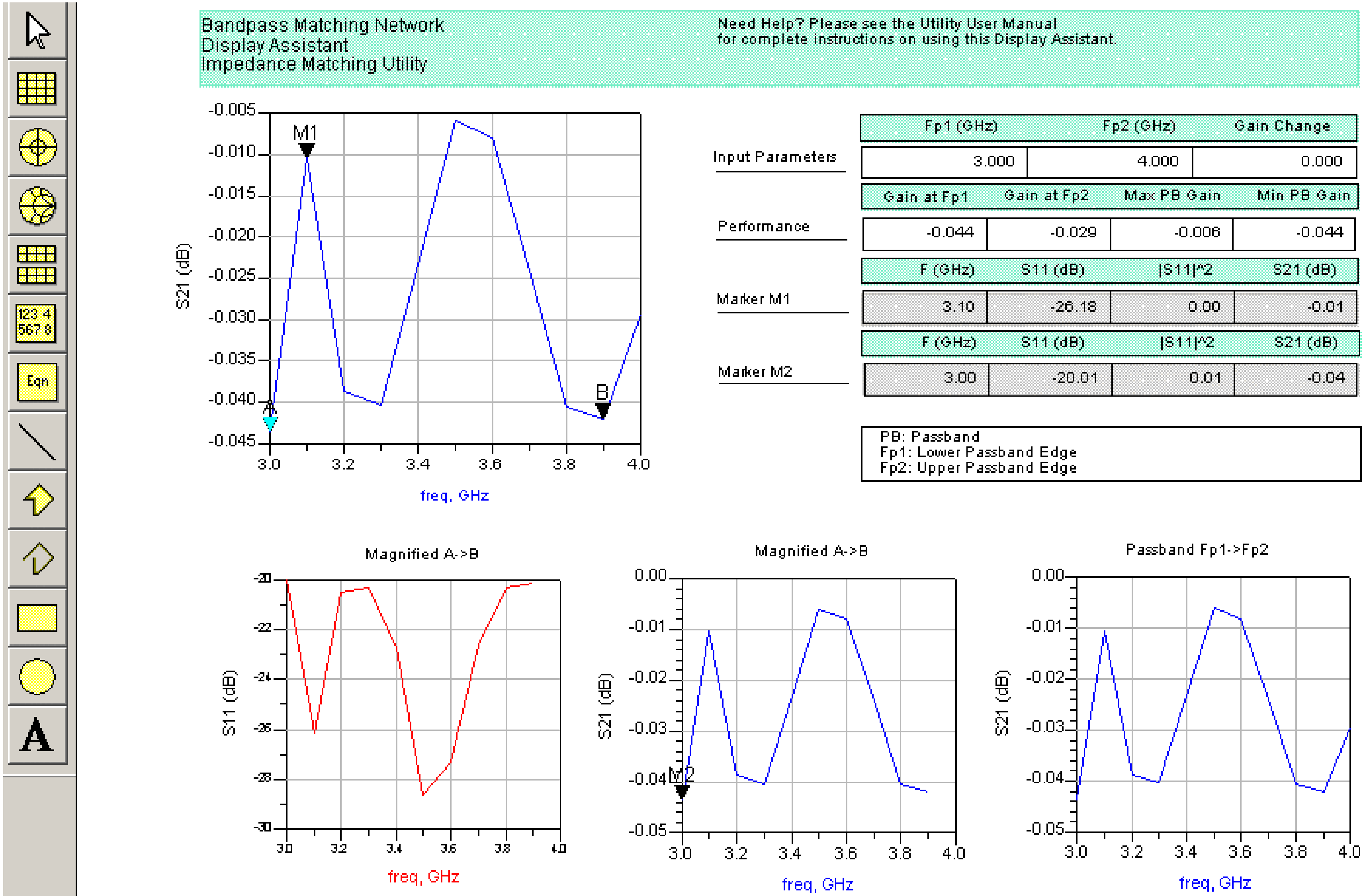
# ADS Matching Tool



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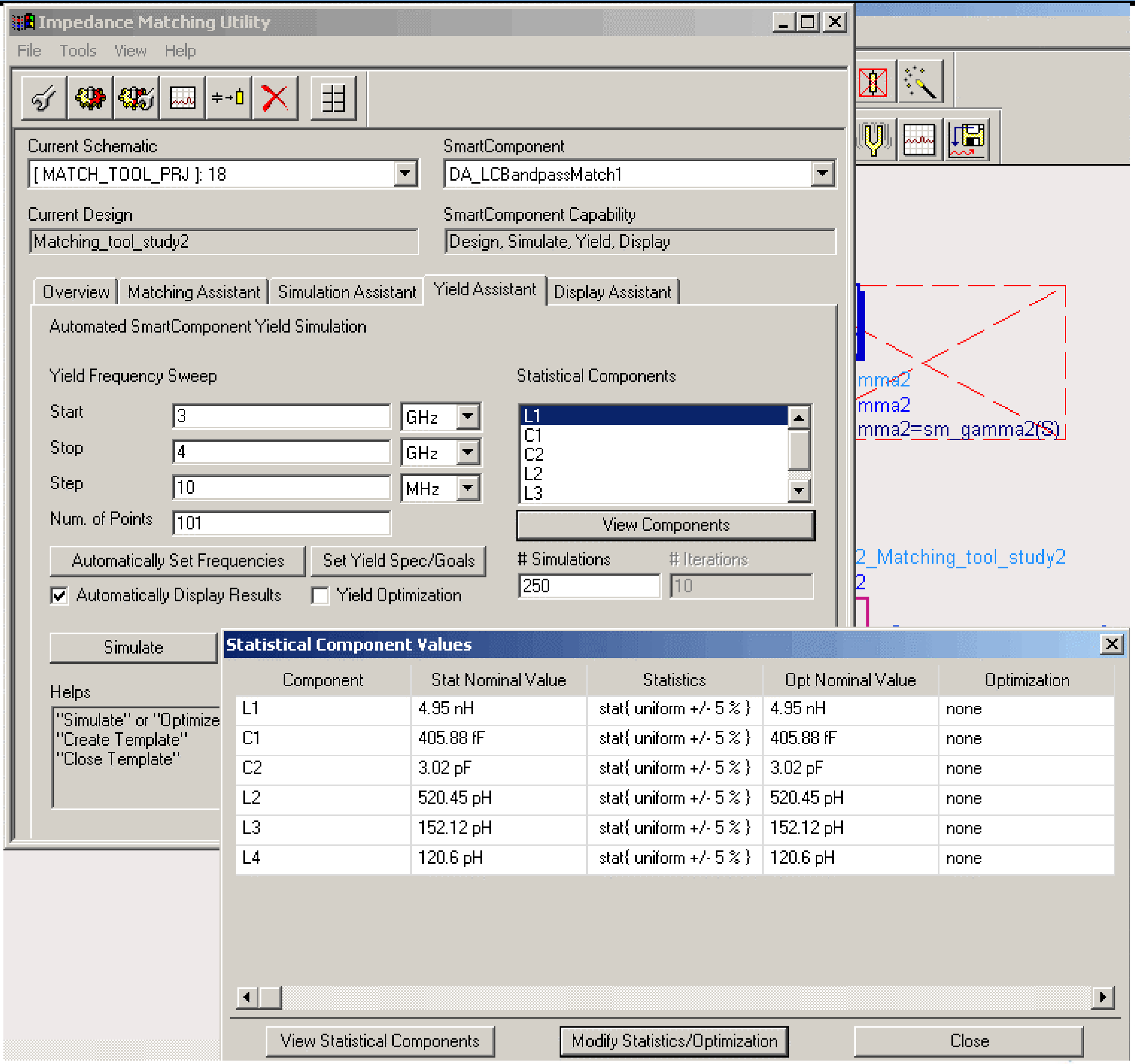
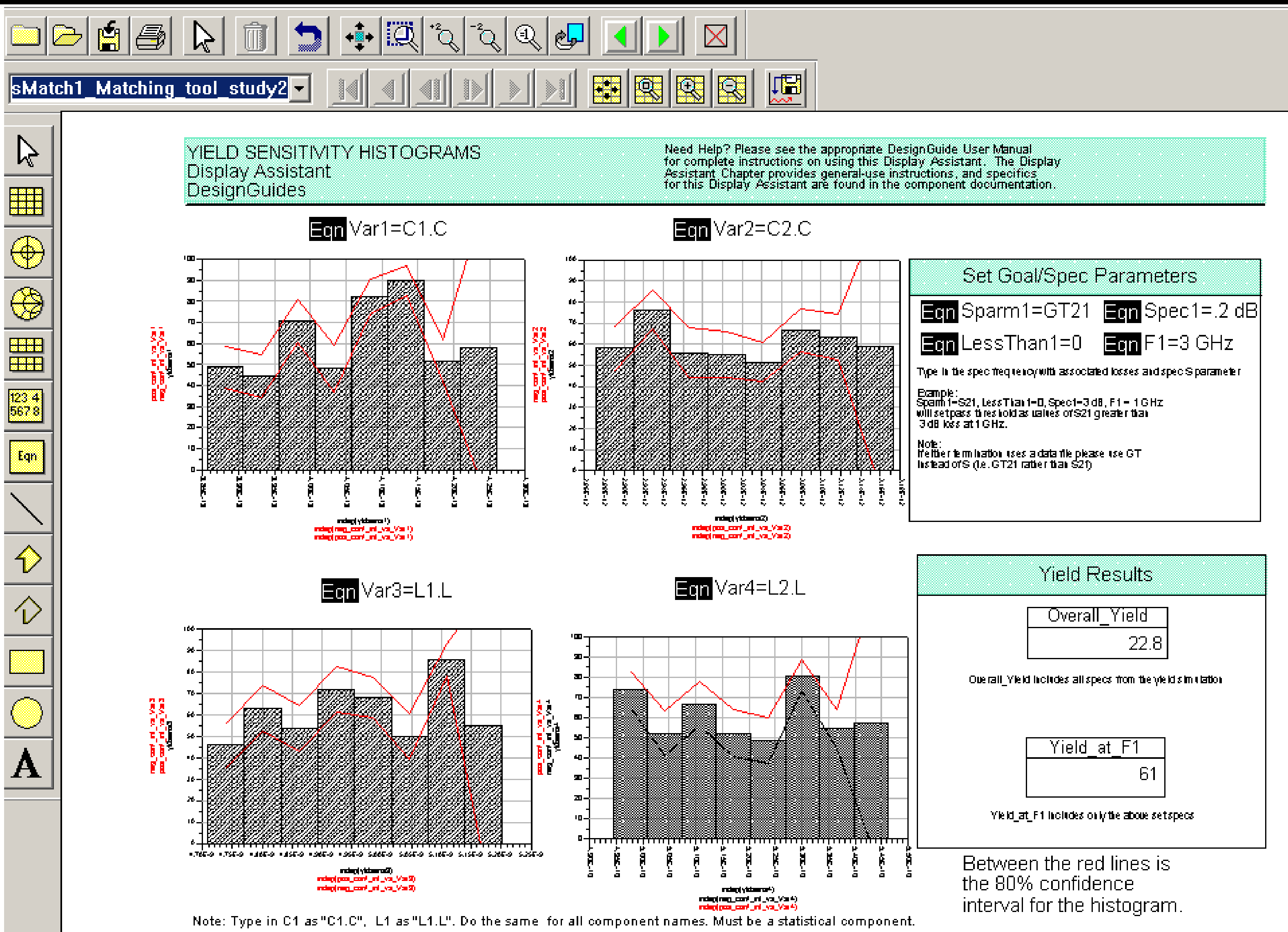
# ADS Matching Tool (Set Yield Specs and Tolerances)




| Component | Stat Nominal Value | Statistics | Opt Nominal Value | Optimization |
|---|---|---|---|---|
| L1 | 4.95 nH | stat{ uniform +/- 5 % } | 4.95 nH | none |
| C1 | 405.88 fF | stat{ uniform +/- 5 % } | 405.88 fF | none |
| C2 | 3.02 pF | stat{ uniform +/- 5 % } | 3.02 pF | none |
| L2 | 520.45 pH | stat{ uniform +/- 5 % } | 520.45 pH | none |
| L3 | 152.12 pH | stat{ uniform +/- 5 % } | 152.12 pH | none |
| L4 | 120.6 pH | stat{ uniform +/- 5 % } | 120.6 pH | none |

# ADS Matching Tool



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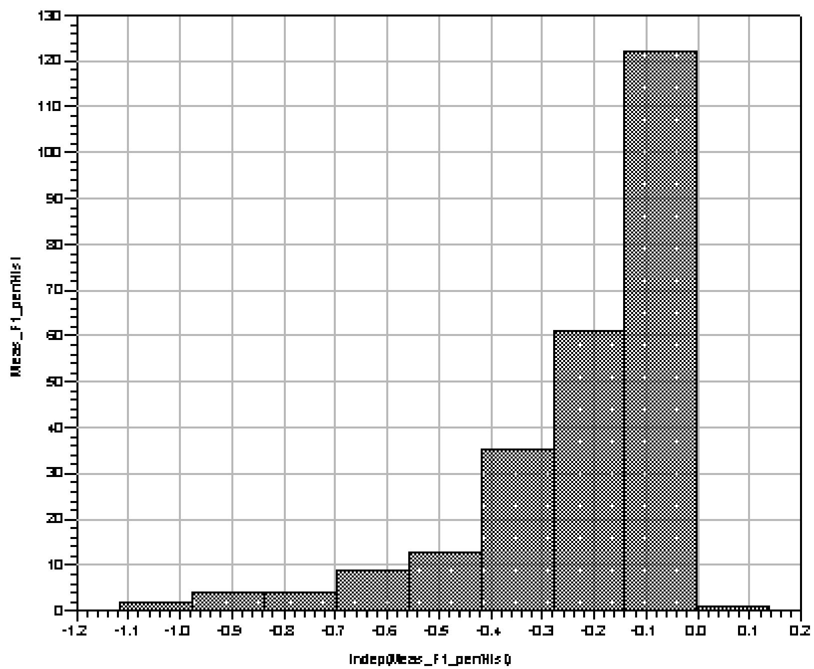
# ADS Matching Tool

MEASUREMENT HISTOGRAMS
Display Assistant
DesignGuides

Need Help? Please see the appropriate DesignGuide User Manual for complete instructions on using this Display Assistant. The Display Assistant Chapter provides general-use instructions, and specifics for this Display Assistant are found in the component documentation.

Number of Occurrences versus Measurement Value

F1




**Settable Parameters**

Please use the Yield Sensitivity Histogram page in order to set desired frequency as well as associated loss and S parameter.

**Yield Results**

| NumPass |
| --- |
| 57 |

| NumFail |
| --- |
| 193 |

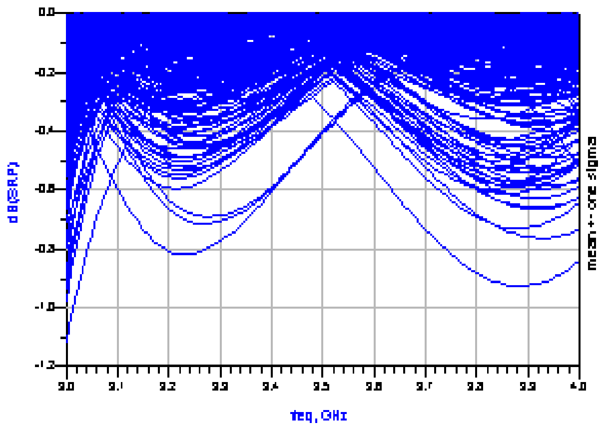
| Yield |
| --- |
| 23 |

# ADS Matching Tool

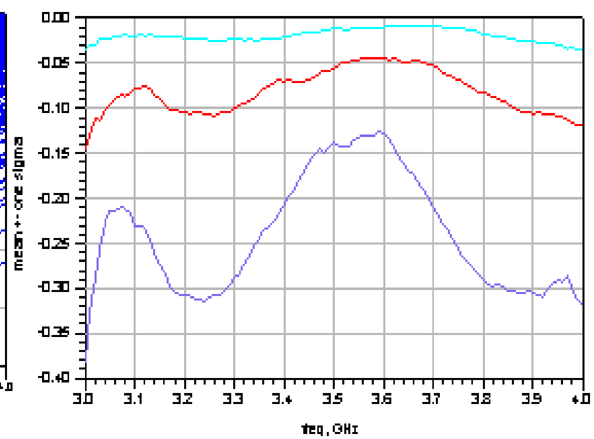
STATISTICAL RESPONSE PLOTS
Display Assistant
DesignGuides

Need Help? Please see the appropriate DesignGuide User Manual for complete instructions on using this Display Assistant. The Display Assistant Chapter provides general-use instructions, and specifics for this Display Assistant are found in the component documentation.

dB(SRP) vs Frequency




dB(SRP) Statistical Response Plot




In this Statistical Response plot, the center line is the average of the measurements, the top and bottom lines are, respectively, the average measurement plus and minus, one measurement standard deviation.

## Settable Parameters

Please use Yield Sensitivity Histogram page to set desired frequency with associated loss.

Eqn SRP = GT21

Type in the desired frequency response

Note:
If either termination uses a data file please use GT instead of S (i.e. GT21 rather than S21)

## Yield Results

| freq | mean_SRP | ...RP + SD_SRP | ...SRP - SD_SRP |
|---|---|---|---|
| 3.0 GHz | -0.2 | -4.0E-3 | -0.4 |
| 3.0 GHz | -0.2 | -2.4E-3 | -0.4 |
| 3.0 GHz | -0.2 | -2.9E-3 | -0.3 |
| 3.0 GHz | -0.1 | -4.6E-3 | -0.3 |
| 3.0 GHz | -0.1 | -6.8E-3 | -0.3 |
| 3.0 GHz | -0.1 | -8.8E-3 | -0.2 |
| 3.1 GHz | -0.1 | -9.9E-3 | -0.2 |
| 3.1 GHz | -0.1 | -1.0E-2 | -0.2 |



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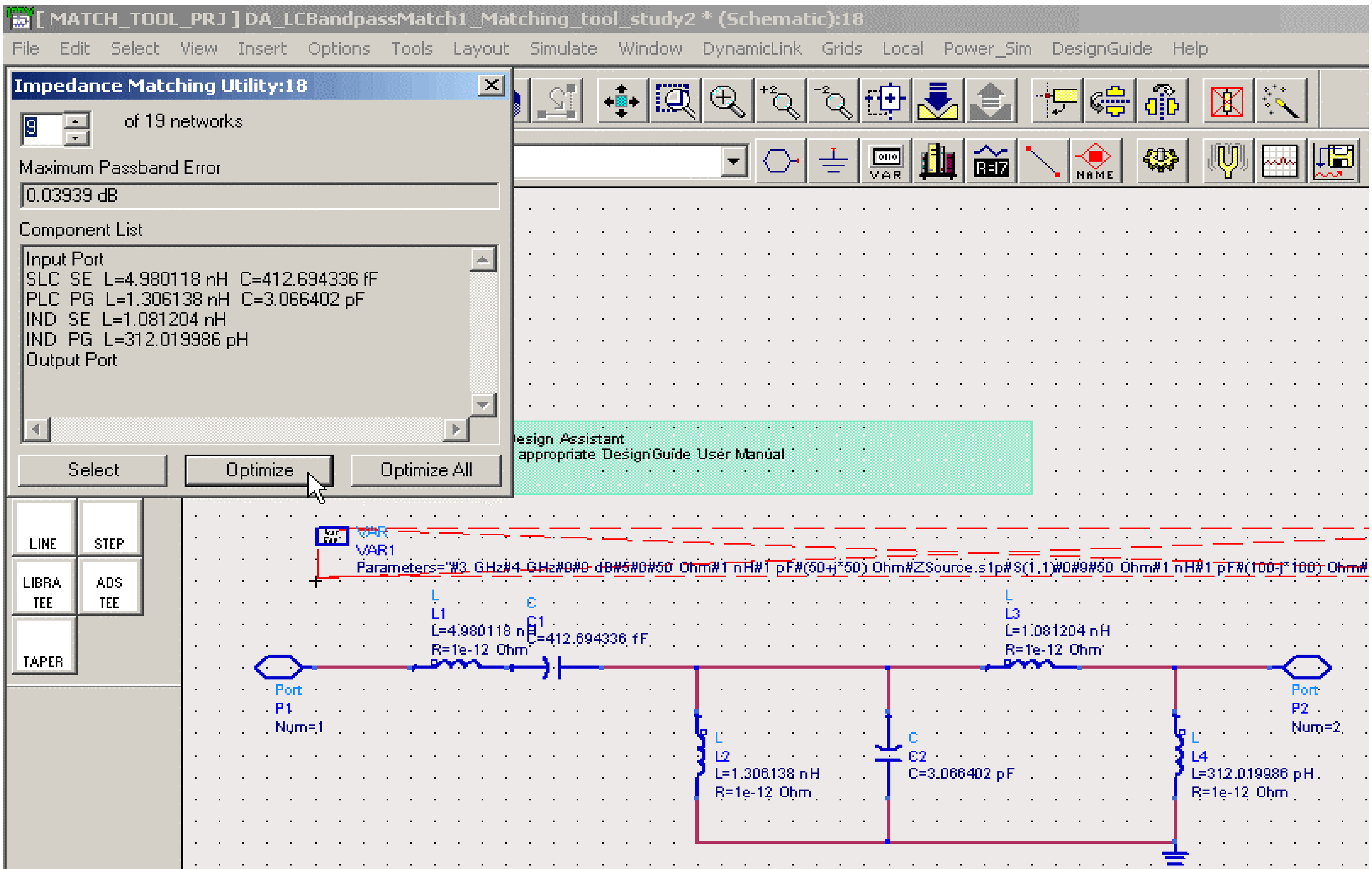
# ADS Matching Tool



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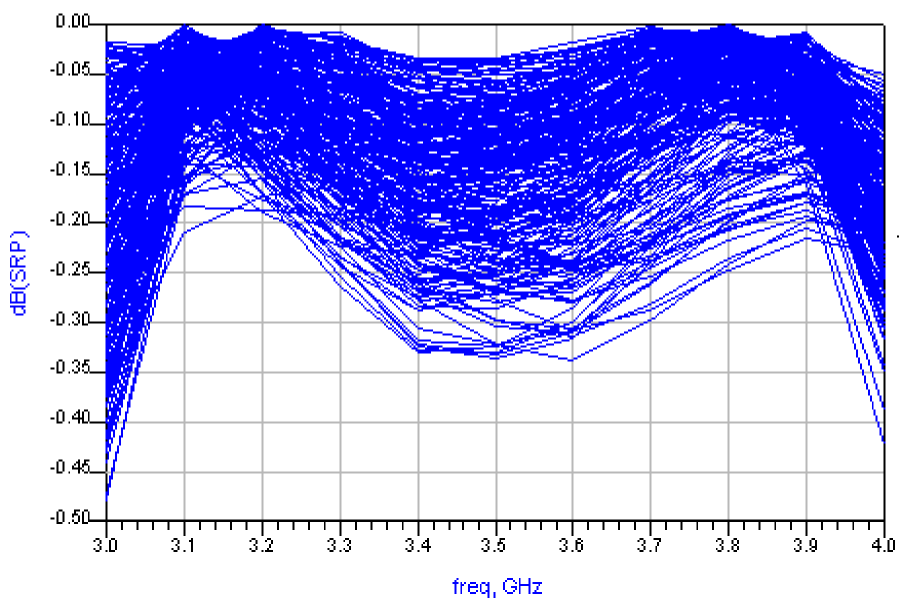
# ADS Matching Tool

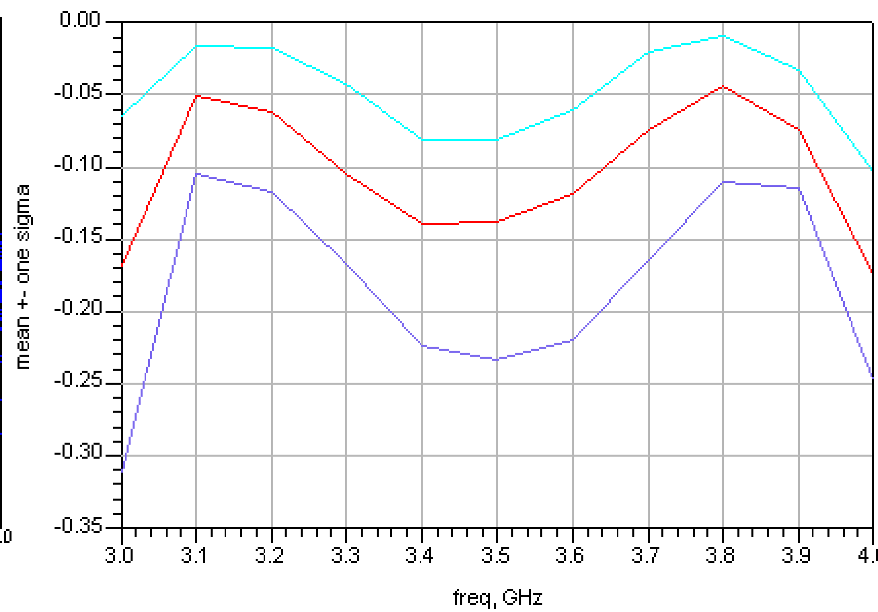
STATISTICAL RESPONSE PLOTS
Display Assistant
DesignGuides

Need Help? Please see the appropriate DesignGu
for complete instructions on using this Display As
Assistant Chapter provides general-use instructic
for this Display Assistant are found in the compor

**dB(SRP) vs Frequency**

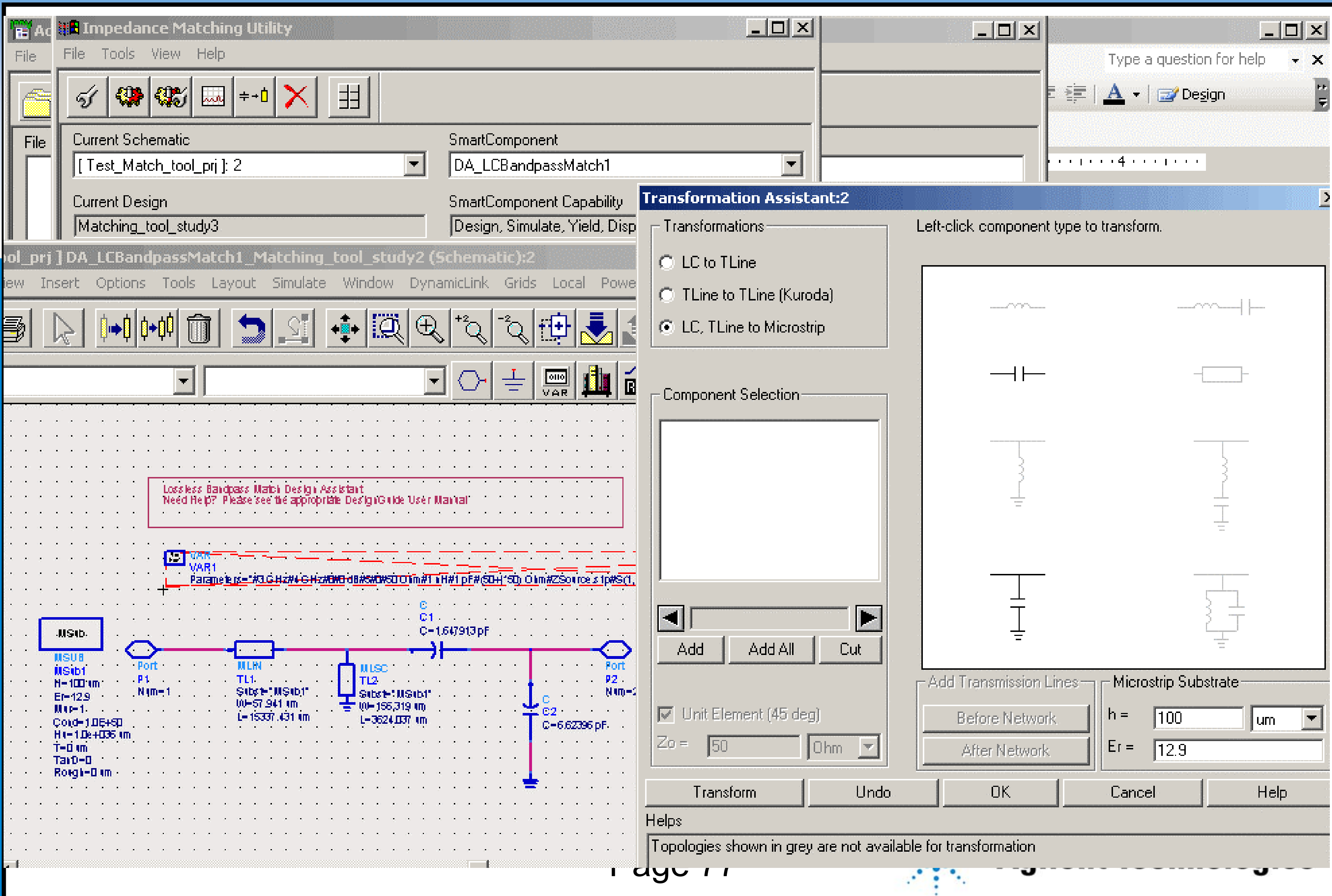



**dB(SRP) Statistical Response Plot**

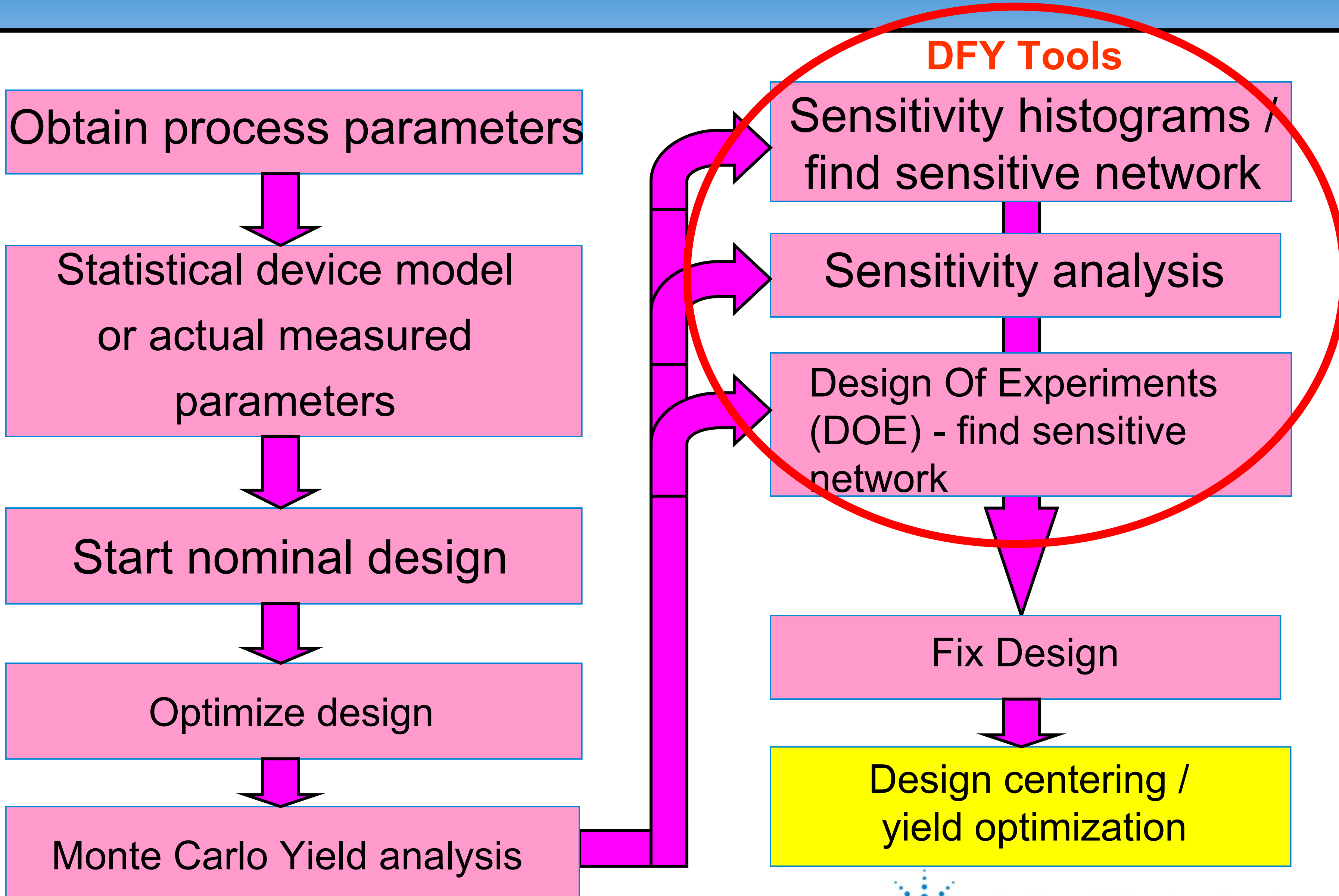



In this Statistical Response plot, the center line is the average
of the measurements, the top and bottom lines are, respectively, the
average measurement plus and minus one measurement standard deviation

# ADS Matching Tool – Transform to Microstrip lines



# The DFY Process for MMIC



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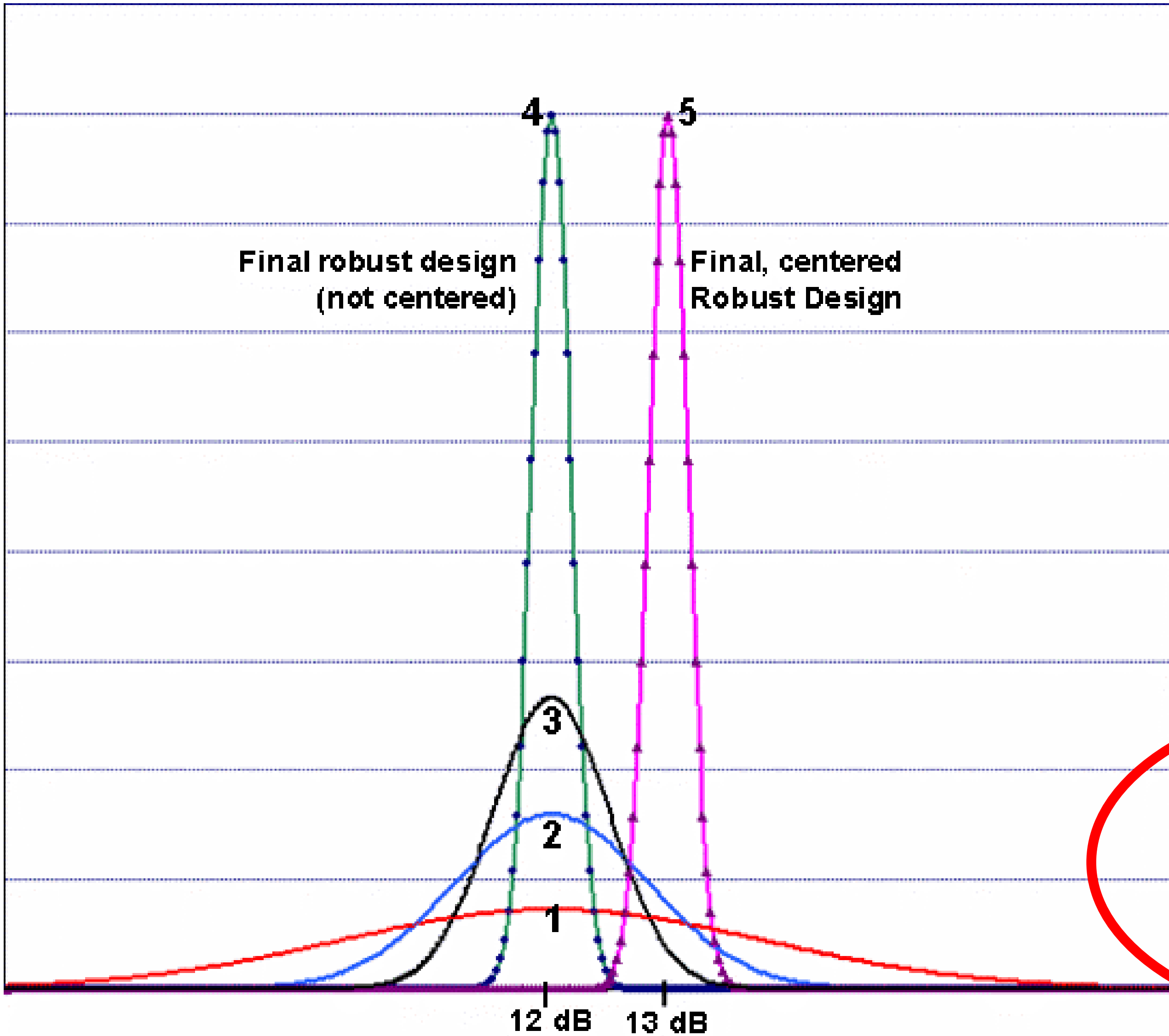
# The DFY Process




**Curve 1**
**Original Design**

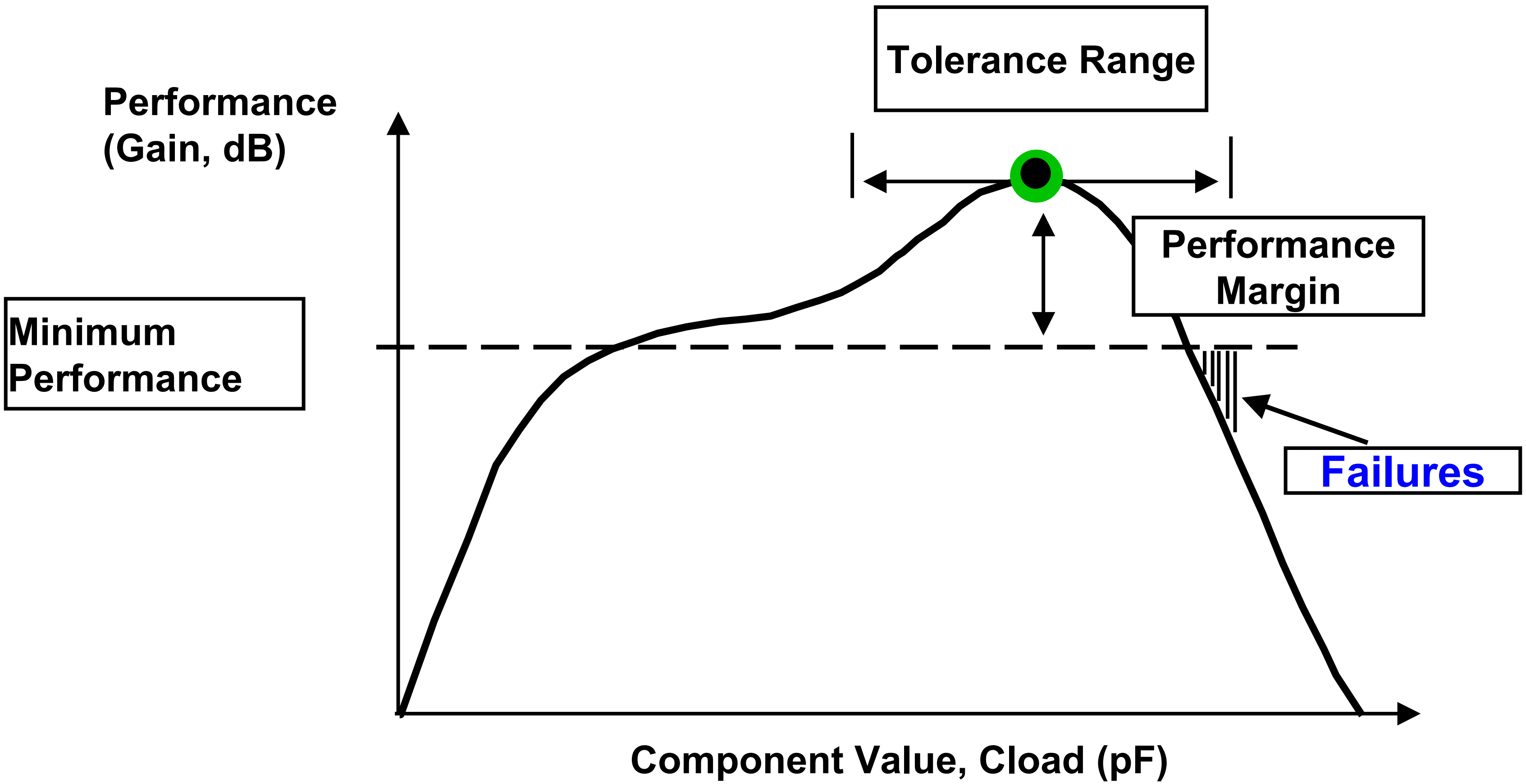
**Curves 2,3**
**Fixing the Design to achieve Robustness**

**Curves 4**
**Further improvement towards achieving Robustness**

**Curve 5**
**Final Shift the Response by Design Centering to meet Specs.**

# Yield Optimization (Design Centering)

## Understanding the Mechanism of Design Centering



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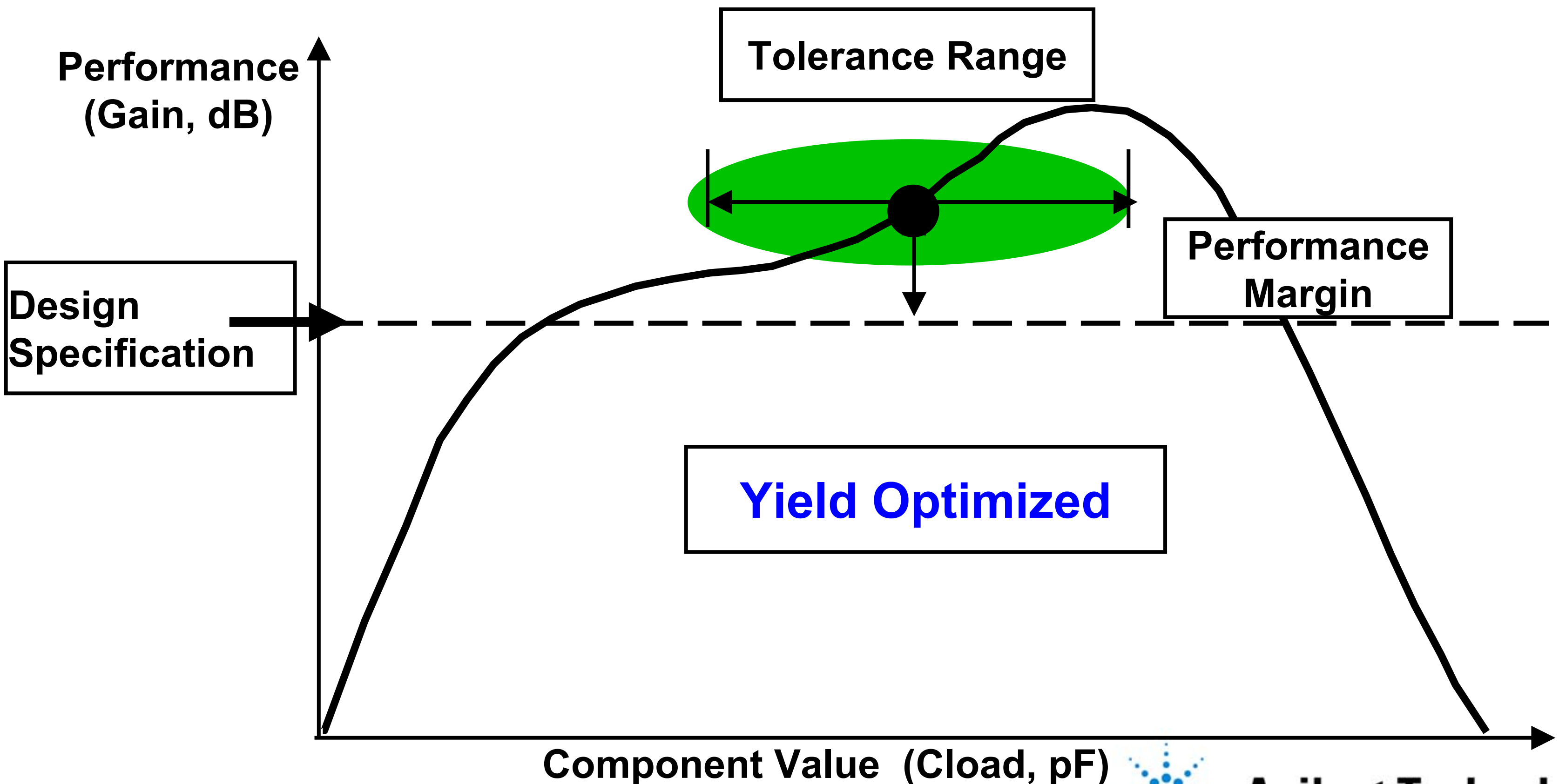
# Yield Optimization (Design Centering)

## Understanding the Mechanism of Design Centering



# Yield Optimization (Design Centering)

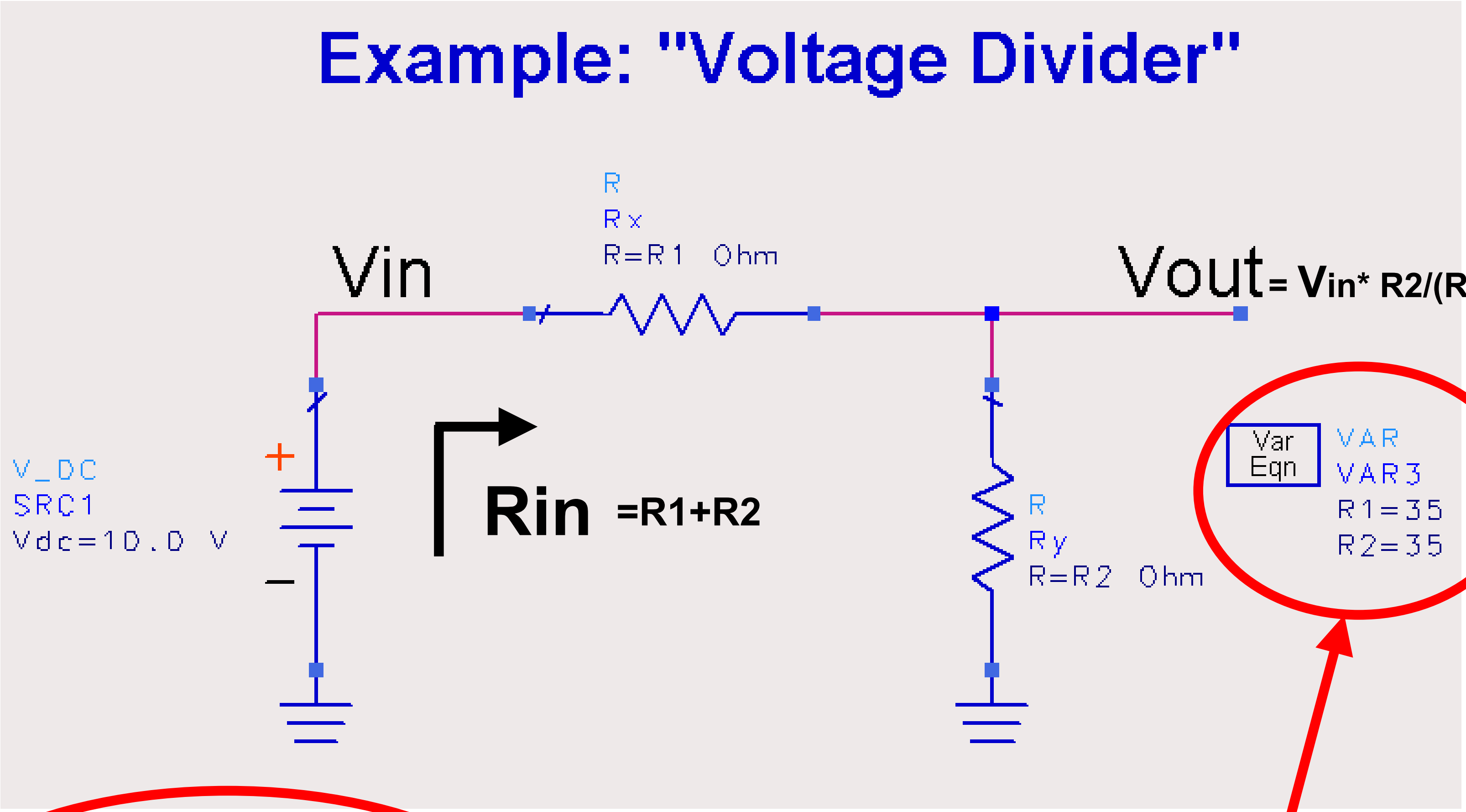
**Understanding the Mechanism of Design Centering**

## *Ex. Resistive Divider*

- **Design Centering**
- **Yield Sensitivity Histograms**

# Yield Optimization (Design Centering) - Example

## Example: "Voltage Divider"




**Specifications:**

**4 ≤ Vout ≤ 5**

**50 Ω ≤ Rin ≤ 70 Ω**

**Initial values meet specs**



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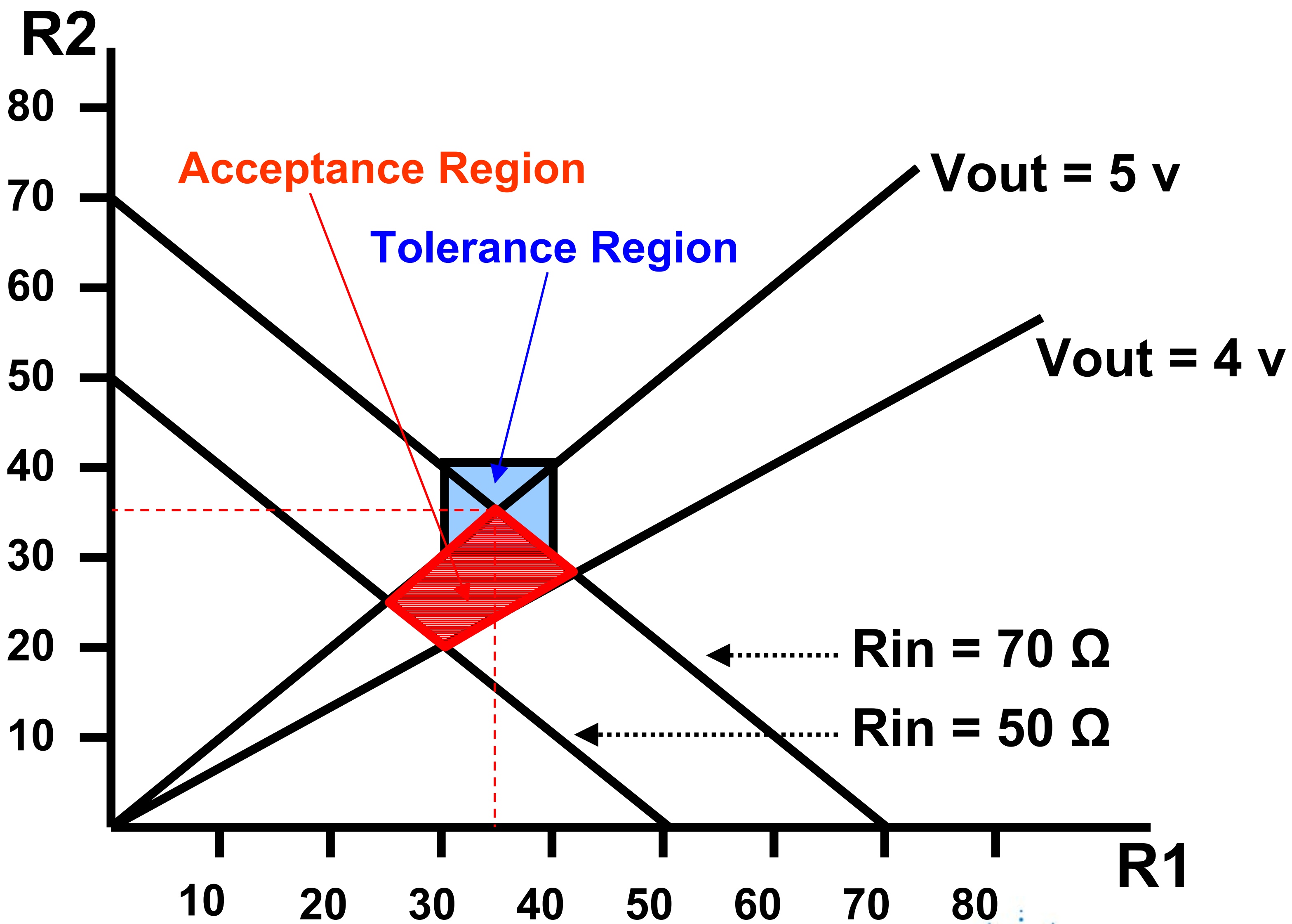
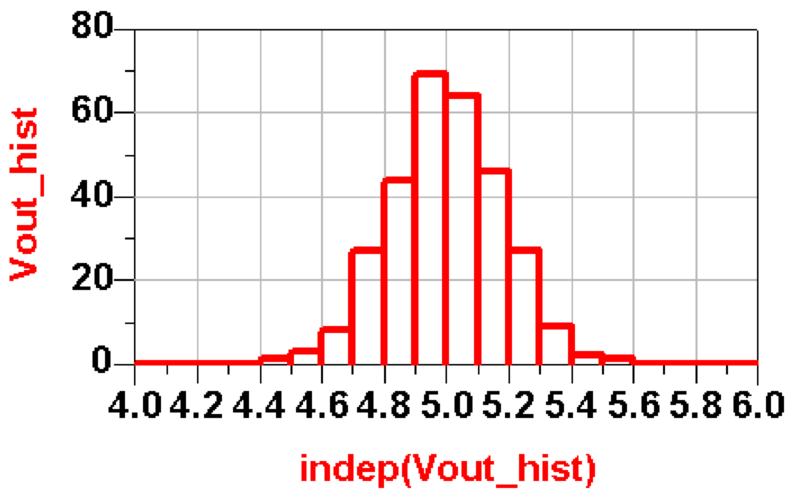
# Plotting the Tolerance and Acceptance Regions

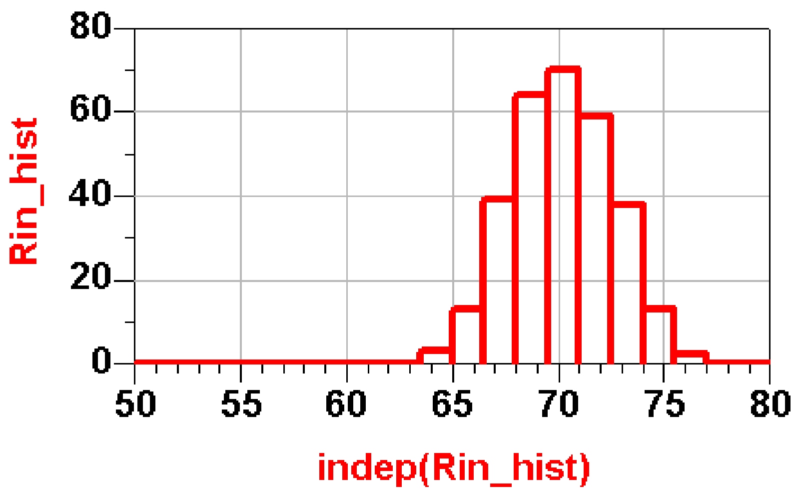


# Monte Carlo Yield Simulation Results

**MonteCarlo Yield Analysis on the Original Circuit**

| NumFail | NumPass | Yield |
|---|---|---|
| 231.000 | 69.000 | 23.000 |

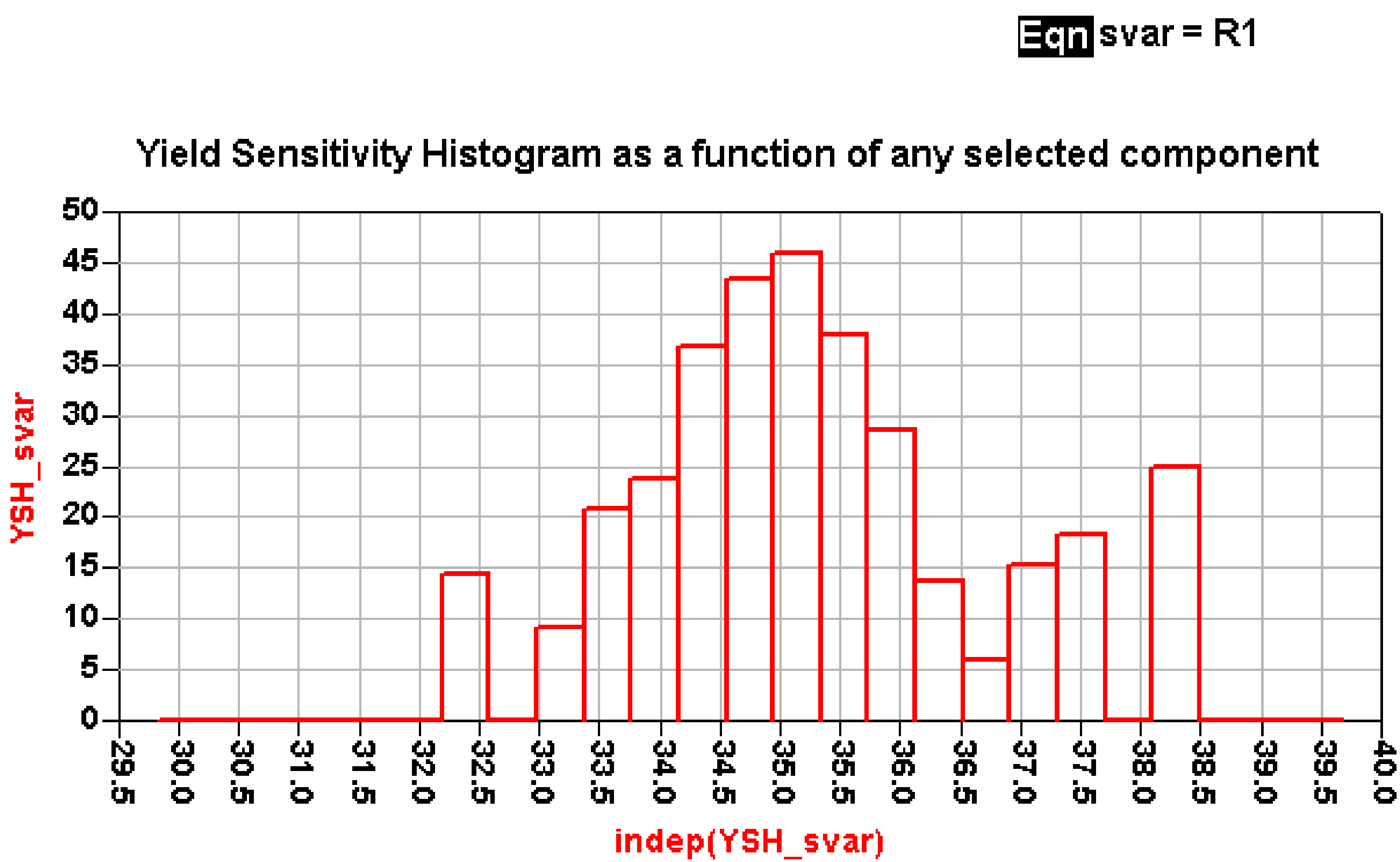


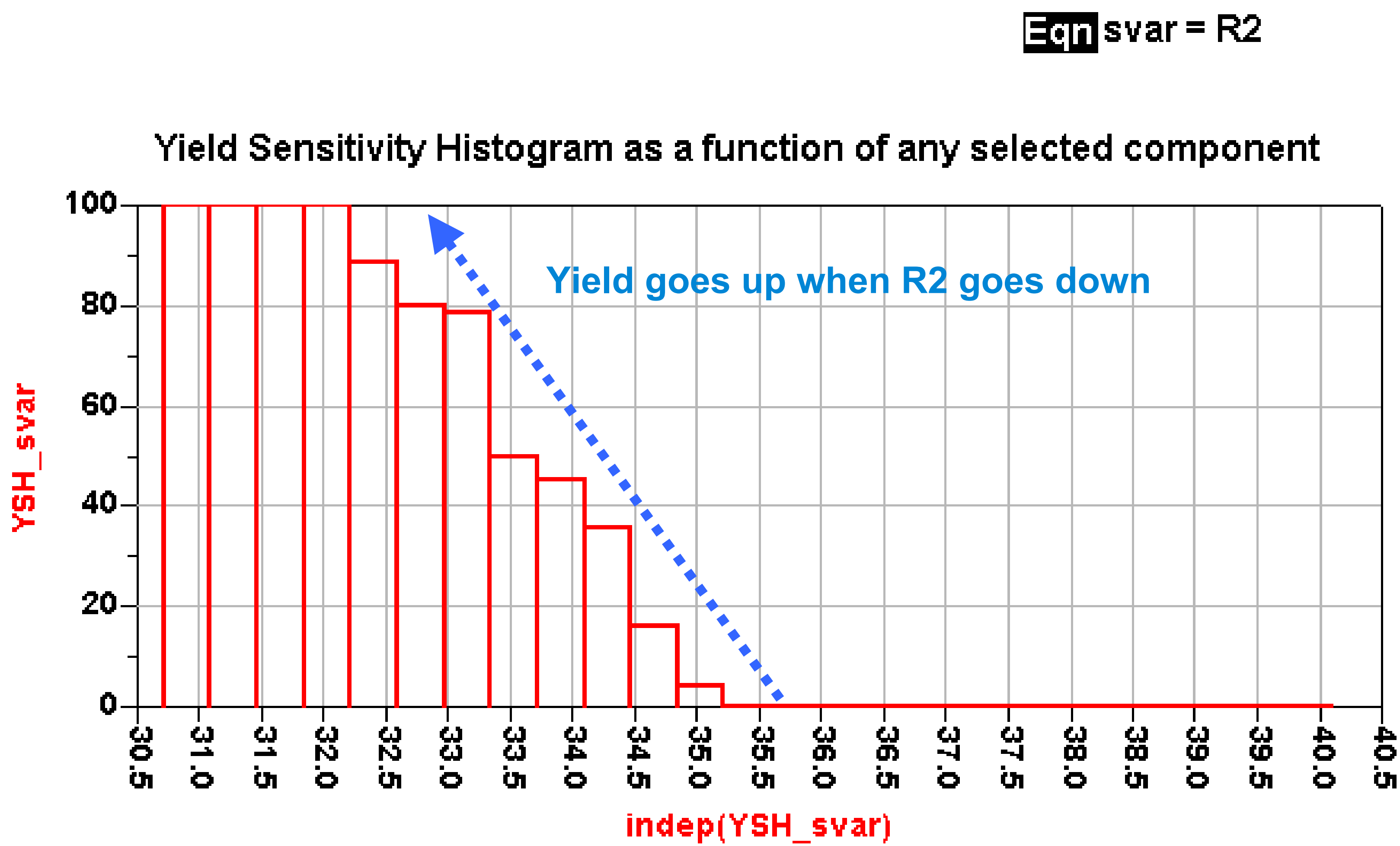

Eqn Vout_hist=histogram(Vout_Spec[0],20,4,6)

Eqn Rin_hist=histogram(Rin_Spec[0],20,50,80)

# Yield Sensitivity Histograms – R1



# Yield Sensitivity Histograms – R2



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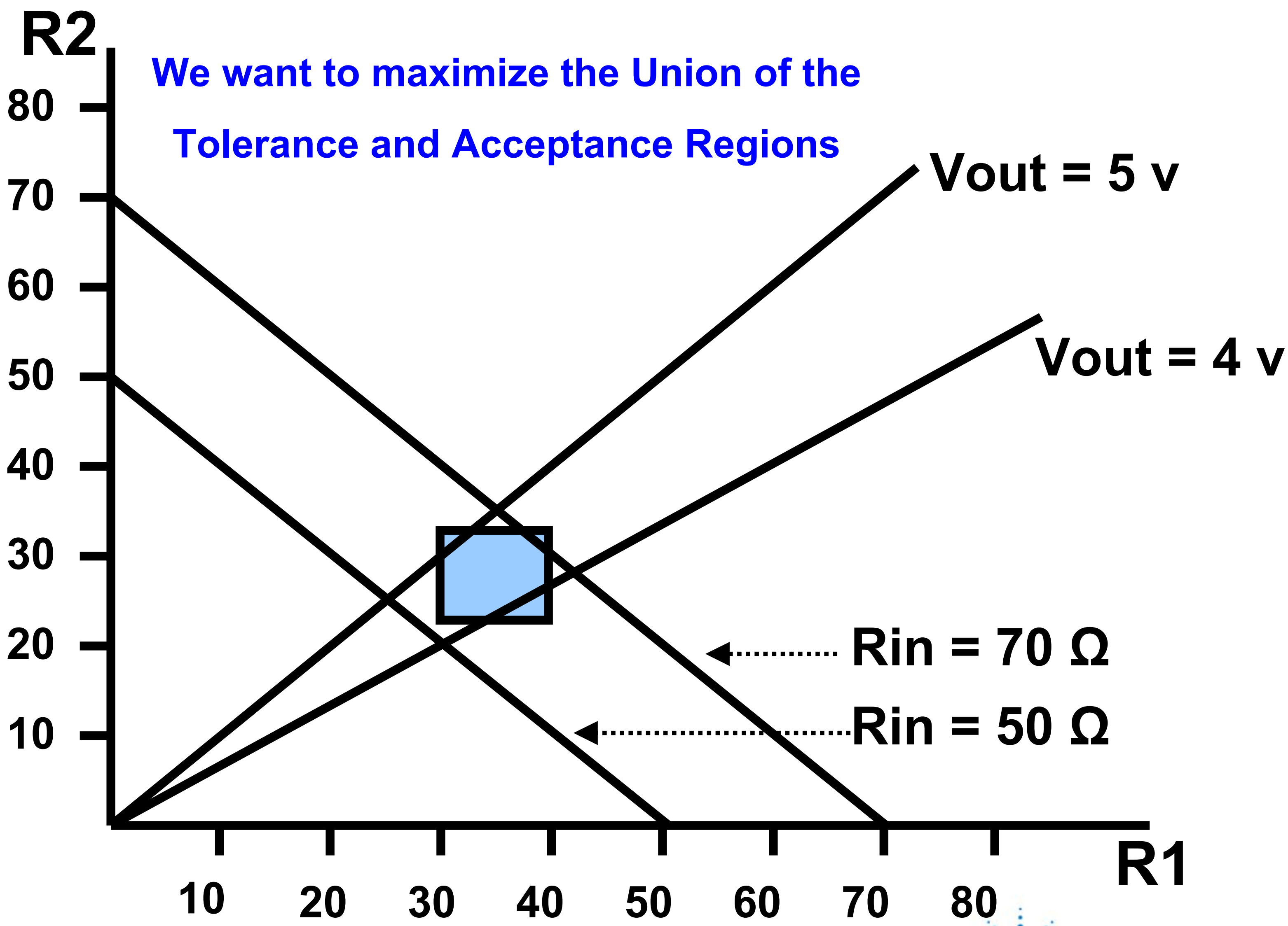
# Design Centering – Maximizing the Yield



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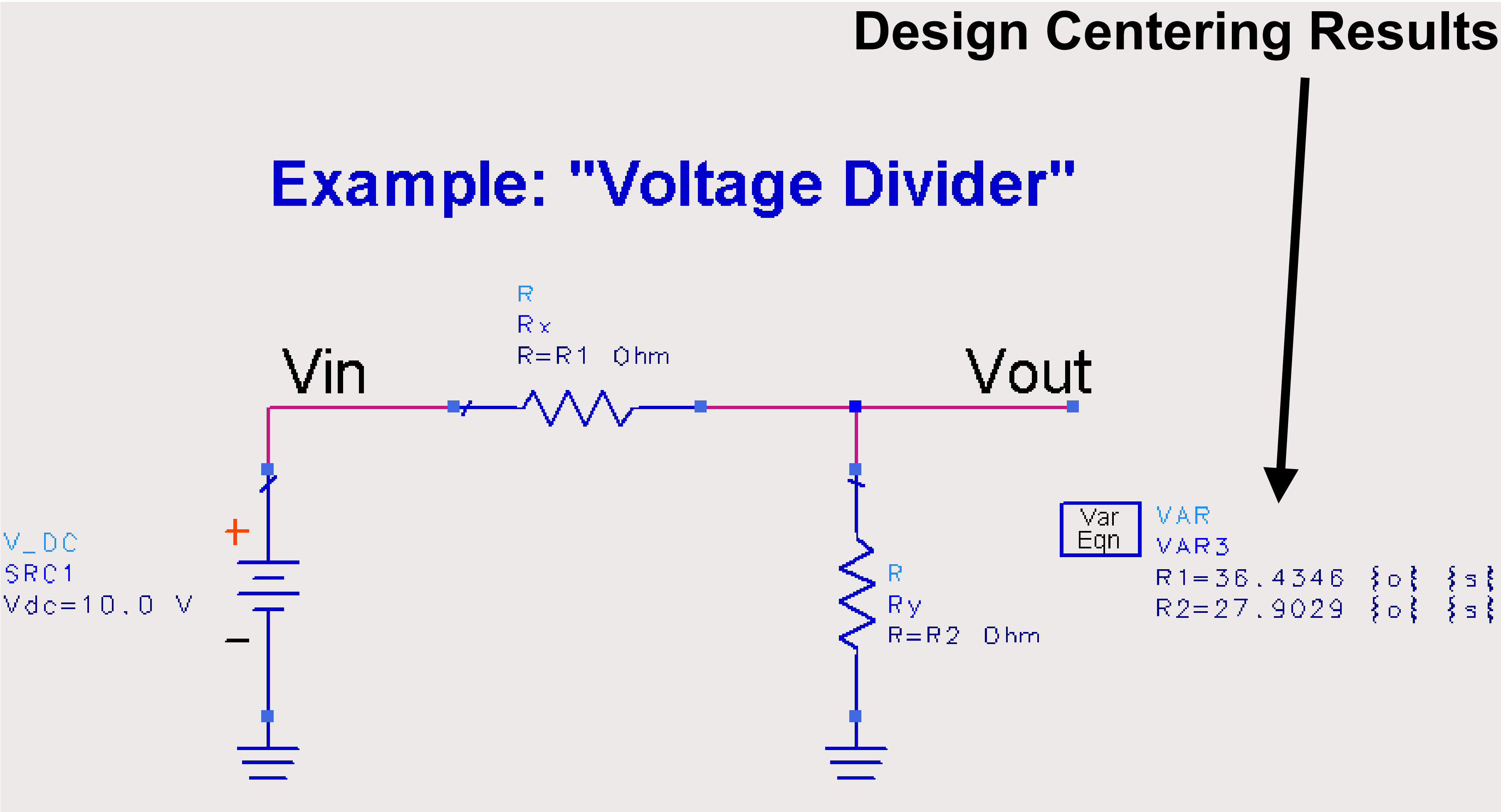
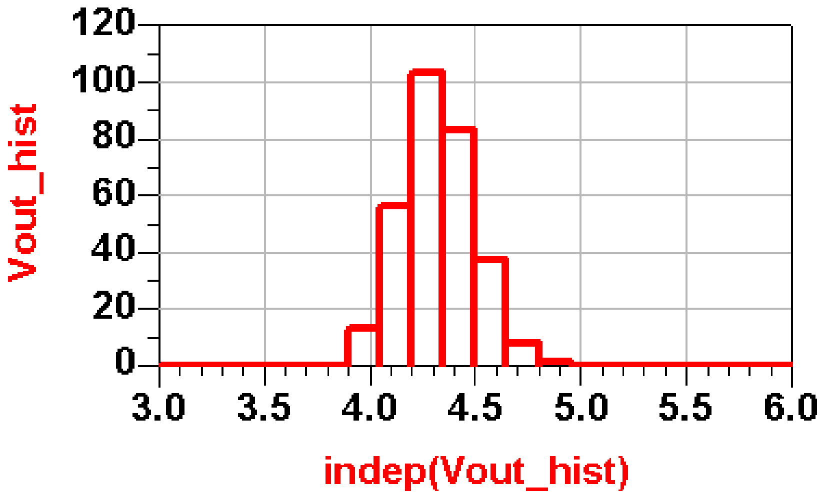
# Running “Yield Optimization / Design Centering”

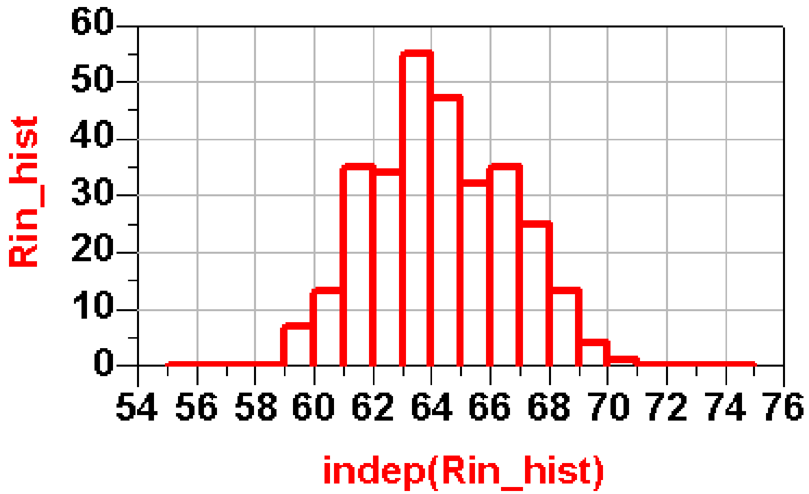


# Yield Sensitivity Histograms

**MonteCarlo Yield Analysis on the Centered Circuit**

| NumFail | NumPass | Yield |
|---|---|---|
| 13.000 | 287.000 | 95.667 |




Eqn Vout_hist=histogram(Vout_Spec[0],20,3,6)

Eqn Rin_hist=histogram(Rin_Spec[0],20,55,75)



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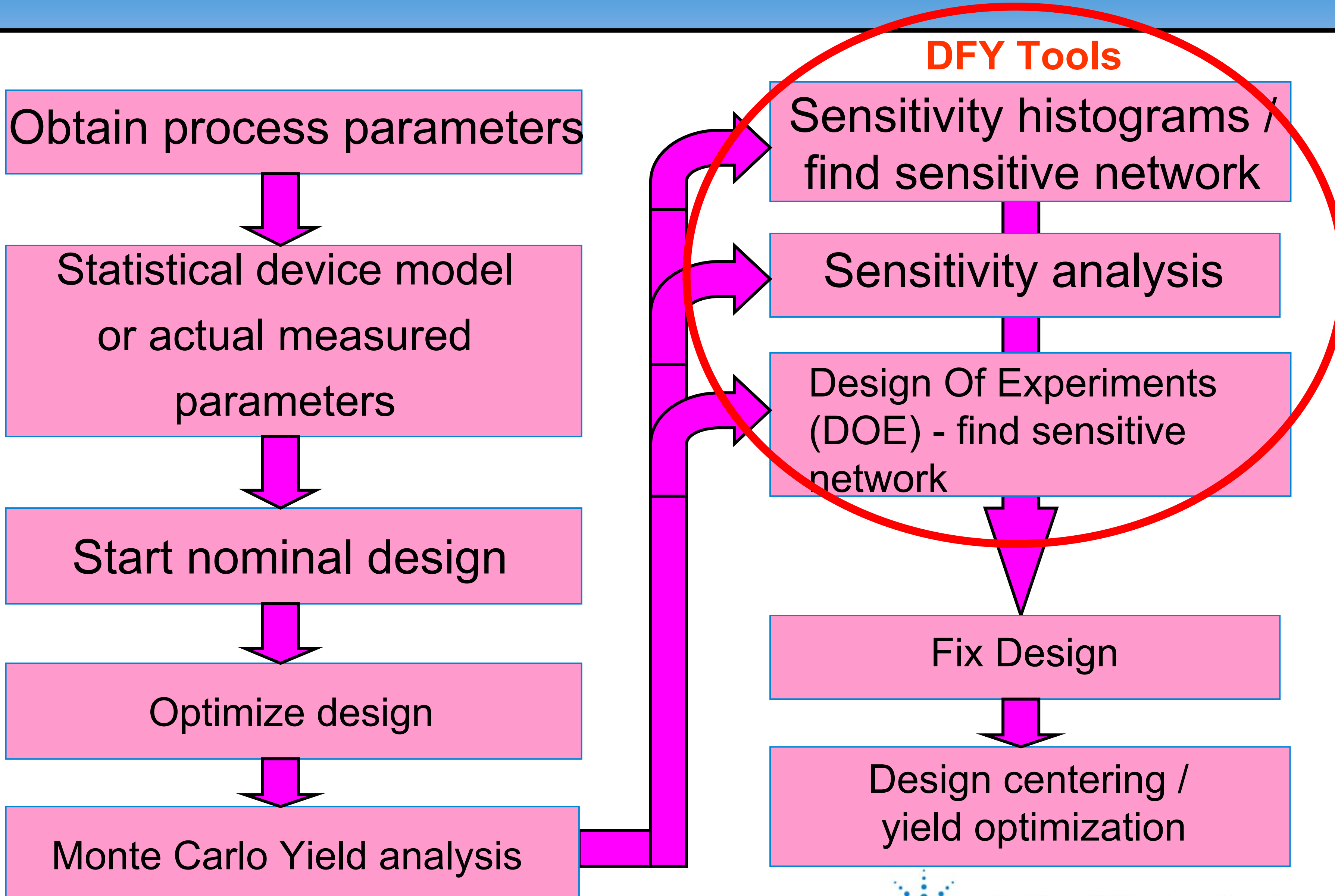
# The DFY Process for MMIC



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# DFY

- Design for nominal performance using performance optimization
- Find the yield
- Use YSH, Sens and/or DOE to find the problematic areas
- Fix them
- Perform Design centering
- Find the final yield.
- Fabricate – Sell – Make Tons of Money and be happy for ever!