Strategies for Designing Microwave Multilayer Printed Circuit Boards Using Stripline Structures

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Multilayer/Stripline Design Considerations Introduction

Brief History of Stripline Design

- ✓ 1964: Matthais, Young and Jones "bible" of microwave coupled circuits published
- ✓ Interim: PTFE substrates used in radome apps-suspended stripline and lumped element design realizations only
- ✓ Stripline on soft substrates developed on Long Island, NY
- ✓ 1974: Harlan Howe Jr "Stripline Circuit Design"
- ✓ 1970's: Woven glass reinforced PTFE laminates introduced
- ✓ 1990's: Development of 2-d and 3-d EM simulation software (ADS, Microwave Office, HFSS, etc.)
- ✓ Today: Reliable PTFE/multilayer materials and techniques allow for empirical realizations of simulated performance

Outline

- Stripline vs Microstrip….or both in one pwb?
- Broadside vs Edge Coupled Traces (Designers Perspective)
- Via Design…often the limiting factor at High Frequency
- Registration and effect on RF Properties
- Prepreg Characteristics to 40 GHz
- Fusion Bonding Thermoplastics vs Low Temperature Bonding with Thermosets
- Fabricating multilayers with PTFE and thermoplastic films
- Quick Word on Hybrid Multilayers….
- Thermal Reliability of thermoplastics vs thermosets
- Copper Roughness and effect on Line Widths
- Sequential Lamination

Stripline vs Microstrip

STRIPLINE

(1) Allows densification-multilayer designs

Can combine SMT amplifier and converter

Circuits with embedded couplers, filters,

Feed networks, external radiators, and dc

Power/digital control features in reduced size,

Streamline structures

(2) Eliminate cross talk between

multiple channels, more confined fields

(3) Stripline EM field distribution is

more symmetrical offering better control

over even/odd mode impedances

(5) Striplines don't radiate as readily and

Exhibit better RF confinement…less

Propensity for intercavity oscillation

(6) Broadband; multioctave couplers and filters

MICROSTRIP

(1) Lower cost, cheaper fabricators

(2) Can be tuned, stripline can't

(3) In Microstrip one worries that the grounds

are properly brought to the ground layer

(4) Microstrip doesn't have concerns of

prepreg variation, easier to fabricate

STRIPLINE WITH MICROSTRIP

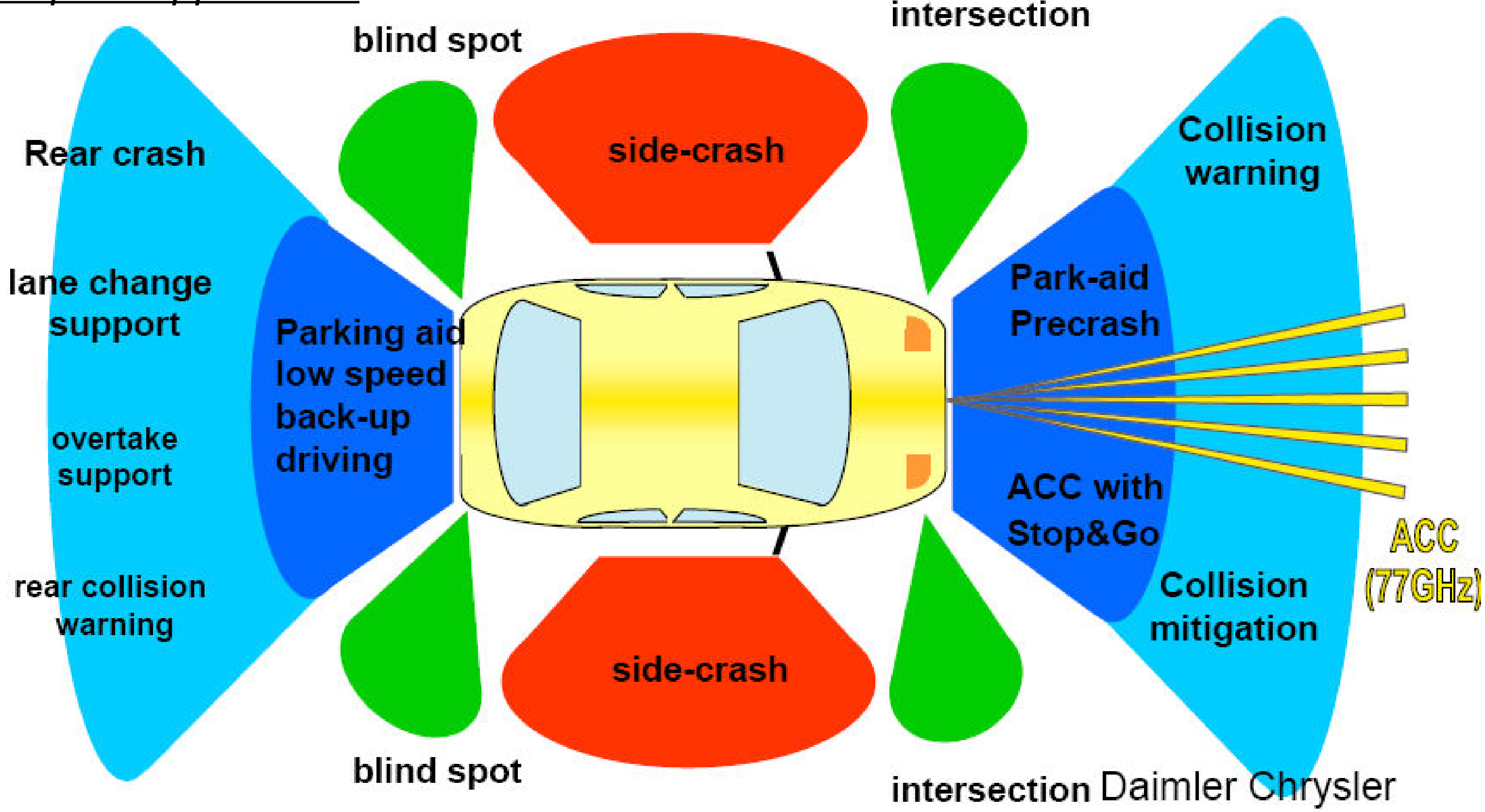
(1) Combining the benefits of both approaches

(2) Power amplifier can be put on surface

in microstrip with capacitors, transistors, resistors ect,

Automotive Radar (Adaptive Cruise Control @77 GHz)

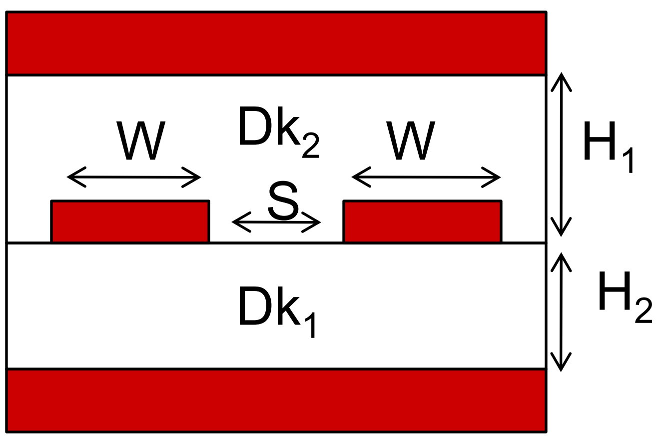
typical stripline application:



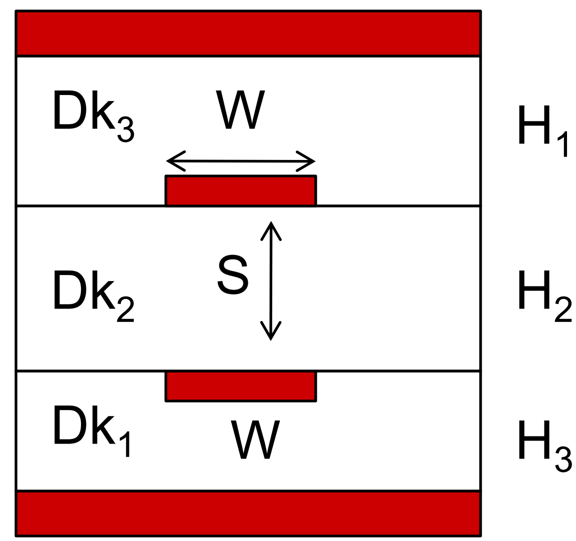
Stripline – you might be combining many radiating elements with multiple feed elements
Radiating and receiving at high frequency where you need the lowest loss feed to the radiators
(suspended striplines also common for 24-26GHz…air bag deployment)

Edge Coupled vs Broadside

Edge Coupled



Broadside Coupled



Coupling driven by etching Tolerance (0.5 to 1 mil)

(1) Coupling driven by core thickness tolerance in typical RF app.
(2) Puts burden of registration from top to bottom layer on core for simple RF pwbs
(3) For many layer digital apps the S distance will have to be controlled by both cores and prepregs….need very tight fabrication
(4) Uses more PWB real estate
(5) More asymetrical – signal via drives to deeper depth on one signal layer.

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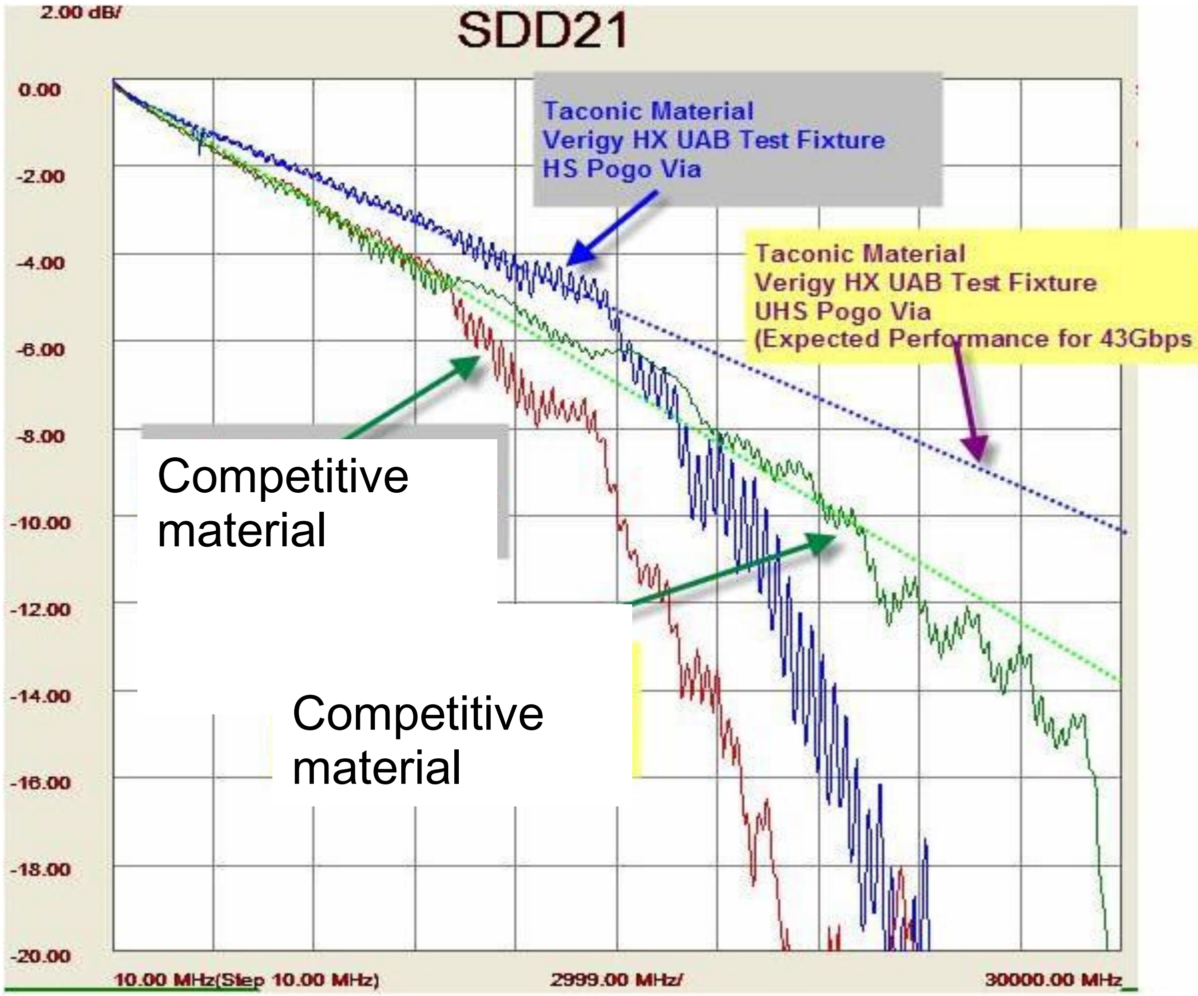
Via Design

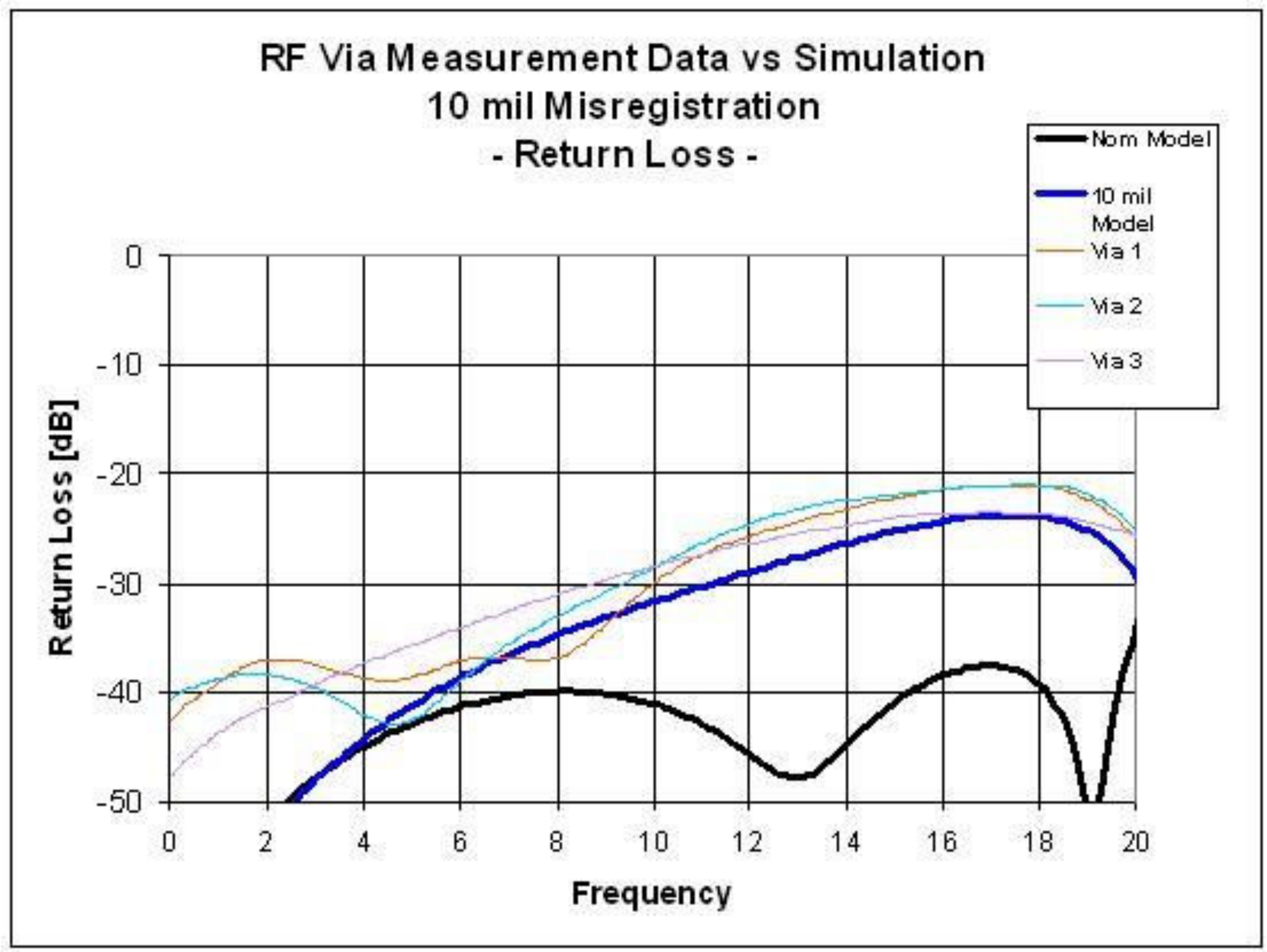
Optimized Vias vs Non Optimized Vias

(Smooth transition through via should not cause S21 rolloff)

measured



An optimized via should show no roll off of S21 with frequency and no impedance Spikes by TDR



Provided by Anaren Microwave

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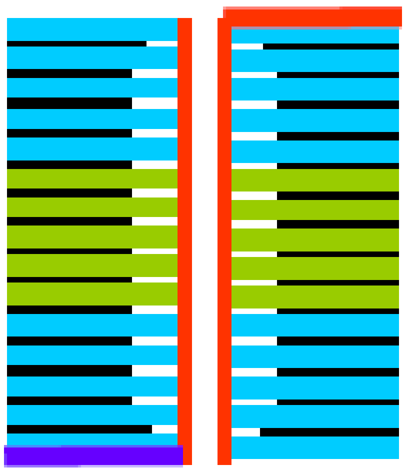
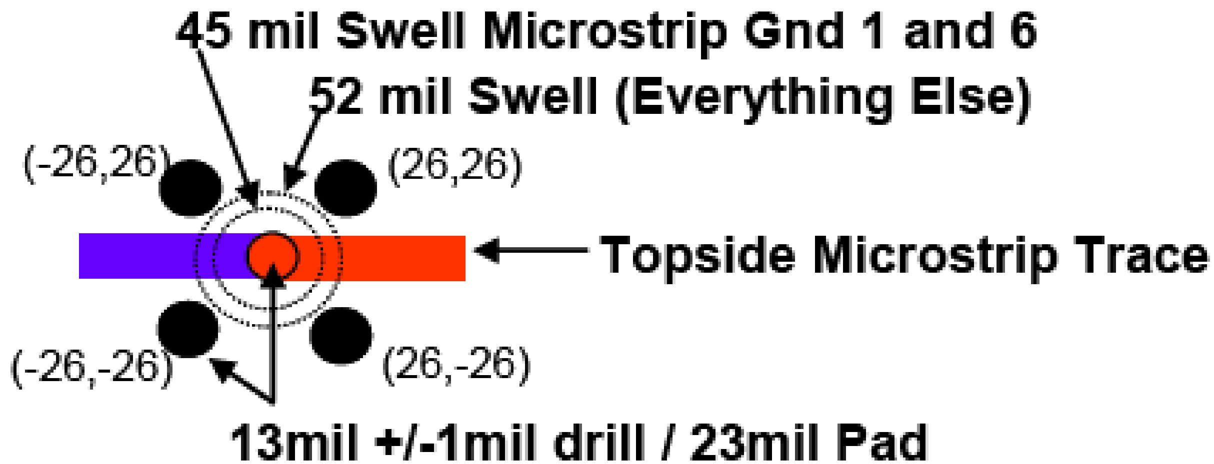
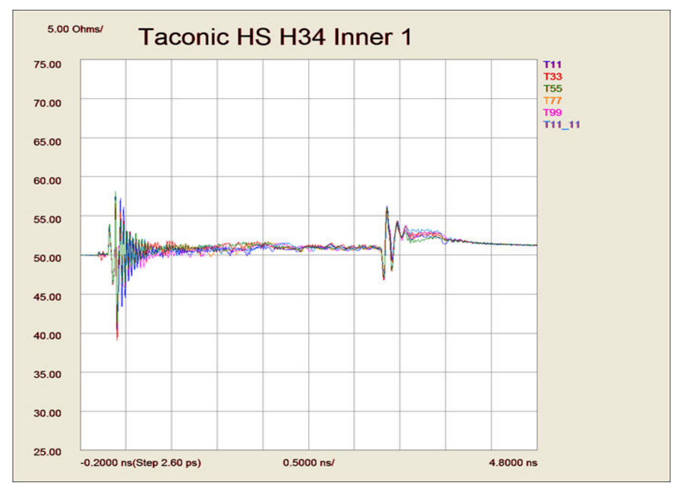
Via Design for Semiconductor Test

Verigy (former Agilent) Optimized Via – Heidi Barnes



Through Via



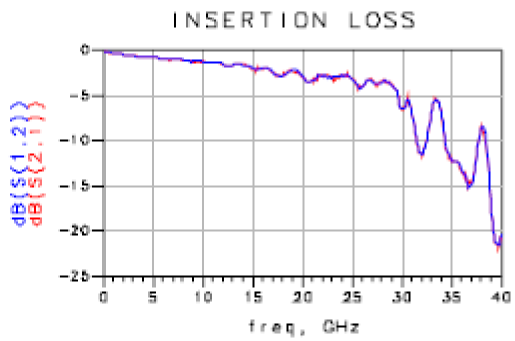


Variables:

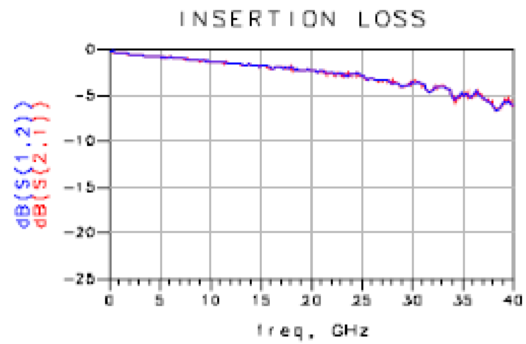
(1) Number of ground vias (4 vs 6?)
(2) Size of pads and anti pads
(3) Distance of pad to antipads on grounds
(4) Thru via vs back drilled via vs blind/buried via

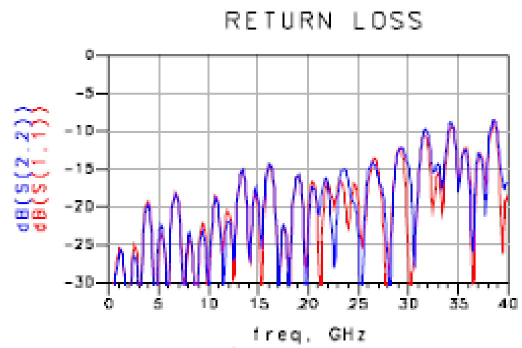
Verigy Optimized Via

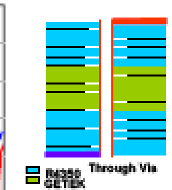
Non optimized

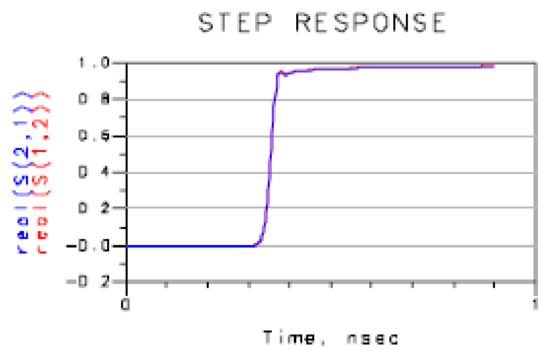


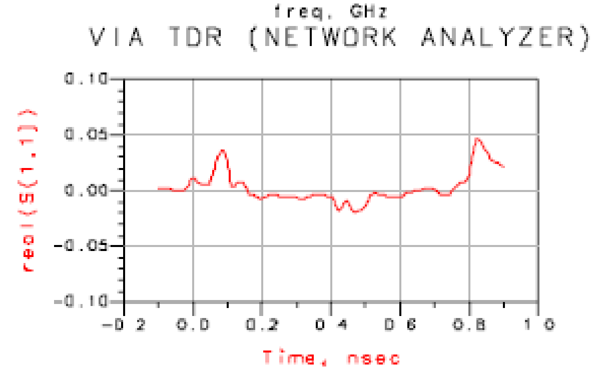
optimized

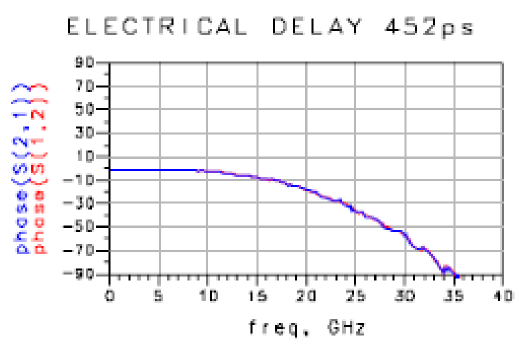


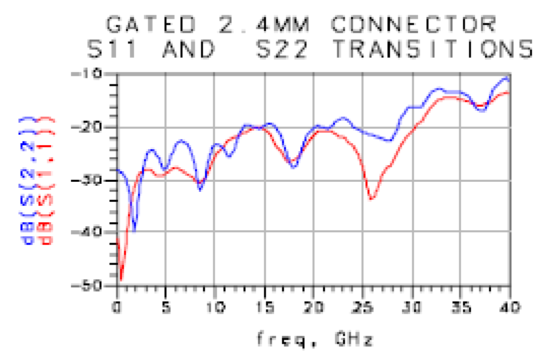












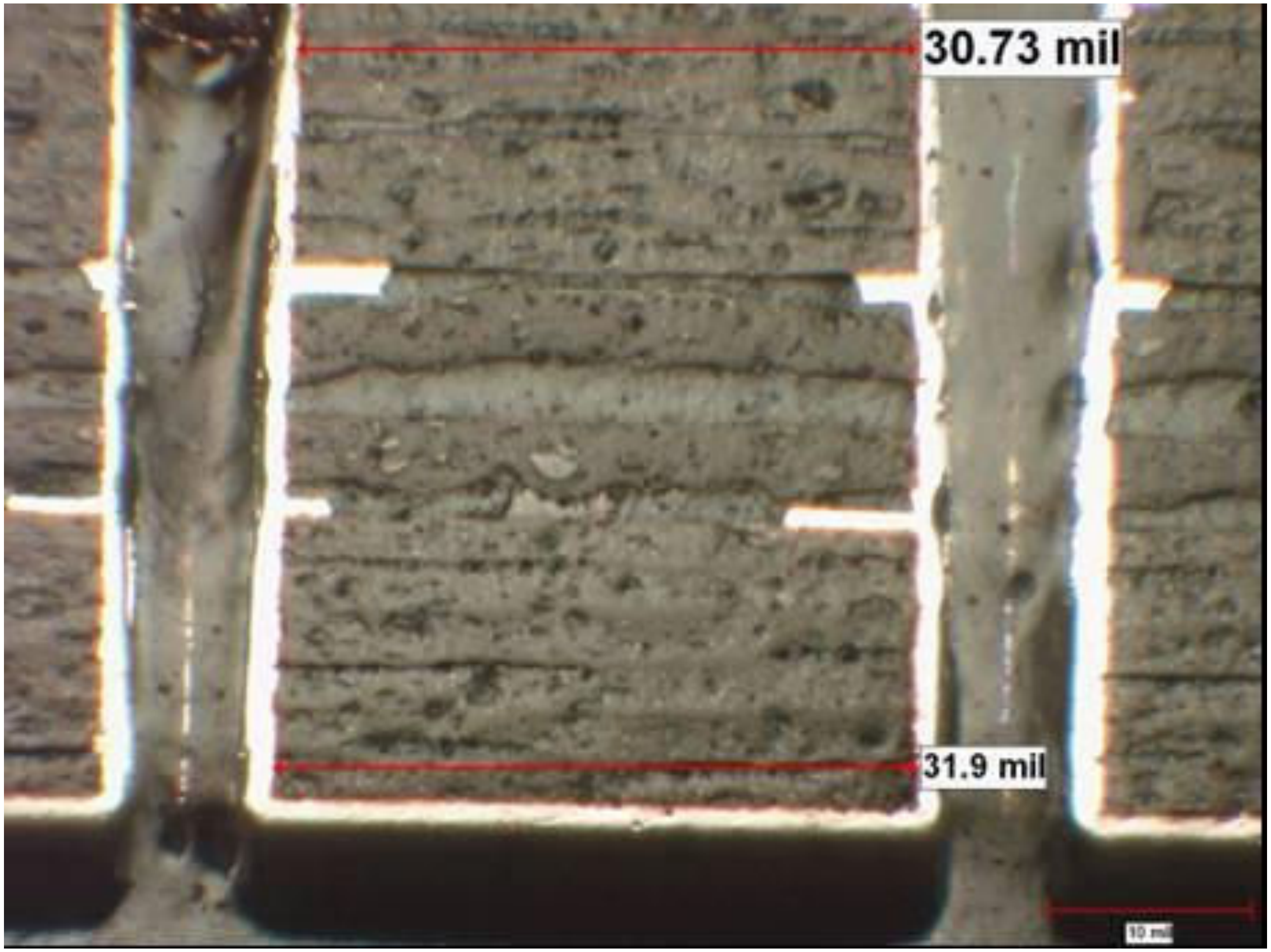
Measured by Heidi Barnes at Verigy

Dimensional Stability

Registration

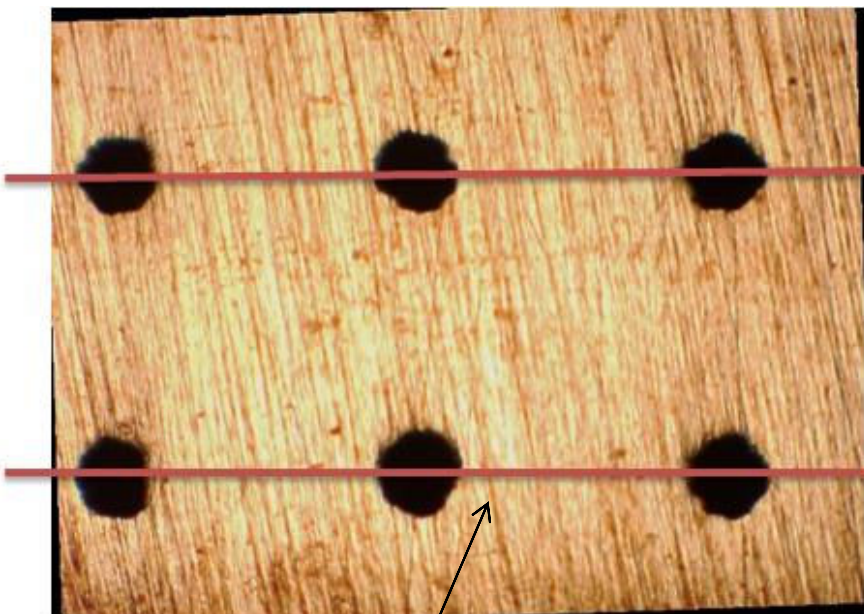
RF Properties

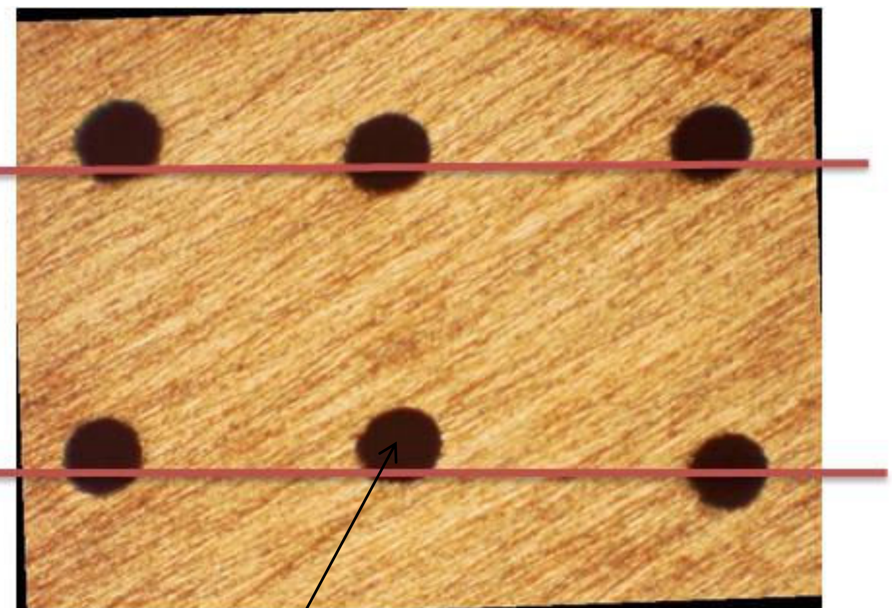
Poor Registration Around Pads



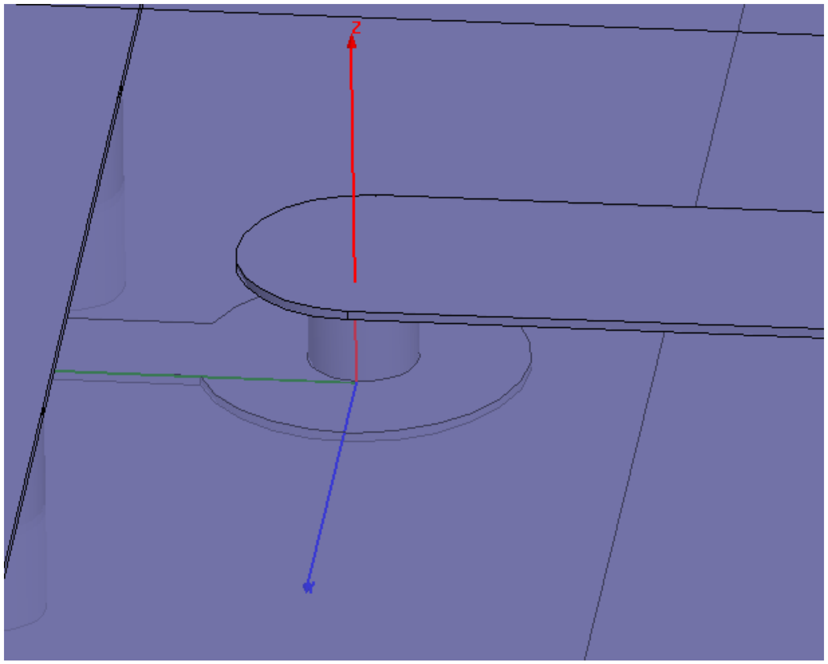
Factors Leading to Poor Registration

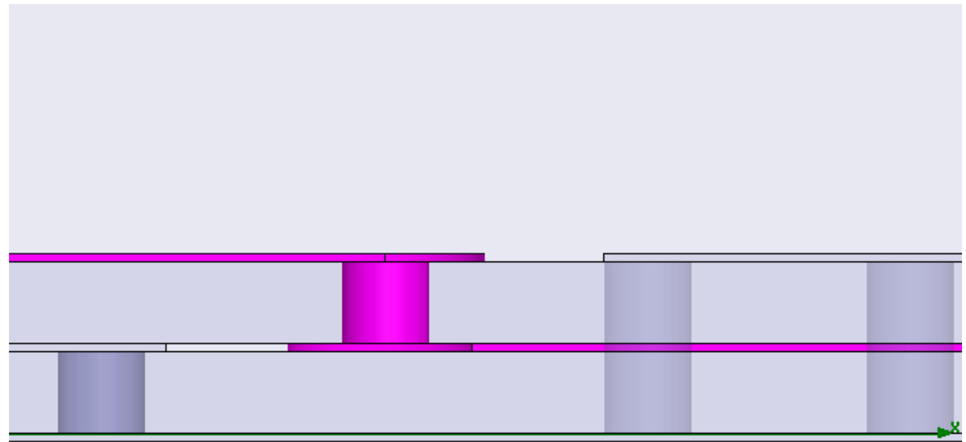
(1) PWB Thickness and drill deflection
(2) Dimensional stability of core
(3) Dimensional stability of core at lamination temperature
(4) Dimensional stability/melting of prepreg during drilling

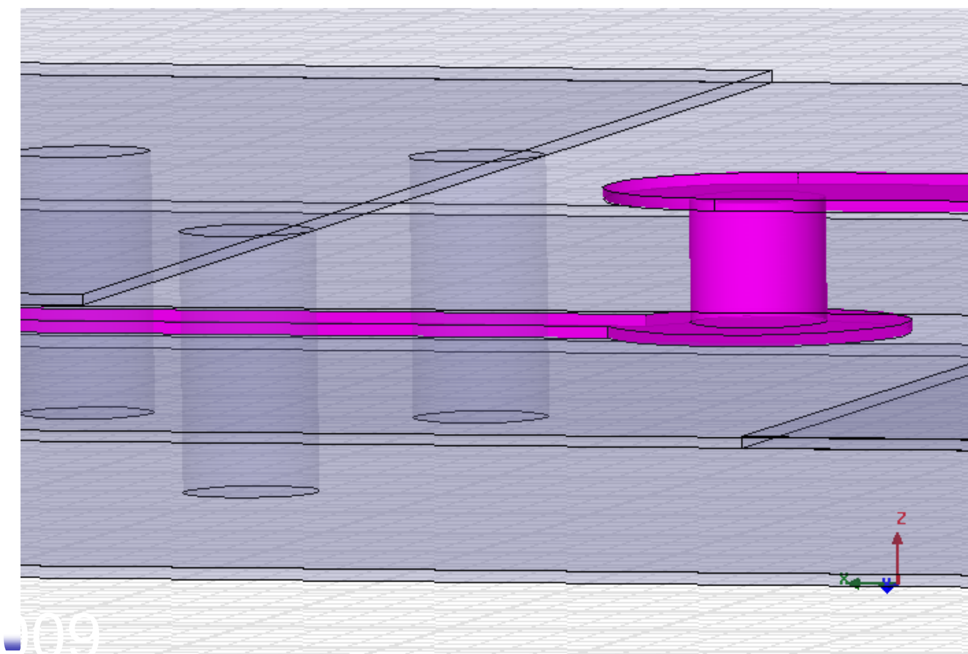




HFSS Simulation of 50 Ohm Microstrip to Stripline Via Transition

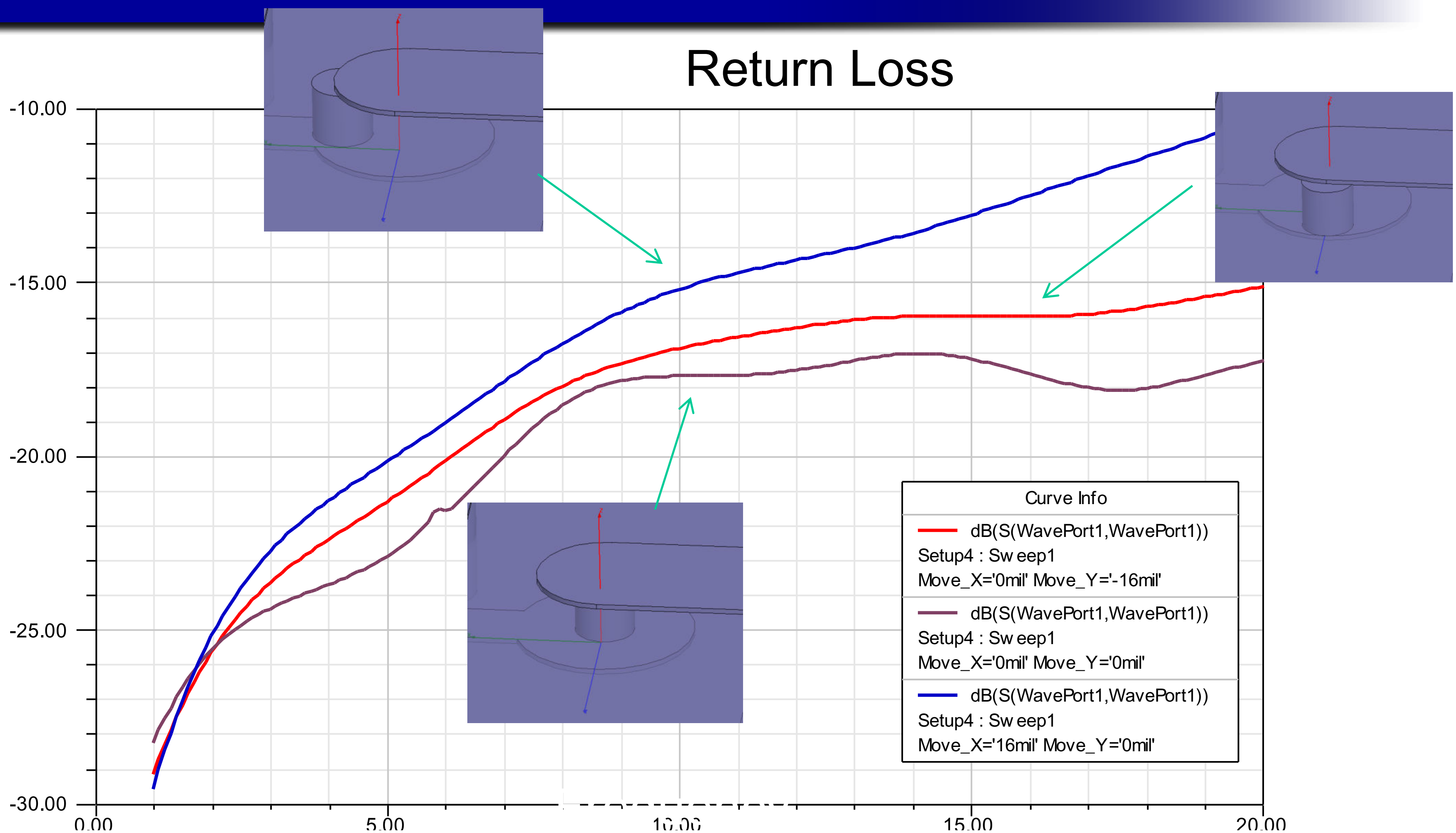






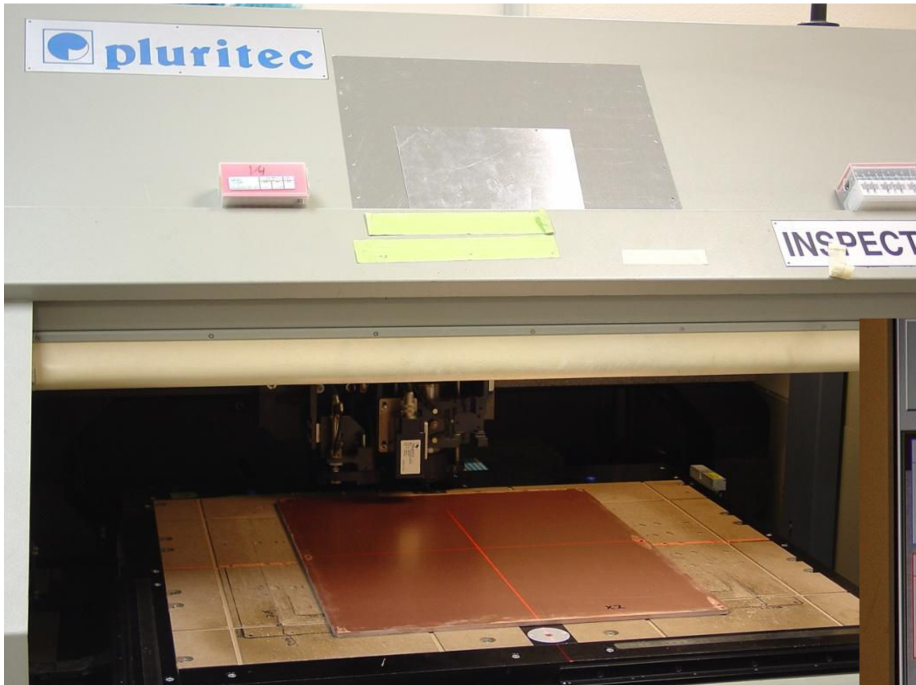
-Taconic TSM-30 dielectric, each of two sections is 0.015” in height
- 1 oz Cu
- Microstrip linewidth is 0.036”
- Stripline linewidth is 0.0165”
- Via diameter is 0.016”
- Pad diameter is 0.036”

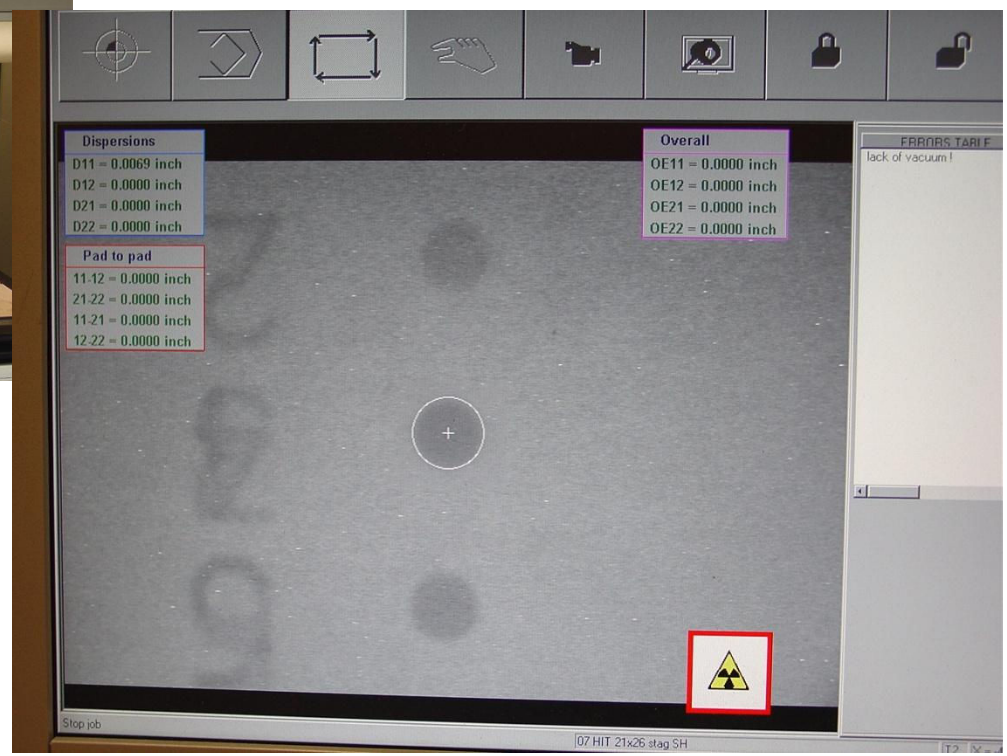
HFSS Simulation of Microstrip to Stripline 50 Ohm Line Input



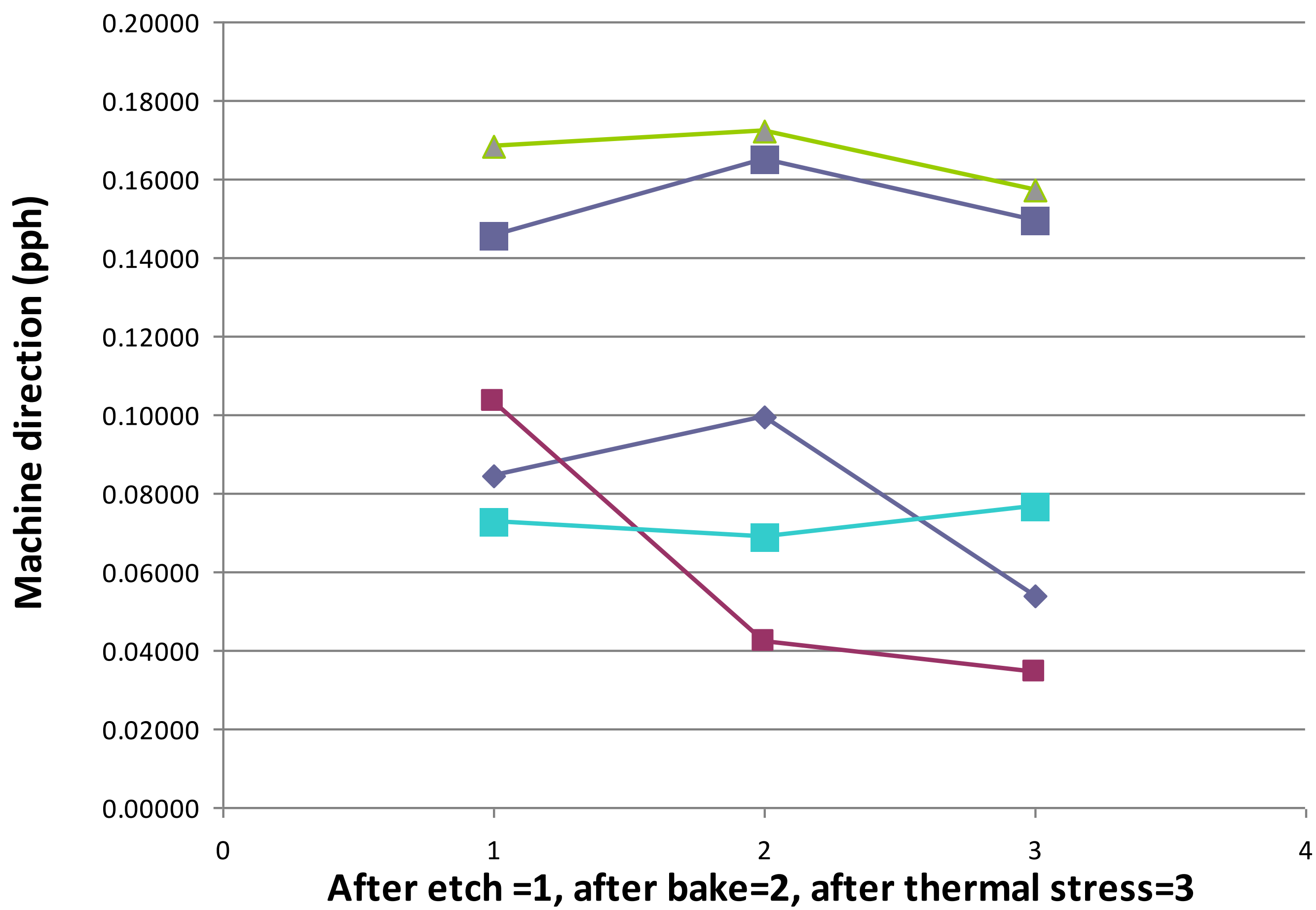
Courtesy of L3 Narda

Ensuring Via to Pad Registration

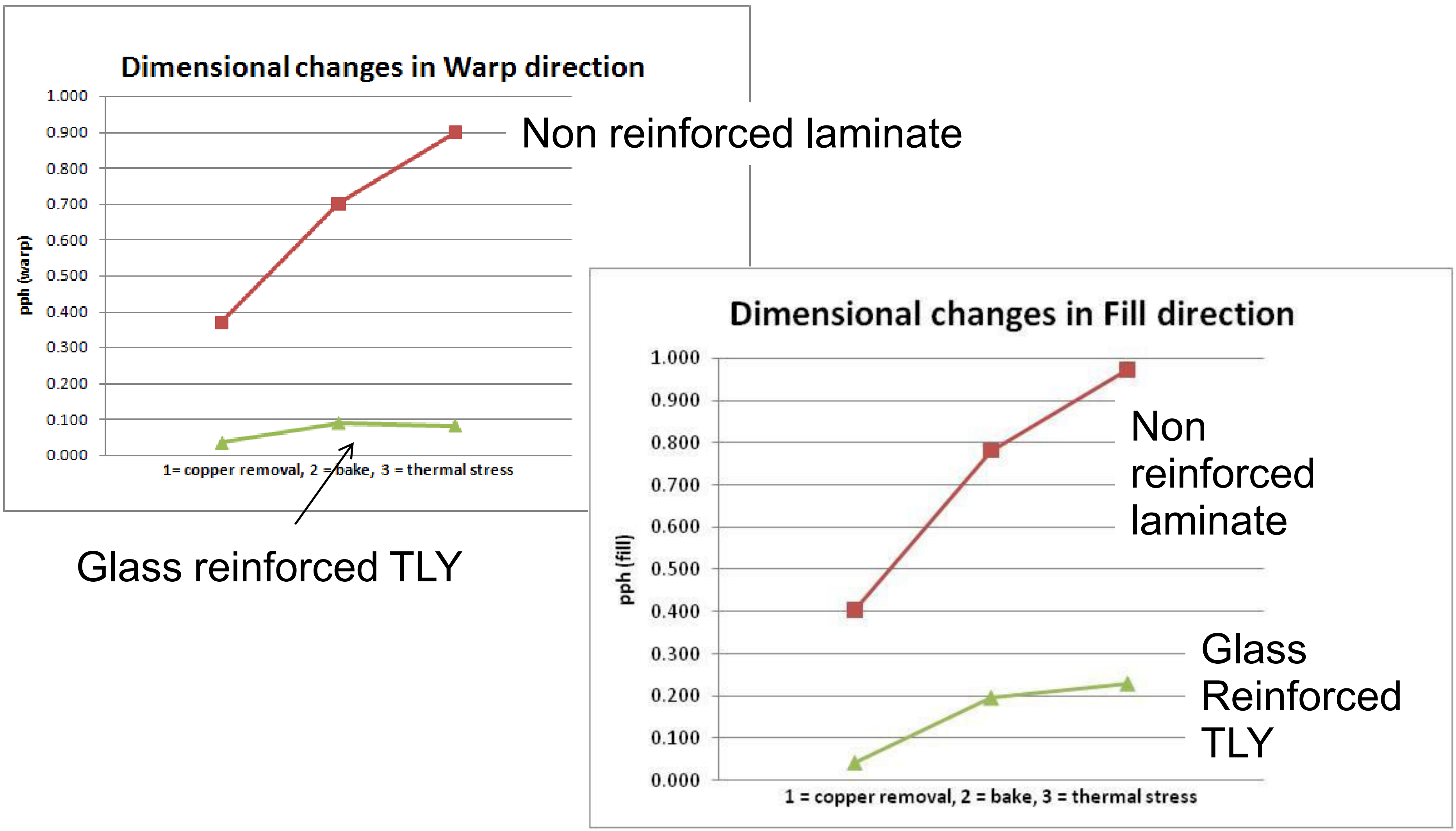




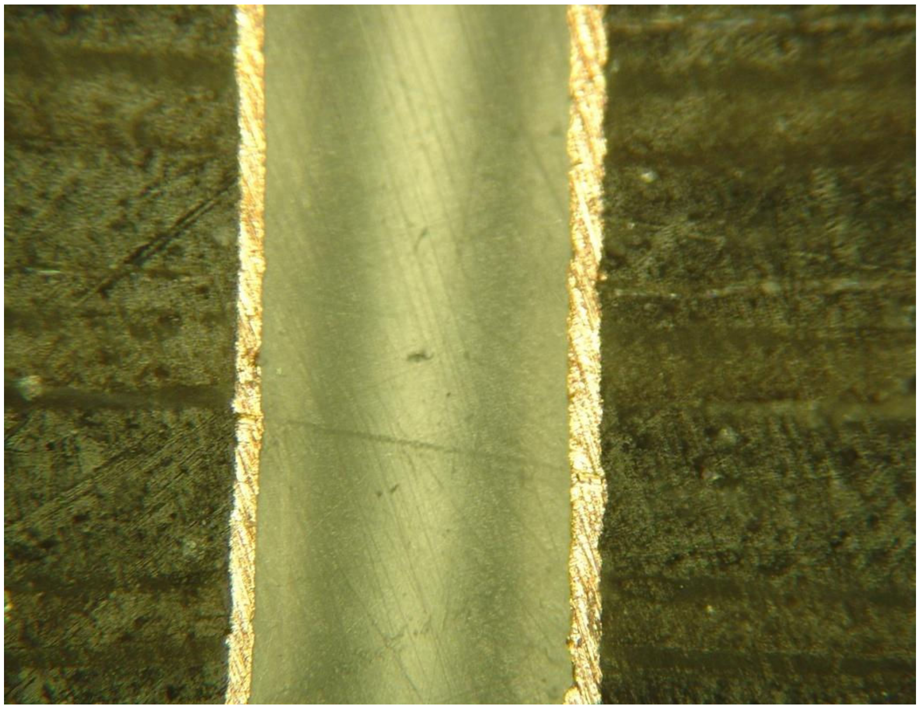
Dimensional Stability Optimization of Copper Clad Laminate Core

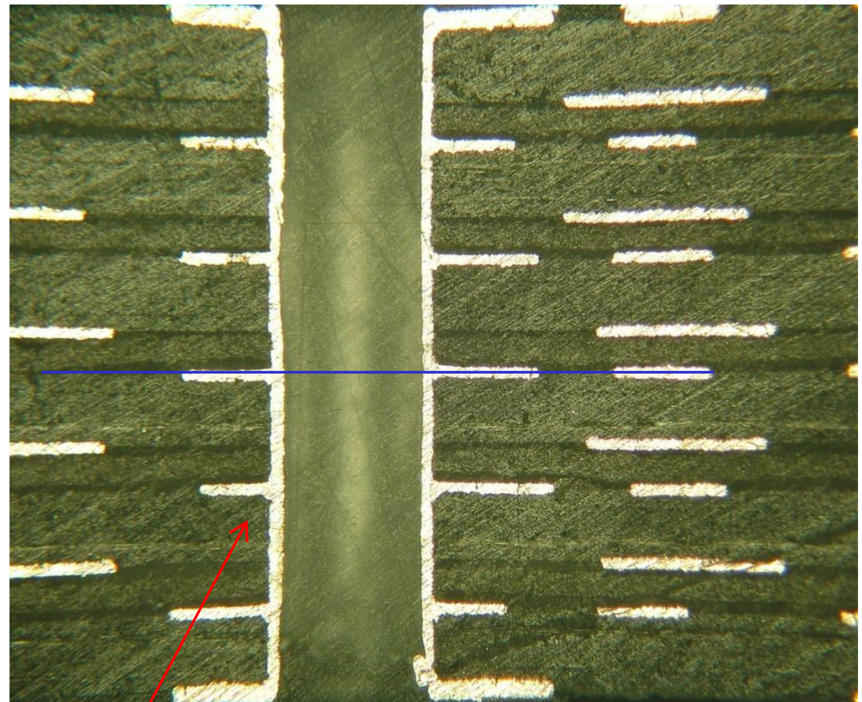


Dimensional Changes in Glass Reinforced TLY vs Non Reinforced Laminate



Ceramic filled PTFE/fastRise27 low temperature thermoset lamination





Almost no fiberglass reinforcement

Good layer to layer registration, no pad distortion

Registration consistency of Dimensionally Stable Core

Values are mils/inch

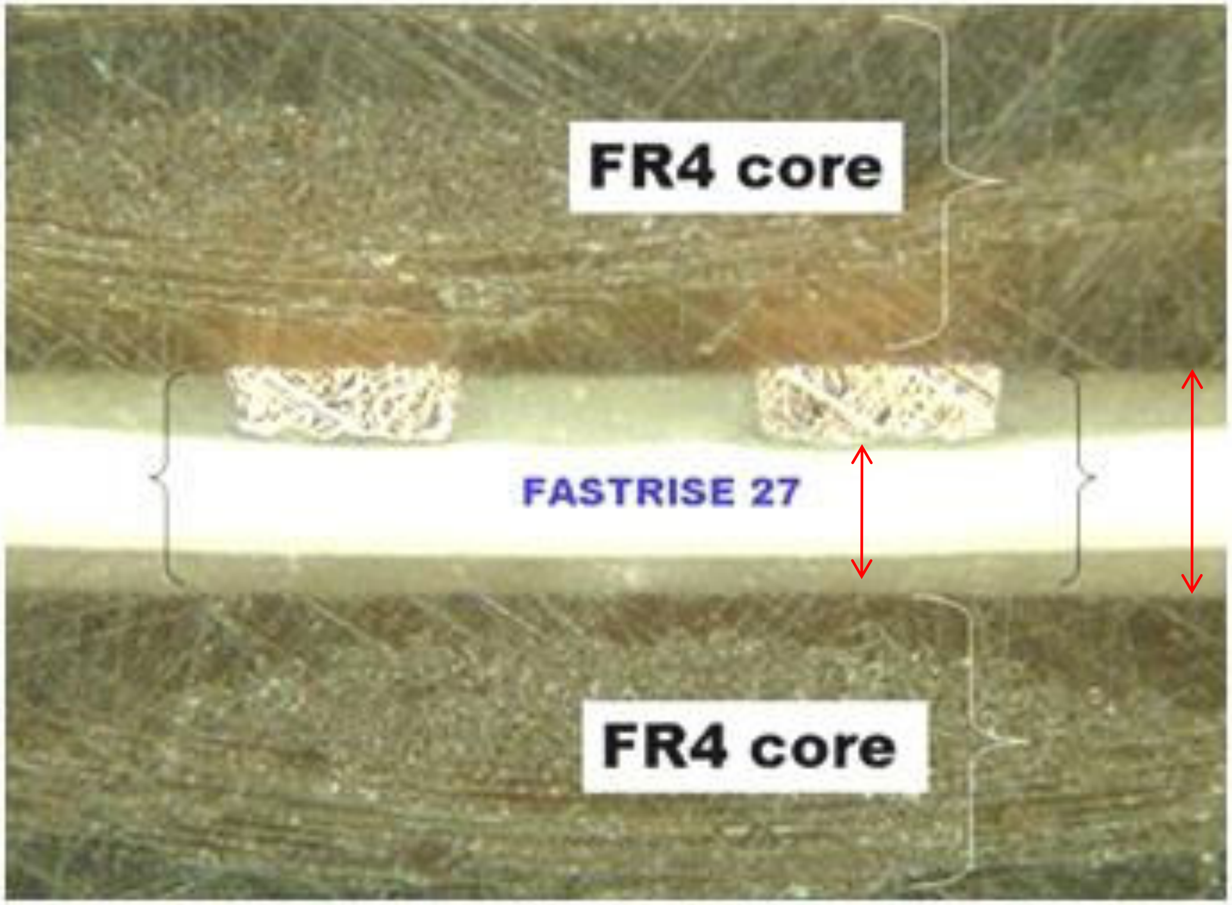
CORE	Calculated Scale factor x	y
	1.0009	1.0004
1	1.00132	1.00038
2	1.00013	1.00029
3	1.00016	1.00026
4	1.00019	1.00025
5	1.00022	1.00027
6	1.00022	1.00026
7	1.00022	1.00027
8	1.00021	1.00075
9	1.00019	1.00072
10	1.00018	1.00072
11	1.00020	1.00072
12	1.00023	1.00028
13	1.00024	1.00029
14	1.00024	1.00027
15	1.00022	1.00037
16	1.00022	1.00034

1.00021 1.00029

The key is layer to layer consistency

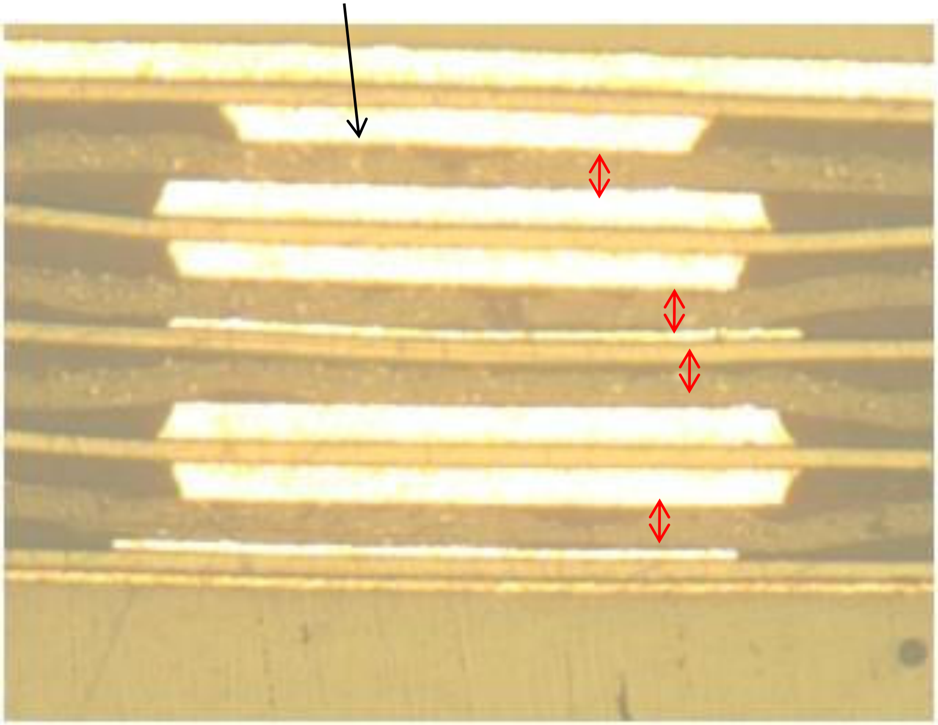
Prepreg Thickness Variation

Prepreg Dielectric Thickness Variation

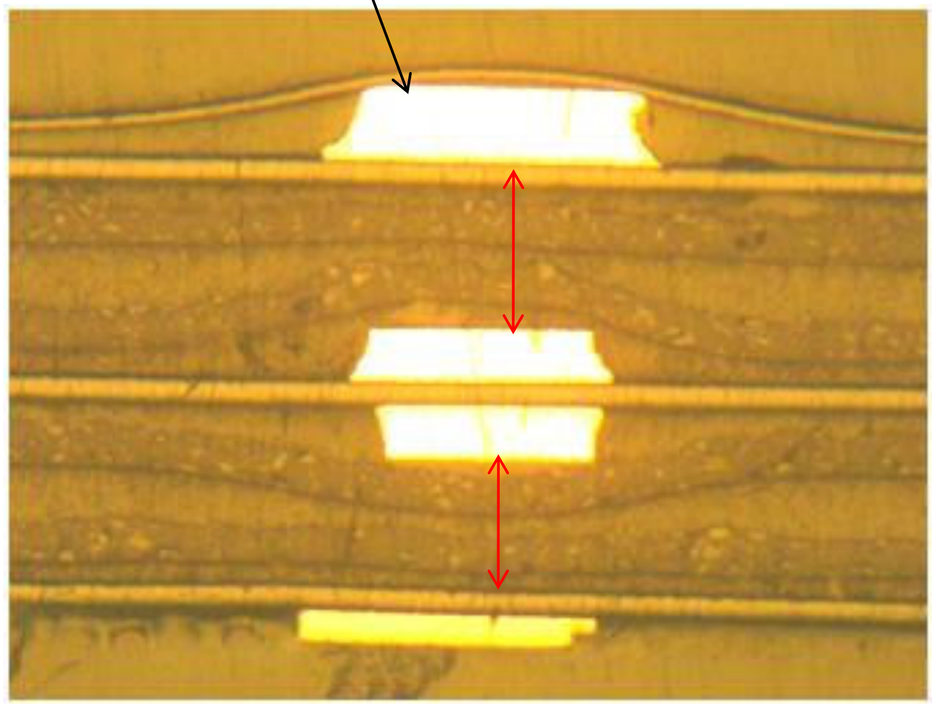


Dielectric Thickness spacing of prepreg will vary with artwork – the amount of copper etched, the thickness of the copper etc.

Prepreg Filling Difficult Circuitry



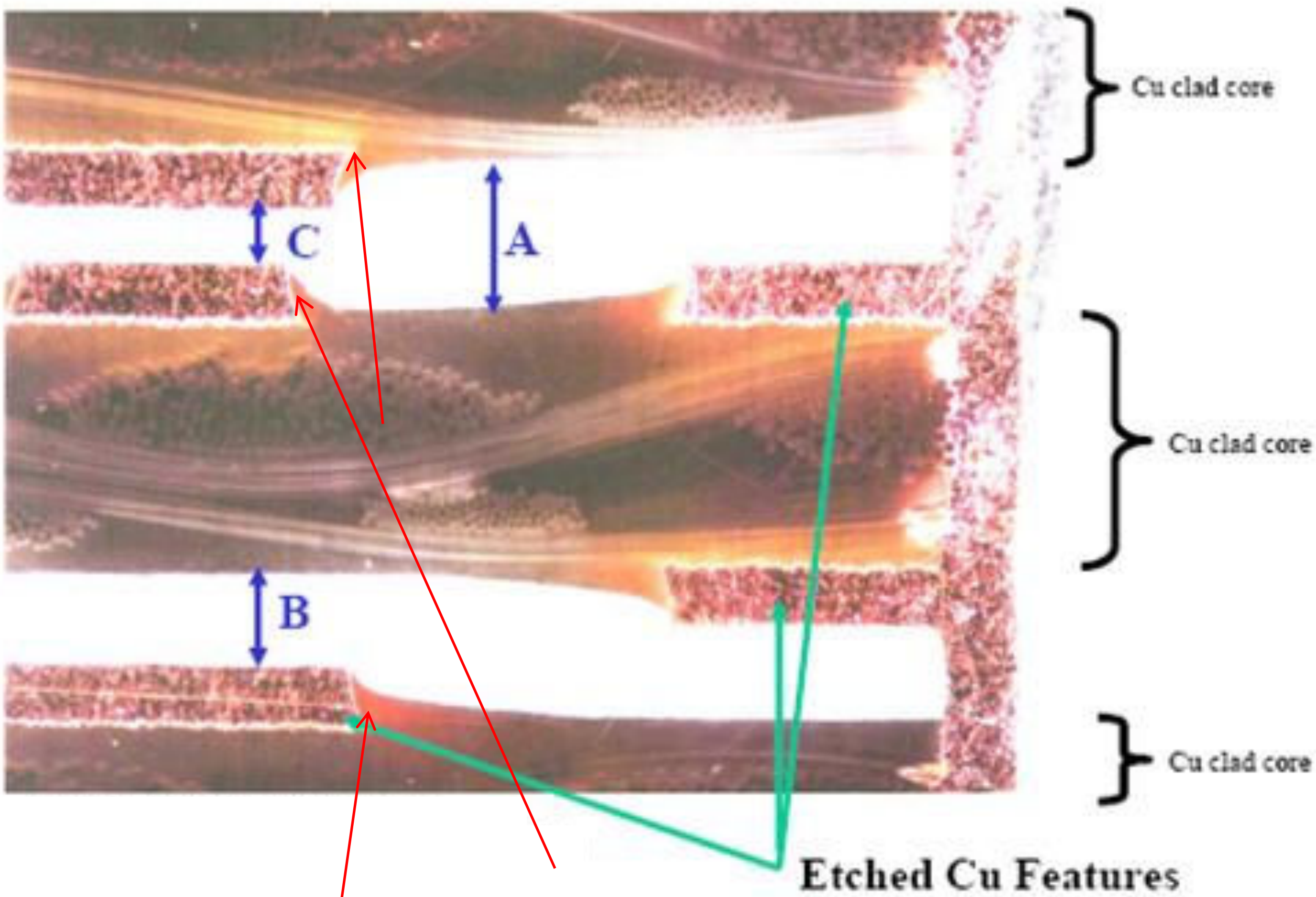
One ply fastRise27 prepreg



2 plies fastRise27 prepreg

Lamination pressure and stacking of artwork affect flow and final prepre Thickness.

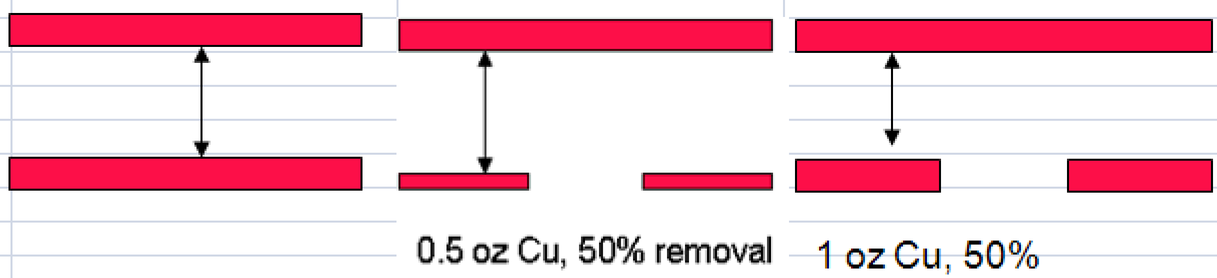
Variations in Dielectric Thickness



There can be variations in dielectric constant – pure resin or voids?

Predicting Dielectric Thickness of Pressed Prepregs

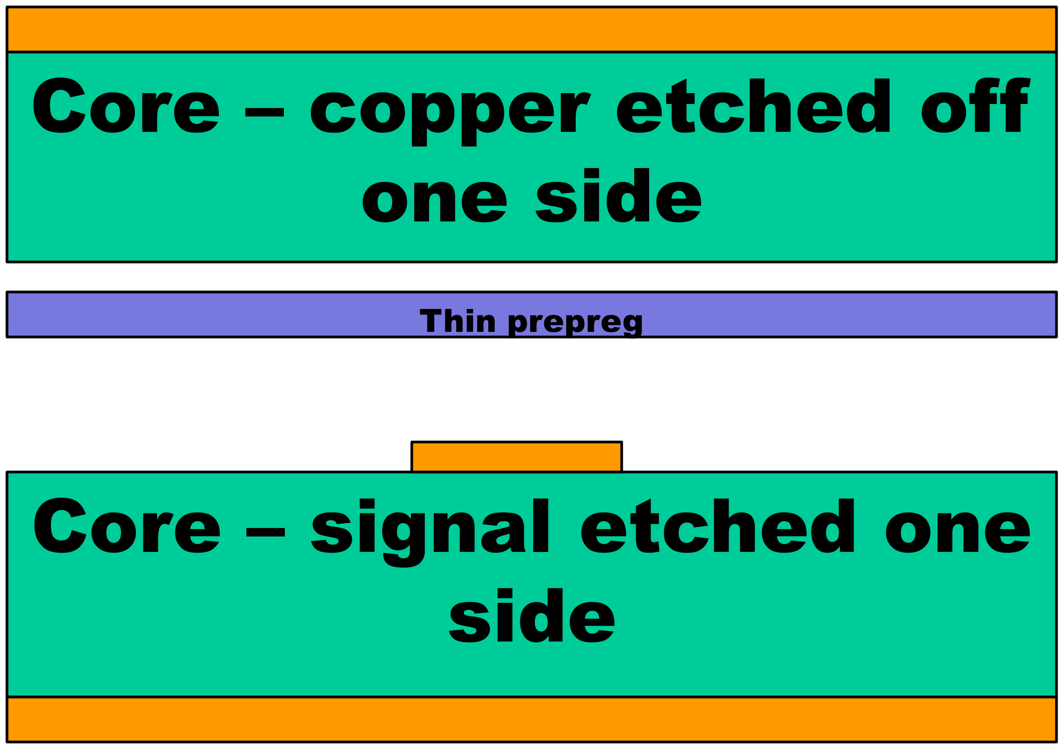
	Pressed Thickness (mil)	Pressed Thickness (mil)	Pressed Thickness (mil)
FR270030-25	3.5	2.13	1.82
FR270040-25	4.9	3.74	3.51
FR27-0045-35	5.8	4.61	4.23
FR27-0050-40	6.1	5.5	4.85



With stripline structures there is a balancing act between:

(1) Do I have enough flow to fill all the artwork without voids?
(2) Do I have excessive flow where resin flows into a cavity?
(3) Can I accurately product the z axis distances for impedance and how reproducible will they be?

Strategy for Simple RF Multilayers



Strategy allows you to minimize prepreg thickness and overall variation of dielectric thickness on impedance – not practical for high layer count multilayers

Dielectric Materials for Multilayer Stripline Applications

MATERIAL		ε_R (10GHz)	DF (10 GHz)	DF (40 GHz)	Fiberglass (wt%)	Construction
FR4	prepreg/core	4.4	0.025		35-75	epoxy, E fiberglass
Nelco 4000-13EP SI	prepreg/core	3.13-3.28	0.008		55-75	epoxy, CE, NE glass Nittobo
Rogers 4403	prepreg					
Rogers 4450B	prepreg	3.54	0.004		≈25-35	butadiene rubber, silica, E glass
Speedboard C	prepreg	2.6	0.004	0.0064 X 0.0061 Y	0	Explanded PTFE/ silica, epoxy
PCTFE thermoplastic	prepreg	2.26	0.0035	0.0057 X 0.0076 Y		polychlorotrifluoroethylene (HT1.5 Bondfilm, RO3001, Arlon 6700)
Taconic *fast*Rise27	prepreg	2.7	0.0014	0.0017 X, Y	0	silica (≥50%), thermoset, ptfe
Taconic TSM29	core	2.94	0.0014		9	PTFE/ E glass / silica
Taconic TSM-DS	core	2.85	0.0010			PTFE/ E glass / ceramic
Arlon CLTE-XT	core	2.94	0.0012			PTFE/ E glass / silica
RO3003	core	3.00	0.0013		0	PTFE / silica
Taconic TLY-5 RO5880	core	2.8	0.009			PTFE/ E glass

Design Considerations	DK	DF (10 GHz)
E Fiberglass	6.4	0.0067
NE Glass Nittobo	4.6	0.0035
Epoxy	3.2 - 3.8	0.02
Butadiene Rubber	2.3	0.004
Silica	3.2	0.0028
PTFE	2.1	0.0006

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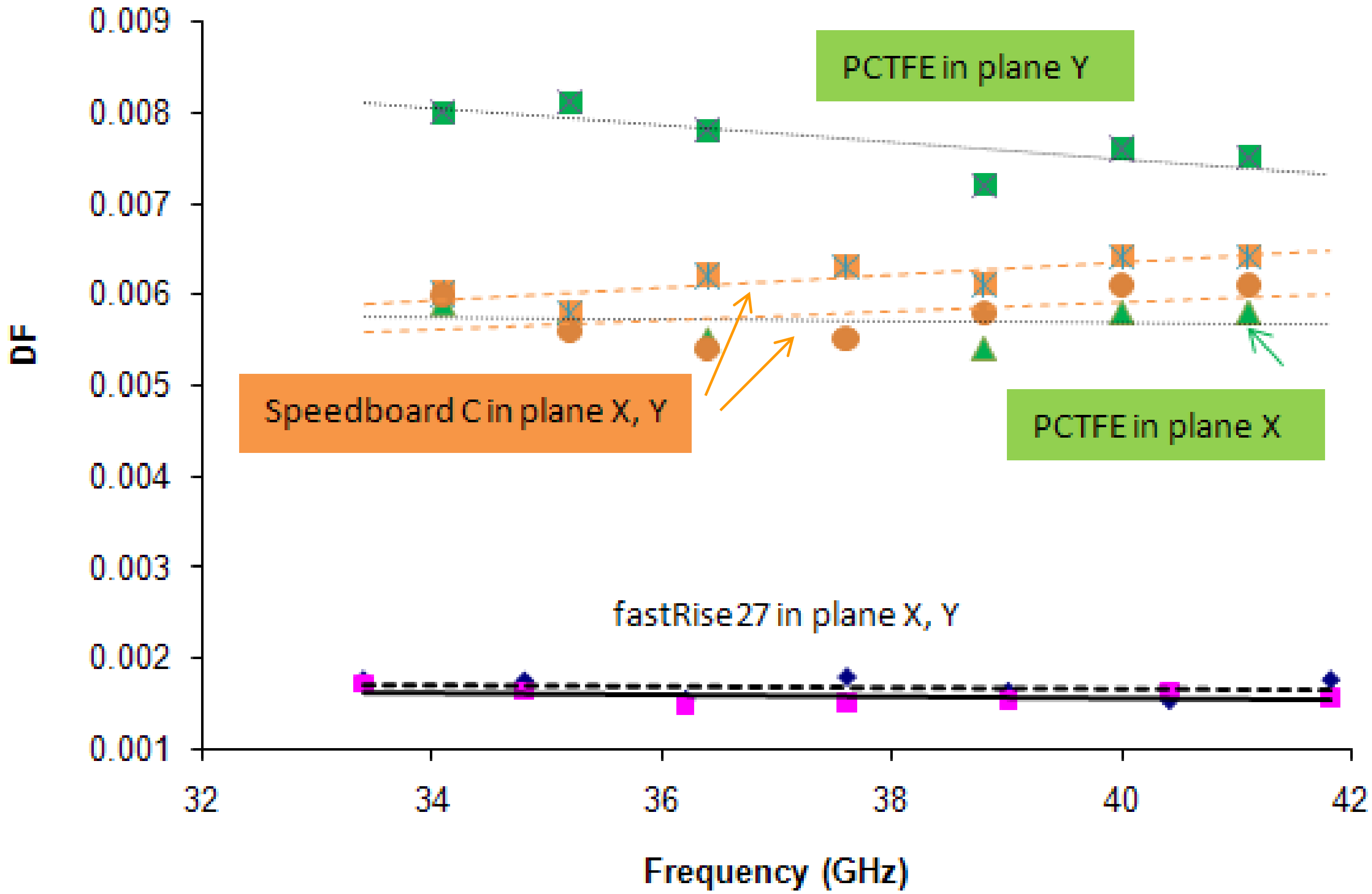
mmWave Loss Tangents for Various Multilayer Bonding Films



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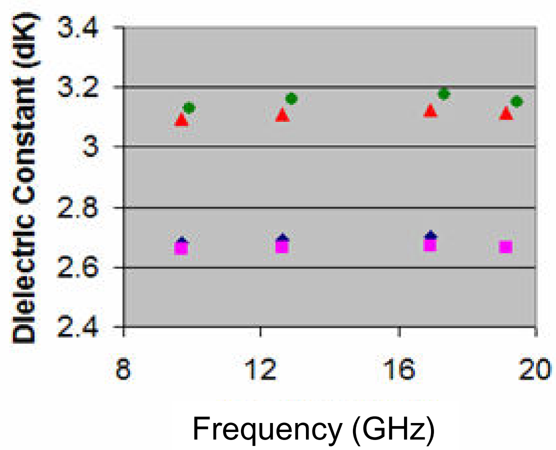
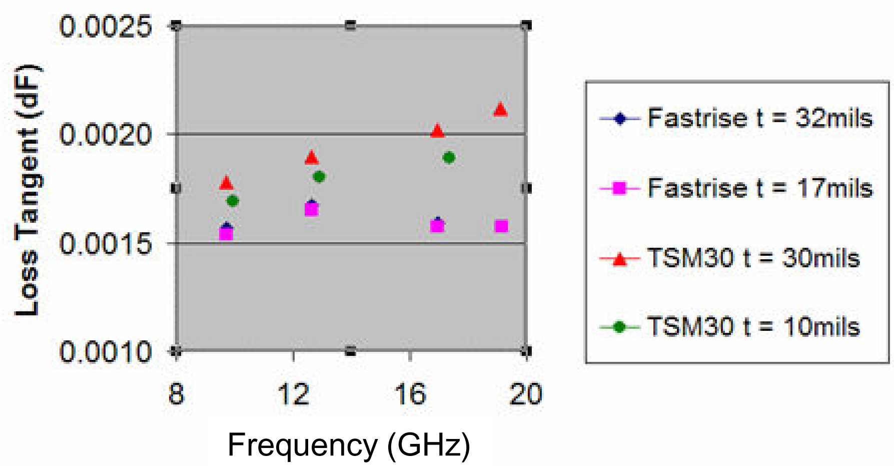
Glass Reinforced vs non glass reinforced mmWave Properties

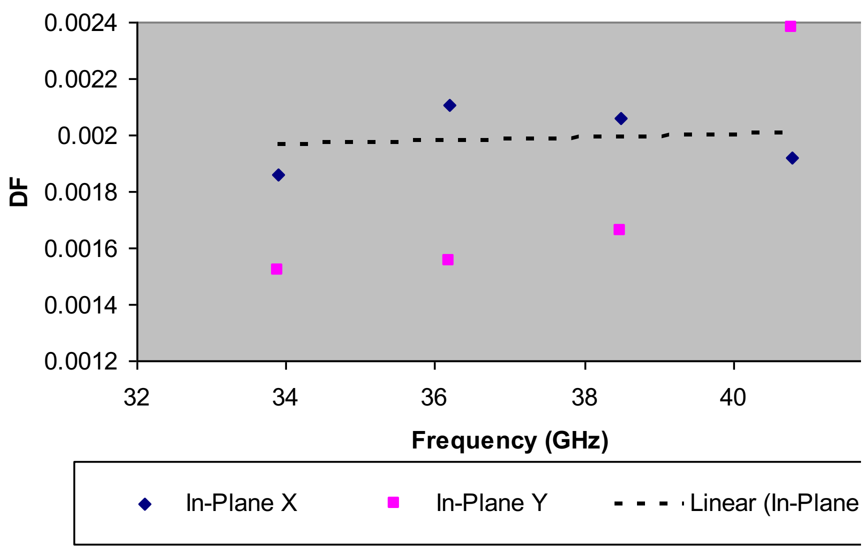
Resonant Split Cavity DK Data



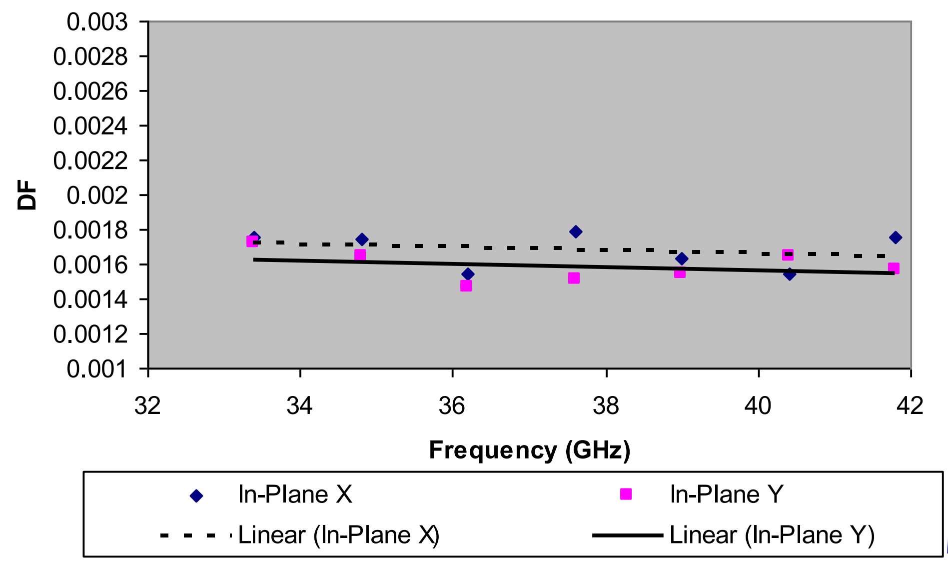
Resonant Split Cavity DF Data



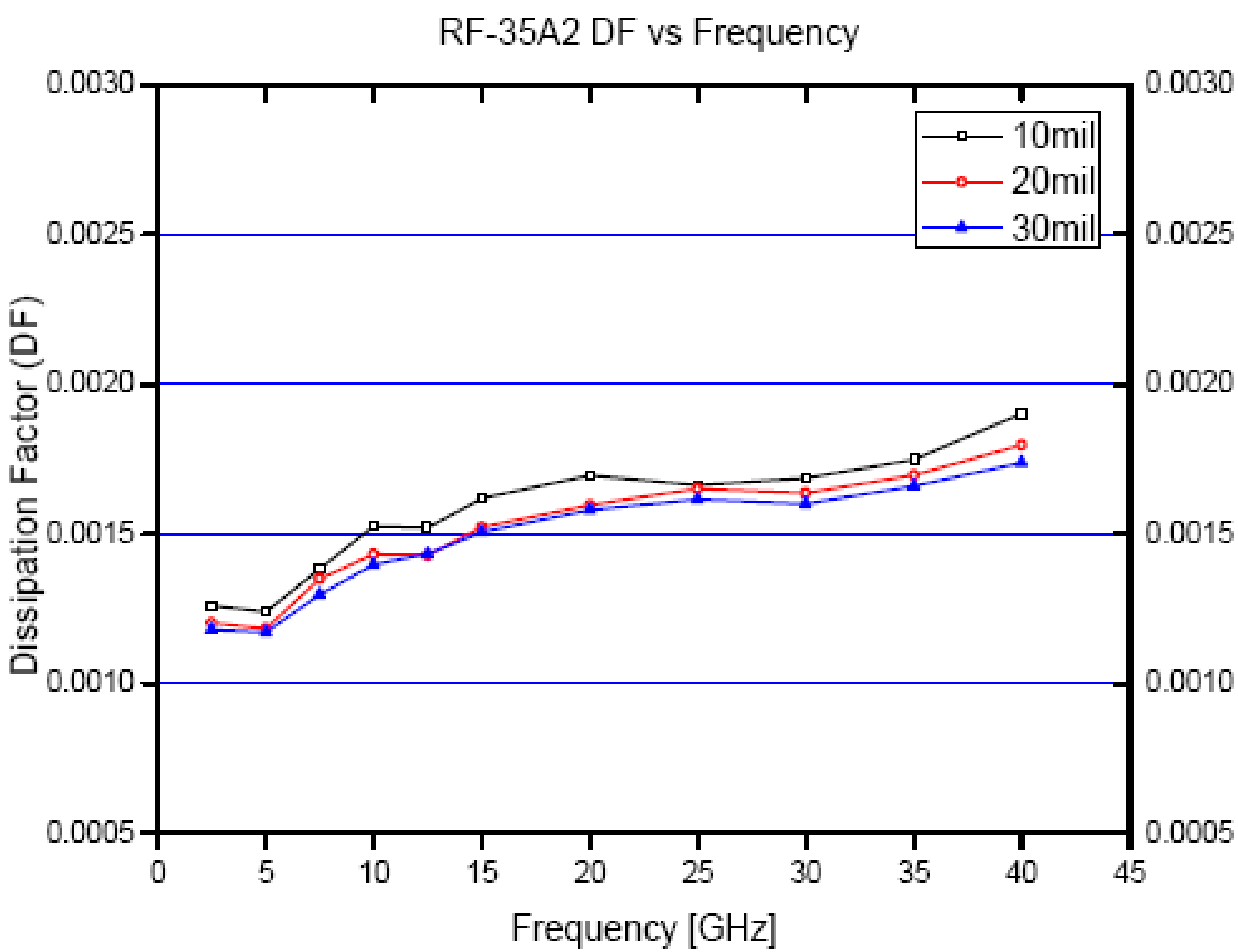
TSM mmWave Performance (Damaskos)

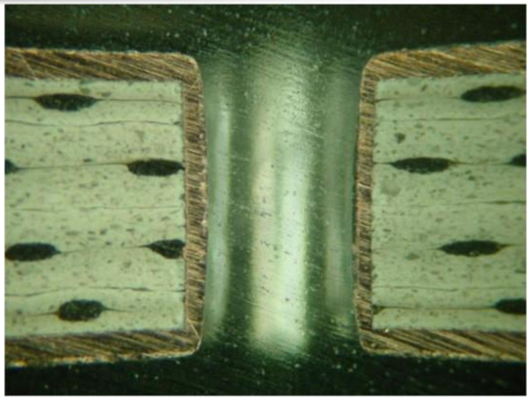


***fast*Rise27 (Damaskos)**



Fiberglass Reinforced Laminate at mmWave





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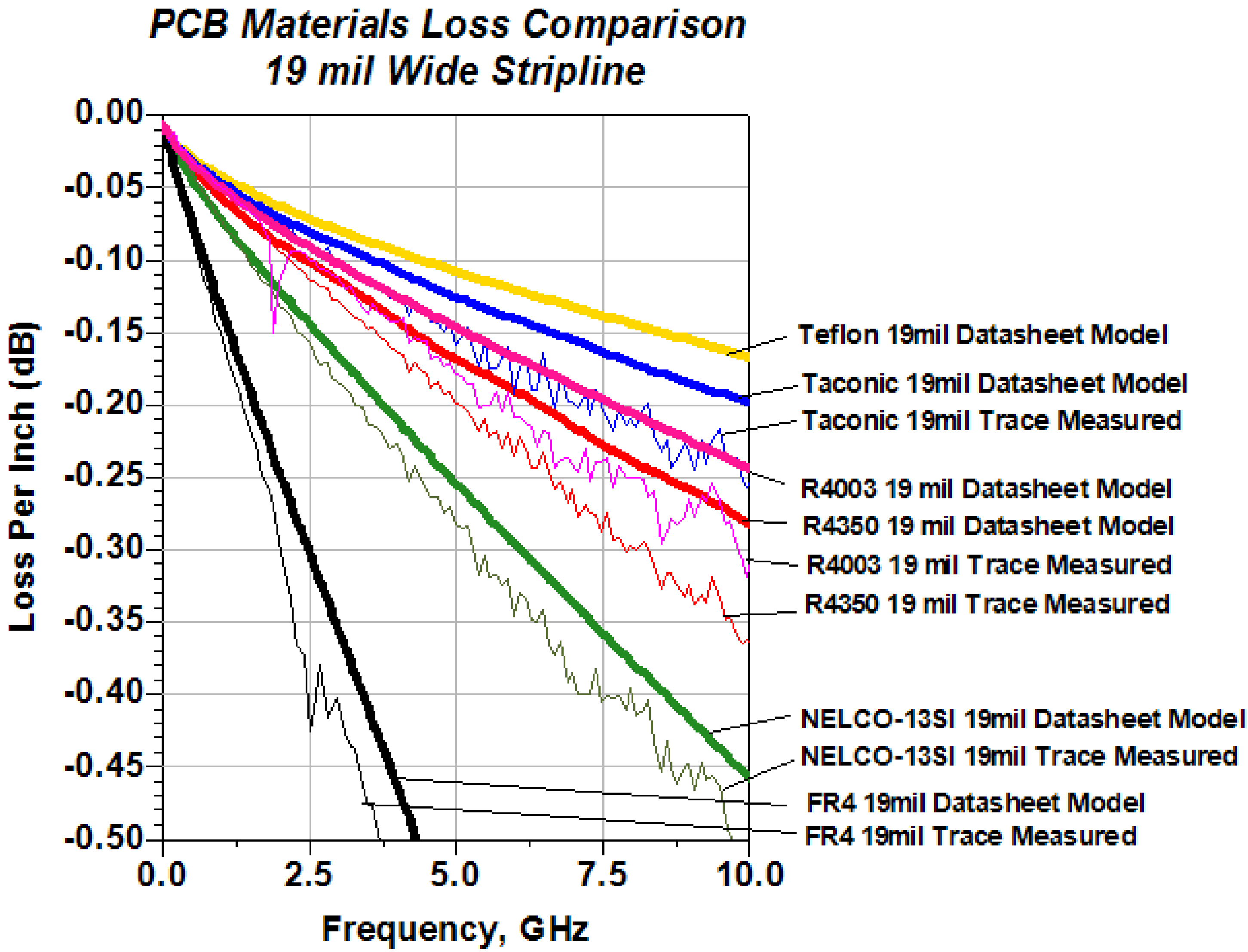
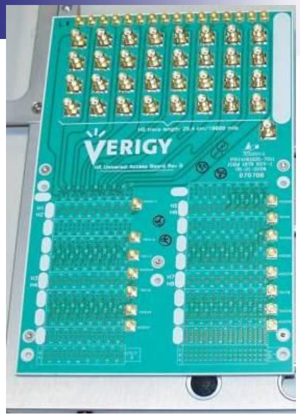
Experimental Insertion Loss Results

(provided by Verigy)





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Impedance Fluctuations with Fiber Glass Weave

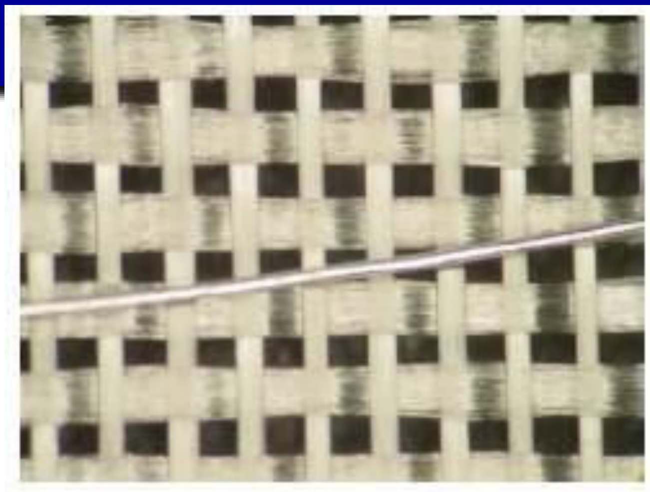

Figure 1. 1080 Glass Cloth with 3.5 Mil Wire

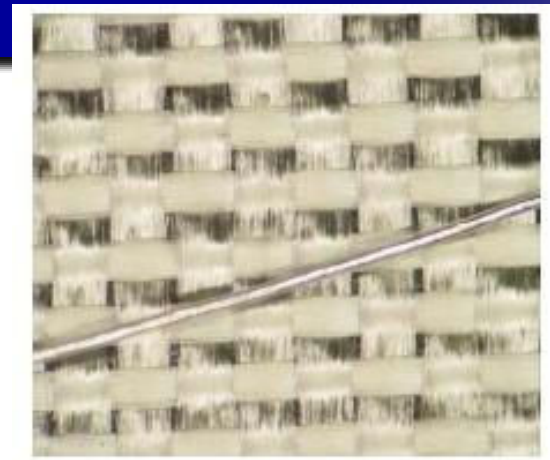

Figure 3.3313 Glass Cloth with 3.5 Mil Wire

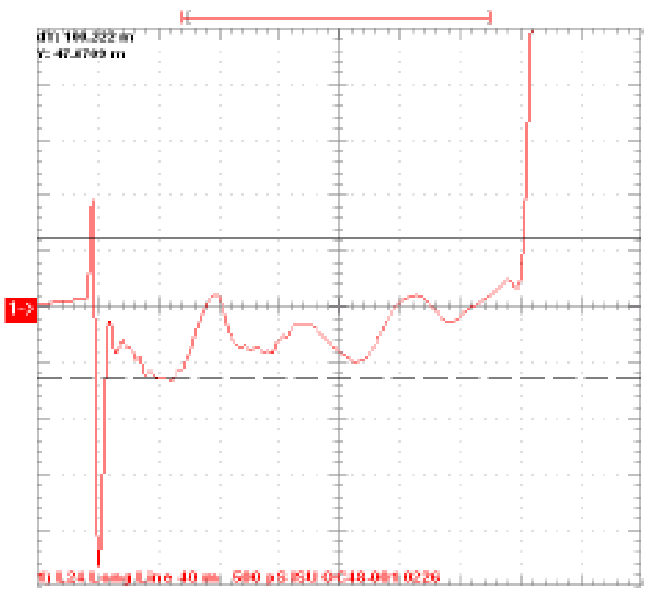

Figure 2. Impedance vs. Length Over 1080 Glass

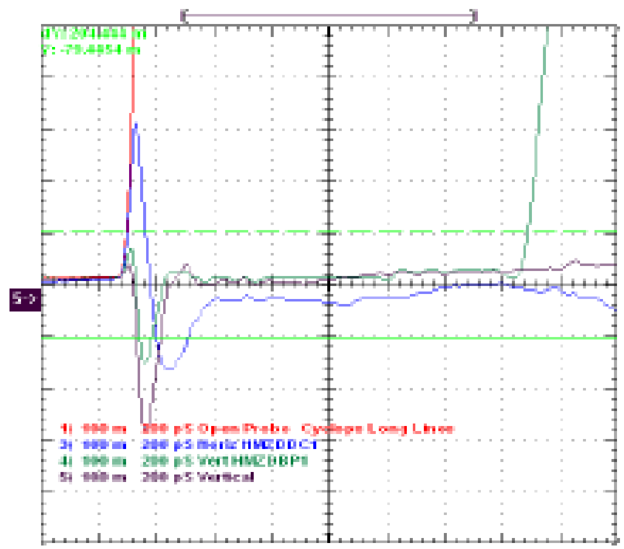

Figure 4. Impedance vs. Length Over 3313 Glass

(With permission of Lee W. Ritchey – Speeding Edge)

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Fusion Bonding (295-400ºC)

Fusion Bonding – the multilayer thermoplastic lamination of pure PTFE or ceramic filled PTFE composites with no prepregs (no thermosets)

POSITIVES

(1) Loss tangents of 0.009-0.0014 can be obtained

(2) Homogeneous stackup

Example – 6dk core with 6dk unclad

(3) Low moisture absorption, high Temperature stability of pure PTFE

(4) Capable out to very high frequency

NEGATIVES:

(1) 10-12 Hour press cycle – high cost

Other options 3-4 hour press cycle

(2) Limited fabricator base – high cost

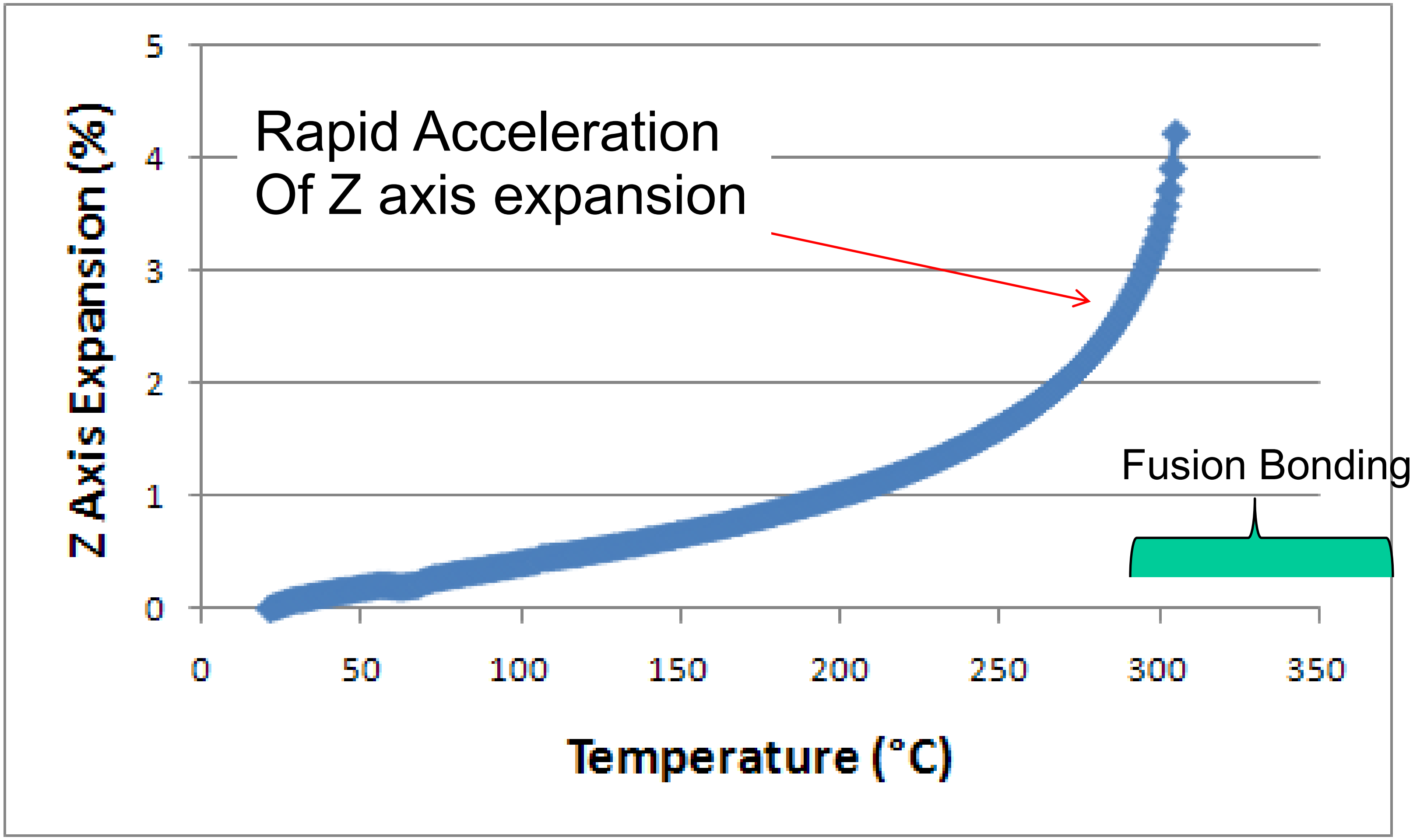
(3) High temperatures and pressures cause circuitry to float

(4) High viscosity of PTFE not ideal for encapsulating copper

(5) FEP bonding prone to melting during drilling, thermal reliability problems

(6) High loadings of PTFE → drill smear

Fiberglass Reinforced PTFE Laminate Thermal Expansion



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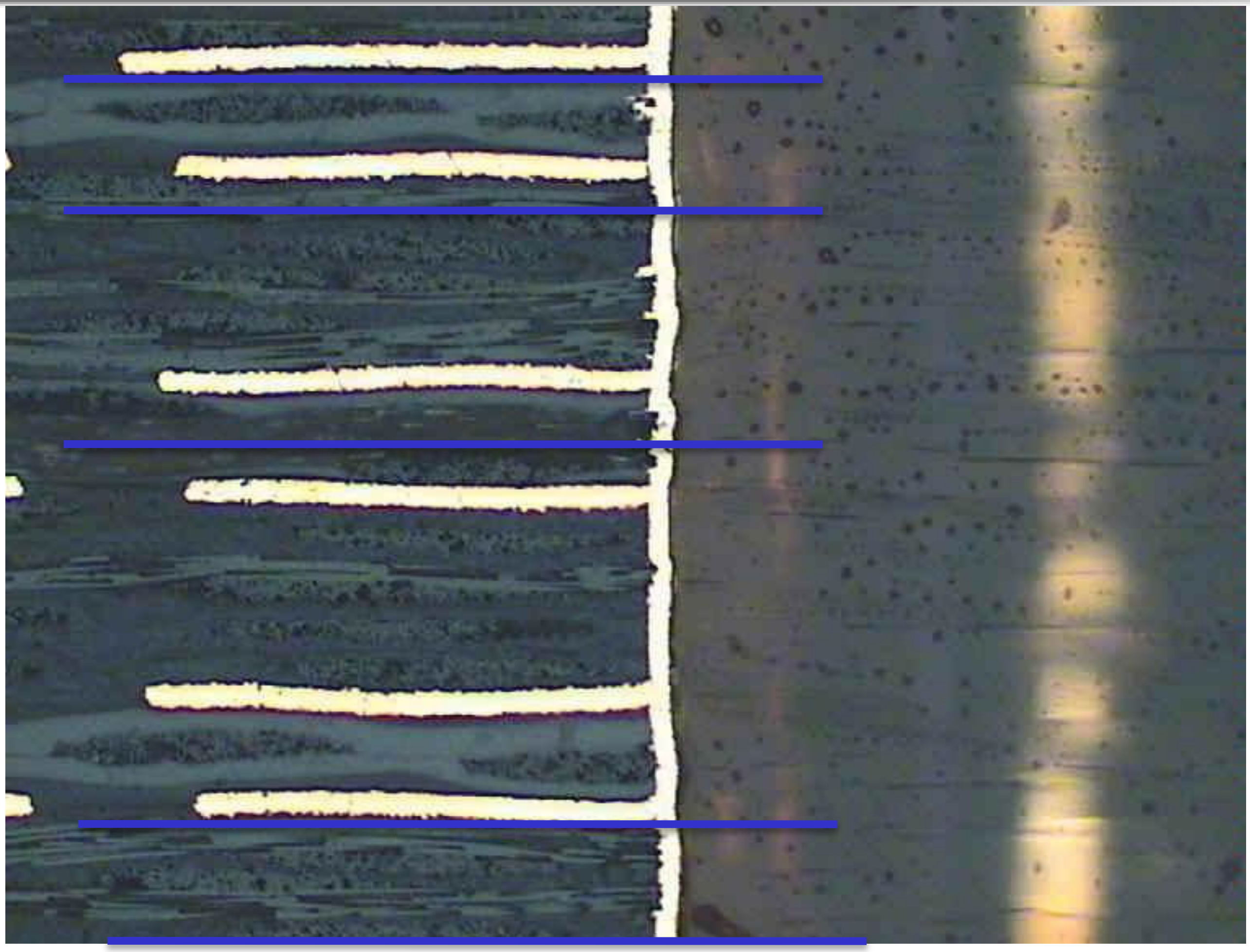
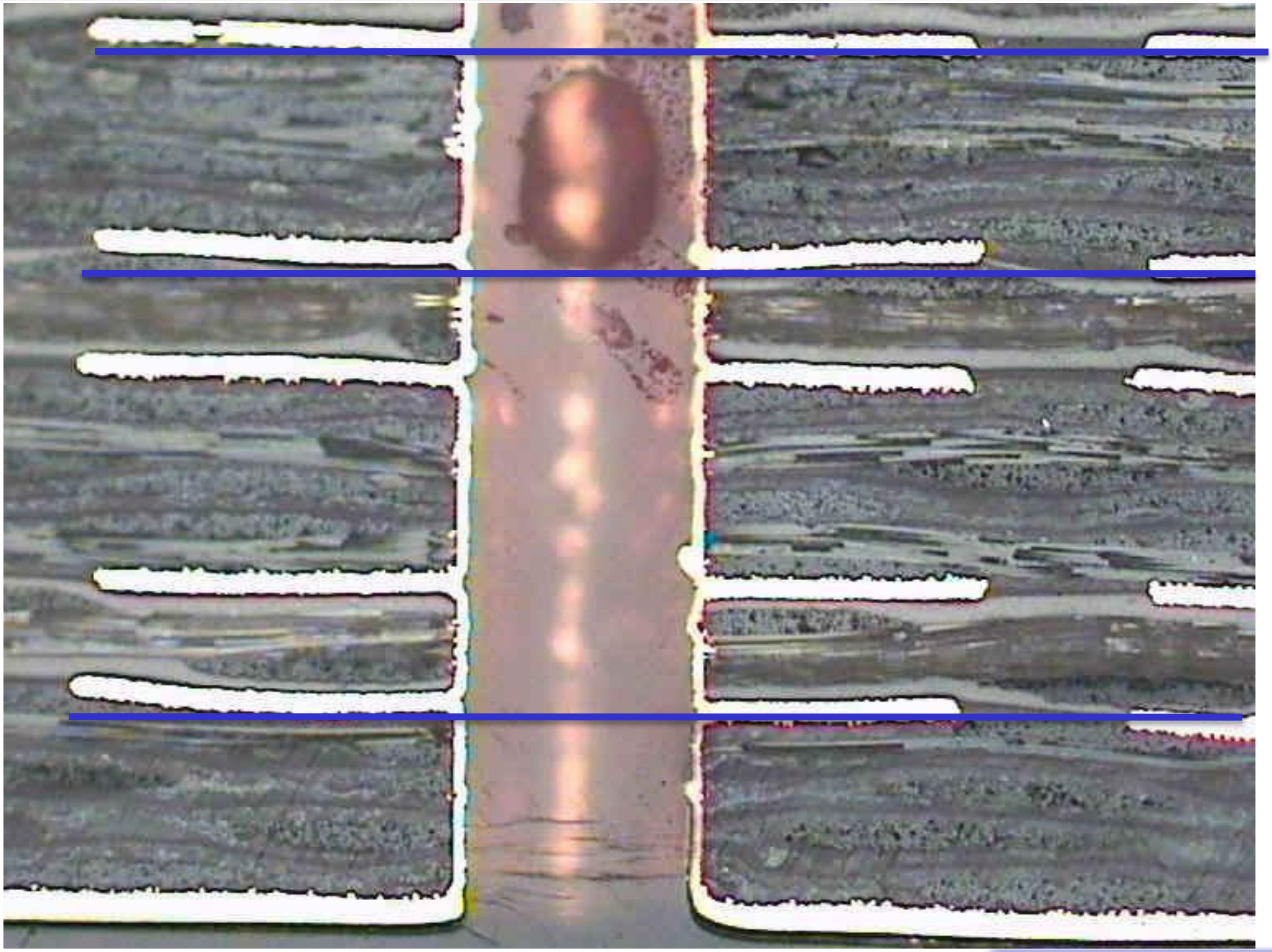
Fusion Bonded Multilayer

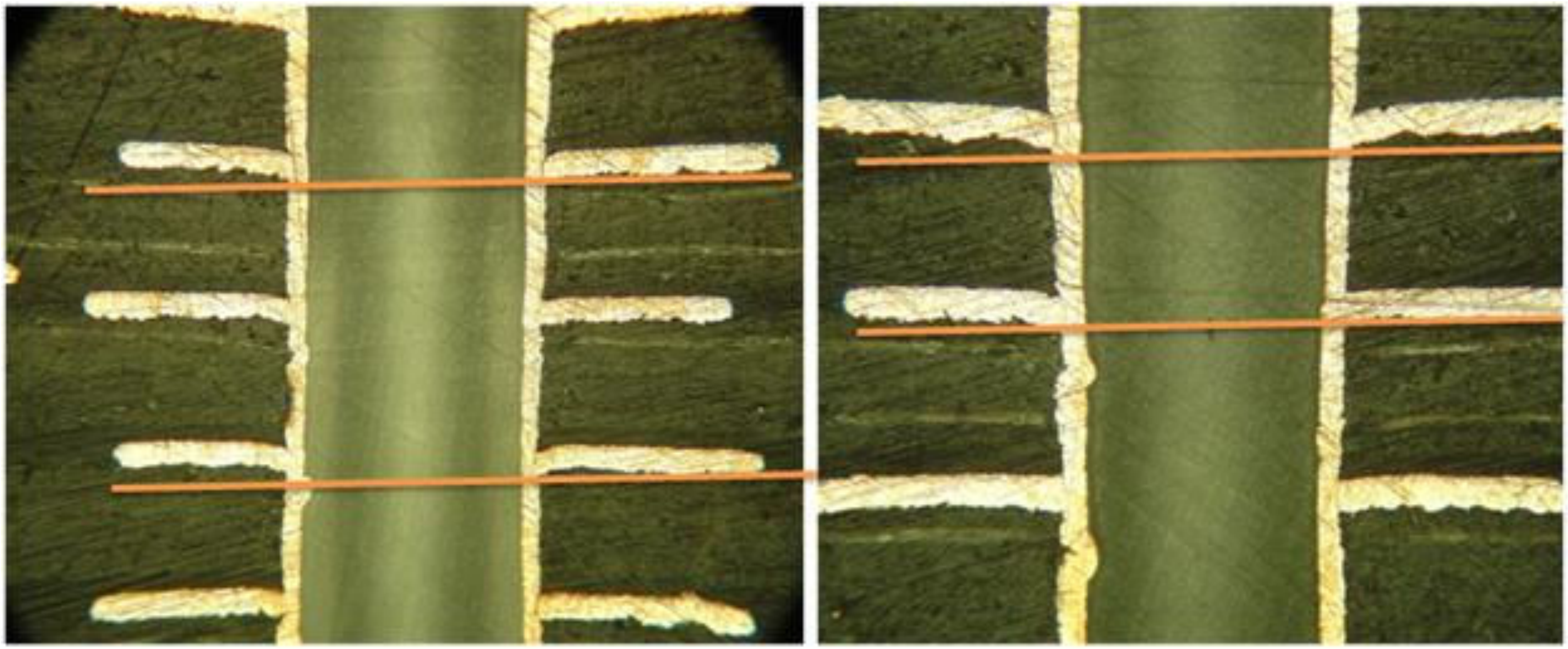


Fusion bonding may cause change in dielectric thickness, dielectric constant, and build in residual stress

Fusion Bonded Multilayer

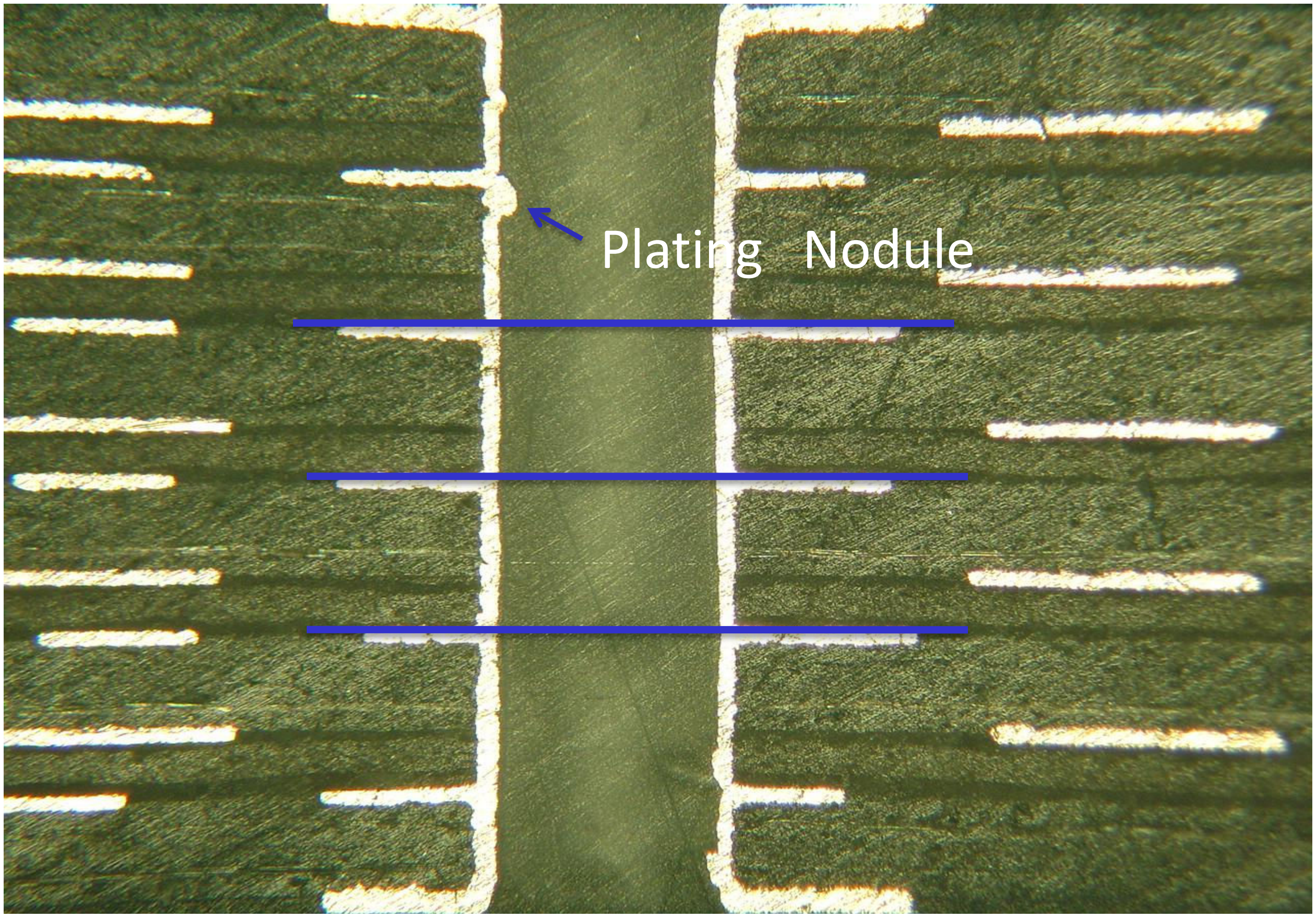


FEP fusion bonded Multilayer



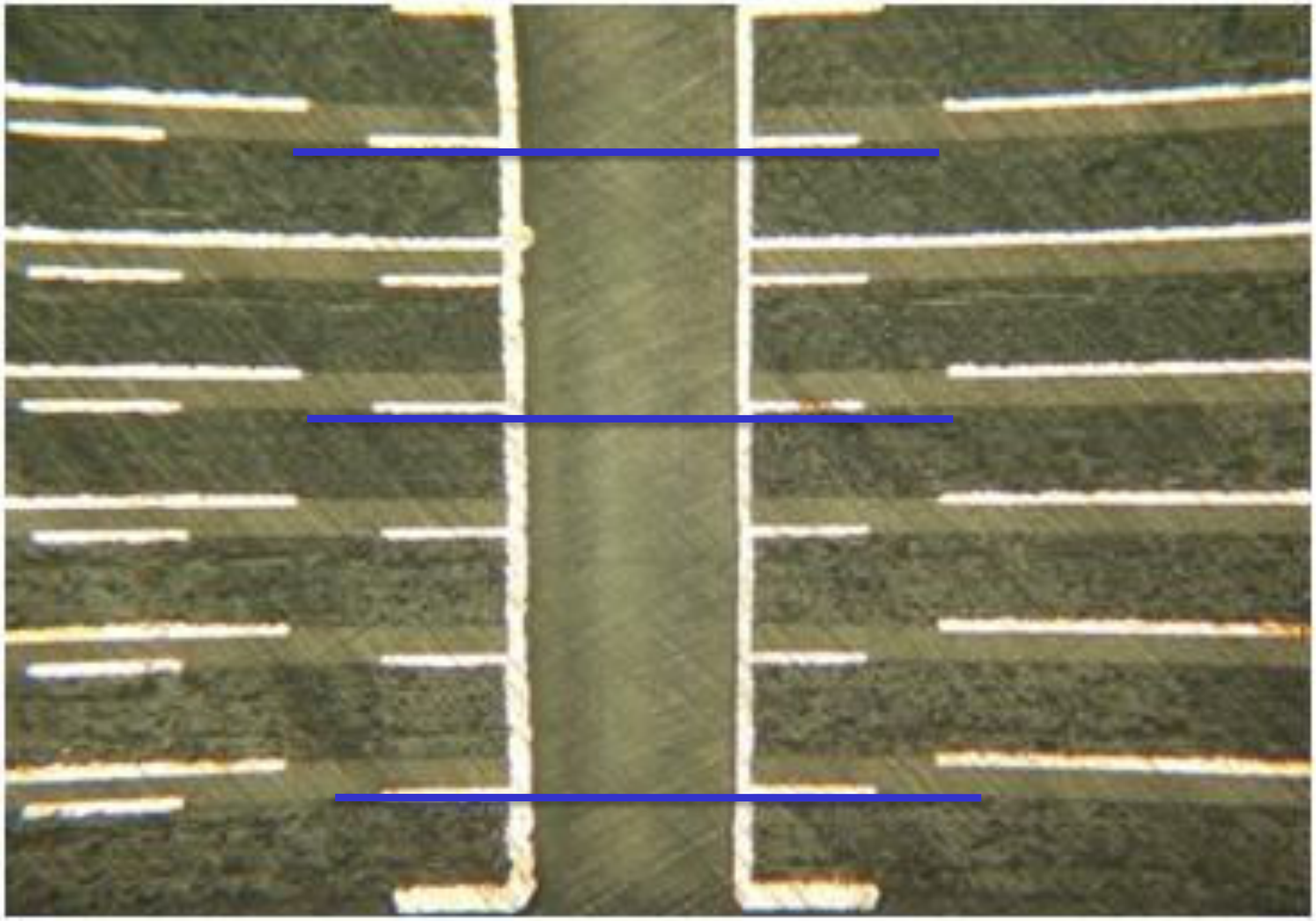
Pad distortion during high temperature lamination and
Remelting of the FEP film during drilling can lead to
Pad /post reliability questions

Ceramic filled PTFE/fastRise27
(215ºC Lamination)



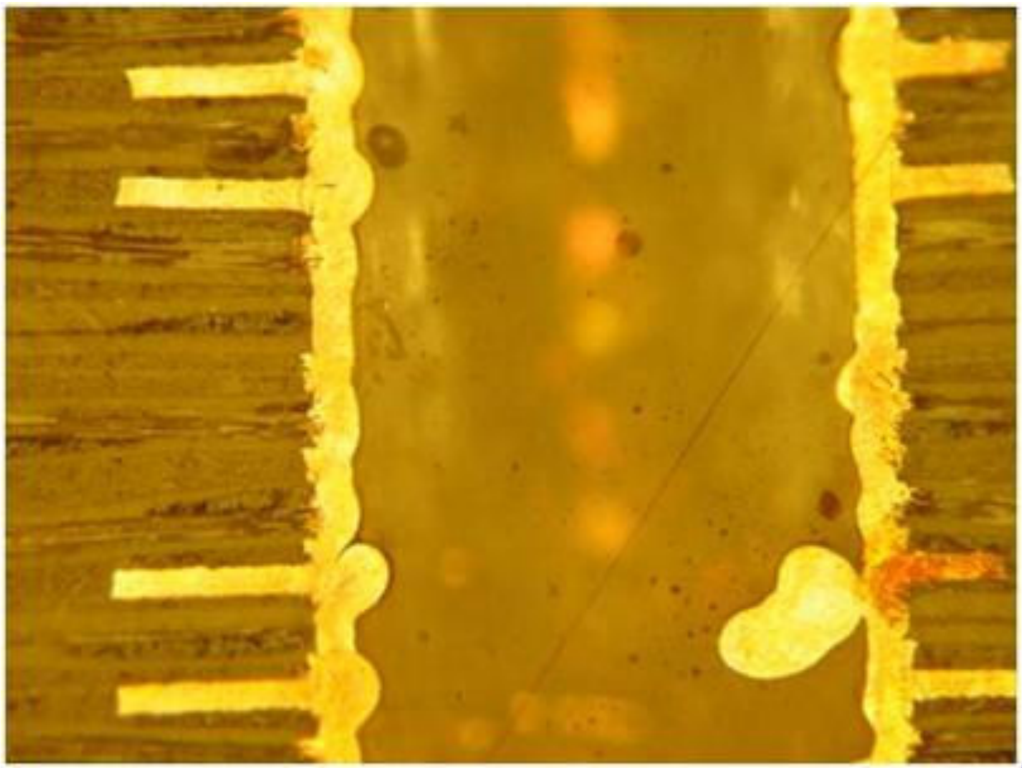
Low temperature lamination – no pad/post distortion

Ceramic filled PTFE/Speedboard C
(215ºC Lamination)

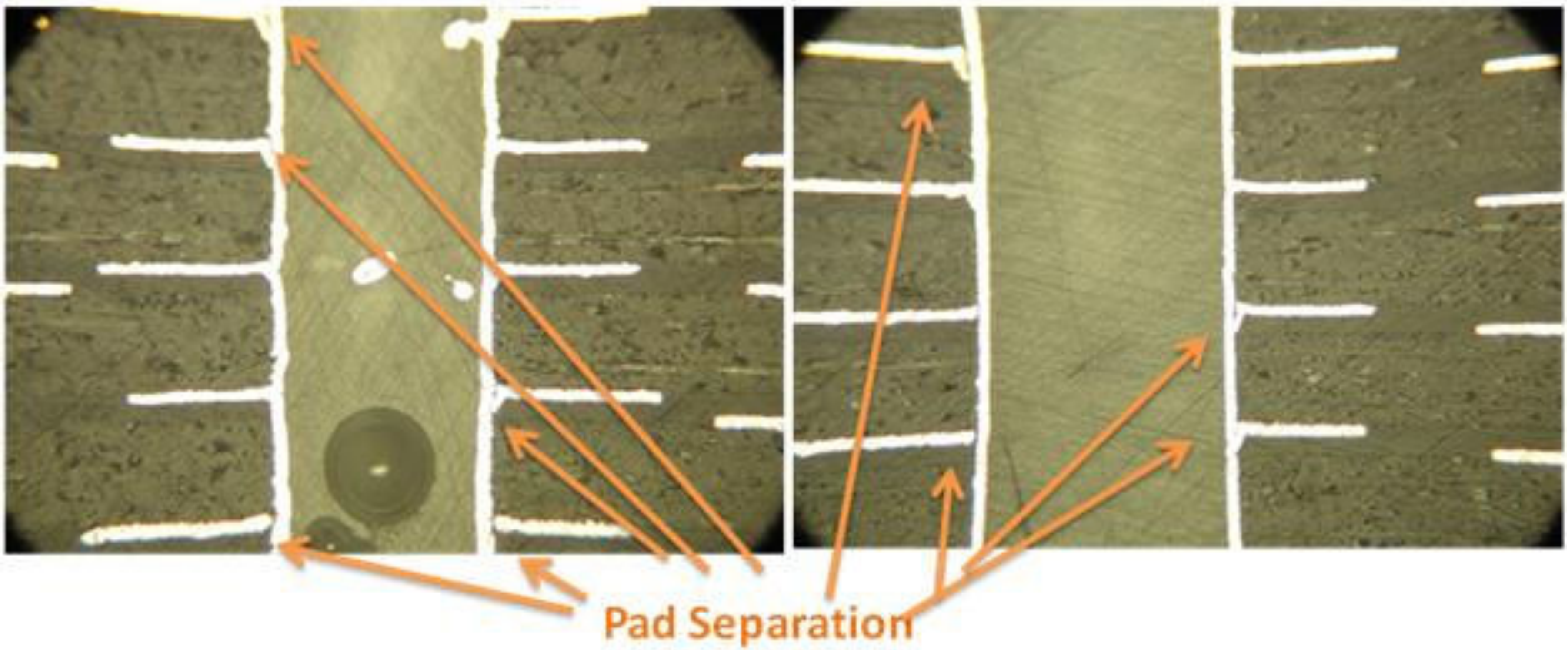


Low temperature lamination – no pad/post distortion

Fabricating with High PTFE Content Laminates and Thermoplastic Films (little or no ceramic….not advised)



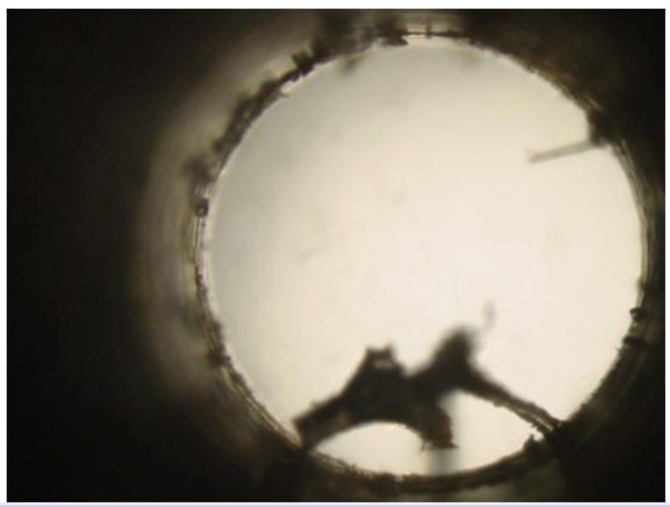
Drilling / Plating Defects (FEP Bonded multilayer)



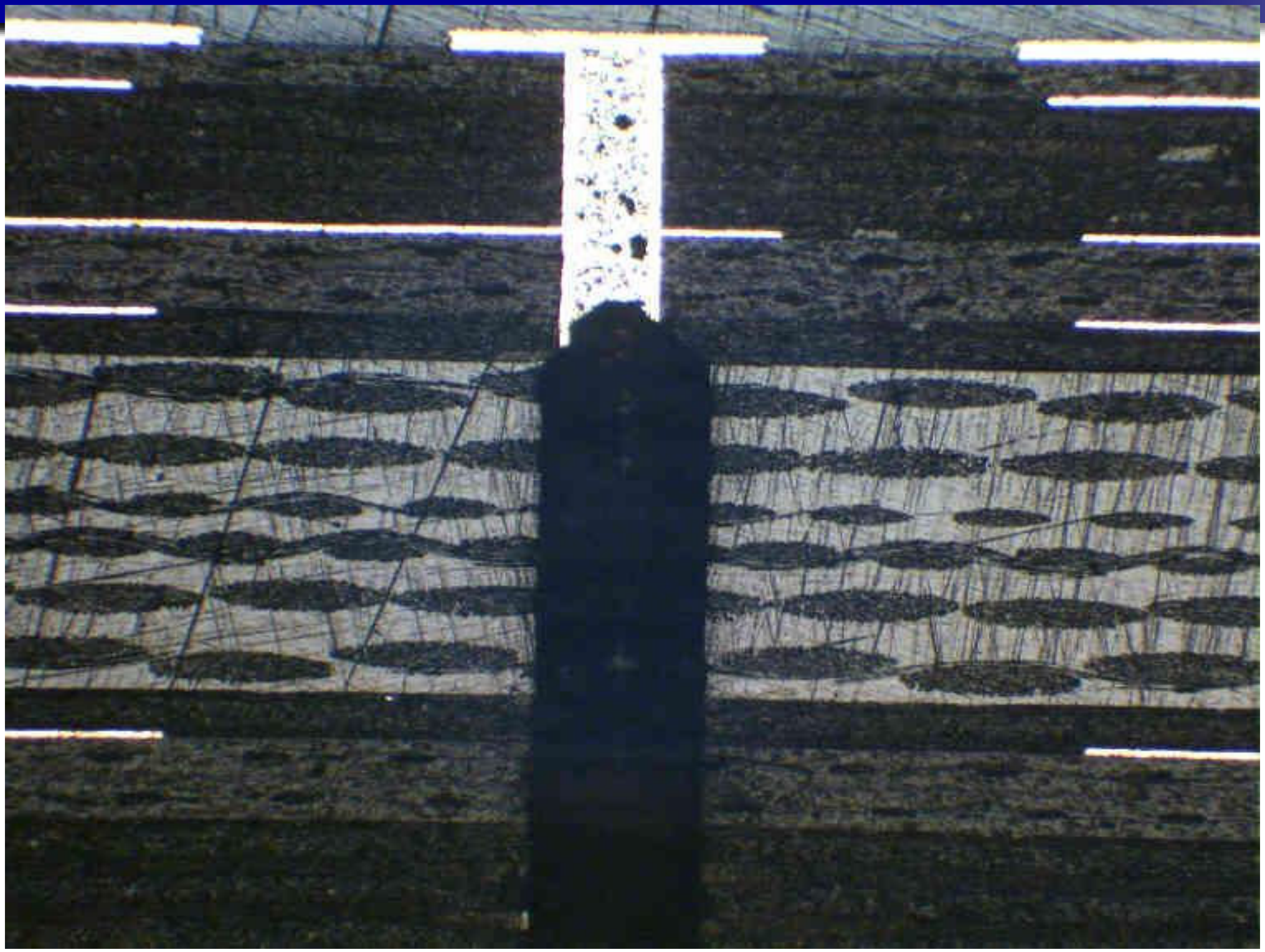
Does the melting of the thermoplastic film cause all these drilling defects…..serious problem for long term reliability.

Problems with High Resin Content PTFE and Thermoplastic Films (RO5880, TLY5 etc)

- PTFE (gel = 325C), FEP (mp = 255C), and PCTFE (mp = 215C)….melt during drilling
- Melting or softening causes smearing of thermoplastic across posts
- Plating chemistry does not get a 3 point connection to pad, worst case an open



Taconic fastRise27-TSM29/epoxy hybrid
"balance the construction "



TSM29

FR27

TSM29

FR27

7628
based
FR4

FR27

TSM29

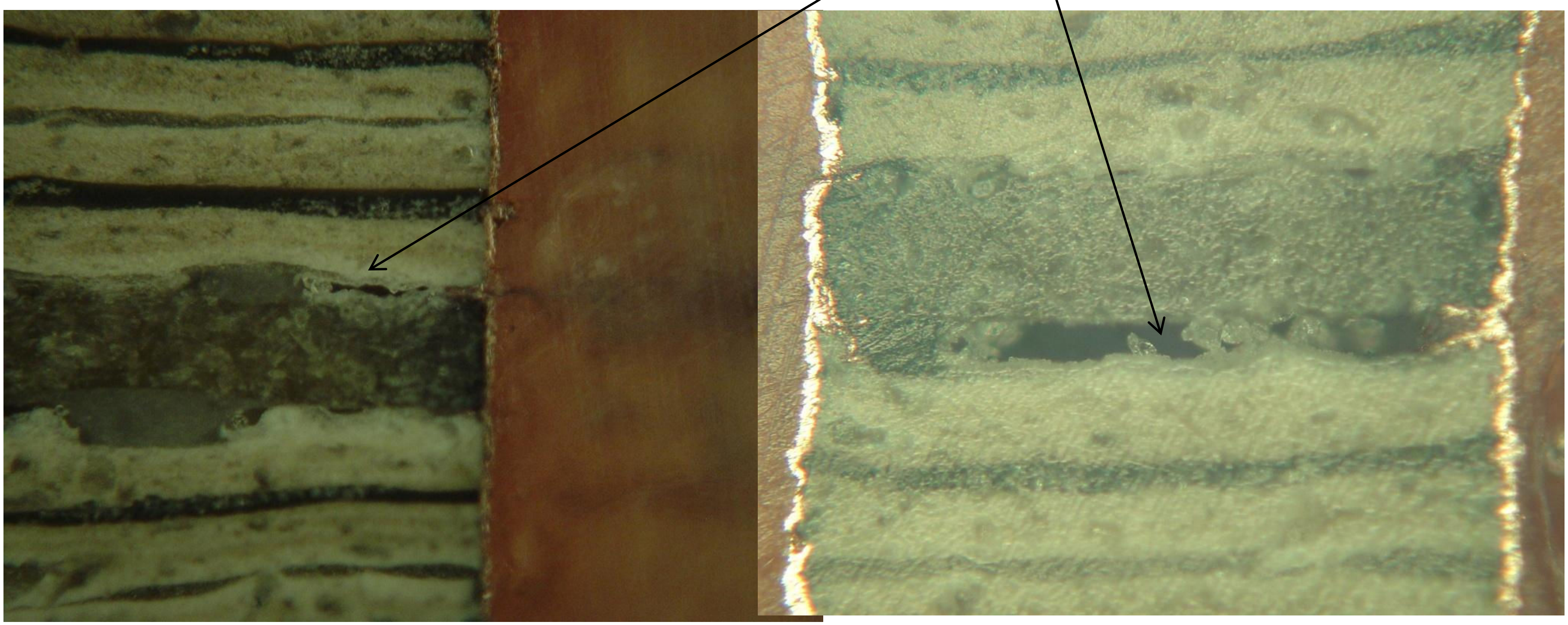
FR27

A balanced construction with a low glass content will lie flat and conform to the higher modulus

Unbalanced Hybrid subassemblies or pwbs may warp, crack, bow, twist, and delaminate

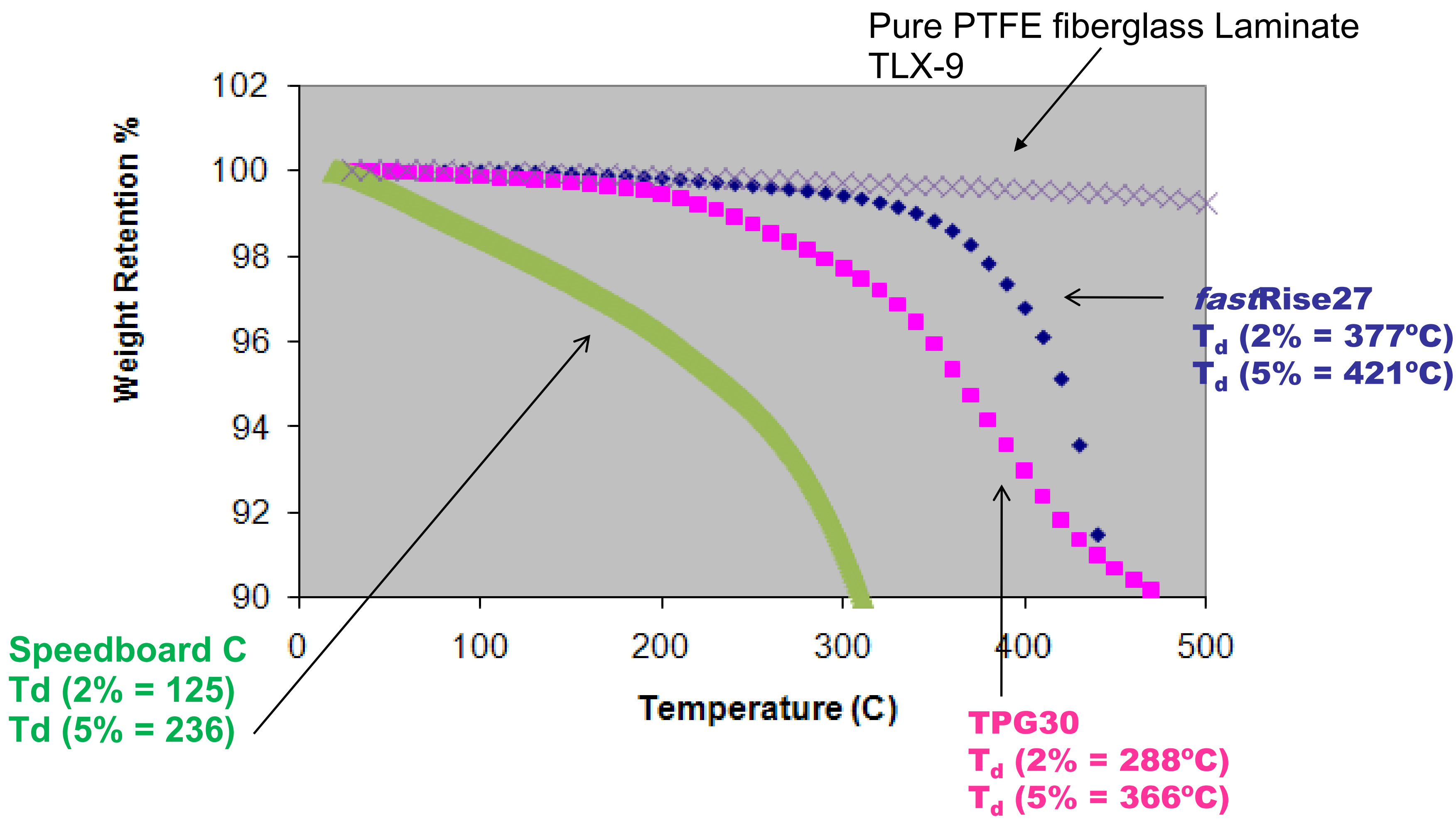
FR4
Other

Unbalanced construction leading
To stress induced delamination

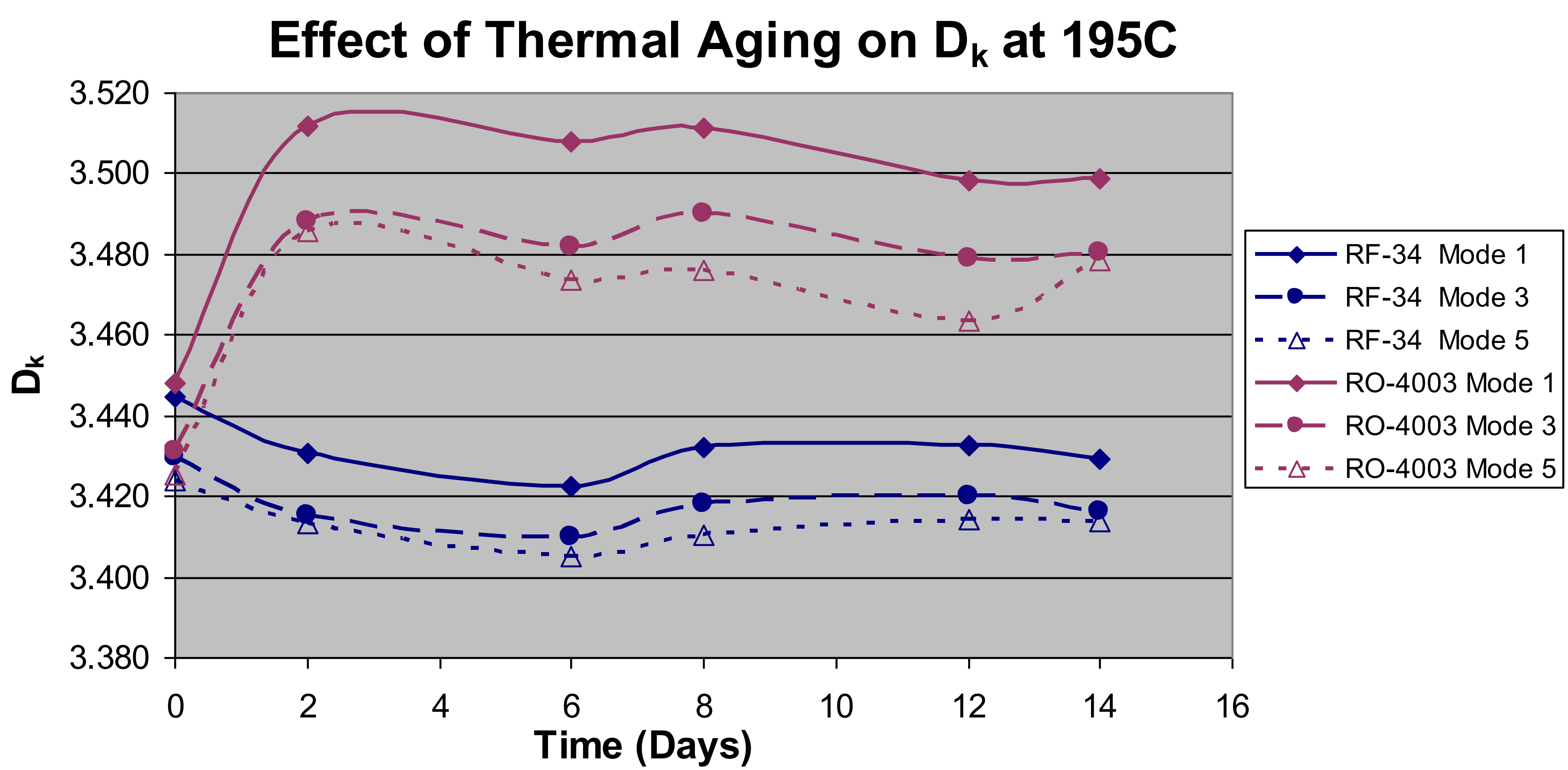


Temperature of Decomposition

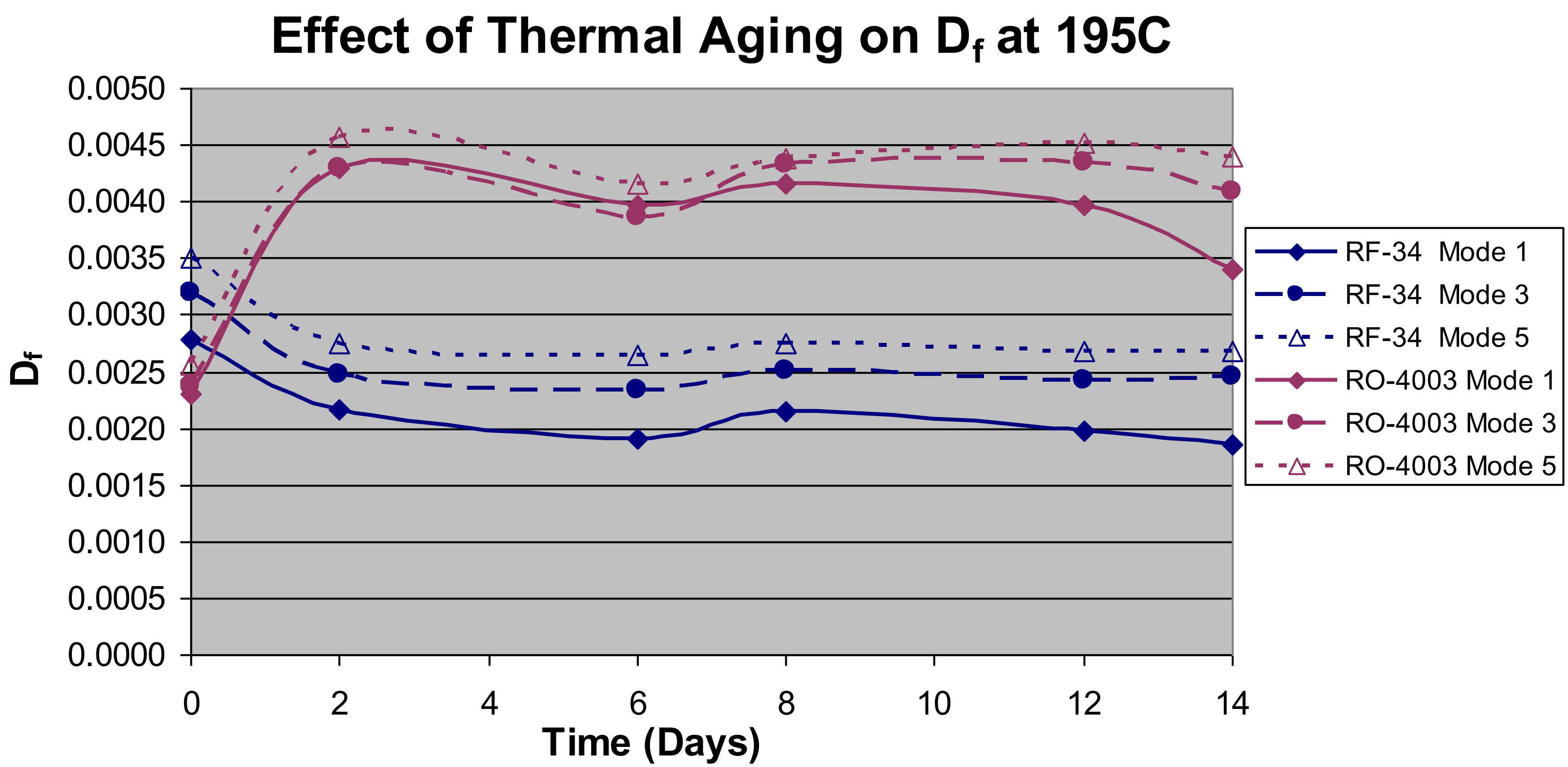
Various thermoset Prepregs vs PTFE Benchmark



Effect of Thermal Aging on Dielectric Constant (PTFE vs RO4003 series rubber)



Effect of Thermal Aging on Dissipation Factor (PTFE vs RO4003 series rubber)



Z axis Expansion and Reliability

(standard ED copper expands 3.5%)

TLY

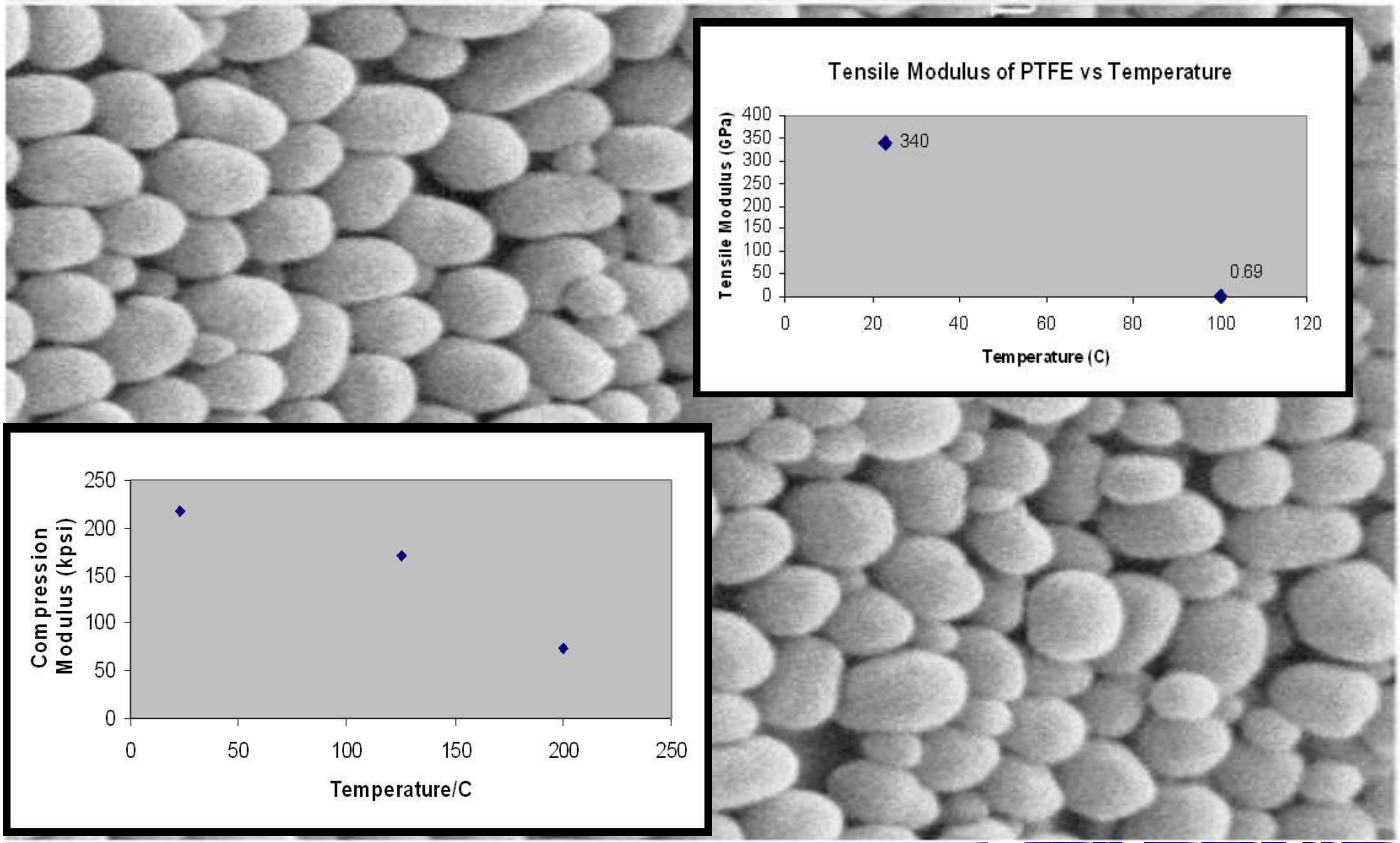
		CORE THICKNESS (mil)				
SUBSTRATE	(25 to 288C)	5	10	20	30	60
Z AXIS EXPANSION (PPM)	(%)	Expansion in mils (-65C to 125C)				
280	7.36	0.37	0.74	1.47	2.21	4.42
200	5.26	0.26	0.53	1.05	1.58	3.16
100	2.63	0.13	0.26	0.53	0.79	1.58
48	1.26	0.06	0.13	0.25	0.38	0.76
20	0.53	0.03	0.05	0.11	0.16	0.32

TLY

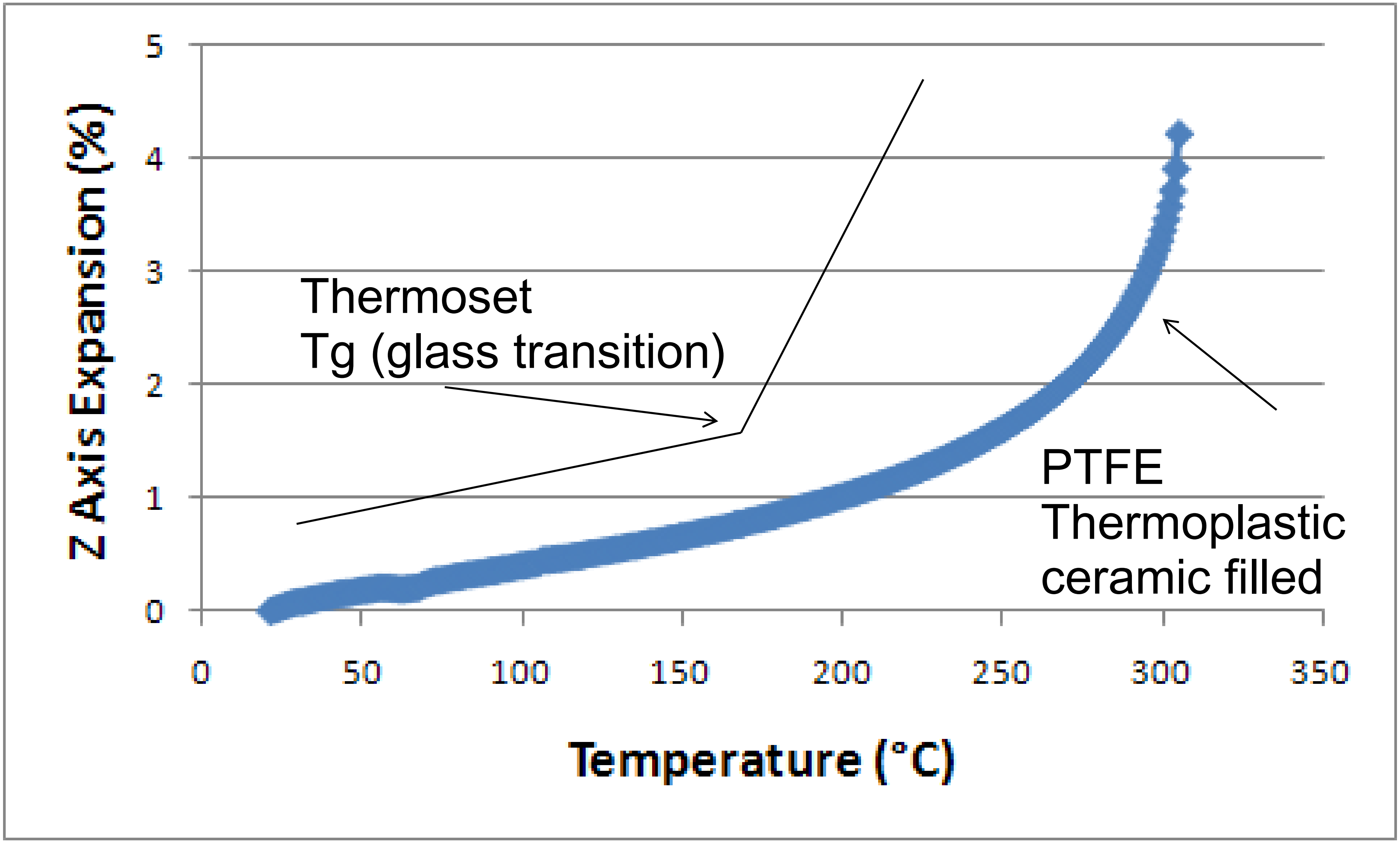
		CORE THICKNESS (mil)				
SUBSTRATE	(-65 to 125C)	5	10	20	30	60
Z AXIS EXPANSION (PPM)	(%)	Expansion in mils (-65C to 125C)				
280	5.32	0.27	0.53	1.06	1.60	3.19
200	3.80	0.19	0.38	0.76	1.14	2.28
100	1.90	0.10	0.19	0.38	0.57	1.14
48	0.91	0.05	0.09	0.18	0.27	0.55
20	0.38	0.02	0.04	0.08	0.11	0.23

TLY does well in a lot of thin multilayer applications
Z axis expansion is not the whole story!!!!

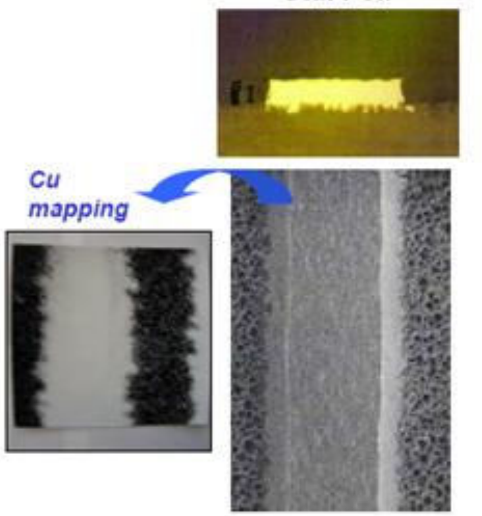
How does Modulus affect the stress on solder joints? Young's modulus is directly related to stress

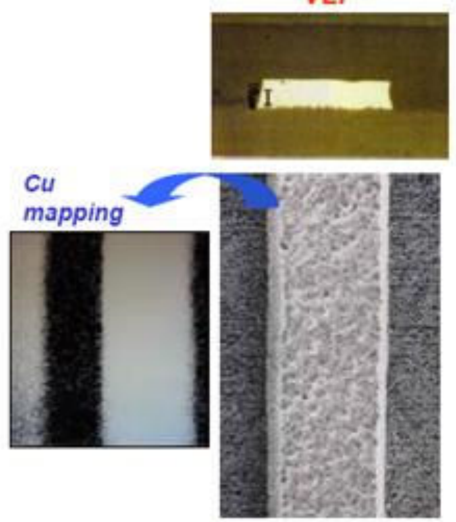


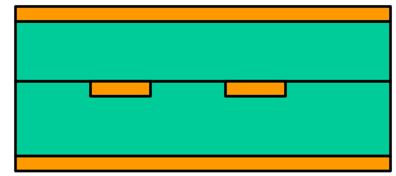
Thermoset vs Thermoplastic Z Axis Expansion



Copper Line Width Variations







$$k_{even} = \tanh\left(\frac{\pi}{2}\frac{w}{b}\right)\tanh\left(\frac{\pi}{2}\frac{(w+s)}{b}\right)$$

$$K'_{even} = \sqrt{1 - k^2_{even}}$$

$$Zo_{even} = \frac{30\pi}{\sqrt{\varepsilon_r}}\frac{K(k'_{even})}{K(k_{even})}$$

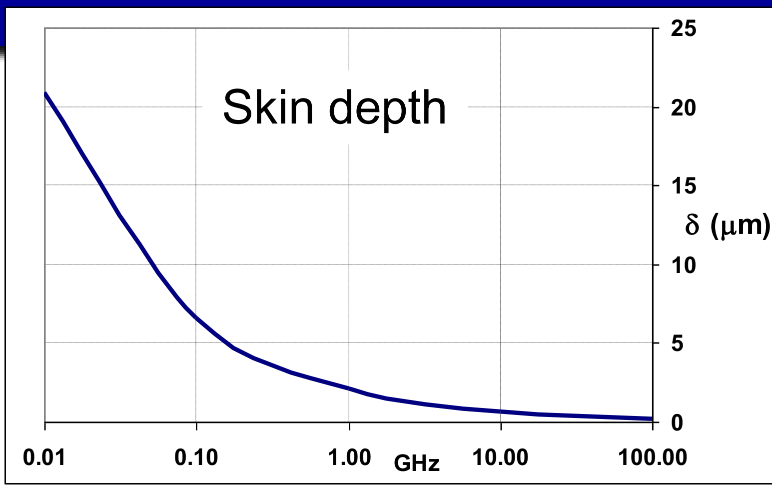
$$k_{odd} = \tanh\left(\frac{\pi}{2}\frac{w}{b}\right)\coth\left(\frac{\pi}{2}\frac{(w+s)}{b}\right)$$

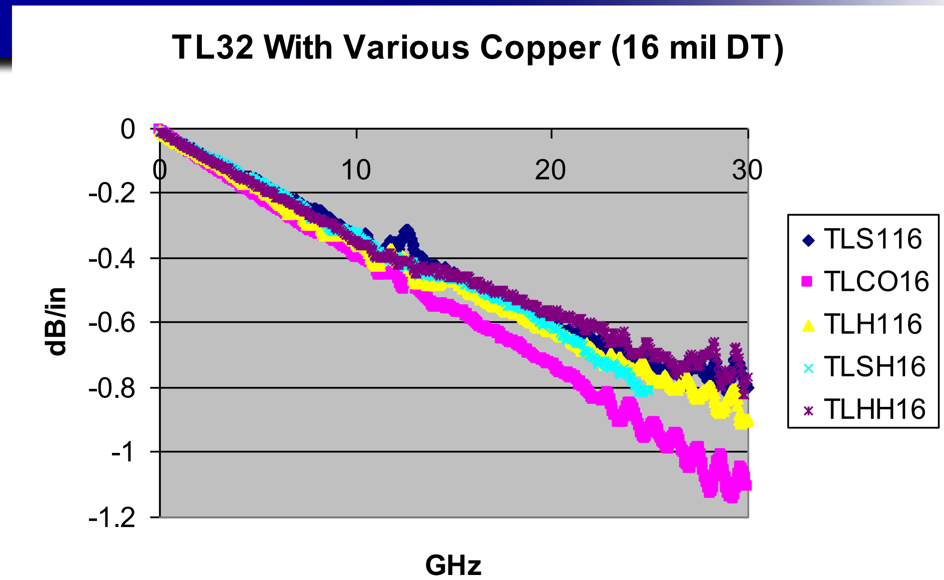
$$K'_{odd} = \sqrt{1-k^2_{odd}}$$

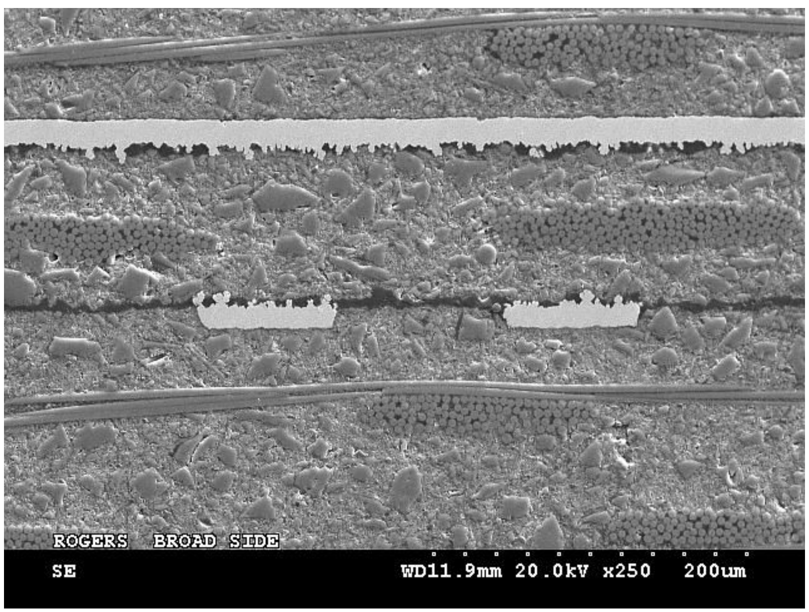
$$Zo_{odd} = \frac{30\pi}{\sqrt{\varepsilon_r}}\frac{K(k'_{odd})}{K(k_{odd})}$$

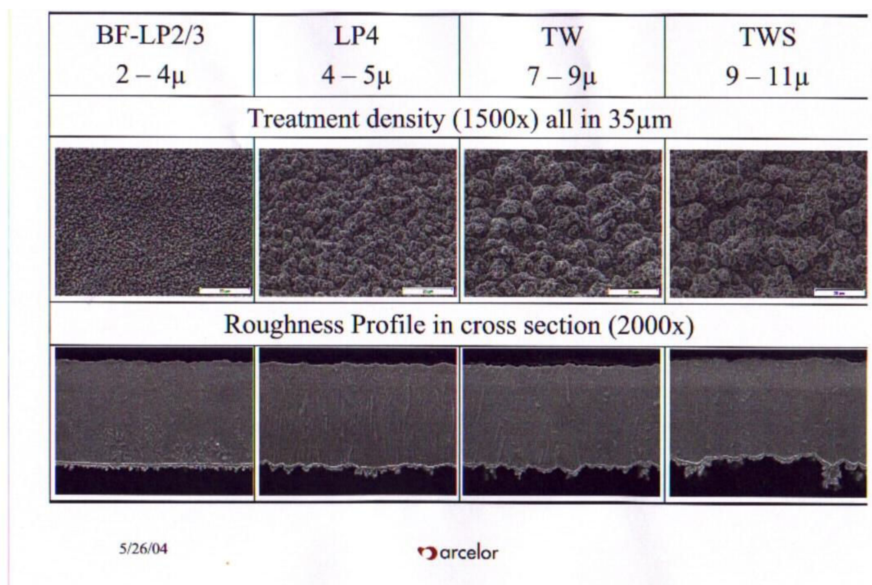
Inconsistent etching can lead to varying trace width, varying distances between trace widths, copper nuggets left behind in laminate (shadow copper) that can attract other plating chemistries (shadow ENIG)… ……real problem for fine lines and spaces

Copper Roughness Considerations









BF-LP2/3 2 – 4μ	LP4 4 – 5μ	TW 7 – 9μ	TWS 9 – 11μ
Treatment density (1500x) all in 35μm			
Roughness Profile in cross section (2000x)			

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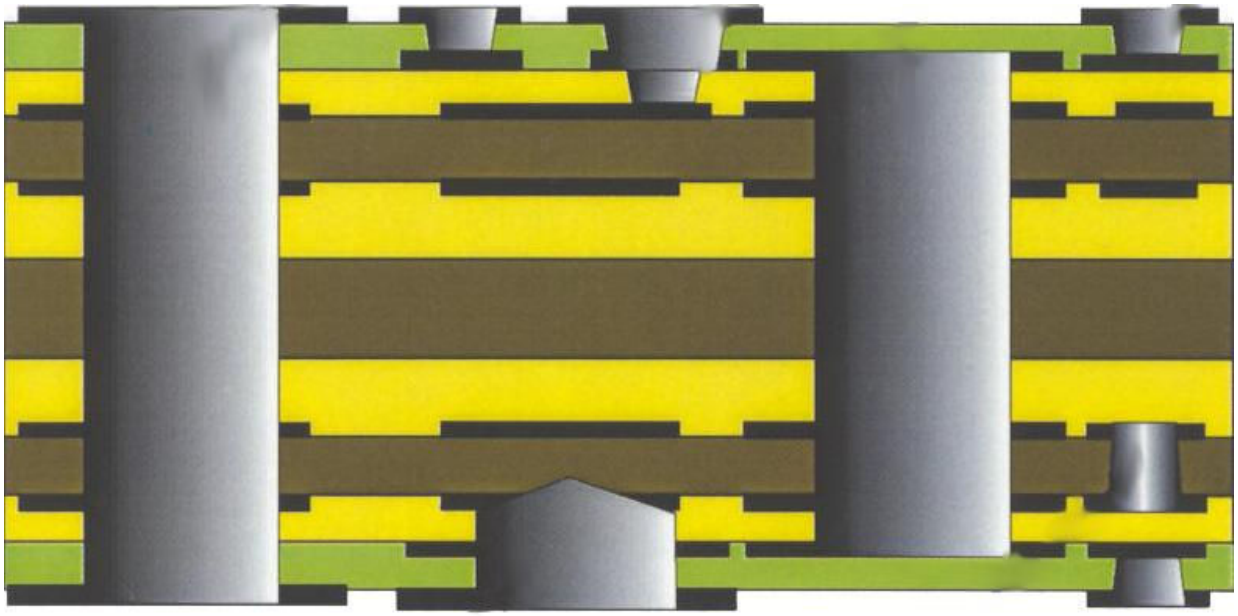
Sequential Laminations Enable Buried Vias and Elimination of Stubs



(IPC Technology Roadmap 2000-2001)

✓ Thermal reliability of prepregs necessary for multiple Lamination cycles, high temp 260C lead free reflow temperatures and multiple rework cycles

✓ Buried and blind vias with no stubs offer smoothest via transitions

TACONIC

Summary

Many Variables Affect Stripline RF Performance and Reliability

- Via Design and Registration to pads critical to performance
- Low temperature lamination an advantage to maintaining dimensional control, reducing stress in finished pwbs and reducing costs
- A lot of hidden factors like copper roughness and smooth etching affect RF performance
- Less obvious factors like low modulus, high drill quality affect reliability
- Final pwb quality will vary significantly with the fabricator
- Many variables not captured on any data sheet