Three-Dimensional Integrated Circuits
Challenges and Opportunities

Prof. Emre Salman

Nanoscale Circuits and Systems (NanoCAS) Laboratory

Department of Electrical and Computer Engineering
Stony Brook University, New York

http://nanocas.ece.stonybrook.edu

Stony Brook University

NanoCAS Lab at Stony Brook

- Established in 2011
- 3 PhD students
- 2 MS students
- 7 MS alumni
  - Employment at
    - Intel, NVIDIA, Hynix, Marvell,
    - Continue PhD
- Several undergraduate researchers
  - URECA, senior design
  - ECE Honors Program

http://nanocas.ece.stonybrook.edu

Research at NanoCAS Lab

Research Themes

Energy-efficient circuit design

- Number 1 design objective for almost *any* application
- "Power Wall"
- "Dark Silicon"

Application Domain

- ASICs, microprocessors
- Low power portable processors
- Implantable ICs

Emerging integrated circuit technologies

- 7 nm by 2022 seems to be the end of traditional CMOS scaling
- Moore's law 50th year anniversary

SIMONS FOUNDATION

NSF

Stony Brook Research

SRC® Semiconductor Research Corporation

Energy-Efficient Circuit Design

Low Power Clocking

- Clocks consume significant power
  - 20% to 60% of the total power
- Application to low power SoCs, embedded/mobile computing

Reliable Power Delivery

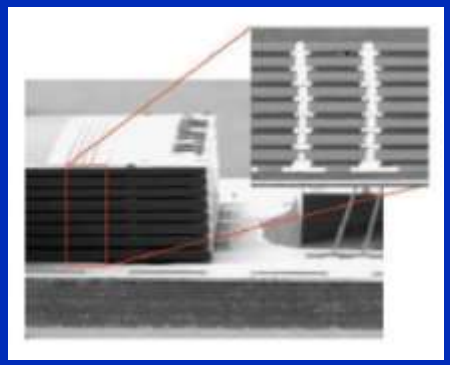
- Modern SoCs demand high current at low voltages
  - 1 Volt to 0.4 Volt
- Power delivery is critical

Industrial liaisons from Freescale Semiconductor, AMD, TI

Emerging IC Technologies

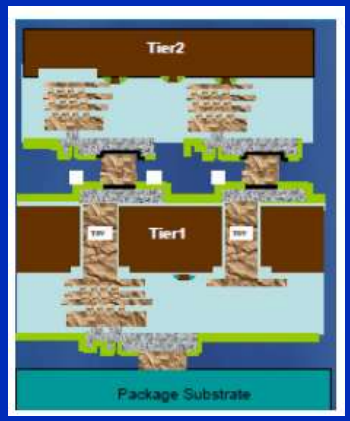
Three-dimensional (3D) integration

- **"An industry game changer" according to SEMATECH**



Source: Samsung

Source: Intel



Source: Qualcomm

- Fabless company

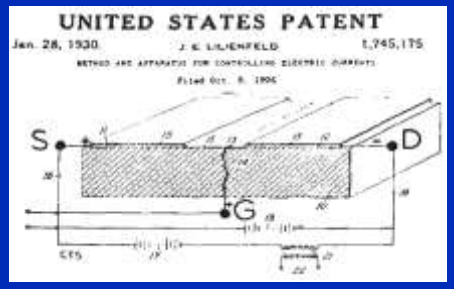
- **CAREER Grant**

Outline

- Motivation
- Background
- Recent Research Results in 3D ICs at NanoCAS Lab
- Conclusions

A Brief History

Conceptual transistor, by J.E. Lilienfeld, 1926

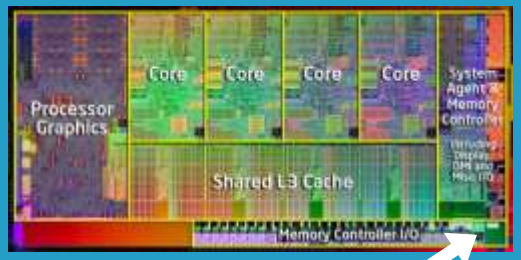


ENIAC, ``the Giant Brain,'' 1946

First transistor, 1947

Functionality

Intel Core i7, 2014



Moore's Law

Monolithic era

First IC, 1959

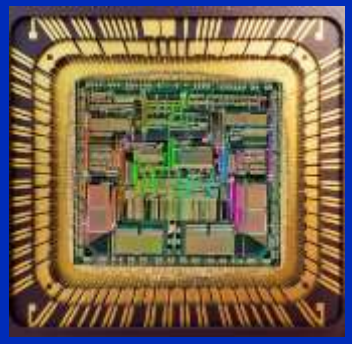
Number of devices

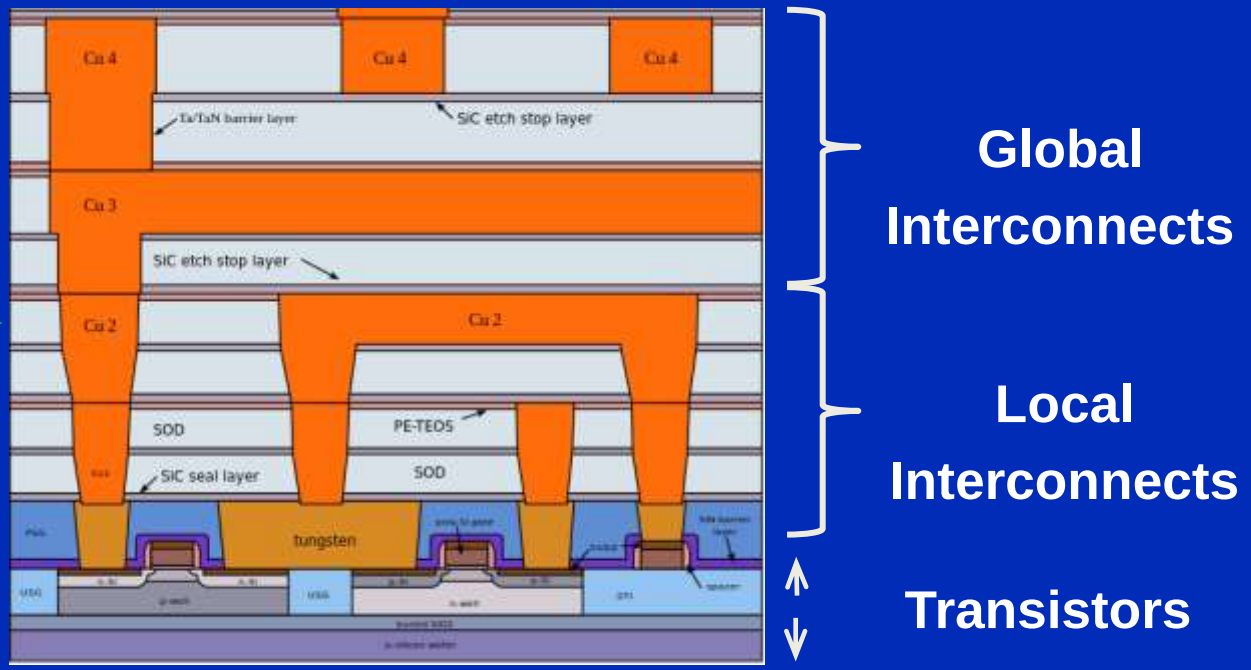
Electronics + biotechnology, ?

Electronics + nanotechnology, ?

Nanoscale Circuit Design

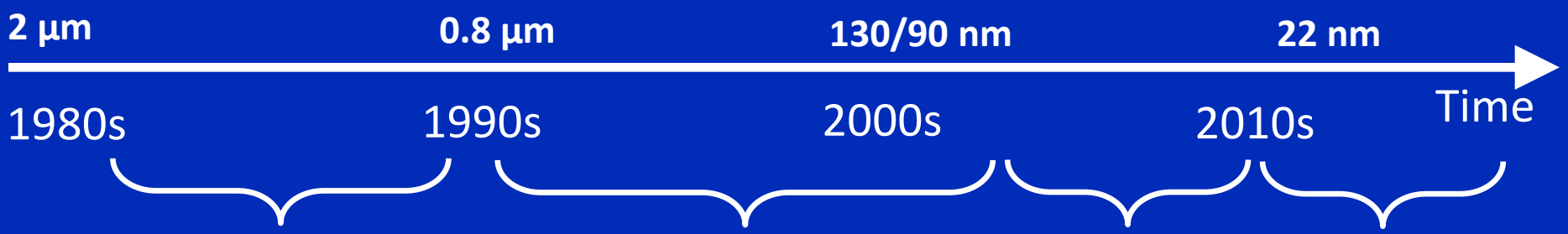
- Transistors
- Interconnections





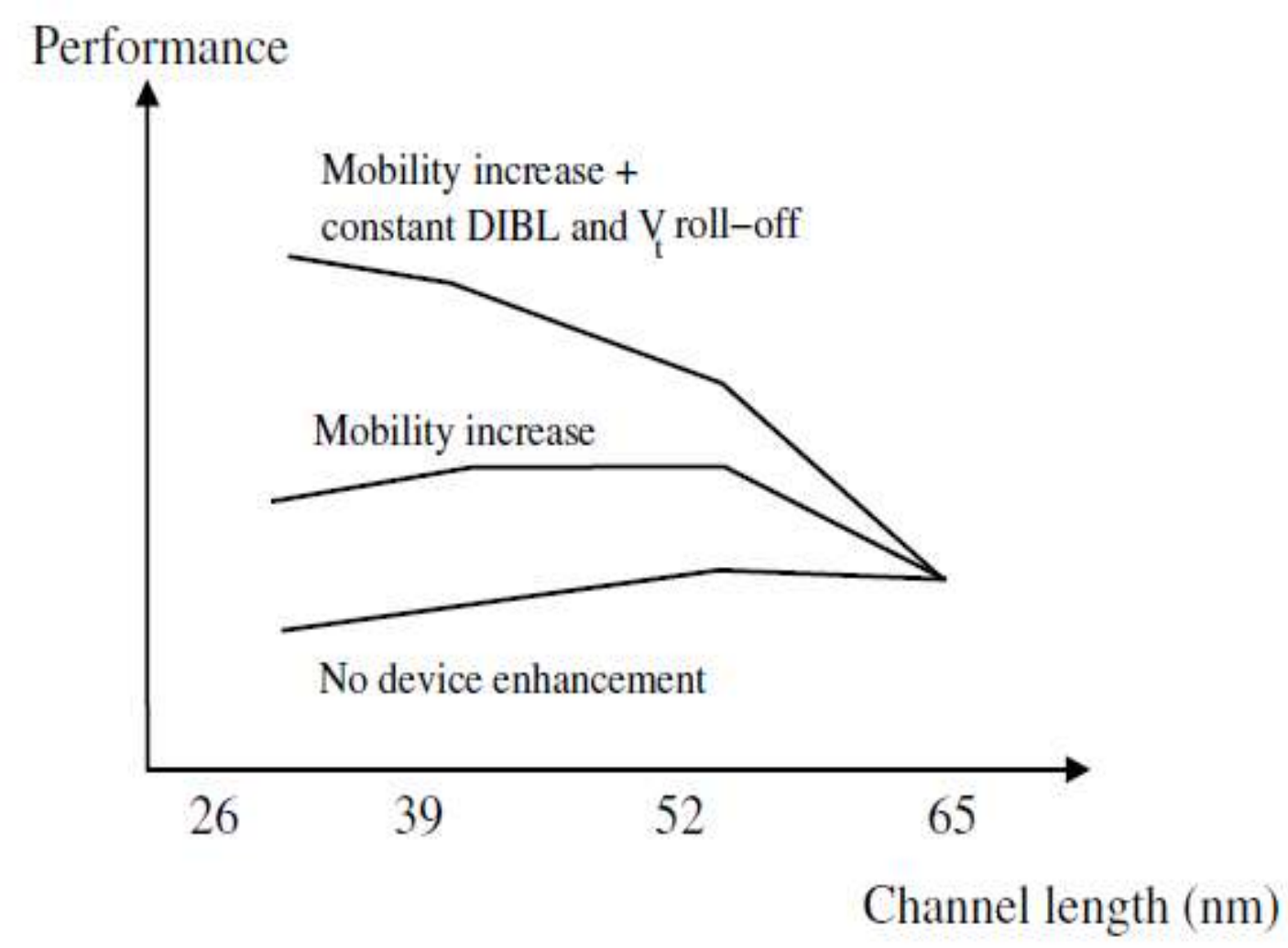
- Transistor vs interconnect scaling?

Overview of Device Scaling



- **Constant voltage**
  - Avoid multiple supply voltages
  - Reduce delay
  - Higher electric fields
- **Constant electric field**
  - Scale supply and threshold voltages
  - Reduce delay
  - Reduce power consumption
  - Constant electric field
- **"Near constant voltage"**
  - Voltages cannot scale further
  - Higher electric fields
  - Significant short channel effects
- **Structural enhancements**

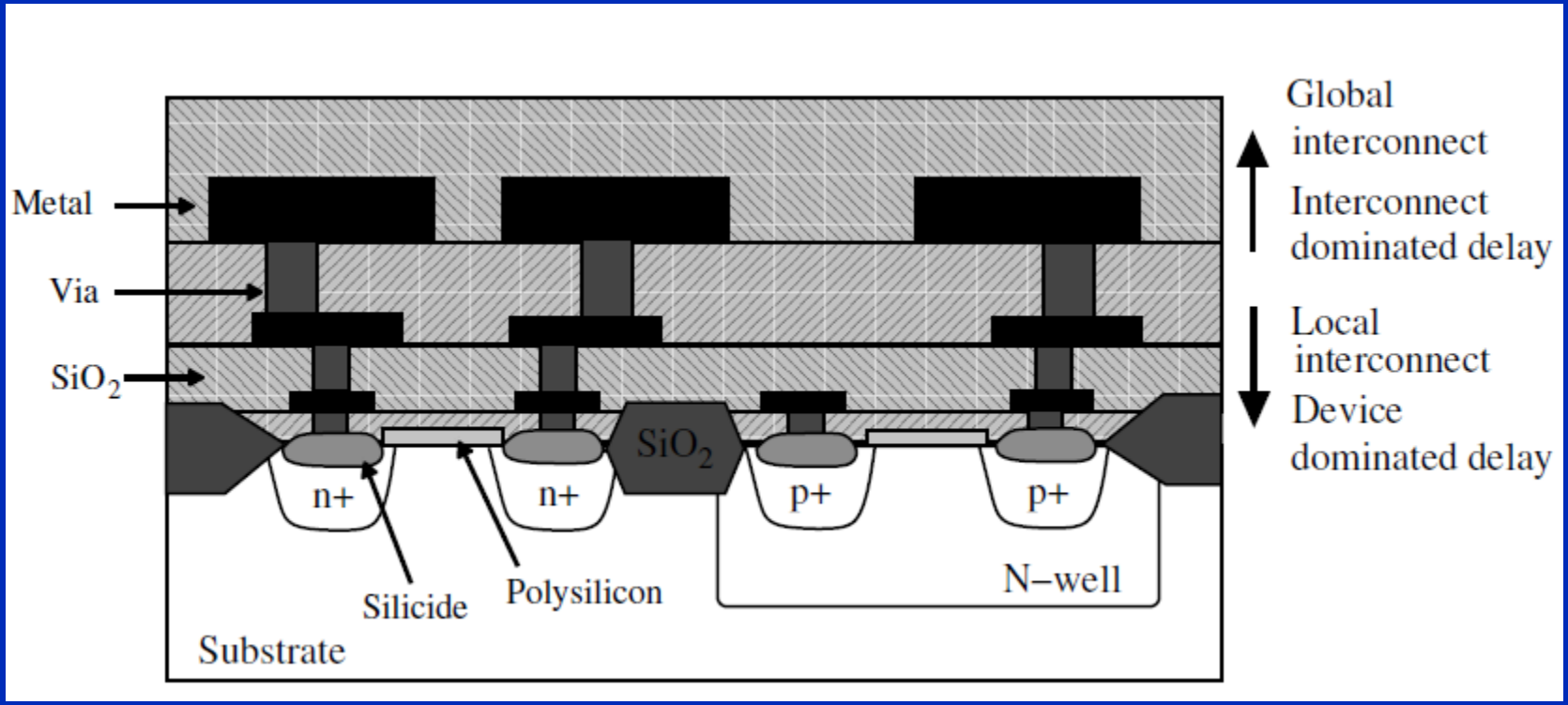
Device Scaling Scenarios



W. Haensch *et al.*, "Silicon CMOS Devices Beyond Scaling", *IBM Journal of Research and Development*, July 2006

Overview of Interconnect Scaling

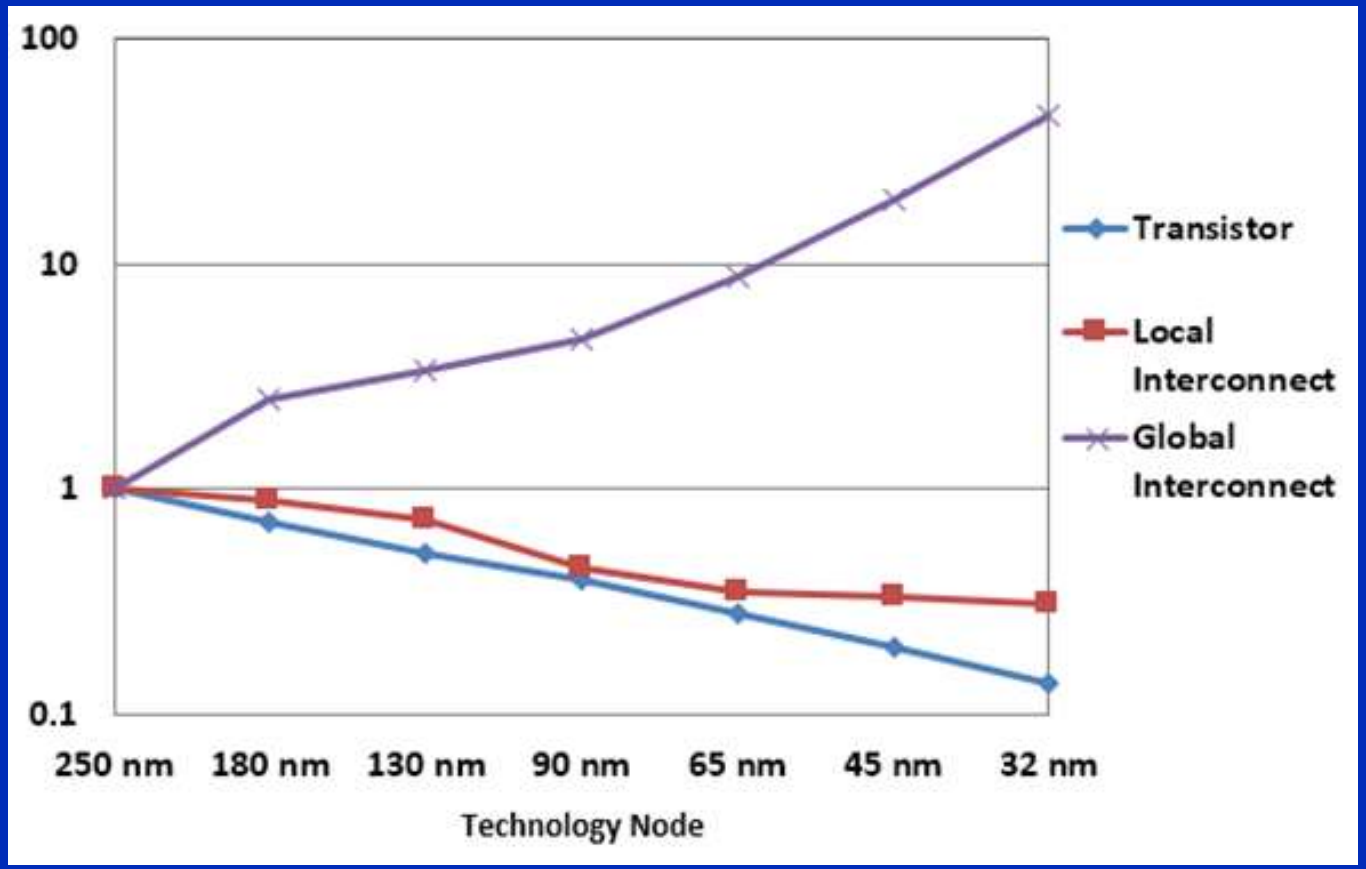
- Metal pitch reduced from 1.8 um in 1994 to a few hundred nanometers in 2011
  - Higher coupling capacitance
- Significant reduction in the cross-sectional area
  - Higher parasitic resistance



Interconnect Scaling Scenarios

Interconnect parameters	Ideal scaling		Quasi-ideal scaling		Constant resistance		Constant thickness	
	Local	Global	Local	Global	Local	Global	Local	Global
Resistance	S	$S_c S^2$	$\sqrt{S}$	$S_c S\sqrt{S}$	1	1	1	SS_c
Coupling capacitance (C^c)	$1/S$	S_c	$1/\sqrt{S}$	$S_c\sqrt{S}$	$1/S$	$S_c^2 S$	1	$S_c S$
Ground capacitance (C^g)	$1/S$	S_c	$1/(S\sqrt{S})$	$S_c/\sqrt{S}$	$1/S$	S_c	$1/S$	S_c
C^c/C^g	1	1	S	S	1	$S_c S$	S	S
RC Delay	1	$S_c^2 S^2$	1/S to 1	$S_c^2 S$ to $S_c^2 S^2$	1/S	S_c to $S_c^2 S$	1/S to S	$S_c^2 S$ to $S_c^2 S^2$

Interconnect Scaling Scenarios

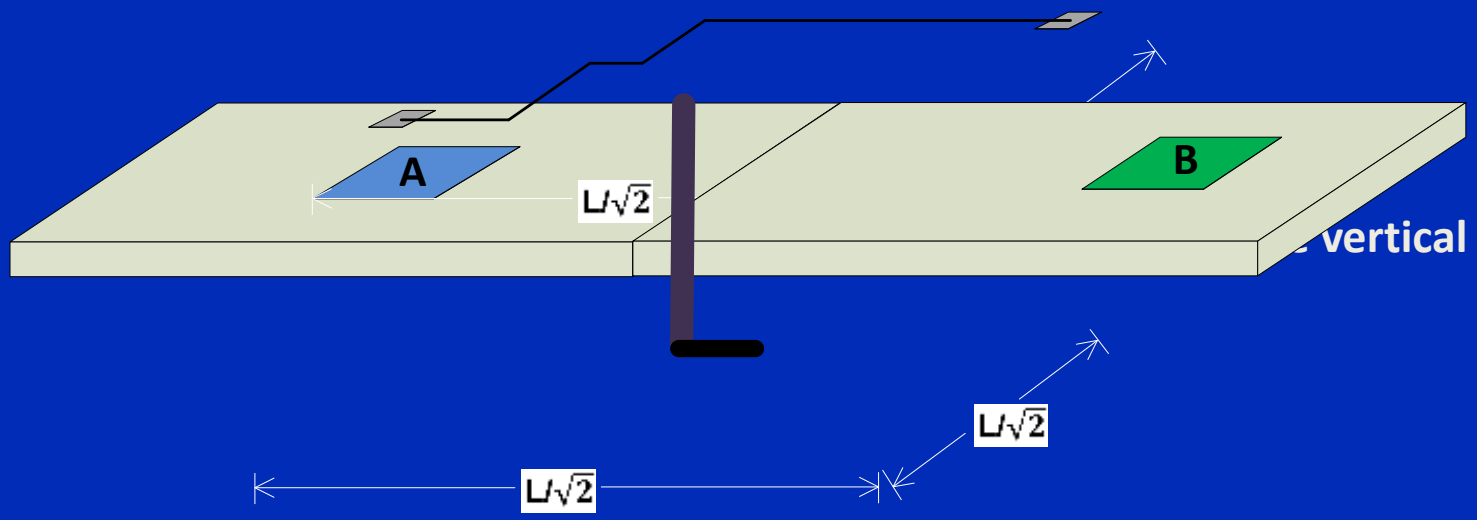


Interconnect-centric design era

Vertical Integration

- One solution: **Go vertical!**

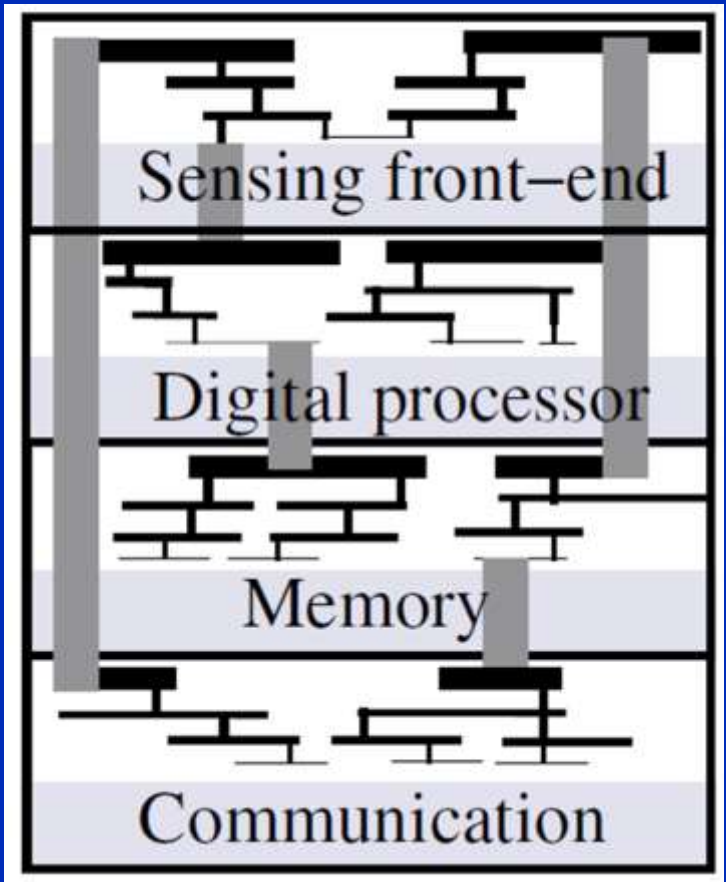
Longest interconnect = $\sqrt{2} \times L$ (Compared with $2 \times L$)

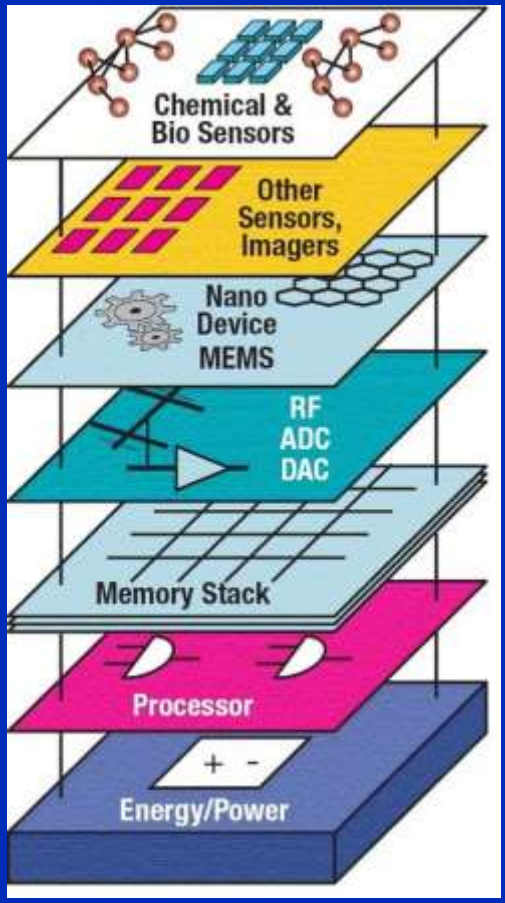


Reduction of longest interconnect length : $\sqrt{N}$

(N = number of planes)

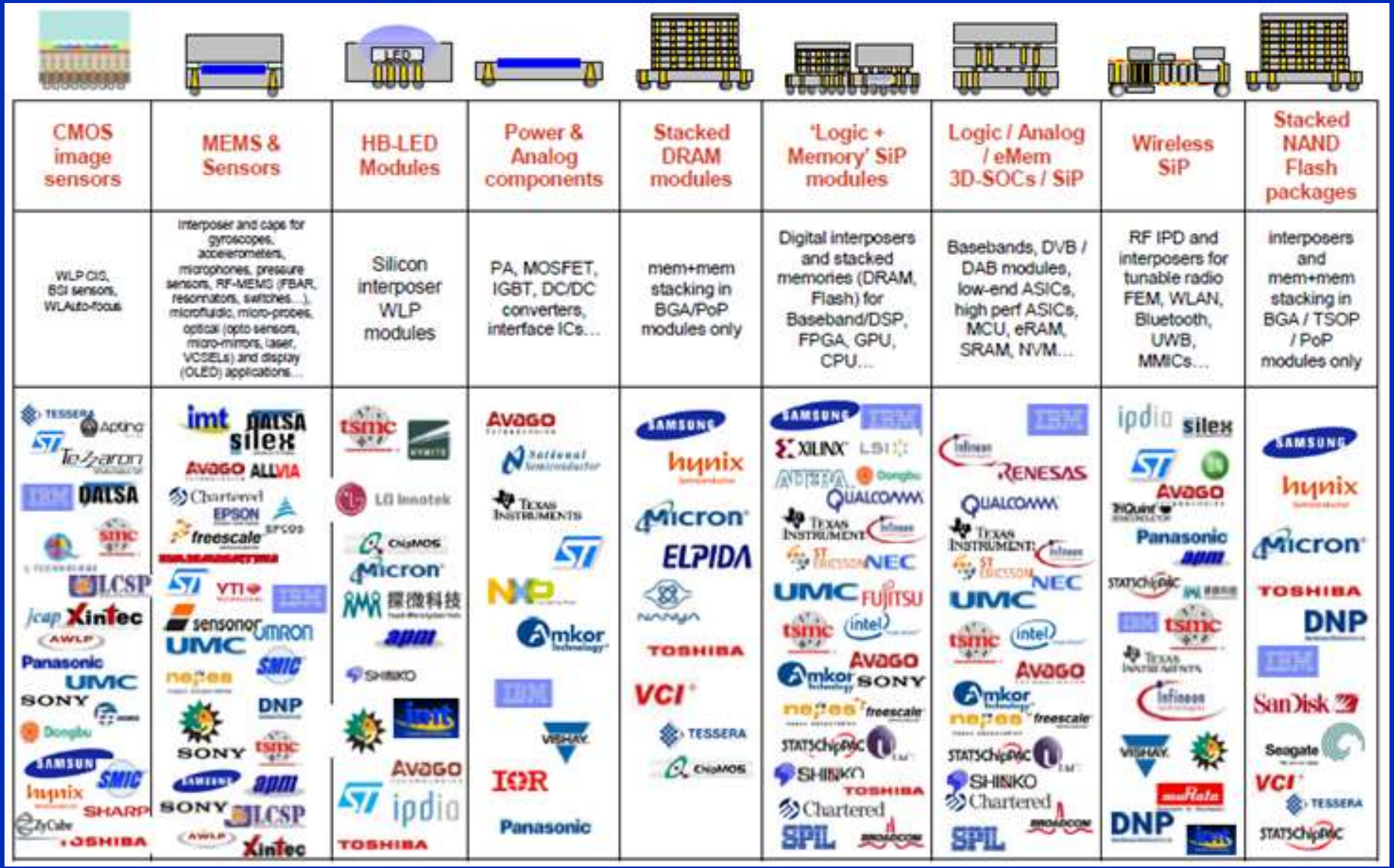
Heterogeneous Integration





Dies with different functions, fabricated with different technologies are integrated

3D Applications and Players

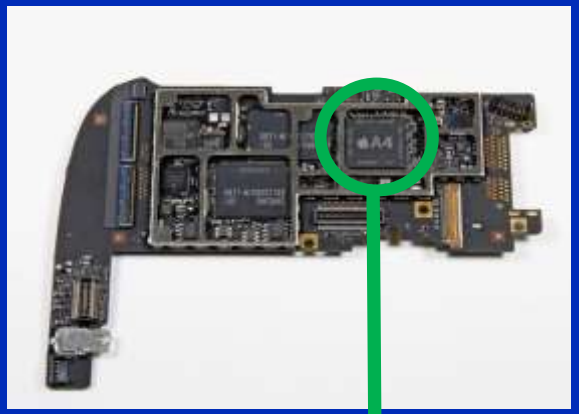


Outline

- Motivation
- Background
  - 3D Integration Technology
  - Power and Signal Integrity
- Recent Research Results in 3D ICs at NanoCAS Lab
- Conclusions

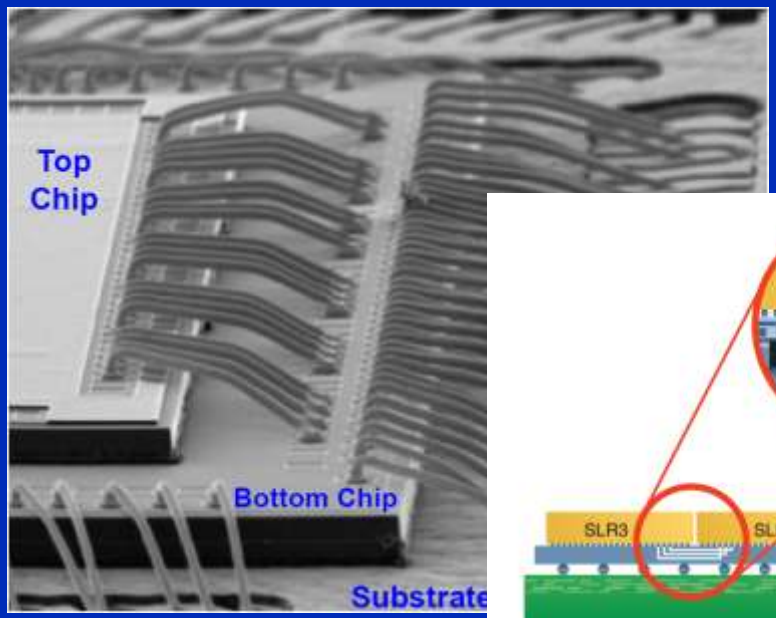
Example

- Apple A4 Chip (for 1st Gen iPad and iPhone 4)

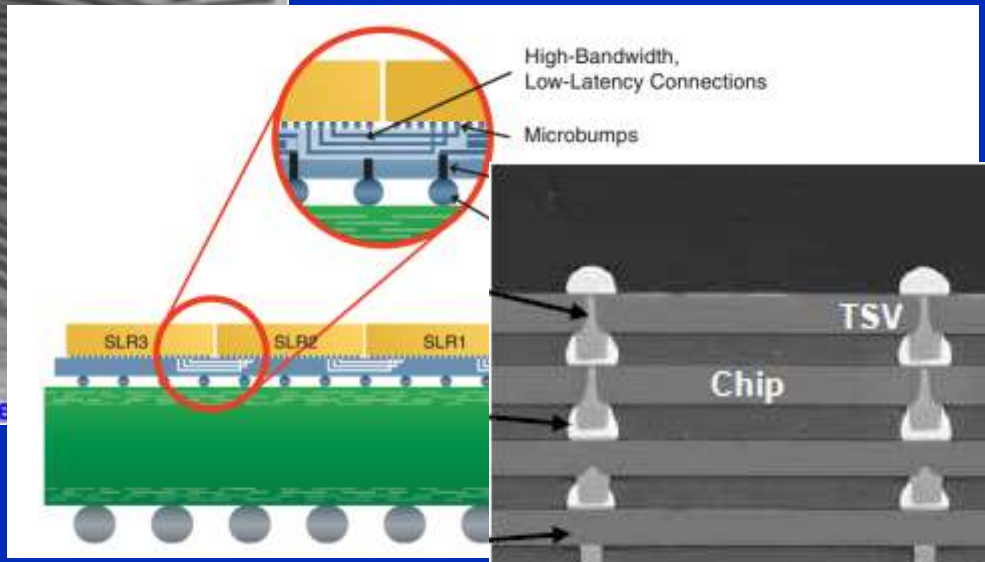


Off-chip vertical connections

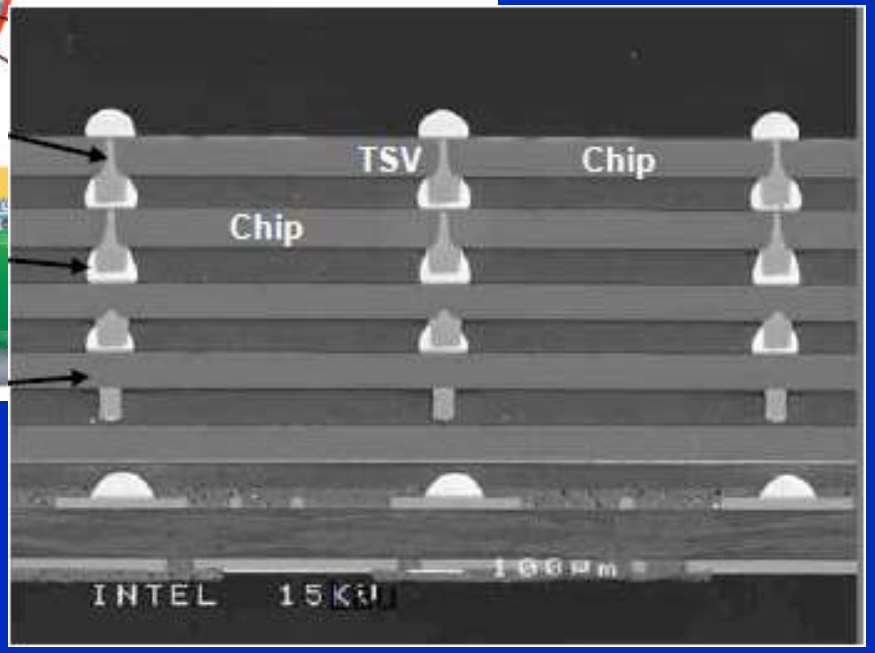
Different Types of 3D ICs



3D Package-on-Package, Amkor



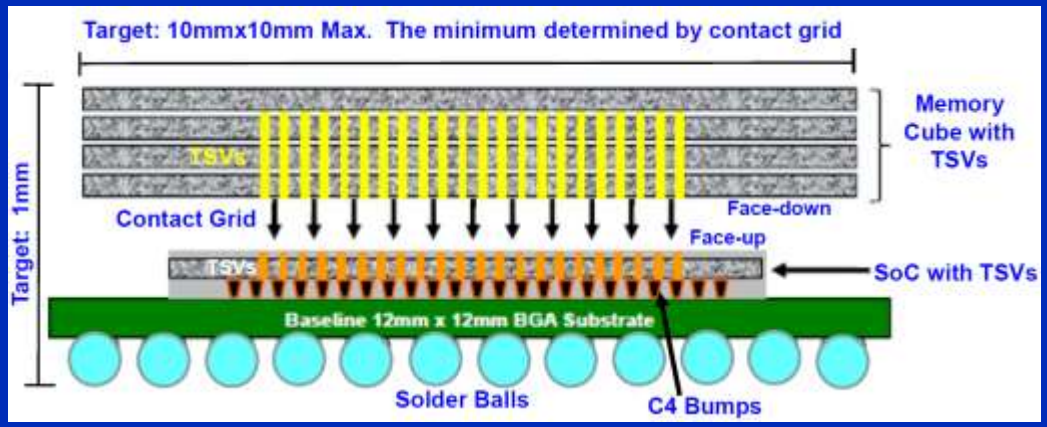
Interposer Based Integration, Xilinx



Through Silicon Via (TSV), Intel

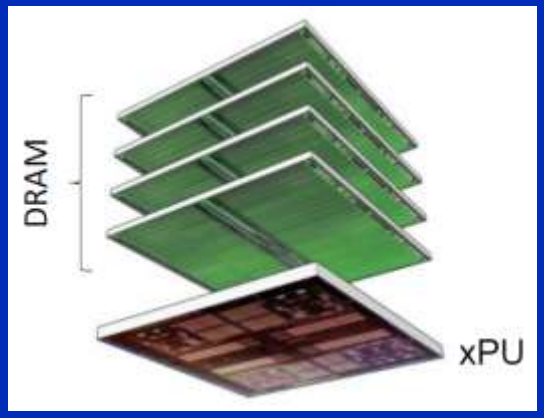
Current Status in Industry

- **Hyper Memory Cube (already commercially available)**



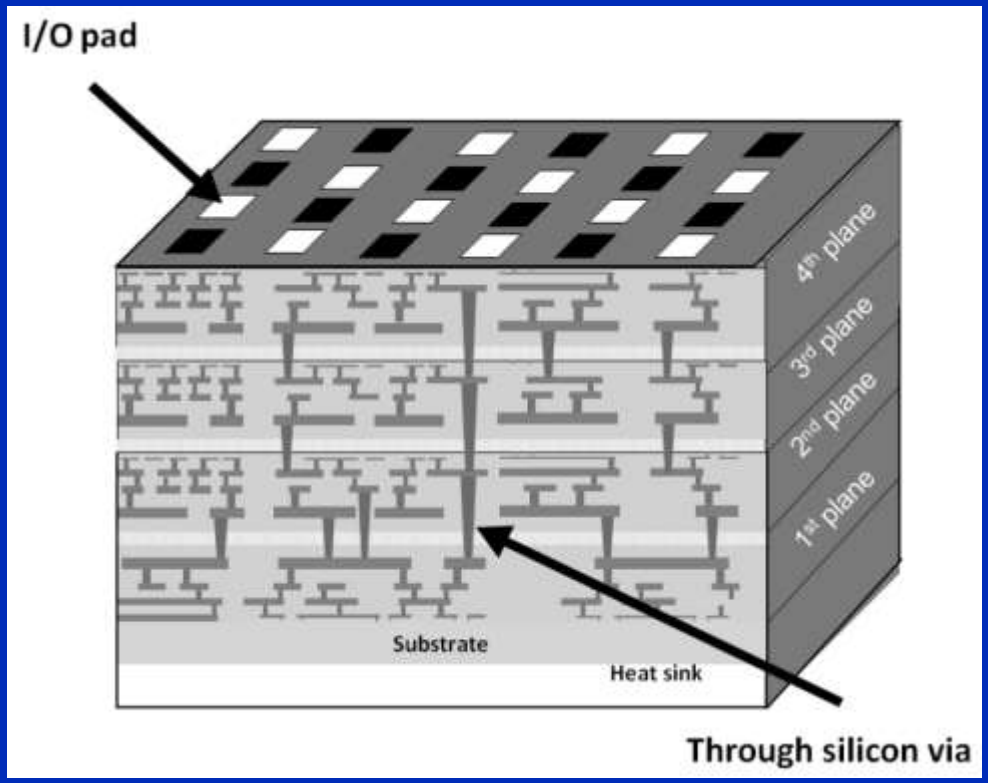
Micron Wide I/O DRAM (15X faster, 70% less energy and 90% less space)

- **Memory-Processor Stack (next step)**



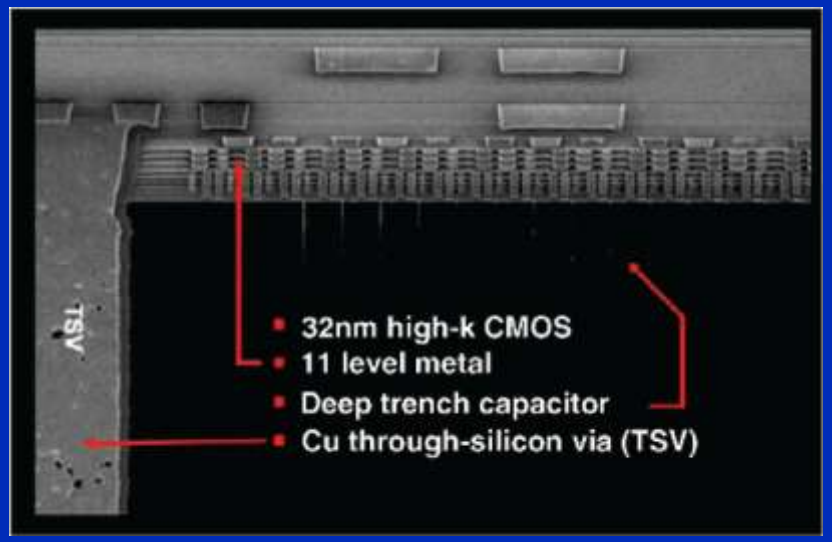
AMD xPU + DRAM stacking

Wafer-Level TSV Based 3D Integration

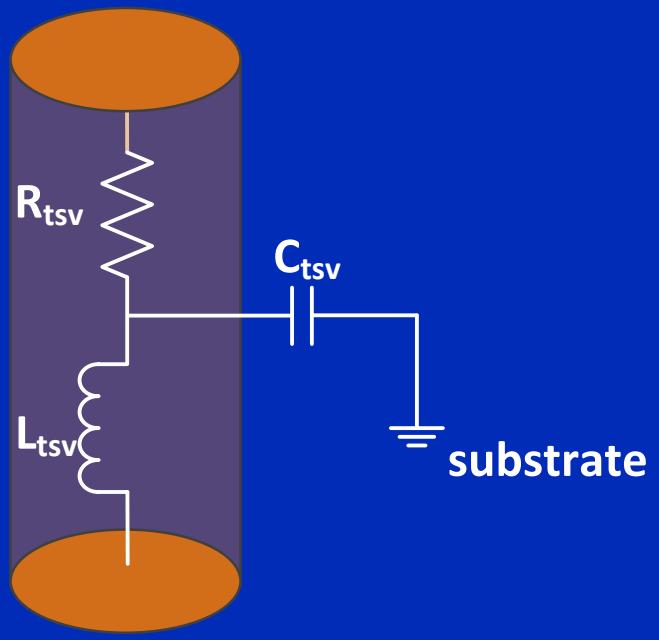


- Multiple wafers are
  - Thinned
  - Aligned
  - Bonded
- No fundamental limitations exist
  - Alignment accuracy of 1 um
  - Adhesive, oxide, metal bonding
  - Wafer thinning capability
    - 0.1 um for SOI
    - 15 um for bulk silicon

Through Silicon Via

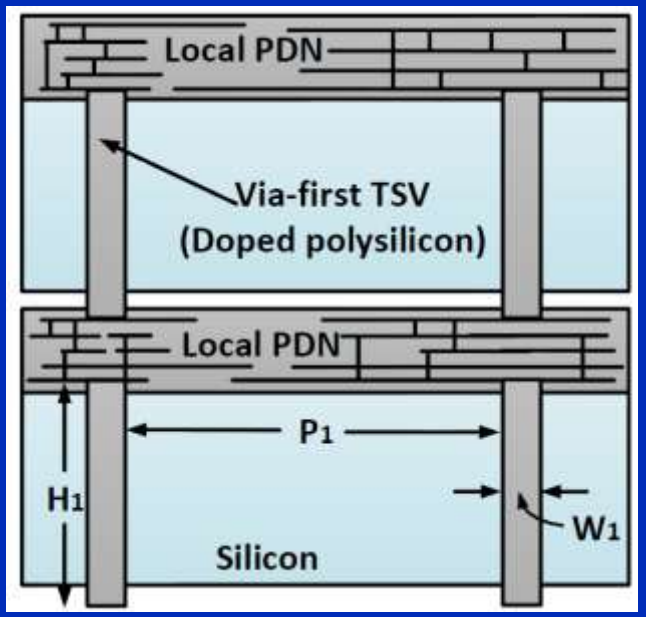


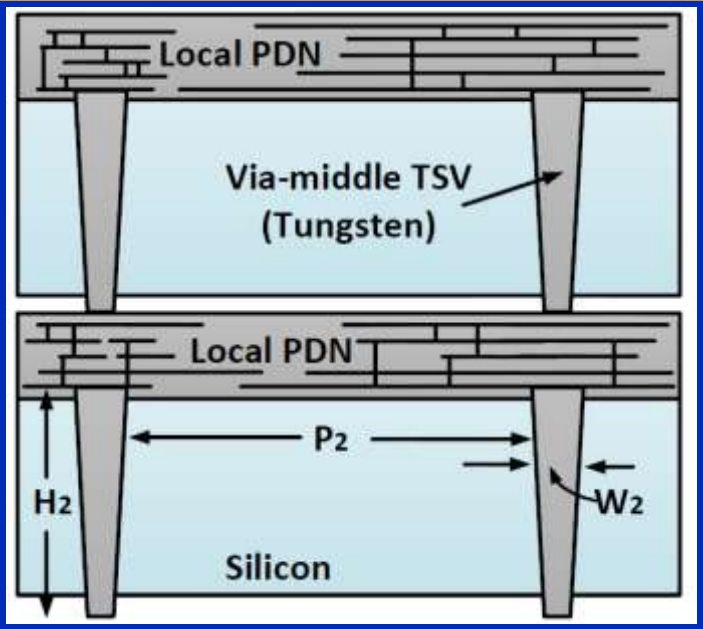
Courtesy of IBM



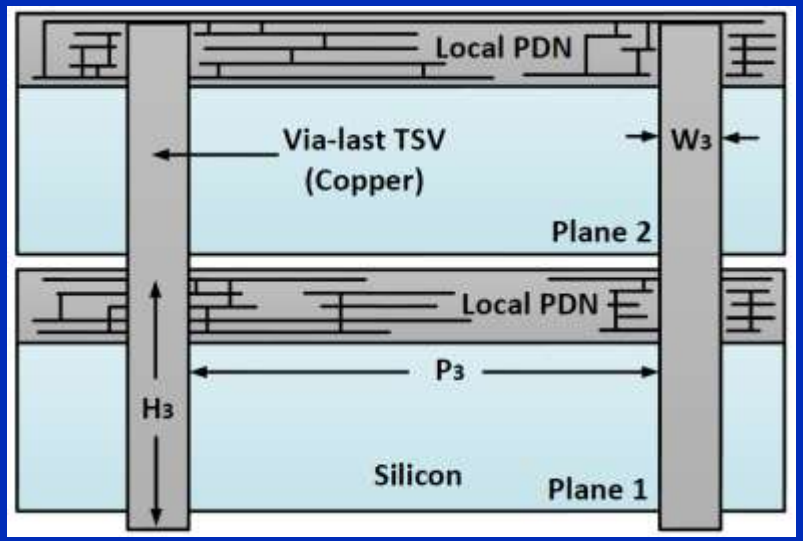
- TSVs are large
  - Diameter in the 2 to 10 um range
  - Height in the 8 to 60 um range
- TSVs have parasitic impedances (RLC)

TSV Fabrication Techniques





- **Via-first**
  - Prior to FEOL process



- **Via-middle**
  - After FEOL
  - Before BEOL
- **Via-last**
  - After BEOL

Primary Challenges

- **Fabrication**
  - TSV reliability and stress
  - Bonding techniques
  - Thermal/Cooling
- **Design**
  - Architecture
  - Design for test
  - EDA tools
  - Design for thermal integrity
  - Physical design
    - Power integrity
    - Signal integrity

Research Focus on 3D ICs

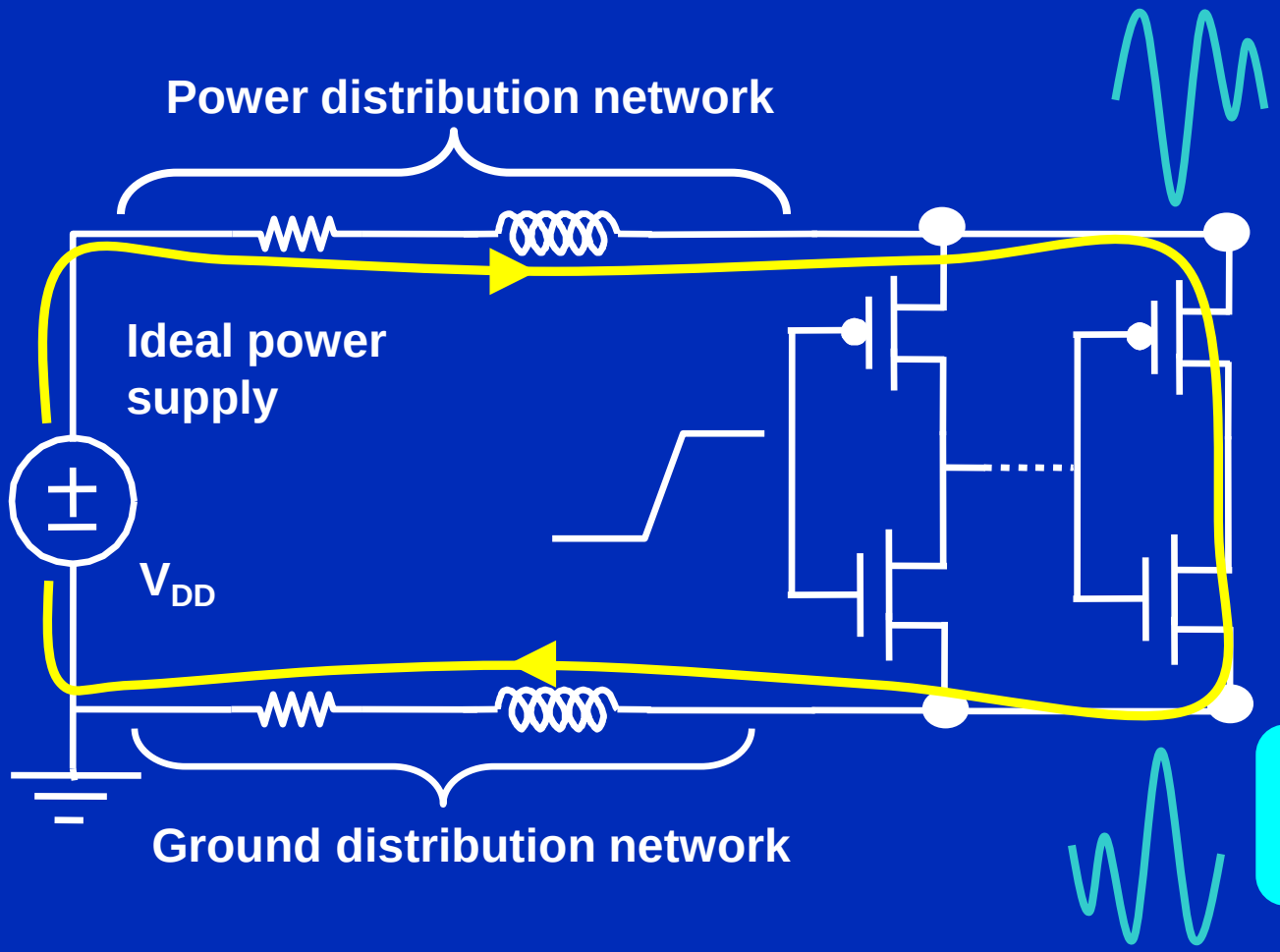
Power integrity and power aware design for 3D ICs

- Power distribution in processor-memory stacks
  - [JETCAS'12, SOCC'12, GLSVLSI, 13]
- Decoupling capacitor topologies for 3D ICs
  - [TVLSI'15, ISQED'15]
- Resource allocation in 3D ICs
  - [ISQED'15, GLSVLSI'13]
- Low power 3D ICs
  - [ISCAS'15]

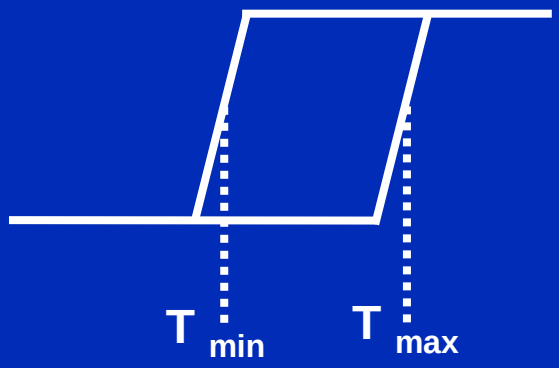
Signal Integrity for 3D ICs

- TSV-to-transistor noise modeling
  - [Integration'14,GLSVLSI'13]
- Noise analysis for implantable 3D ICs
  - [ISCAS'11, BioCAS'11]

Power Integrity and Delay Uncertainty



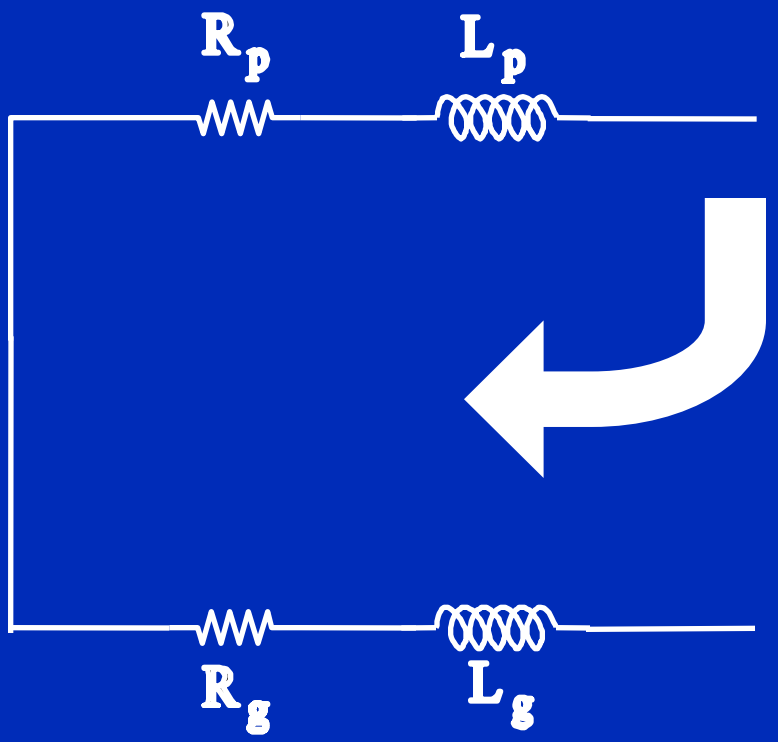
$$V_p = V_{DD} - IR_p - L_p \frac{di}{dt}$$



$$V_g = V_{GND} - IR_g - L_g \frac{di}{dt}$$

- *"I have thought about some of the problems of building electric circuits on a small scale, and the problem of resistance is serious."* **Feynman, 1959**

Impedance Characteristics

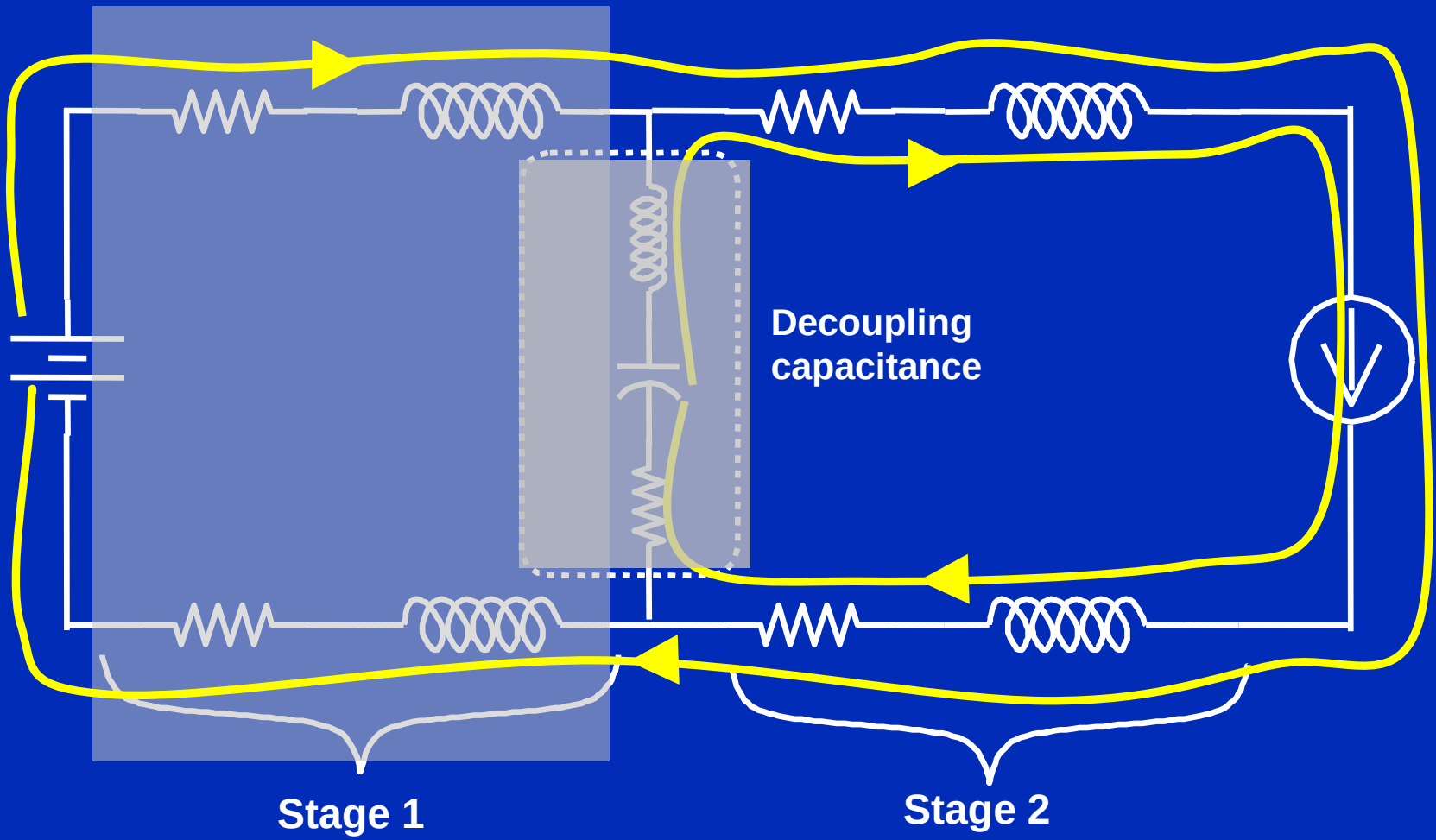


$$Z_{target} = \frac{\text{Nominal voltage} \times \text{Allowed ripple}}{\text{Current}}$$

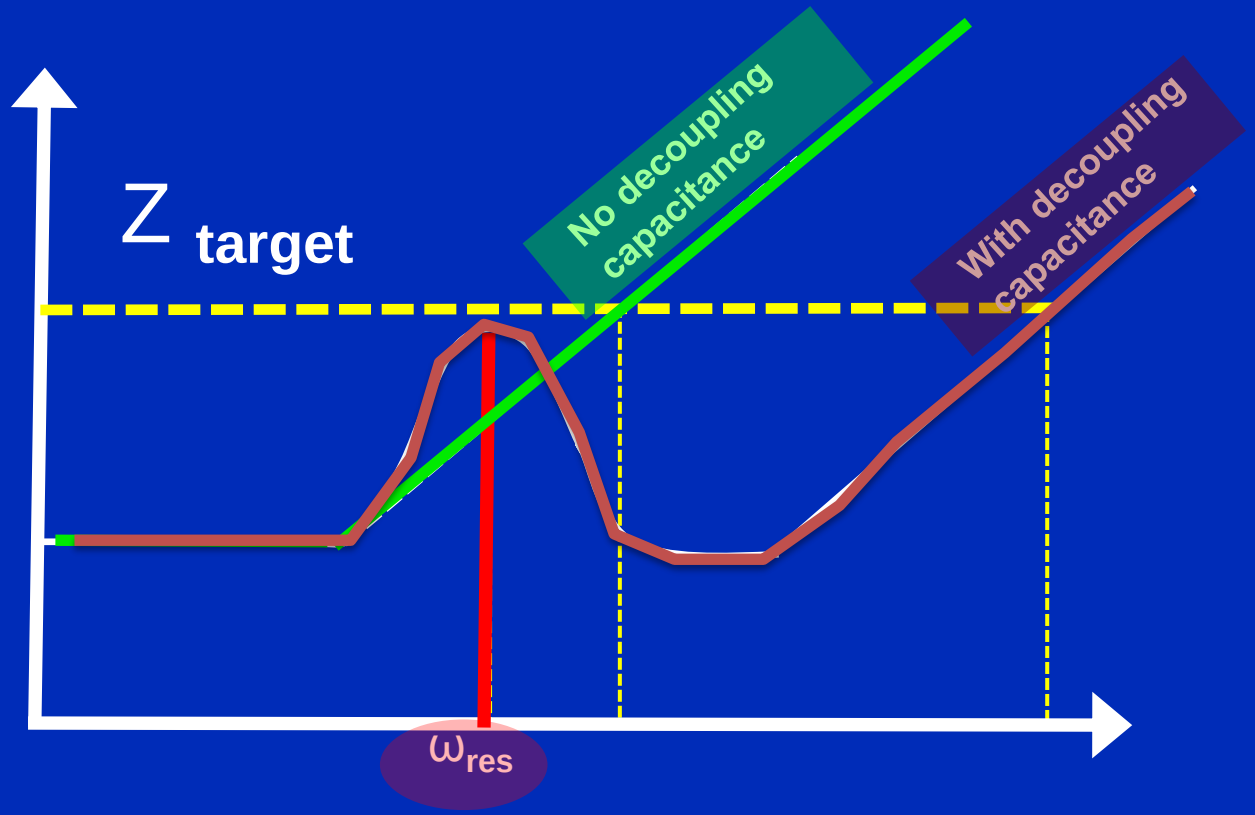
$$= \frac{\text{Nominal voltage}^2 \times \text{Allowed ripple}}{\text{Power consumption}}$$

- 65 nm CMOS microprocessor*
  - P = 250 watts
  - V_{DD} = 1.2 volts
  - Ripple = 10% of V_{DD}
  - Target impedance ≤ 0.3 milliohms

Decoupling Capacitance

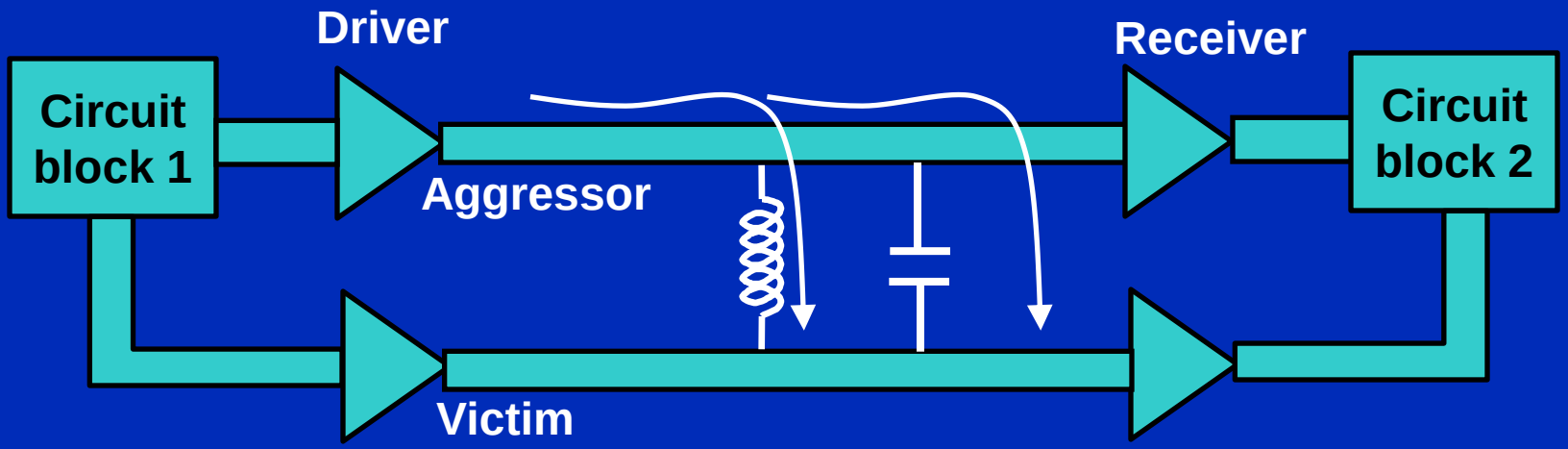


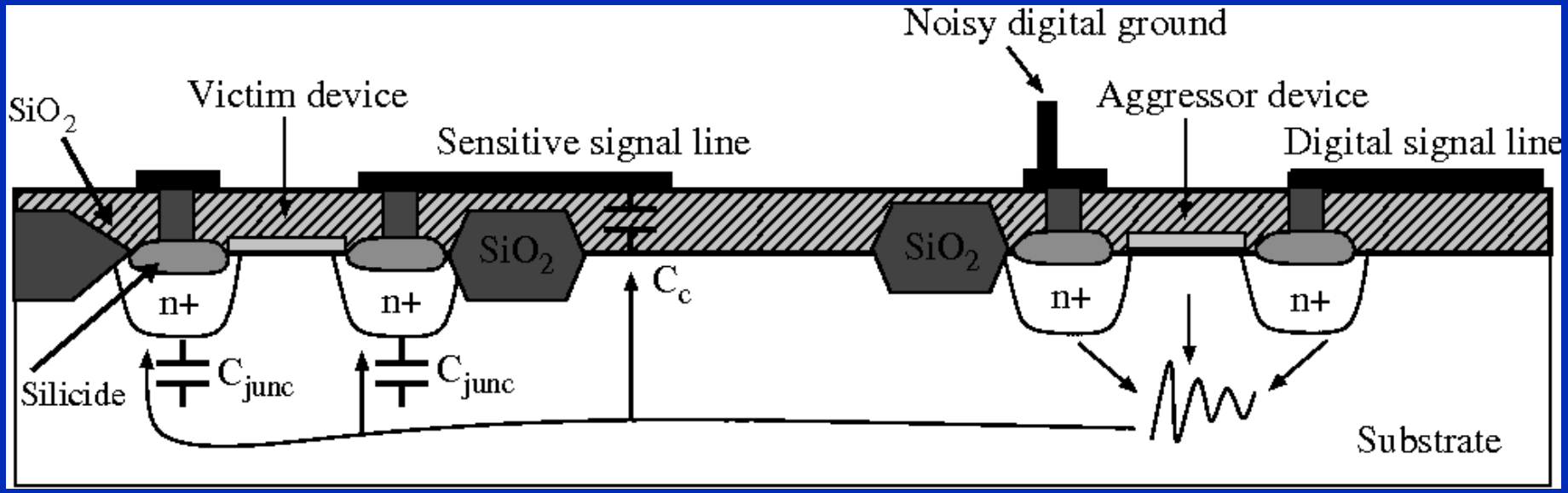
Decoupling Capacitance and Impedance



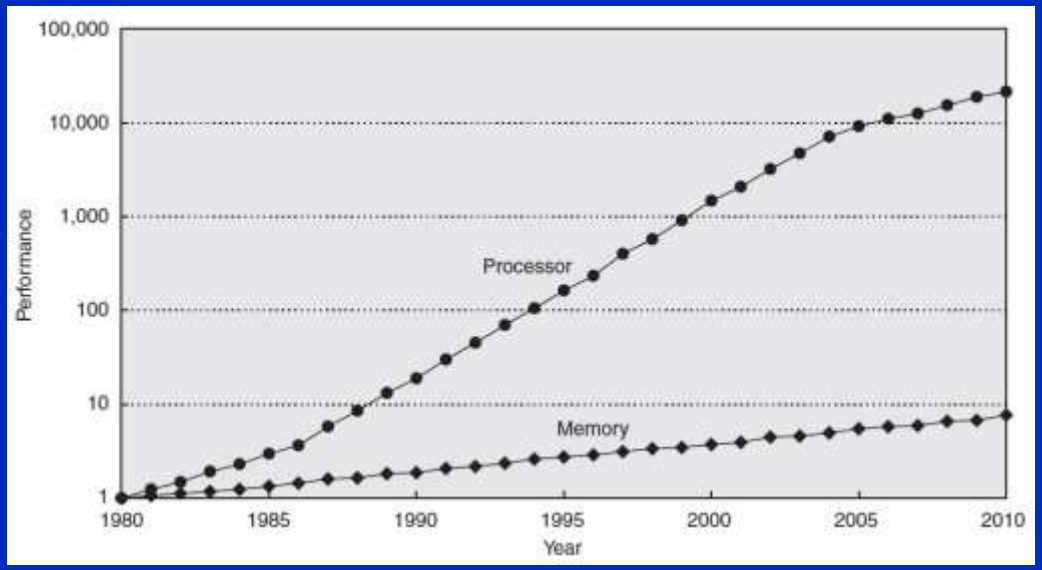
- Decap is required to satisfy target impedance
- Resonance should be carefully considered

Signal Integrity

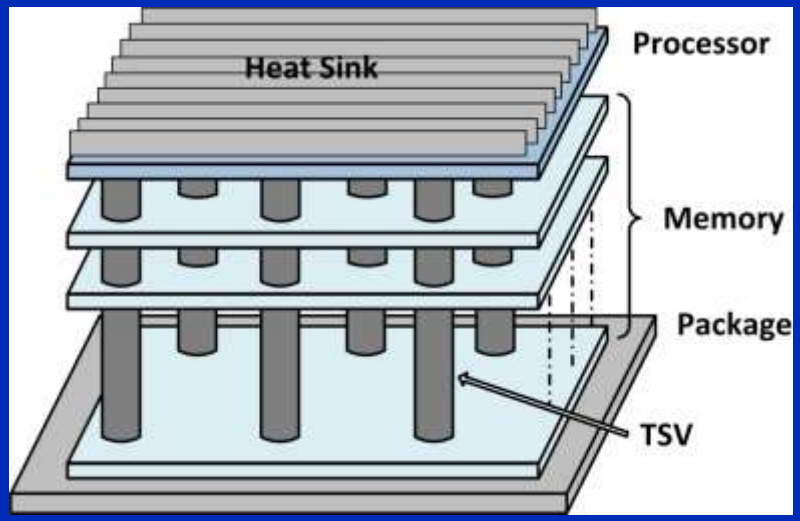




3D Processor-Memory Stacks



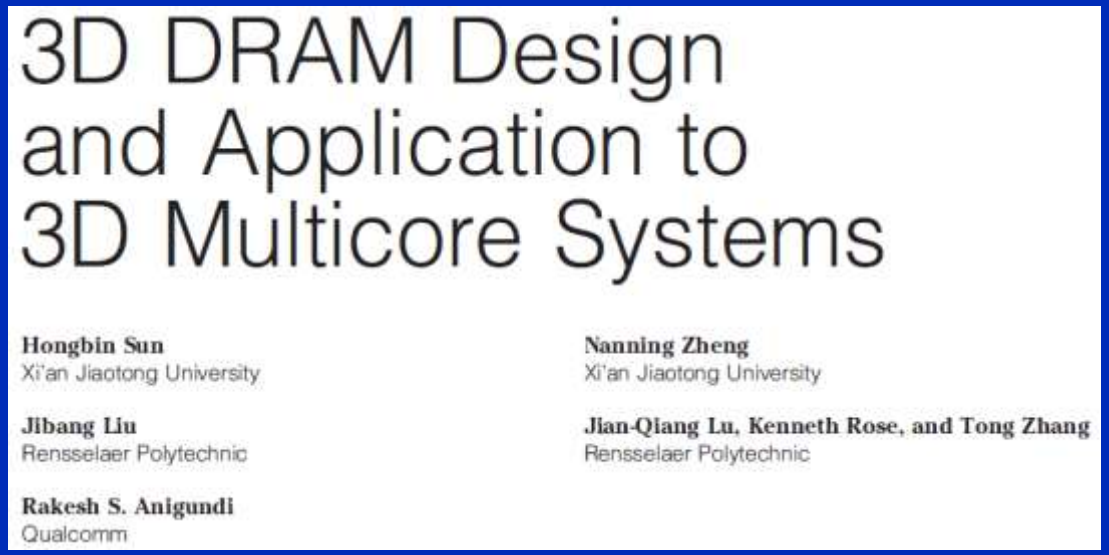
J. L. Hennessy and D. A. Patterson, Morgan Kaufmann 2011



3D processor-memory stack

- Higher on-chip memory bandwidth
- Reliable power delivery is an important challenge

3D Processor-Memory Stacks


3D DRAM Design and Application to 3D Multicore Systems

Hongbin Sun
Xi'an Jiaotong University

Nanning Zheng
Xi'an Jiaotong University

Jibang Liu
Rensselaer Polytechnic

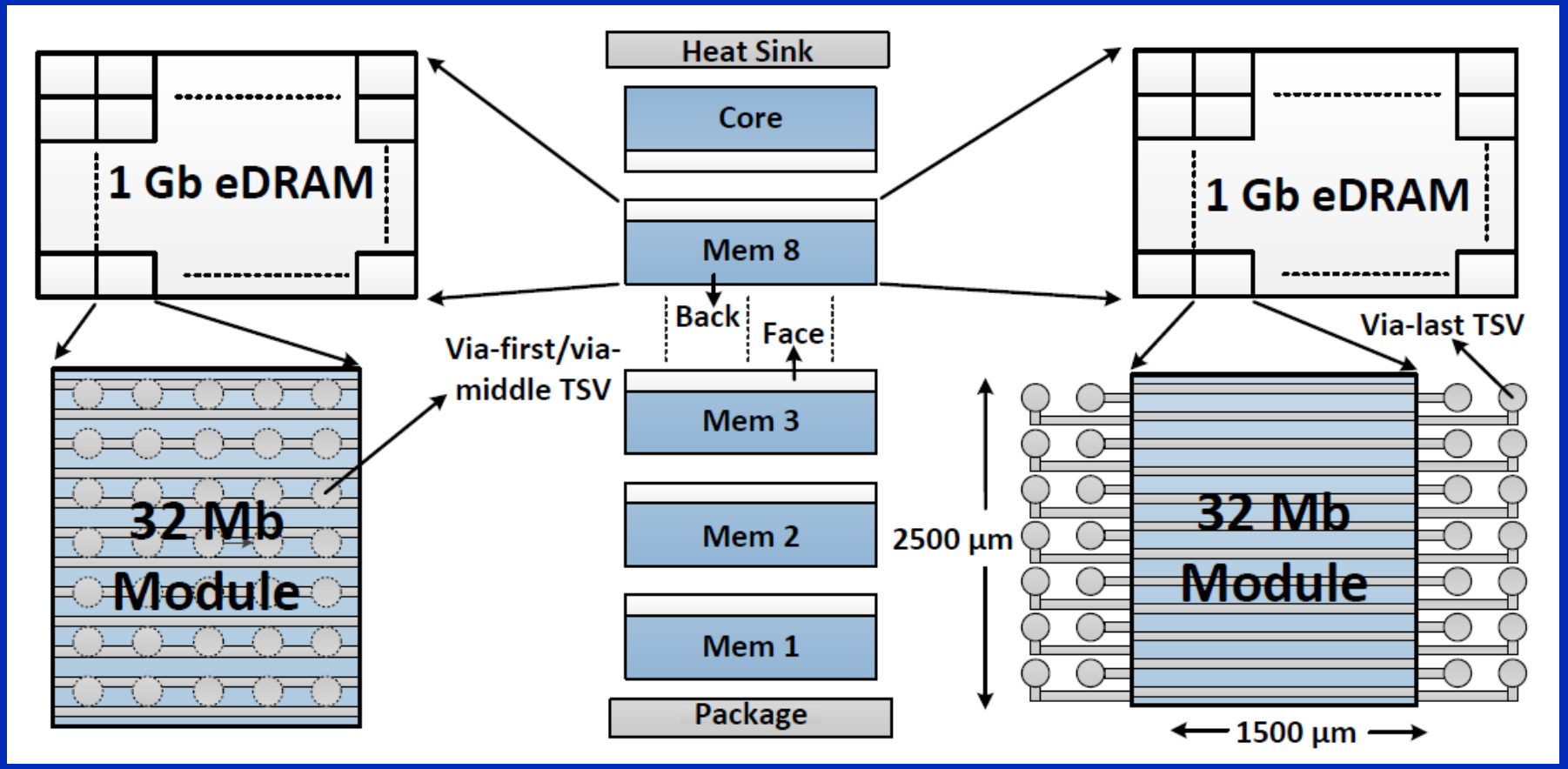
Jian-Qiang Lu, Kenneth Rose, and Tong Zhang
Rensselaer Polytechnic

Rakesh S. Anigundi
Qualcomm

IEEE Design & Test of Computers, 2009

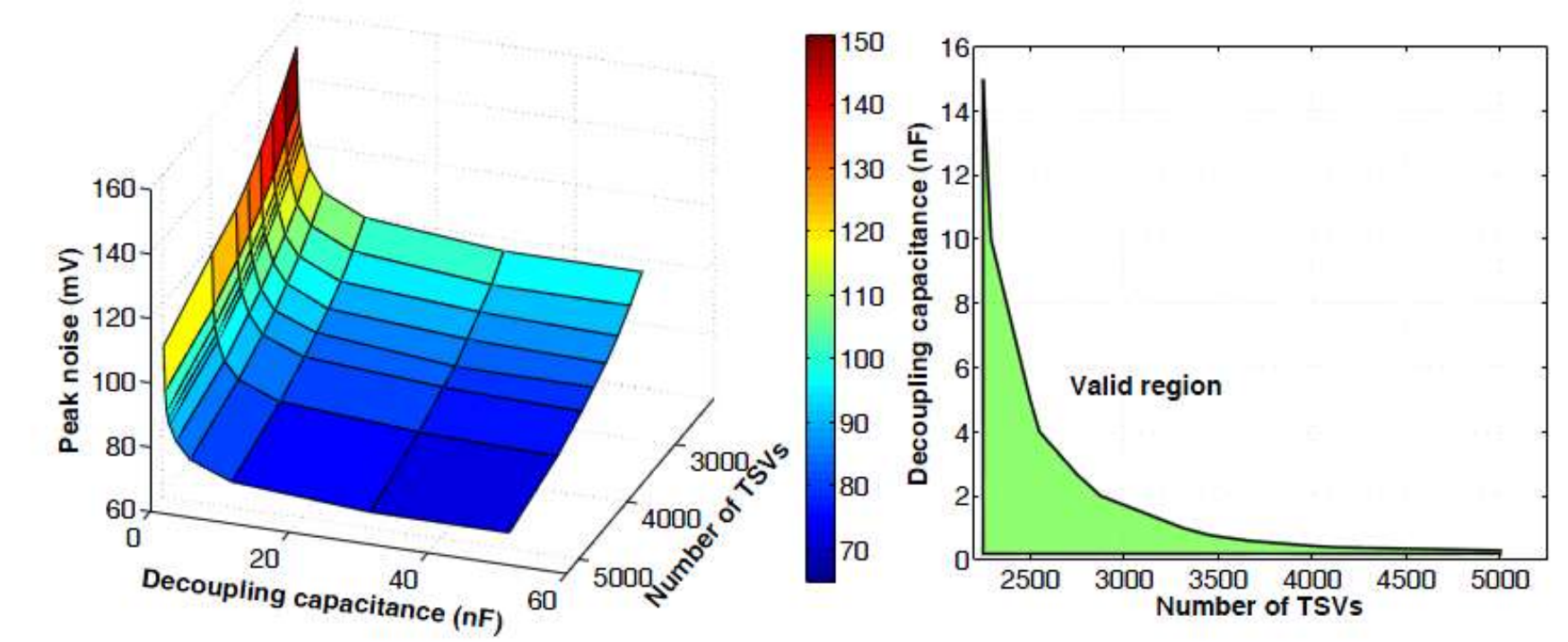
- **Potential architectural benefits of a 9 plane memory + processor stack (1 GB embedded memory)**
  - **Access latency, footprint, energy consumption**
- **Power delivery is identified as a primary challenge**

Nine Plane 3-D Processor-Memory Stack



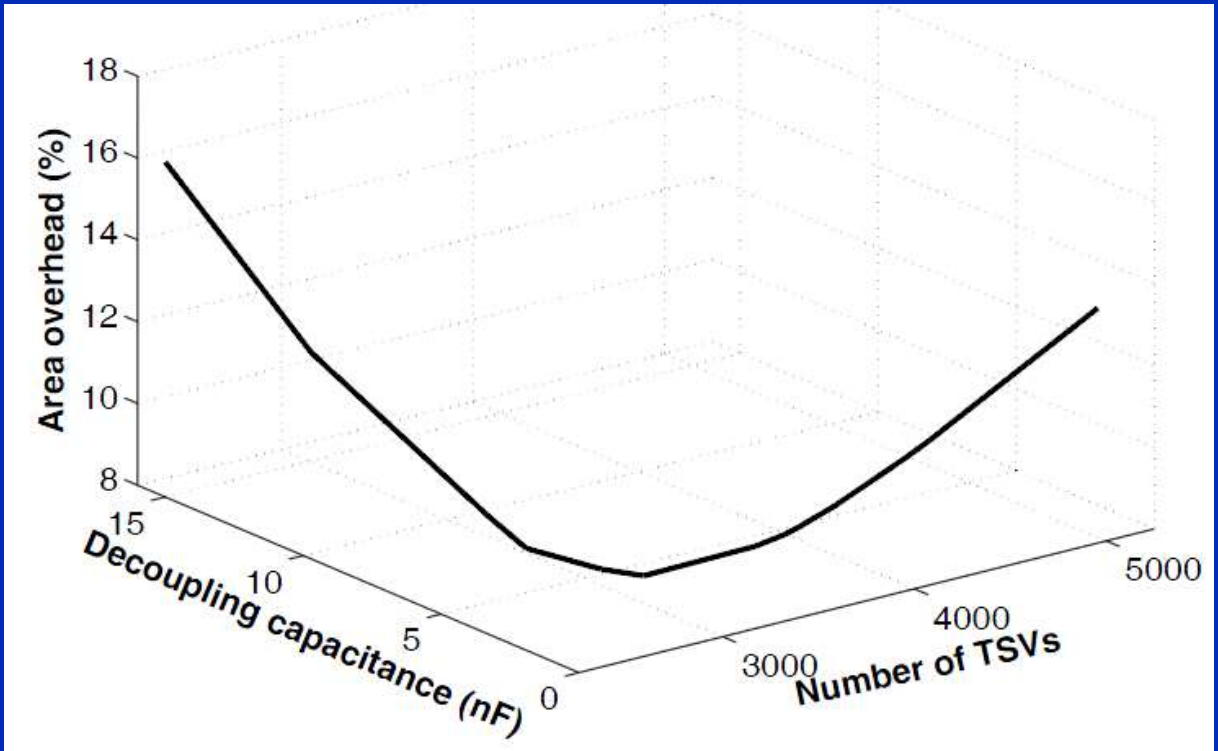
- How many power/ground TSVs are required?
- How much decoupling capacitance is required?
  - Satisfy power supply noise (target impedance)
  - Minimize area

Design Space for Via-First TSV



- Monotonic response
- Typically over-damped
  - Relatively low peak-to-peak noise
- High number of TSVs to reduce effective resistance
- High decoupling capacitance to reduce transient *IR* drop

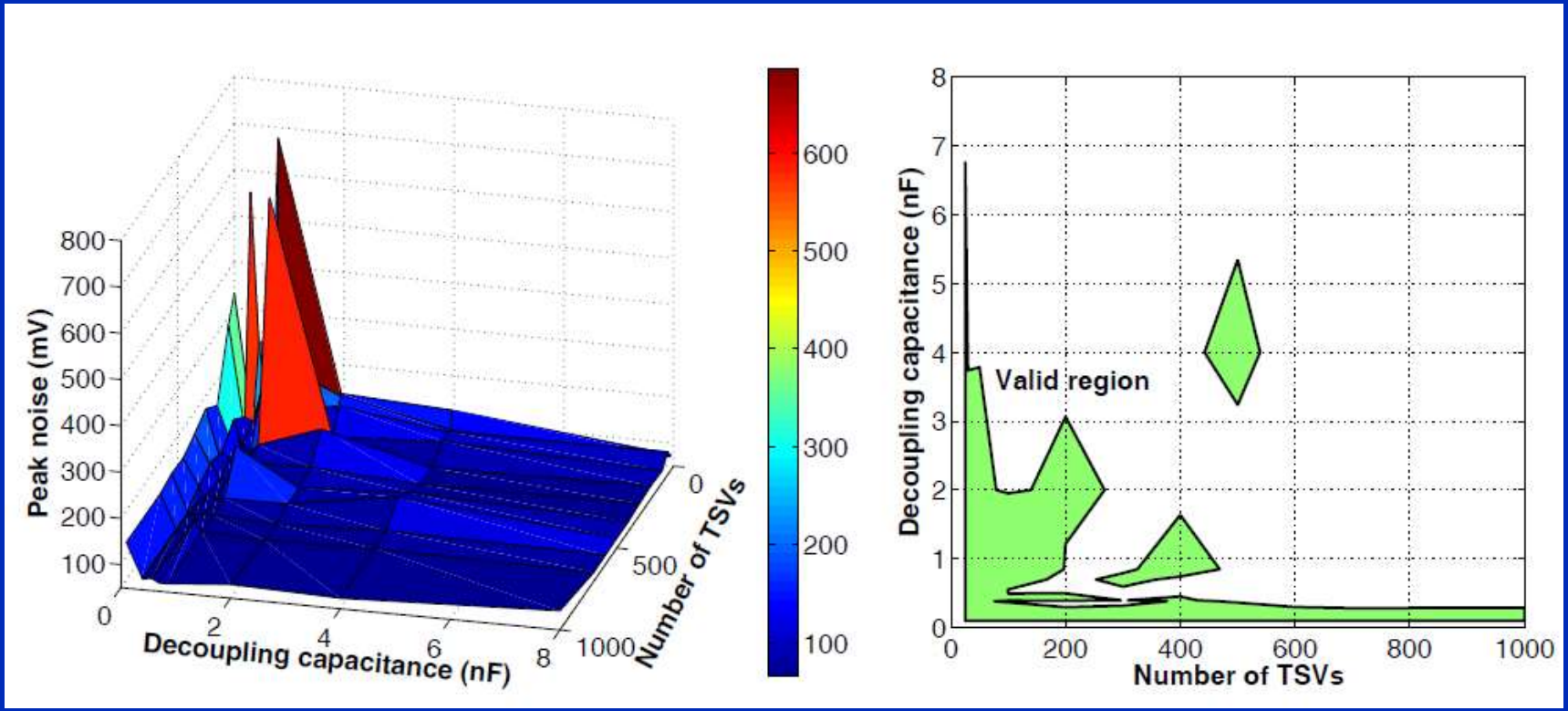
Minimum Physical Area for Via-First TSV



- Decap is implemented as MOS-C
  - 39 fF/um^2 → 32 nm technology node (from EOT)
- Optimum pair exists that minimizes area
  - 2750 TSVs and 2.7 nF of decoupling capacitance
  - 9% area overhead
  - 34 mV peak-to-peak noise

S. M. Satheesh and E. Salman, "Power Distribution in TSV Based 3D Processor-Memory Stacks," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, December 2012

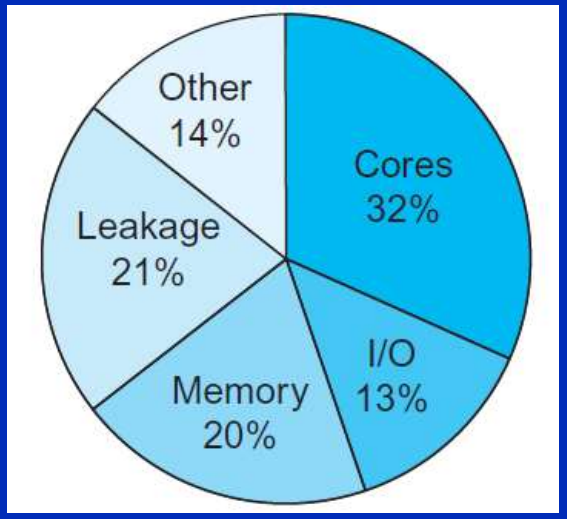
Design Space for Via-Last TSVs



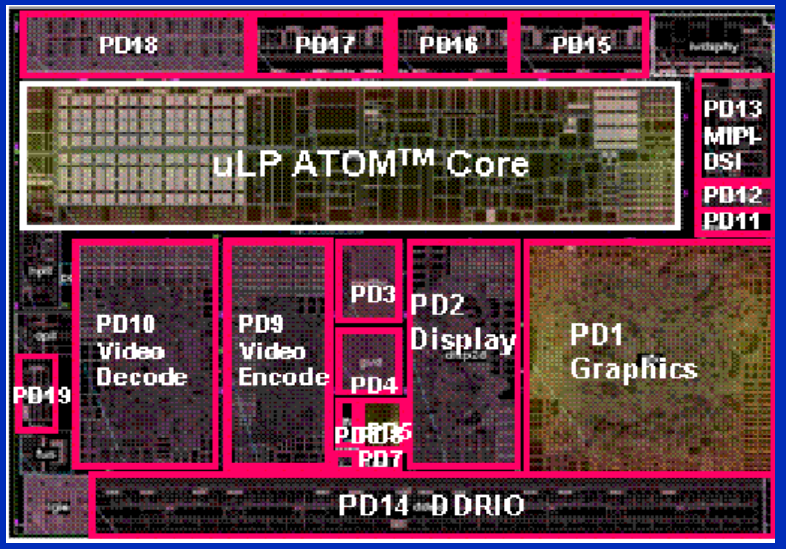
- Non-monotonic response
- Typically under-damped
- Relatively high peak-to-peak noise
- High sensitivity to design variables
- Careful analysis is required

Power Gated 3D ICs

- An effective method to reduce leakage power consumption
- Total power consumption = dynamic power + leakage power



* Niagra 2 (2008)



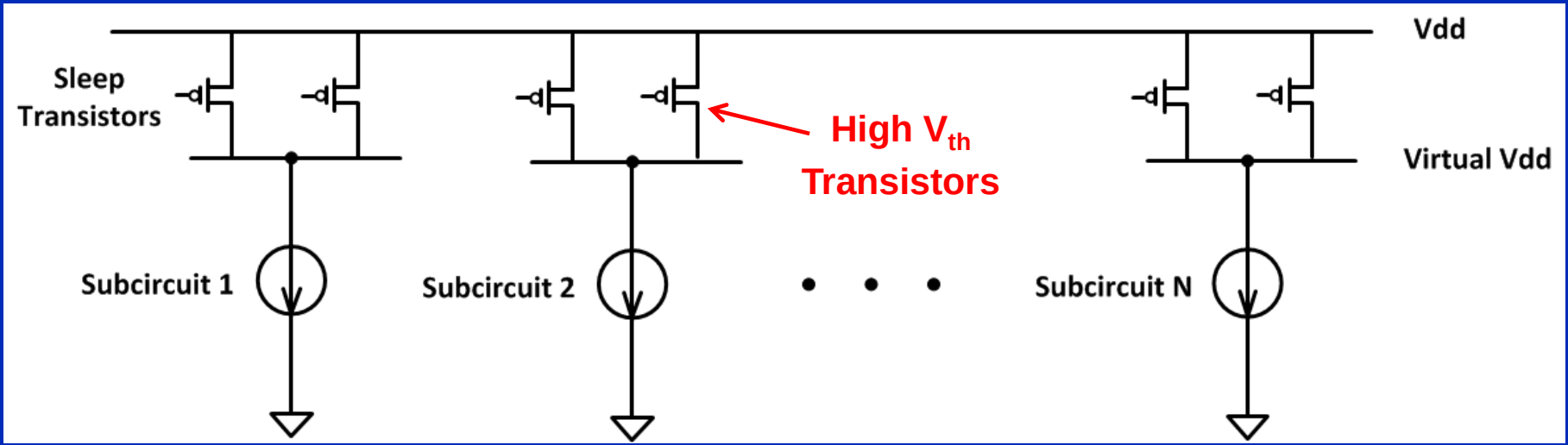
Intel Atom Processor

Power Gating: turn off the inactive blocks to save leakage

* U. Nawathe *et al.*, "Implementation of an 8-core, 64-thread, power-efficient SPARC server on a chip," JSSC, vol. 43, Jan. 2008

Power Gating: Sleep Transistors

- Sleep transistors are inserted along the power delivery path



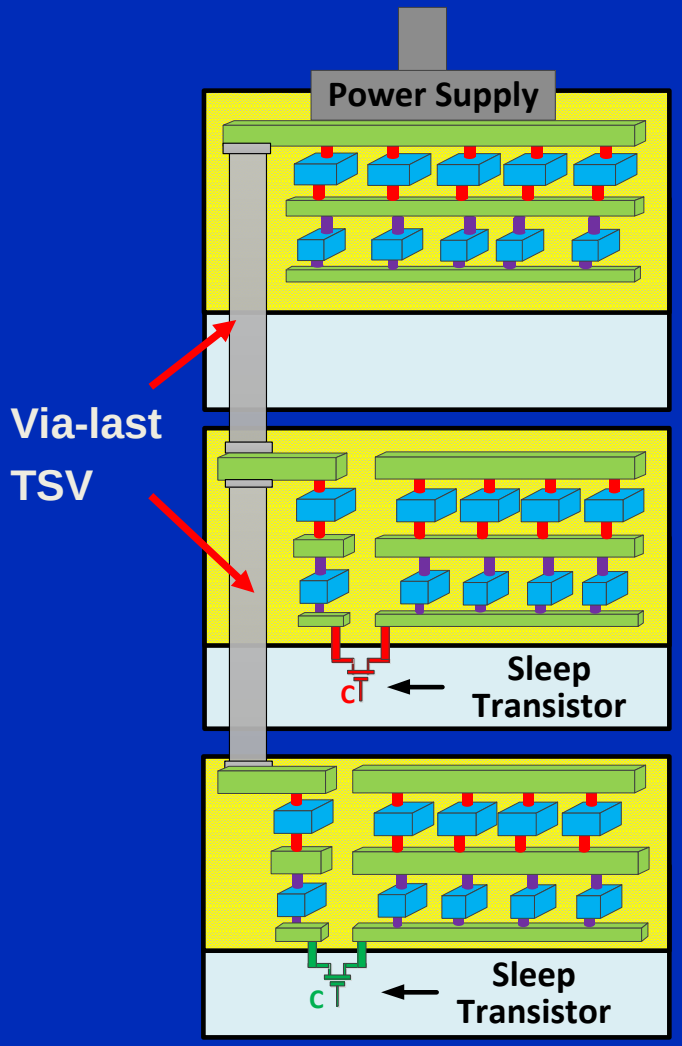
- Sleep transistors also consume significant area
  - More than 1 meter overall width

* R. Jotwani *et al.*, "An x86-64 Core in 32 nm SOI CMOS," JSSC, vol. 46, Jan. 2011

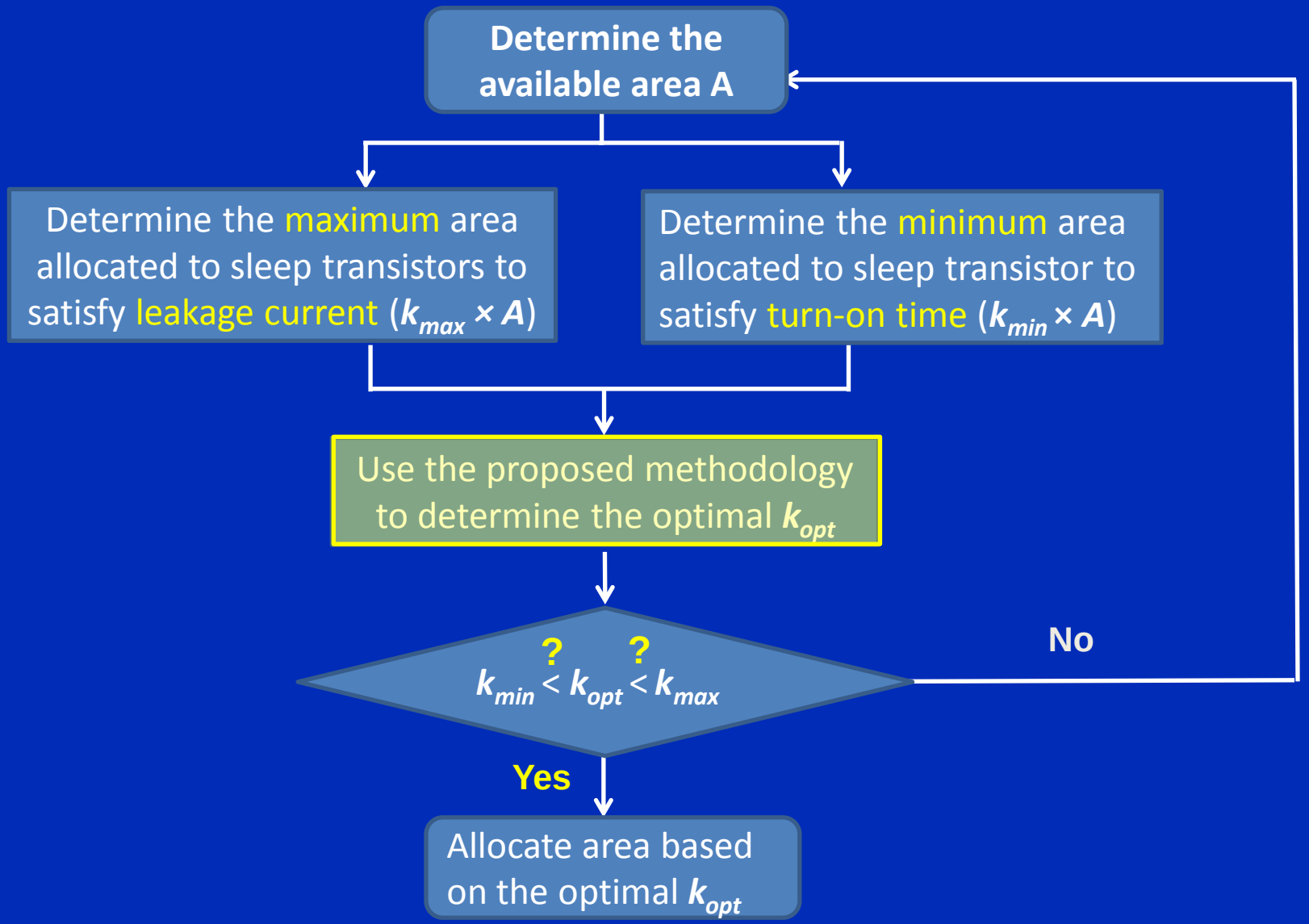
Allocate Area between TSVs and Sleep Transistors

- Area contention
- Both affect power integrity
- Minimize power supply noise

  Subject to:
  - Leakage power
  - Turn on time



Proposed Design Flow



Closed-Form Expressions for Optimum *k*

- **Effective resistance of TSVs**

$$R_{\mathrm{TSV}}^{\mathrm{eff}} = \frac{4\rho h_{\mathrm{TSV}}}{\pi d^2 N_{\mathrm{TSV}}} = \frac{\rho h_{\mathrm{TSV}} \alpha}{(1-k)A}$$

- **Effective resistance of sleep transistors**

$$R_{\mathrm{st}}^{\mathrm{eff}} \approx \frac{L^2 \beta}{\mu C_{ox}(V_{gs}^{st} - V_{th})} \times \frac{1}{kA}$$

- **Optimization objective**

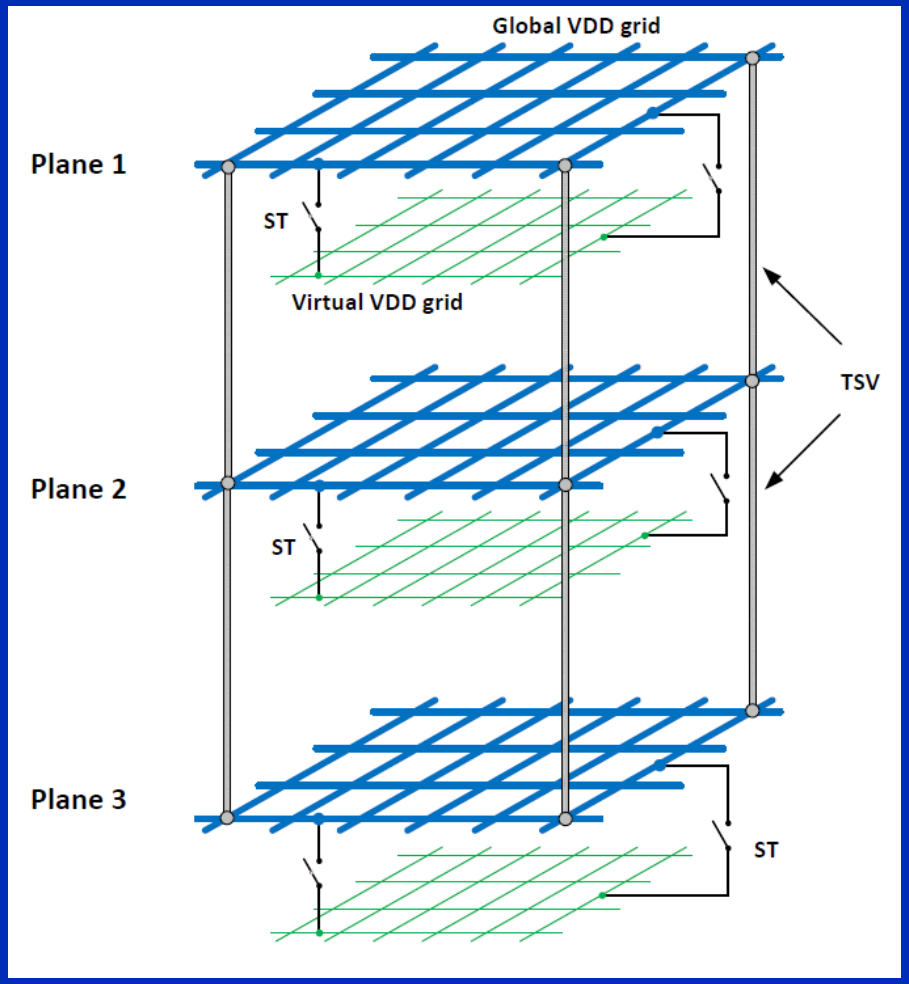
$$Z_{worst} \approx \mu(R_{\mathrm{PDN}} + R_{TSV} + R_{ST}) + \frac{\nu L_{\mathrm{PDN}}}{(R_{\mathrm{PDN}} + R_{TSV} + R_{ST})C_{decap}}$$

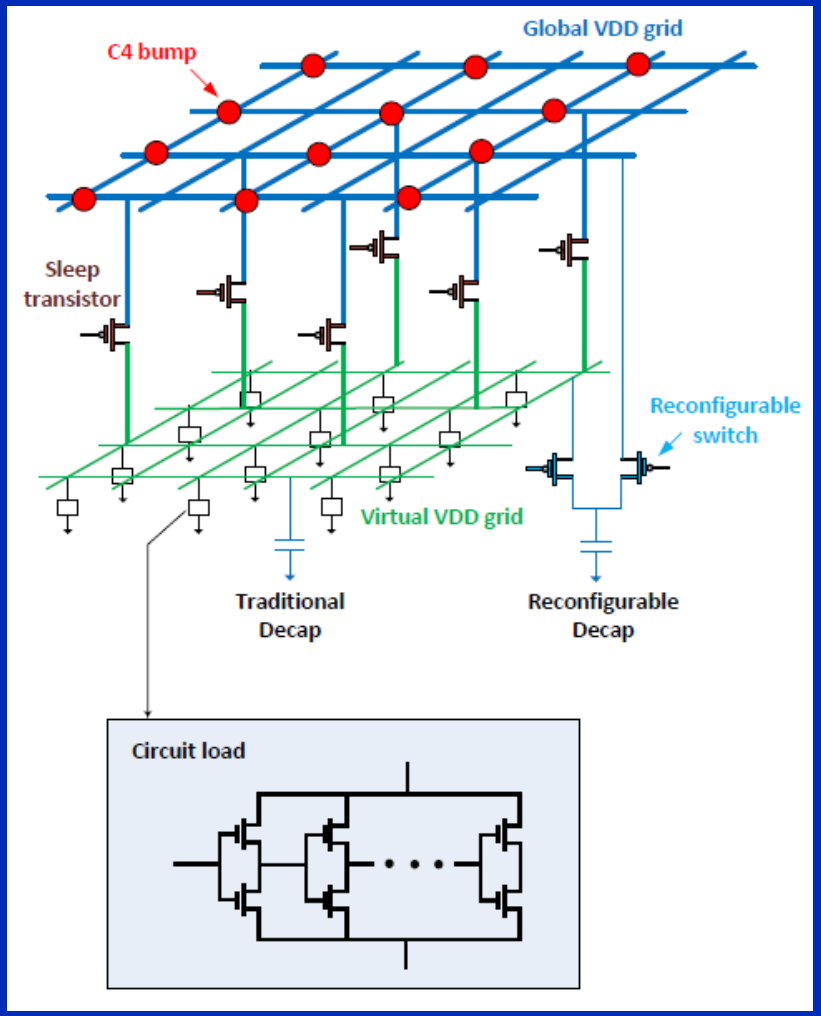
- **Optimum *k***

$$k_{optimal1,2} = \frac{(R_{optimal}A + T_1 - T_2) \pm \sqrt{(R_{optimal}A + T_1 - T_2)^2 - 4R_{optimal} \cdot AT_1}}{2R_{optimal} \cdot A}$$

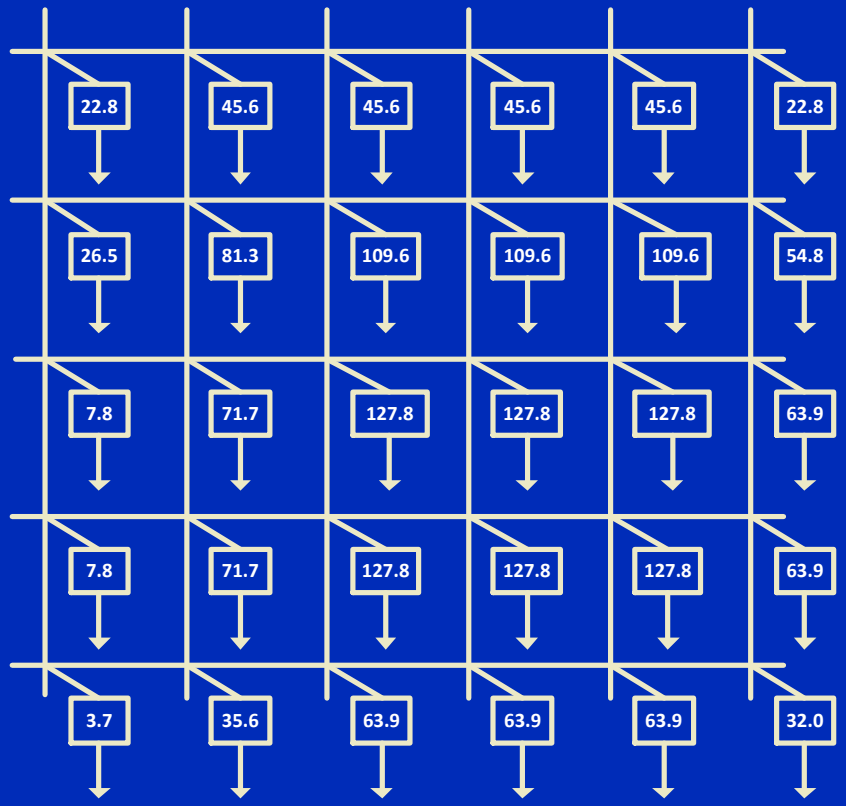
* H. Wang and E. Salman, *IEEE International Symposium on Quality Electronic Design*, March 2015, best paper nomination

Comprehensive Simulation Setup

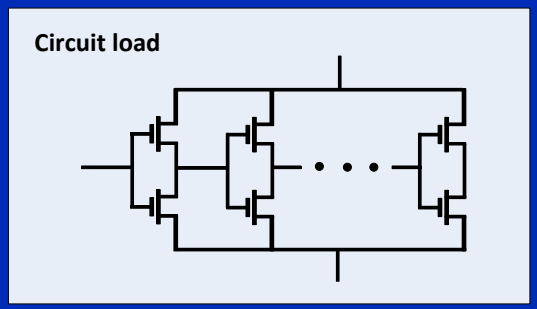




Distributed Circuit Loads



(Unit of peak current: mA)

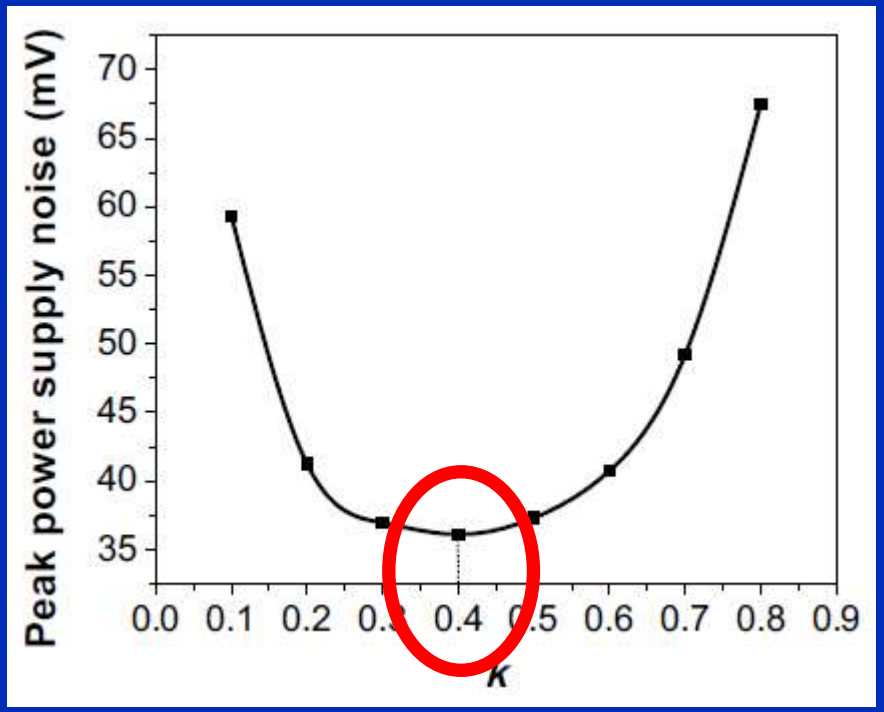


Power density matches OpenSPARC T2 Core: 40 W/cm^2

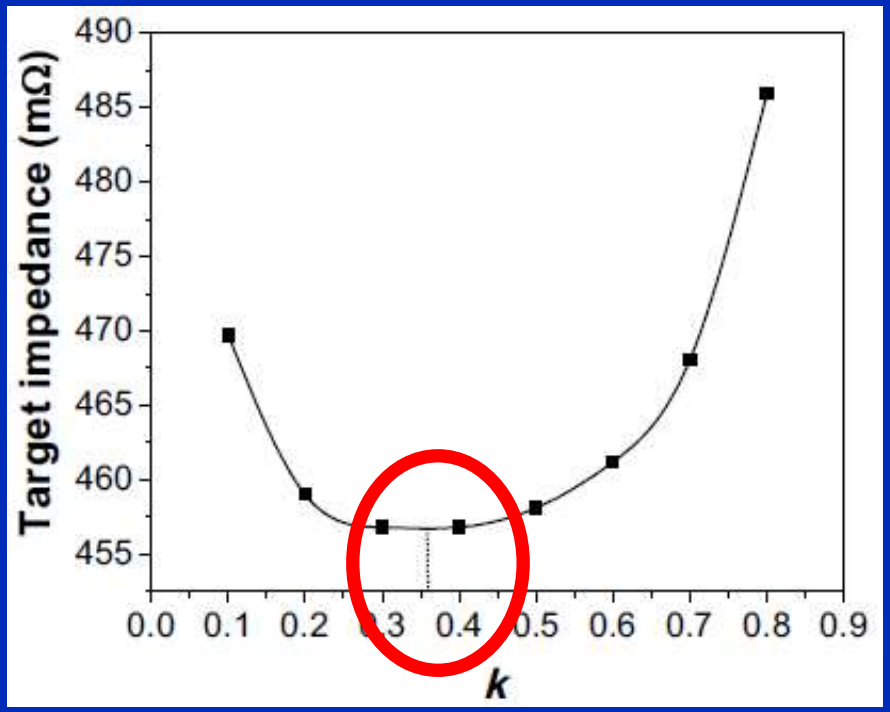
* H. Wei *et al.*, "Cooling 3D Integrated Circuits using Power Delivery Networks," *IEEE Int. Electron Devices Meeting*, 2011

Results

From simulation



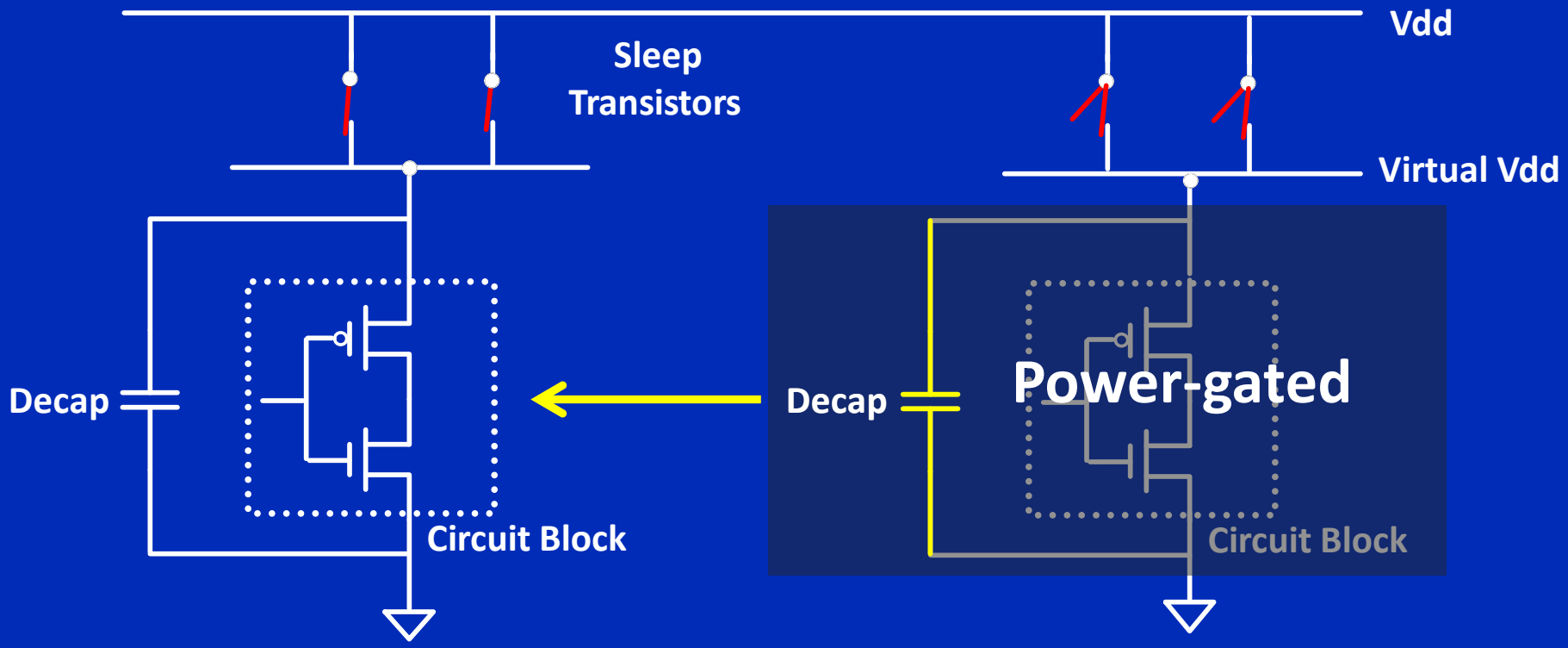
Closed-form expression



Error < 4%

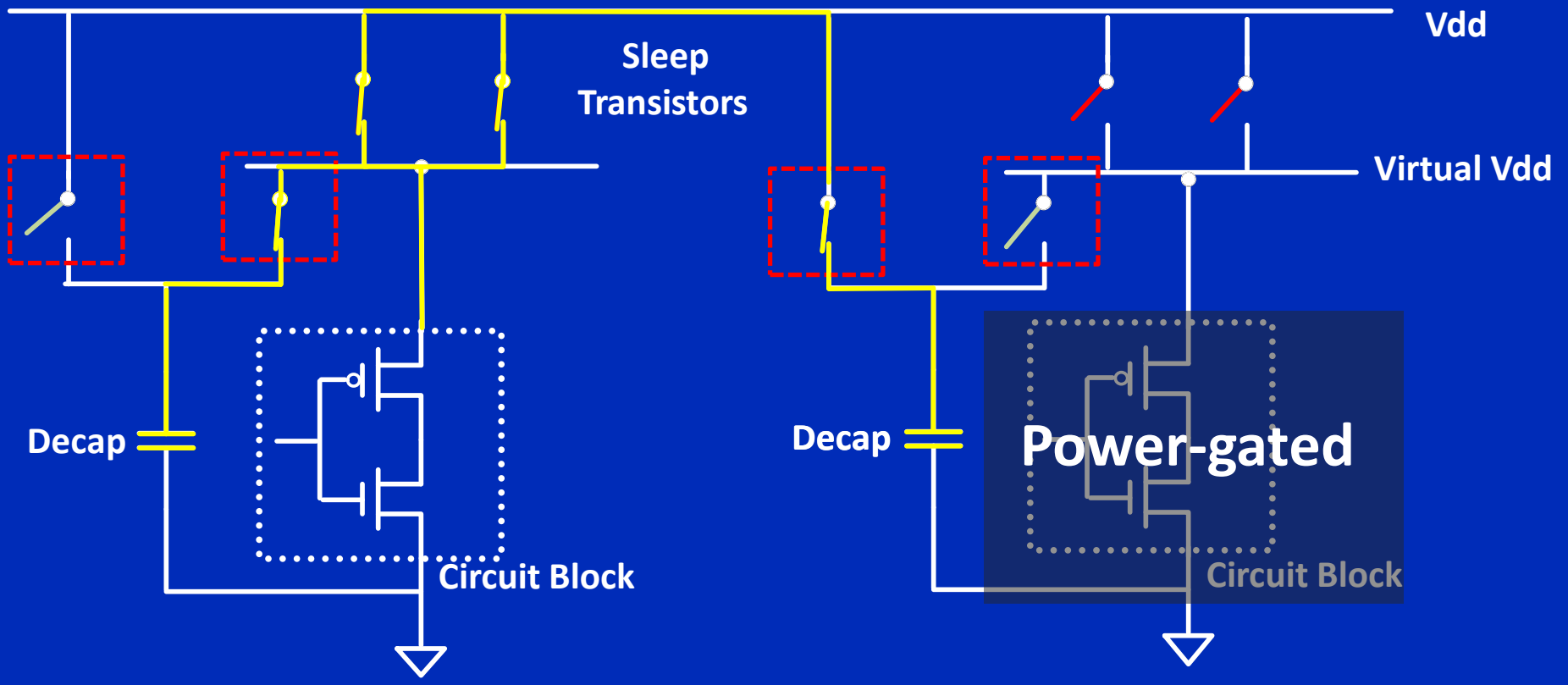
Noise reduction: up to 42%

Problem: Utilization of a Decap



- Utilize decap for nearby blocks
- Not as effective in 2D ICs: large impedance
- New opportunity in TSV-based 3D ICs

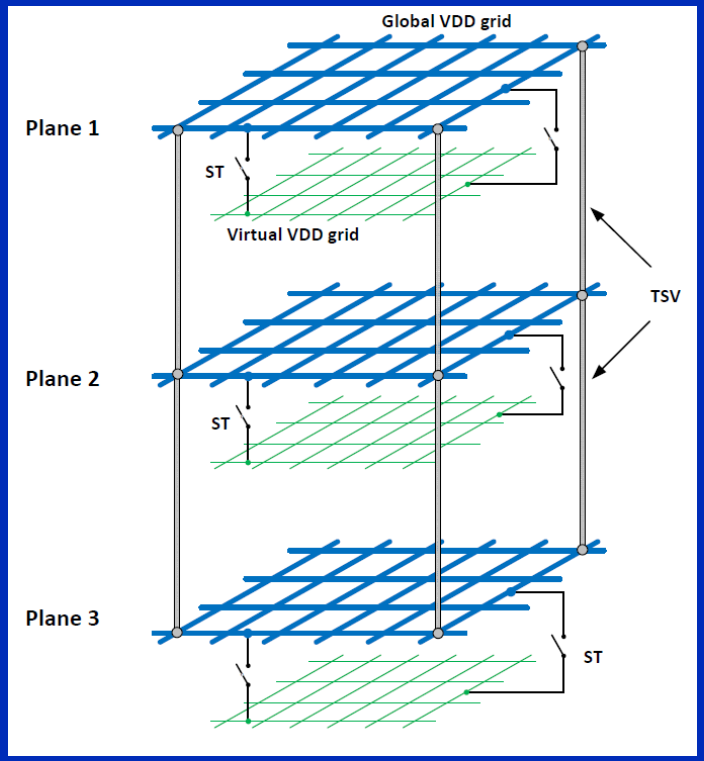
Proposed Reconfigurable Topology



- Two reconfigurable switches are added:
  - When the circuit block is ON, connect decap to virtual Vdd
  - When the circuit block is OFF, connect decap to global Vdd

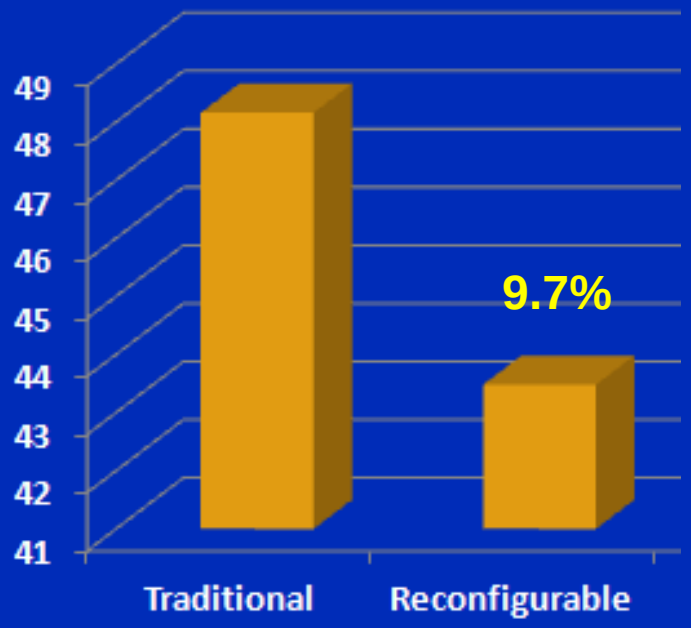
* H. Wang and E. Salman, *IEEE Transactions on VLSI Systems* (in press).

Power Gating Scenarios

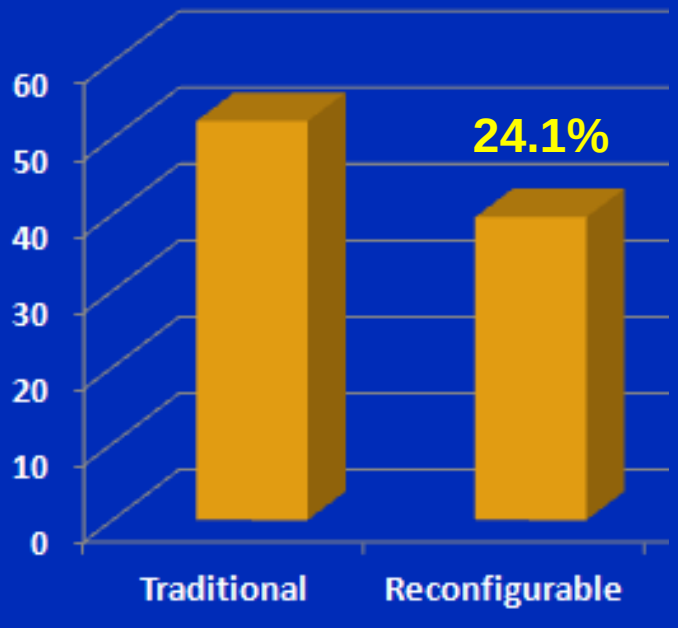


	Top Plane	Middle Plane	Bottom Plane
Scenario 2	ON	OFF	ON
Scenario 3	OFF	OFF	ON

Simulation Results – Peak Power Supply Noise



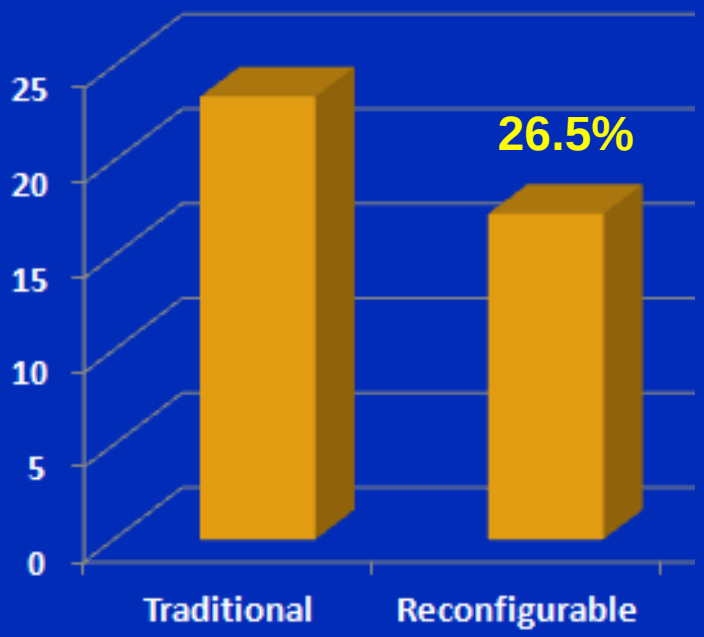
Scenario 2



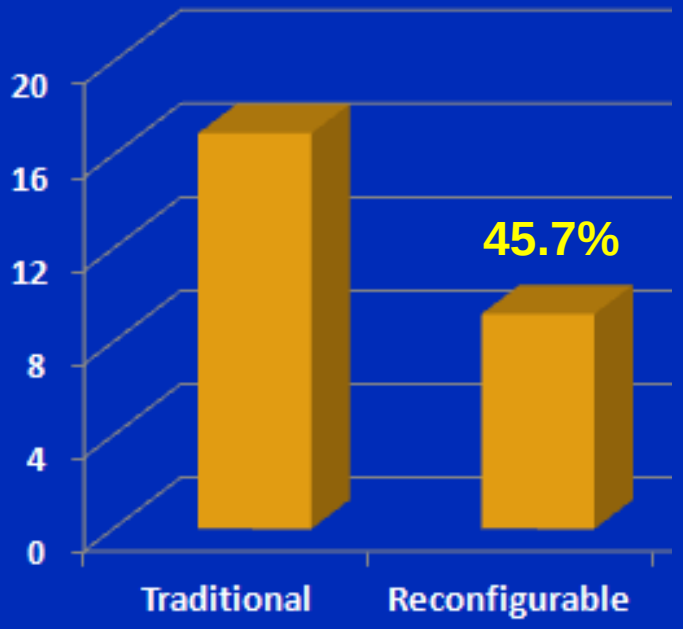
Scenario 3

* H. Wang and E. Salman, *IEEE Transactions on VLSI Systems* (in press).

Simulation Results – RMS Power Supply Noise

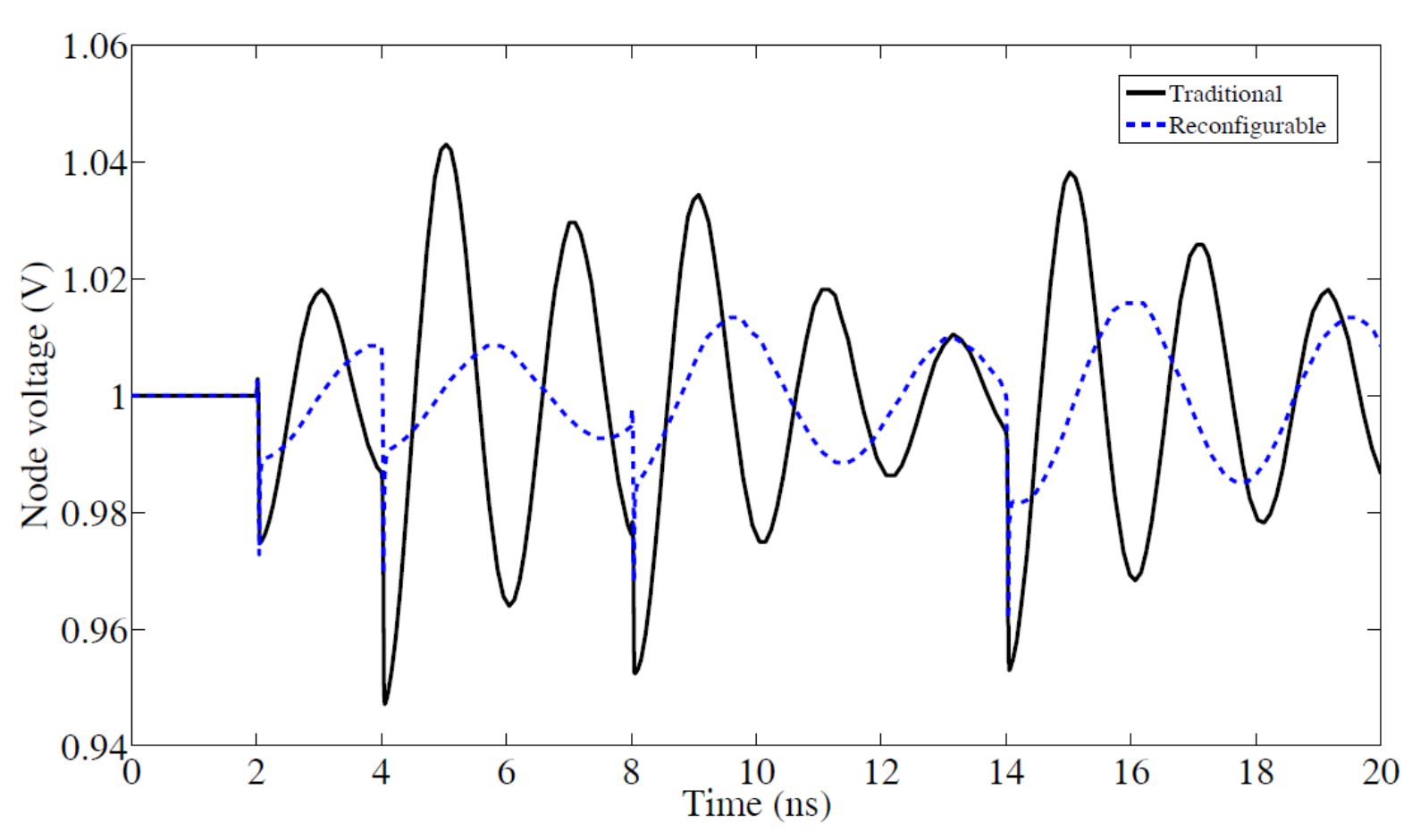


Scenario 2



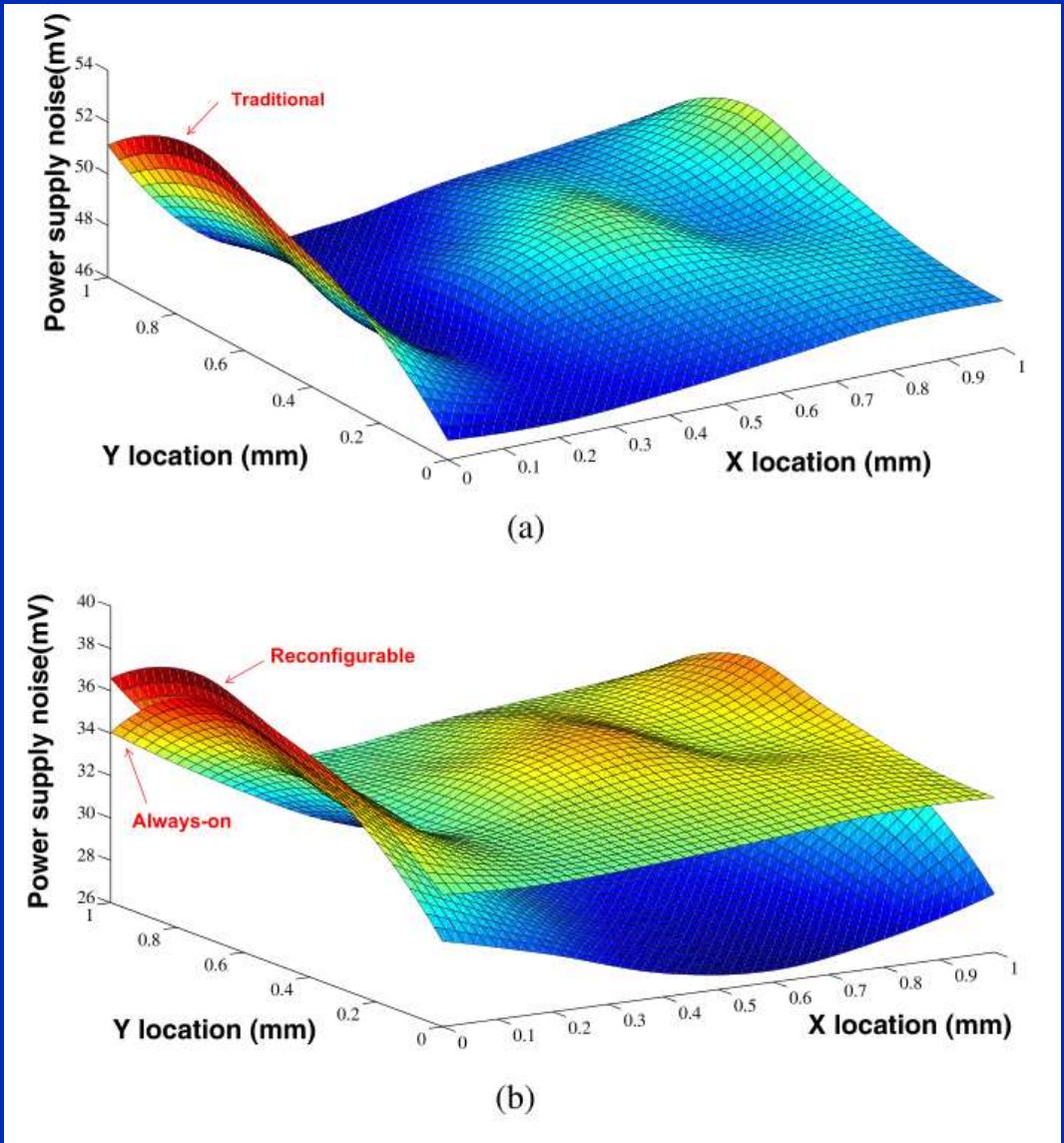
Scenario 3

Temporal Power Supply Noise Waveform



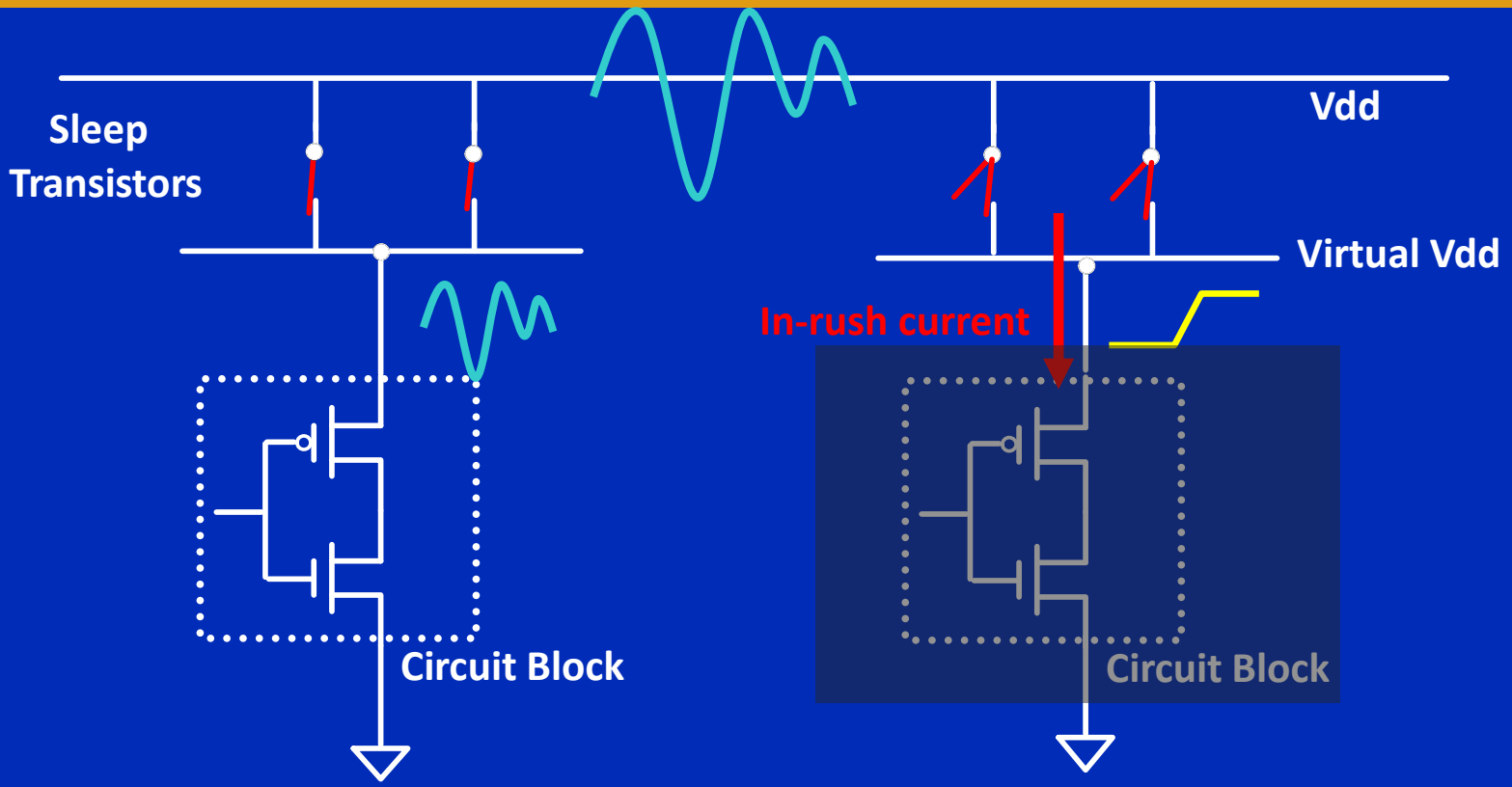
Transient power noise (Scenario 3)

Spatial Power Supply Noise Distribution



Average reduction: 23.1%

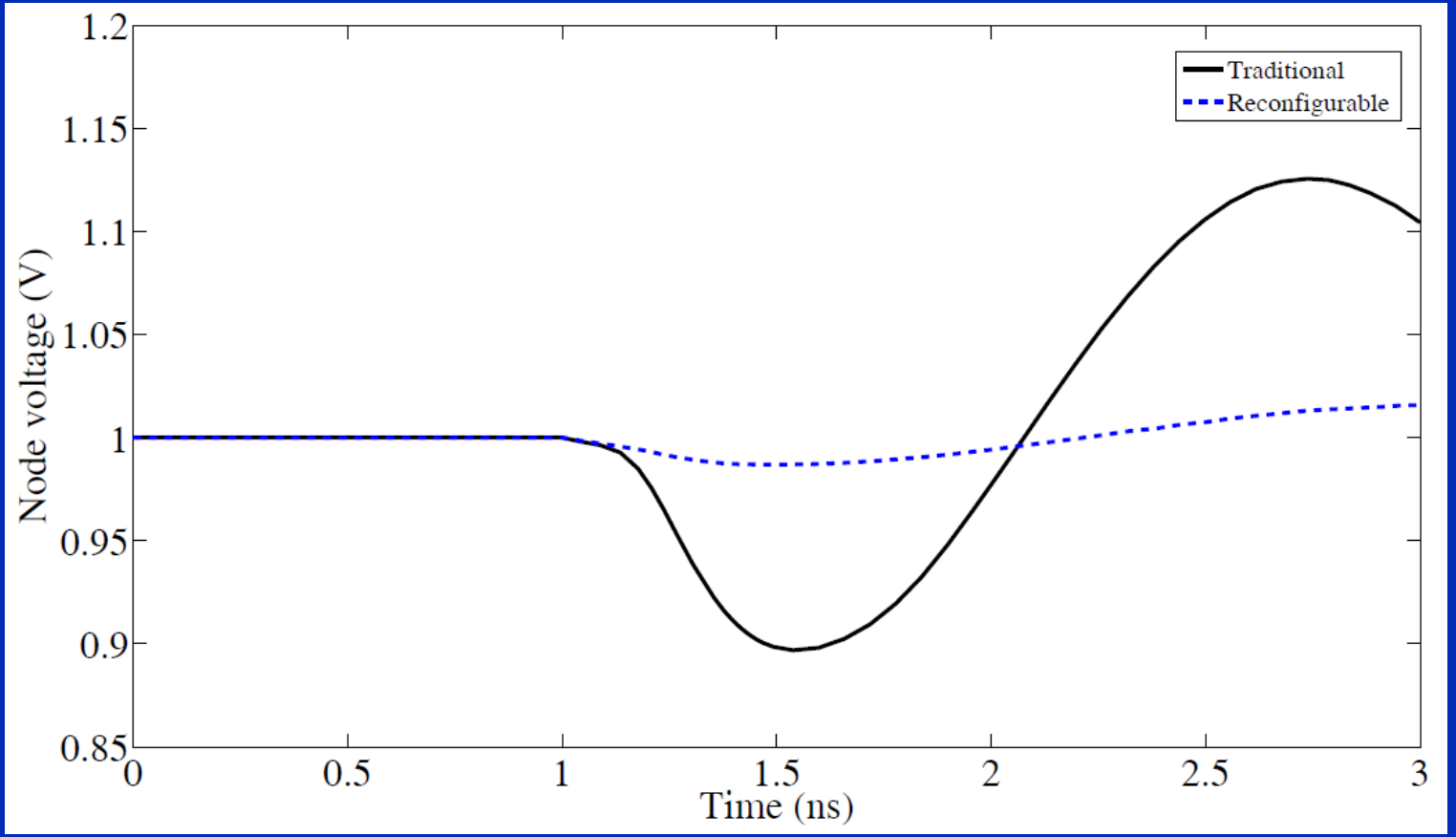
Simulation Results – Power Gating Noise



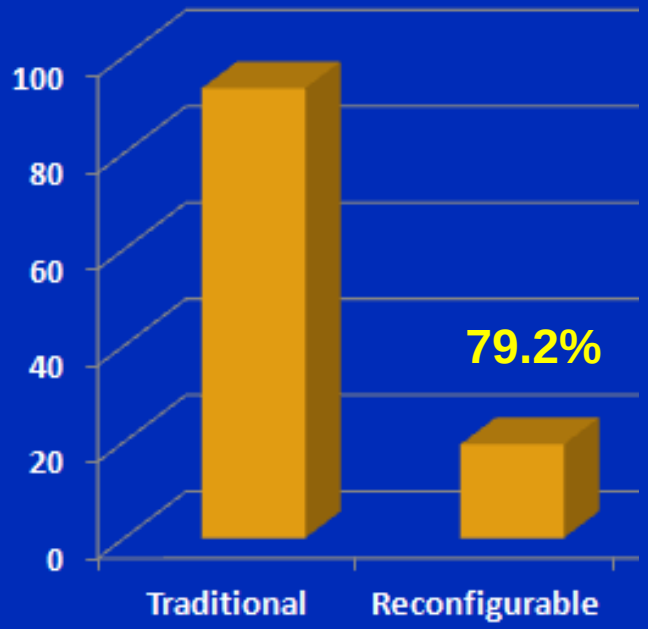
	Top Plane	Middle Plane	Bottom Plane
Scenario 2	ON	OFF → ON	ON
Scenario 3	OFF	OFF → ON	ON

Temporal Power Gating Noise Waveform

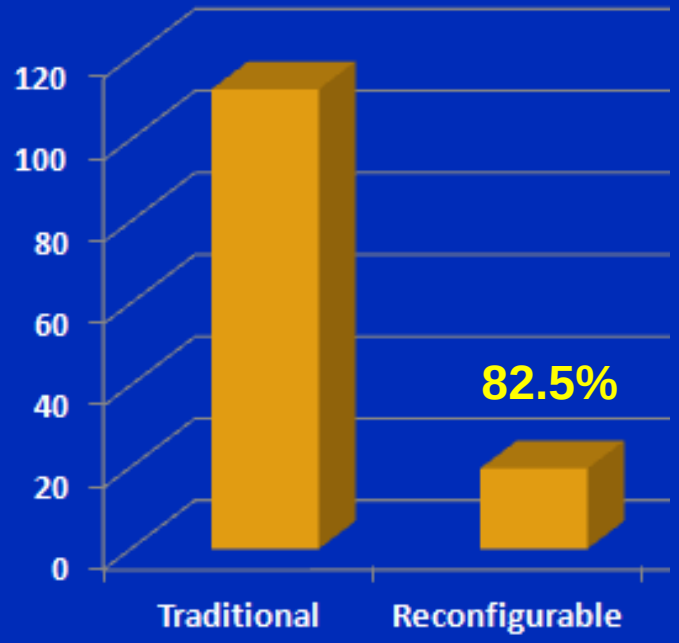
Sleep state → active state at 1 ns



Simulation Results – Power Gating Noise



Scenario 2



Scenario 3

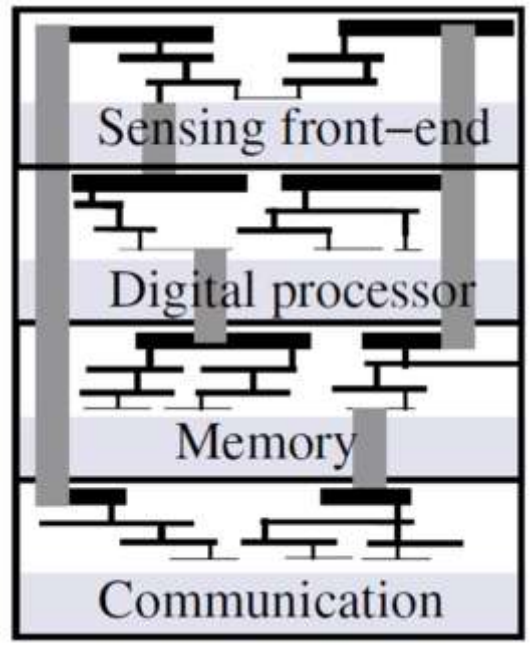
Area and Power Overhead

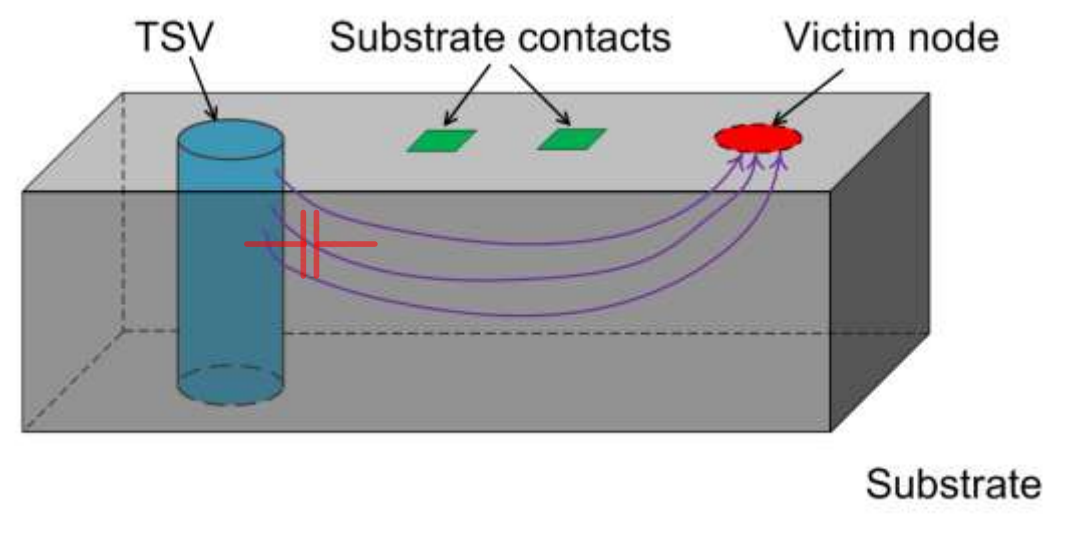
- Physical area increases only by 1.93%

Power consumption (mW)	Traditional	Reconfigurable	Increase (%)
Scenario 1	26.45	26.81	1.36
Scenario 2	17.57	18.07	3.41
Scenario 3	8.89	9.41	5.85

- Power overhead can be further reduced by utulizing metal-insulator-metal (MIM) capacitors

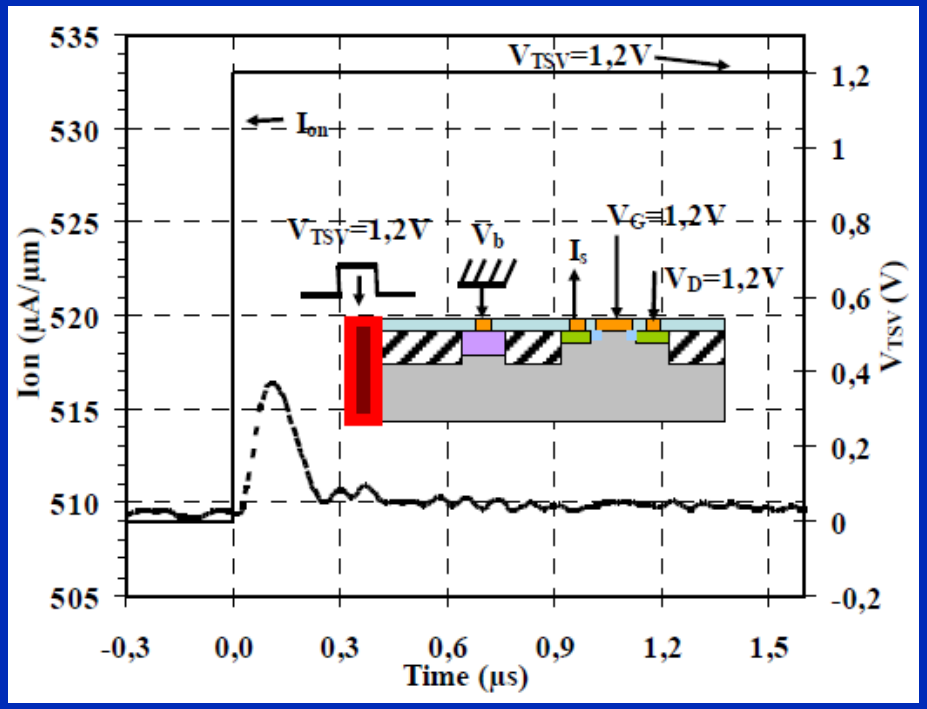
TSV Noise Coupling

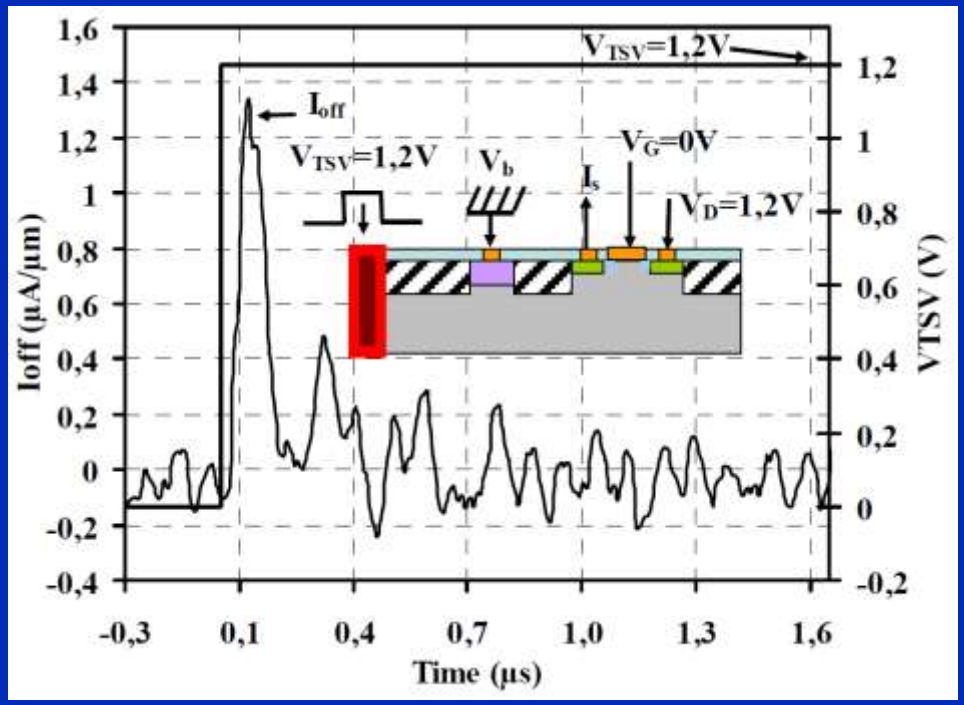




- **Noise couples into the substrate due to both oxide and MOS capacitance**
- **Aggressive signals such as clock networks**
- **Affects the operation of a transistor (both on and off)**
  - **Memory circuits**
  - **Analog devices in heterogeneous 3D integration**

Effect of TSV Noise on Devices

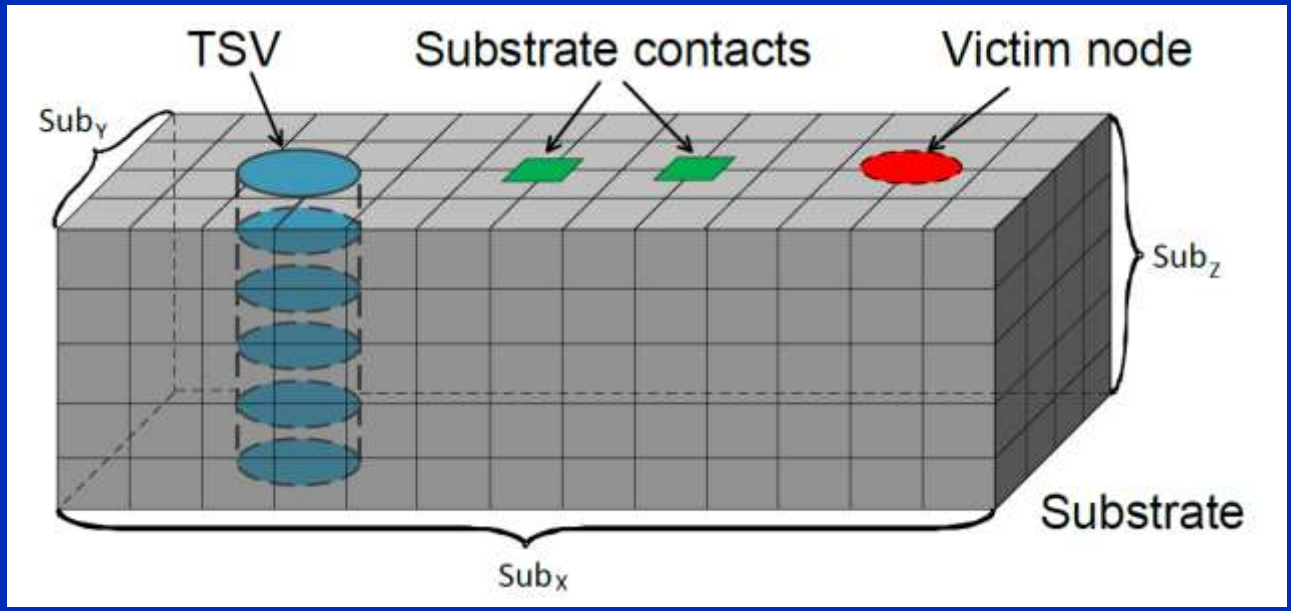




H. Chaabouni, *et al.* "Investigation on TSV impact on 65nm CMOS devices and circuits," *IEEE International Electron Devices Meeting,* 2010.

Modeling TSV Noise Coupling

- 3D field solver: HFSS → not possible for practical circuits
- Discretized model based on transmission line matrix method

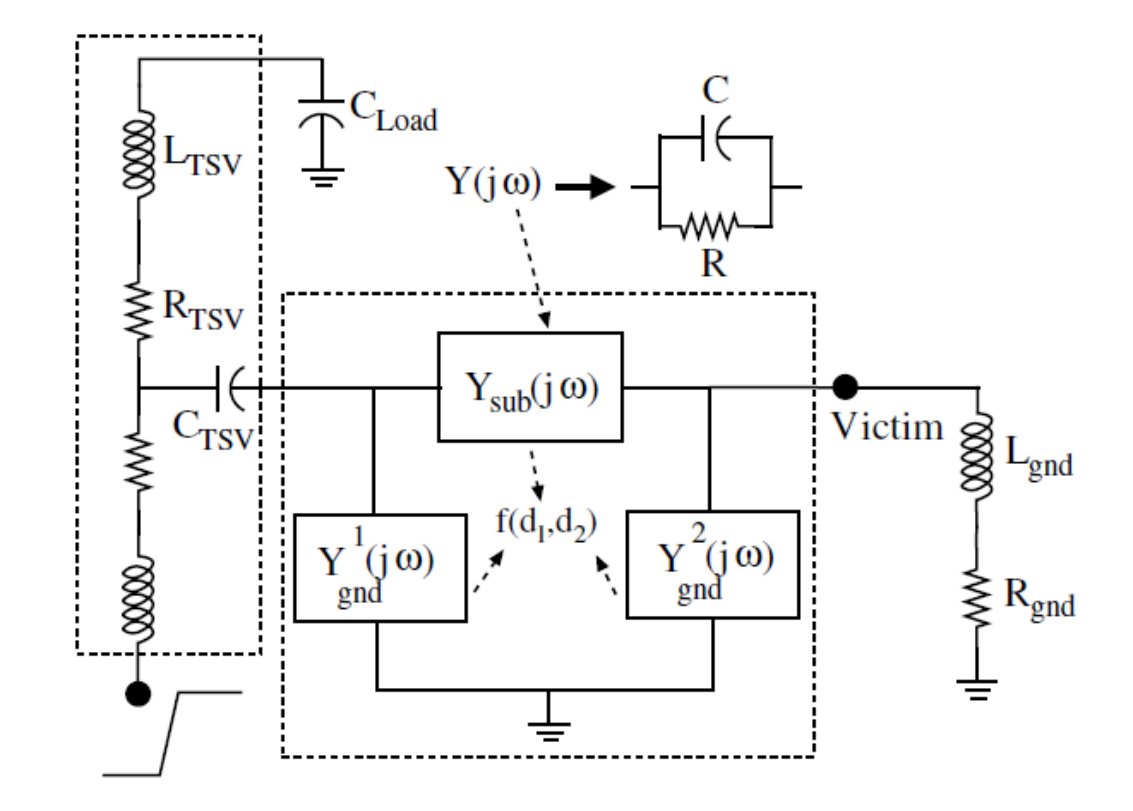


Accurate, but…computationally prohibitive!

- Fast evaluation is difficult
- Early stages of TSV floorplanning
- Substrate contact locations

Compact π Model

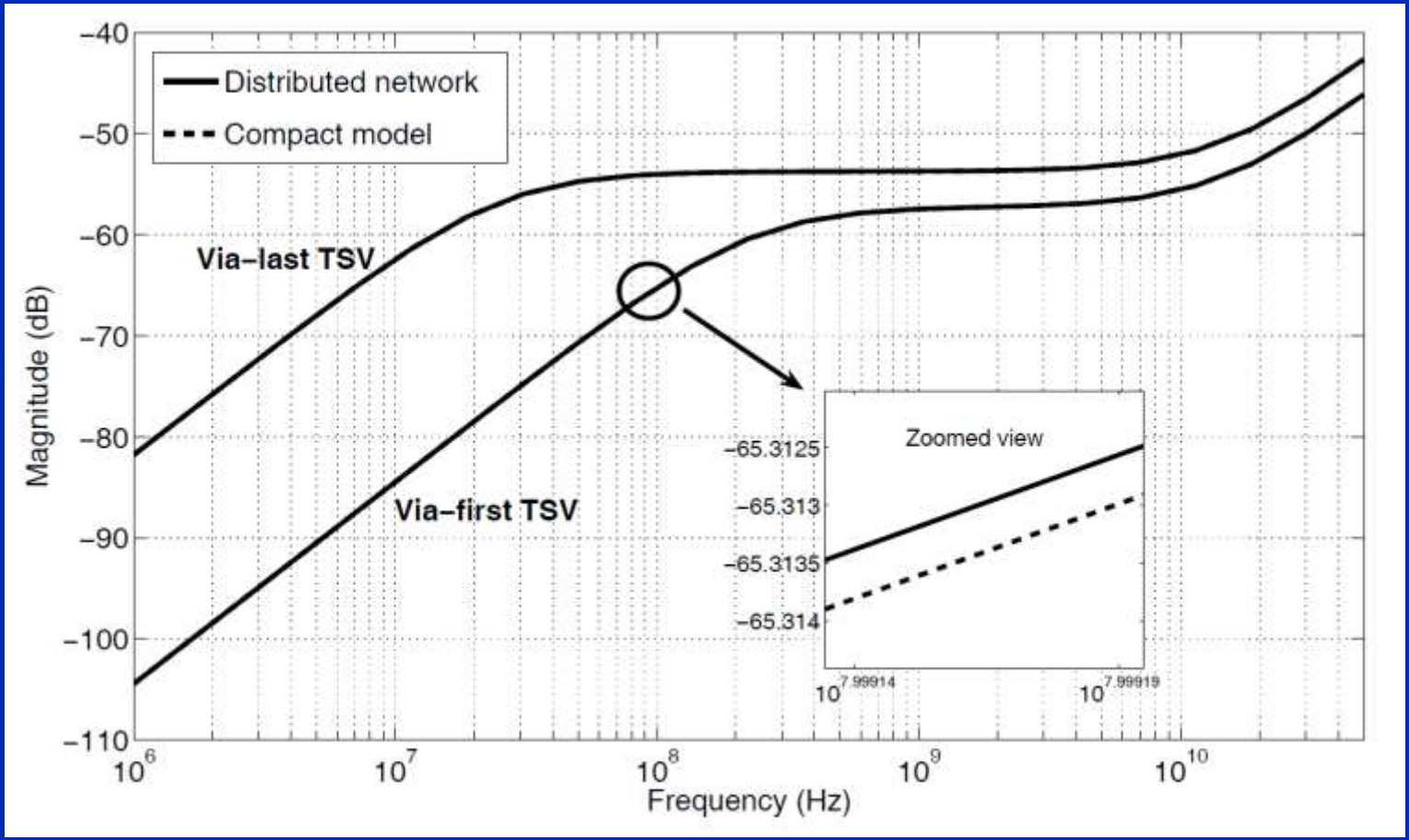
- **Single TSV cell and an *equivalent π network*.**



- **Approach**
  1. **AC analysis of the distributed mesh to obtain $Y_{11}(j\omega)$, $Y_{12}(j\omega)$, $Y_{21}(j\omega)$, $Y_{22}(j\omega)$**
  2. **Obtain the *R* and *C*s within the π network to match the four impedances**
  3. **Single *R* and *C* value until 100 GHz.**

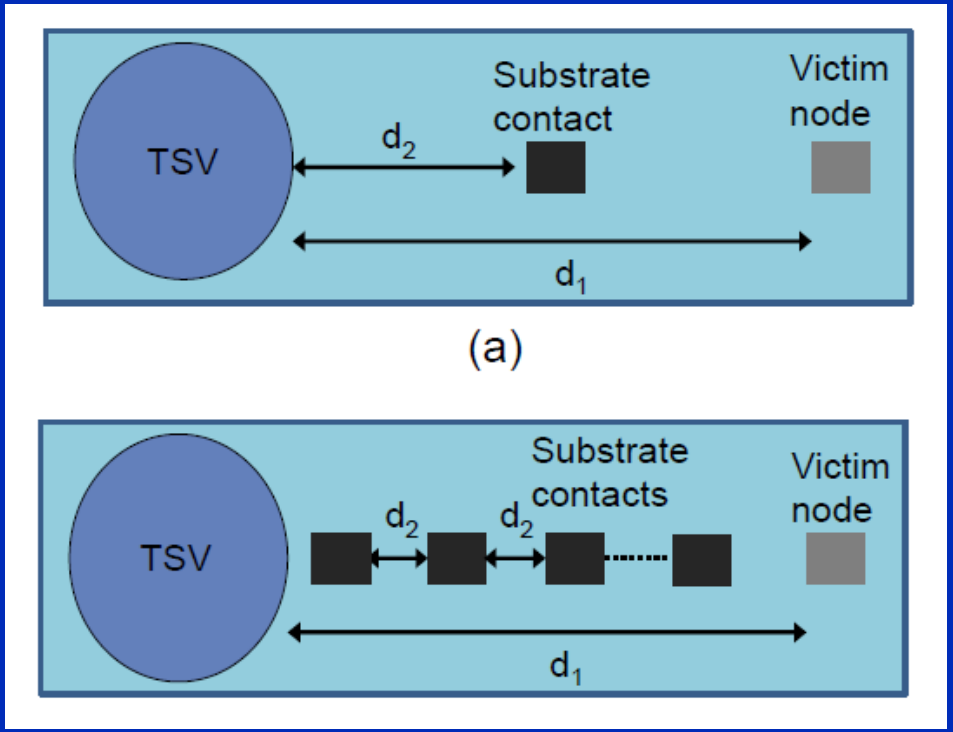
Validation of the Compact π Model

- The transfer function of the compact model is compared with the transfer function of the distributed mesh

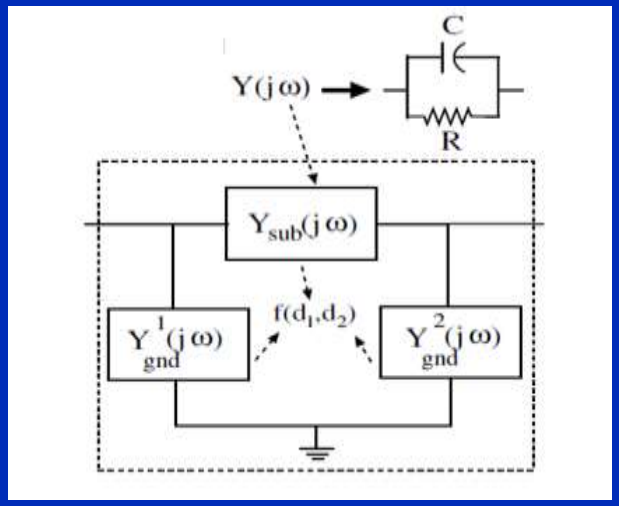


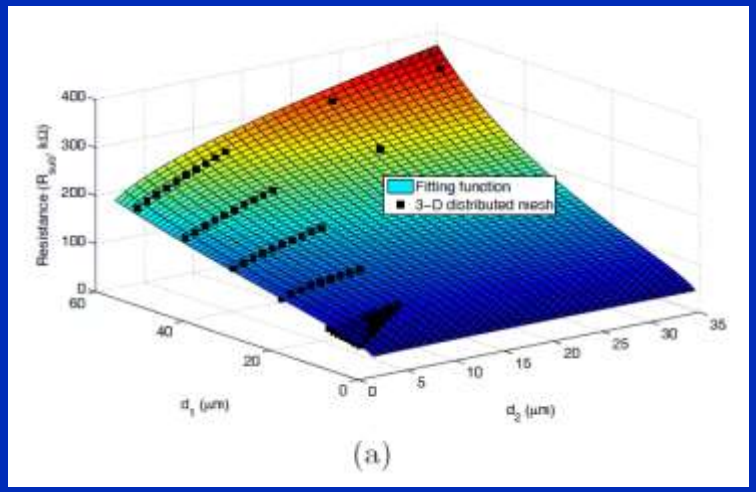
Characterizing TSV-to-Substrate Coupling

- TSV noise is affected by several design parameters
  - Distance between TSV and victim node (d_1)
  - Number and location of substrate contacts (d_2)



Closed-Form Expression for Each Admittance





Resistance R_{sub} of the $Y_{sub}(j\omega)$

- Analyze the distributed mesh to obtain the impedances (**Dots**)
- Approximate the surface with a logarithmic function using 3D least square regression analysis (**Surface**)

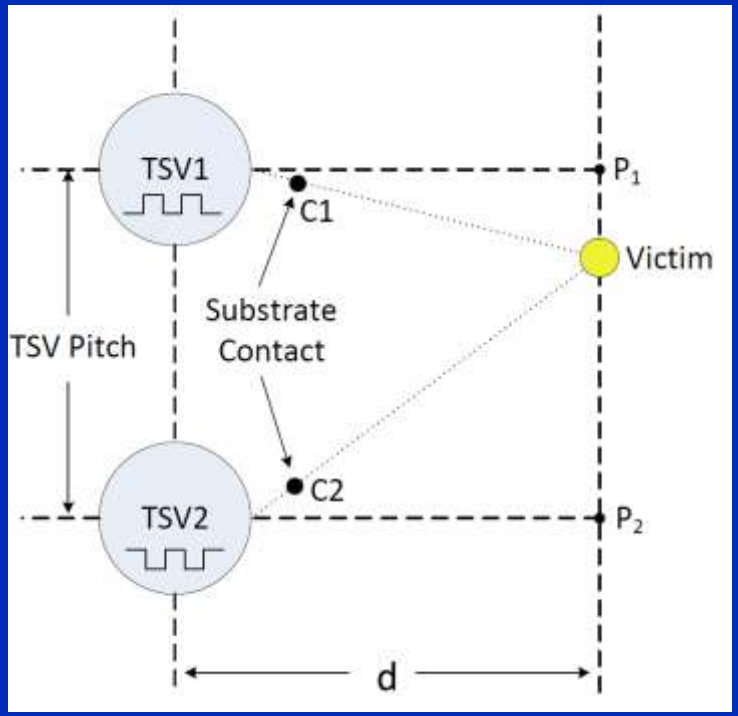
$$F(d_1, d_2) = A + Bd_1 + Cd_2 + D \ln d_2 + E \ln d_1,$$

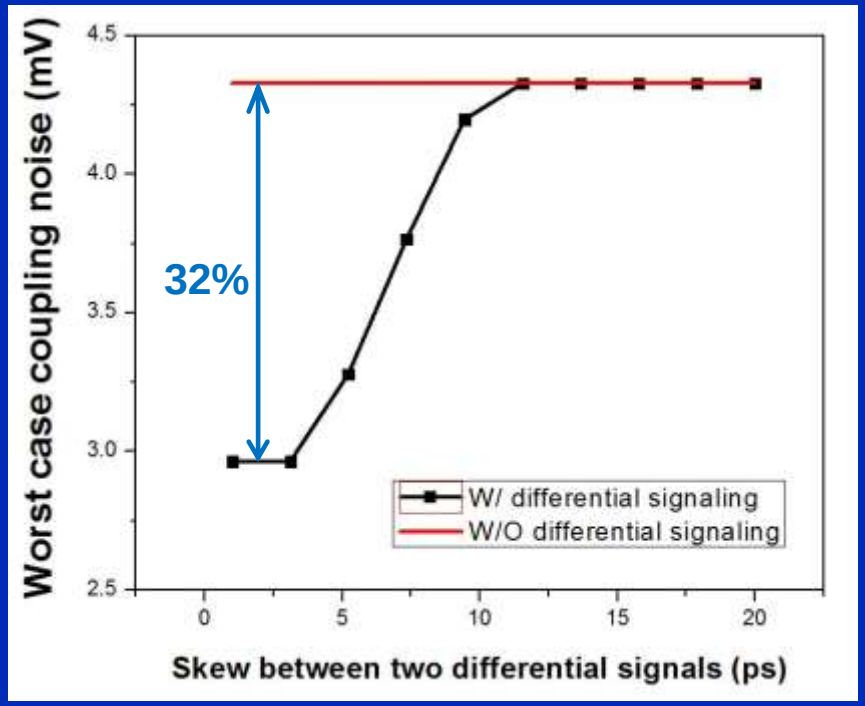
Fitting Coefficients and Accuracy

Cases	Admittances	Fitting coefficients A	B	C	D	E	Average error (%)
Case 1	$R_{sub} = 1000/F$ (kΩ)	27.09	0	0	-0.98	-5.11	6.6
	$C_{sub} = F$ (aF)	326.7	0.41	0.48	-17.26	-67.55	2.8
	$R^1_{gnd} = 1000/F$ (kΩ)	28.31	0	0	-8.14	1.98	1.9
	$C^1_{gnd} = F$ (aF)	301.3	-0.28	0.66	-96.94	30.09	1.6
	$R^2_{gnd} = F$ (kΩ)	45.91	2.30	3.08	-218.3	154.9	9.6
	$C^2_{gnd} = 1000/F$ (aF)	8.05	0.28	0.29	-20.39	12.49	10.4
Case 2	$R_{sub} = 1000/F$ (kΩ)	29.18	0.28	0.38	1.34	-11.78	8.3
	$C_{sub} = F$ (aF)	317.1	2.99	4.24	14.2	-127.6	10.8
	$R^1_{gnd} = 1000/F$ (kΩ)	69.24	-0.046	1.97	-35.05	4.73	0.7
	$C^1_{gnd} = F$ (aF)	758.5	-0.49	21.13	-380.8	51.33	0.7
	$R^2_{gnd} = 1000/F$ (kΩ)	9.50	-0.19	-0.99	-1.95	9.31	1.6
	$C^2_{gnd} = F$ (aF)	106.4	-2.05	-10.99	-20.83	100.7	1.6
Case 3	$R_{sub} = 1000/F$ (kΩ)	27.35	-0.082	0.036	-2.11	-1.12	2.4
	$C_{sub} = F$ (aF)	296.6	-0.89	0.83	-20.78	-13.12	1.9
	$R^1_{gnd} = 1000/F$ (kΩ)	36.16	0.028	0.39	-10.16	1.18	2.4
	$C^1_{gnd} = F$ (aF)	235.6	-1.18	-2.16	-61.86	51.91	6.9
	$R^2_{gnd} = 1000/F$ (kΩ)	11.57	0.11	-0.19	4.43	-5.86	11.6
	$C^2_{gnd} = F$ (aF)	129.1	1.18	-2.22	49.1	-65.23	10.9
Case 4	$R_{sub} = 1000/F$ (kΩ)	24.41	0.13	0.42	1.69	-8.36	8.5
	$C_{sub} = F$ (aF)	265.3	1.40	4.67	17.88	-91.2	7.2
	$R^1_{gnd} = 1000/F$ (kΩ)	117.6	-0.03	0.40	-35.66	3.64	0.3
	$C^1_{gnd} = F$ (aF)	998	0.03	-68.78	37.31	32.11	2.9
	$R^2_{gnd} = 1000/F$ (kΩ)	14.56	-0.01	-0.73	-3.49	5.93	2.4
	$C^2_{gnd} = F$ (aF)	162	-0.13	-8.17	-37.74	64.26	2.5

- **Average error is 4.8%**

Design Guidelines – Differential TSV Signaling





* H. Wang, M. Asgari, and E. Salman, *Integration, the VLSI Journal*, June 2014.

Conclusions

- Among various “emerging” technologies, 3D integration seems to be the most viable in the near-future
- Research is needed, but no fundamental limitations exist
- Opportunities are beyond high performance computing
  - Sensing and actuating
    - Mobile electronics
    - Healthcare
    - Environmental control…
- We have demonstrated several design methodologies to enhance power and signal integrity in 3D ICs

Publications on 3D ICs

- **Book Chapters**
  - E. Salman, "Power and Signal Integrity Challenges in 3D Systems-on-Chip," *Physical Design for 3D Integrated Circuits*, A. Todri-Sanial and C. S. Tan (Eds.), CRC Press, in press
  - M. Stanacevic, Y. Lin, and E. Salman, "Analysis and Design of 3D Potentiostat for Deep Brain Implantable Devices," *Neural Computation, Neural Devices, and Neural Prosthesis*, pp. 261-287, Z. Yang (Ed.), Springer, 2014
- **Journal papers**
  - H. Wang and E. Salman, "Decoupling Capacitor Topologies for TSV-based 3D ICs with Power Gating," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, in press
  - H. Wang, M. H. Asgari, and E. Salman, "Compact Model to Efficiently Characterize TSV-to-Transistor Noise Coupling in 3D ICs," *Integration, the VLSI Journal*, June 2014
  - S. M. Satheesh and E. Salman, ``Power Distribution in TSV Based 3D Processor-Memory Stacks," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, December 2012
- **Conference papers**
  - S. Fang and E. Salman, "Low Swing TSV Signaling Using Novel Level Shifters with Single Supply Voltage," *Proc. of the IEEE International Symposium on Circuits and Systems*, May 2015
  - H. Wang and E. Salman, "Resource Allocation Methodology for Through-Silicon-Vias and Sleep Transistors in 3D ICs," *Proc. of the IEEE Int. Symp. on Quality Electronic Design*, March 2015
  - H. Wang and E. Salman, "Enhancing System-Wide Power Integrity in 3D ICs with Power Gating," *Proc. of the IEEE International Symposium on Quality Electronic Design*, March 2015
  - H. Wang, M. H. Asgari, and E. Salman, "Efficient Characterization of TSV-to-Transistor Noise Coupling in 3D ICs," Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI, pp. 71-76, May 2013.
  - S. M. Satheesh and E. Salman, "Effect of TSV Fabrication Technology on Power Distribution in 3D ICs," Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI, pp. 287-292, May 2013.
  - H. Wang and E. Salman, "Power Gating Topologies in TSV Based 3D Integrated Circuits," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI*, pp. 327-328, May 2013.
  - S. M. Satheesh and E. Salman, "Design Space Exploration for Robust Power Delivery in TSV Based 3D Systems-onChip," *Proceedings of the IEEE International System-on-Chip Conference*, pp. 307-311, September 2012.
  - E. Salman, M. H. Asgari, and M. Stanacevic, "Signal Integrity Analysis of a 2D and 3D Integrated Potentiostat for Neurotransmitter Sensing," *Proc. of the IEEE Biomedical Circuits and Systems Conference*, pp.17-20, November 2011.
  - E. Salman, "Noise Coupling Due to Through Silicon Vias (TSVs) in 3D Integrated Circuits," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 1411-1414, May 2011.