



A Flexible Volterra-Based Adaptive Digital Pre-Distortion Solution for Wideband RF Power Amplifier Linearization

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Abstract

This presentation discusses highlights of a paper published in August, September and October 2008 issues of *Microwaves & RF Magazine*



Base Stations/PA's



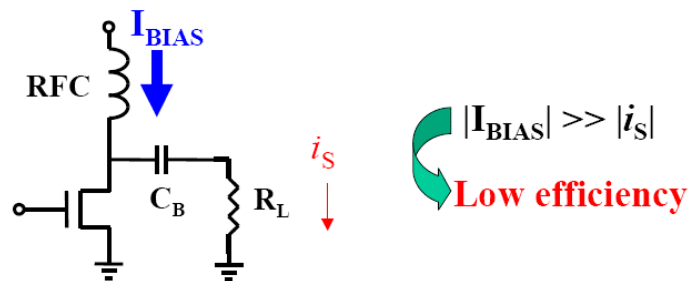


The Problem

The present 3G and other emerging air interfaces use non-constant envelope modulation schemes and are spectrally more efficient than their predecessors

Problem: This technique causes high PAR, necessitating higher PA back-off.

This leads to decrease in PA efficiency and increase in cooling and operational costs of a base-station.





How does DPD fix the problem?

Solution: Drive the PA harder to get more power

Added Problem: Signal distortion occurs

Ultimate Solution: Predict the type of distortion, pre-distort the signal in a reverse manner

Result: Distortion is cancelled out. This extends the linear region of the operation range and produces more output power at an efficiency approaching 40%. Now a smaller amplifier at higher efficiency can be used with DPD to achieve the desired output power

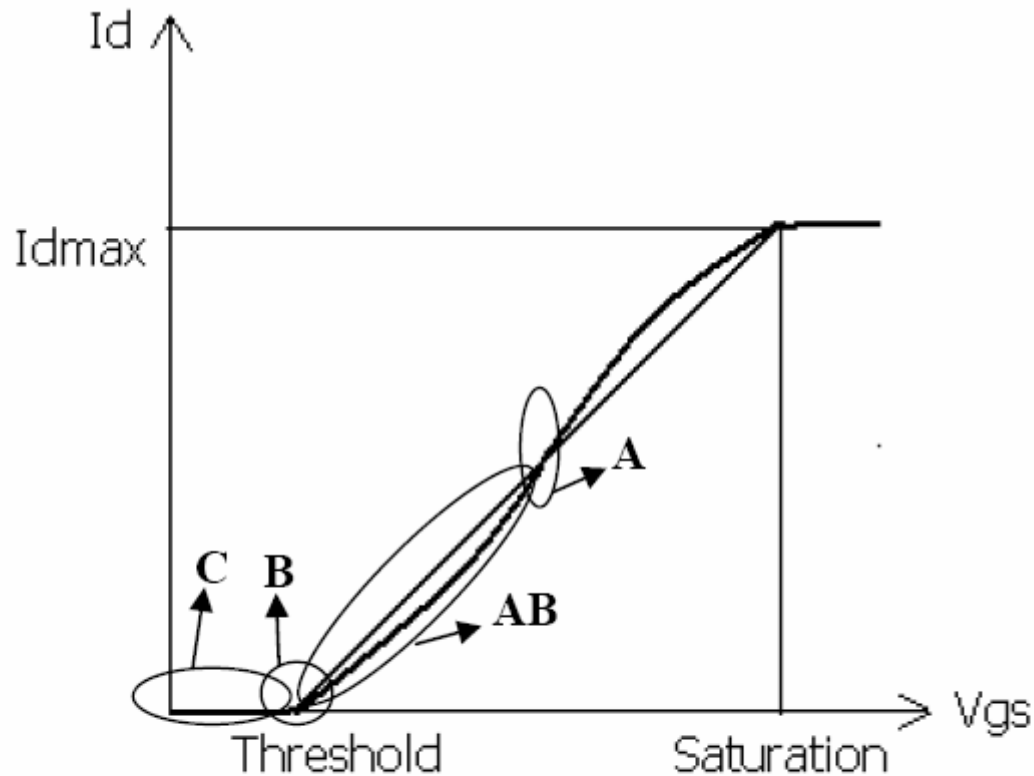


Introduction

- DPD (Digital Pre-Distortion) improves efficiency of PA's
- Most PA's are LDMOS class AB designs and rarely achieve 10% efficiency
- This inefficiency is inherent in the class AB design but also is a result of having to reduce the PA output to deal with signals that exhibit high PAR (Crest Factor) power and to prevent distortion that results in adjacent channel power leakage



Classes of PA's



Classes of operation of Power amplifier based on transfer characteristics



Typical PA improvement from this DPD solution

- Reduce PAR's (or Crest Factor) for 3G signals up to 6 dB
- Reduce PAR's (or Crest Factor) for OFDM signals by up to 4 dB
- All while meeting ACPR (Adjacent Channel Power Ratio) and EVM (Error Vector Magnitude) specs
 - Correct for up to 11th order non-linearities and PA (Power Amplifier) memory effects up to 200 ns
 - Greater than 20 dB ACPR improvement
 - Over 4X increase in power efficiency
- As much as 60% reduction in static power consumption



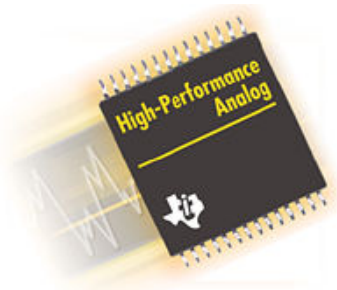
PAR/Crest Factor

The crest factor or peak-to-average ratio (PAR) or peak-to-average power ratio (PAPR) is a measurement of a waveform, calculated from the peak amplitude of the waveform divided by the RMS (time-averaged) value of the waveform.

$$C = \frac{|x|_{\text{peak}}}{x_{\text{RMS}}}$$

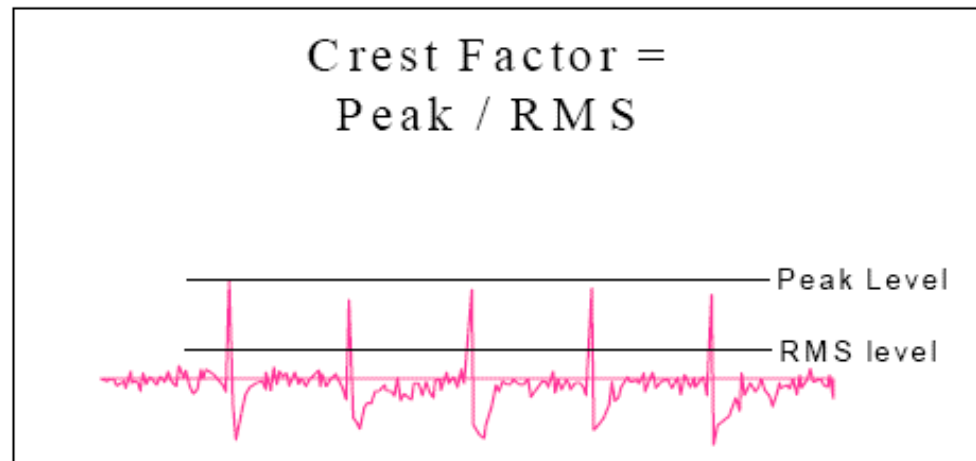
It is therefore a dimensionless value. While this quotient is most simply expressed by a positive rational number, as shown below, in commercial products it is also commonly stated as the ratio of two whole numbers, e.g., 2:1.

The minimum possible crest factor is 1.



PAR/Crest Factor

DC voltages have a crest factor of 1 since the RMS and the peak amplitude are equal, and it is the same for a square wave (of 50% duty cycle).





PAR/Crest Factor

This table provides values for some other normalized waveforms:

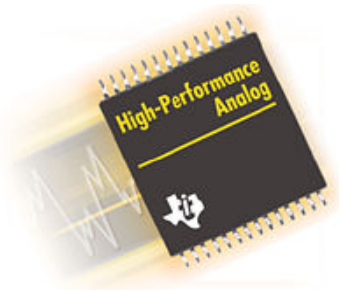
<u>Wave type</u>	<u>Crest factor (dB)</u>
DC	0.00 dB
Sine wave	3.01 dB
Full-wave rectified sine	3.01 dB
Half-wave rectified sine	6.02 dB
Triangle wave	4.77 dB
Square wave	0.00 dB
QPSK	3.5 - 4 dB
64 QAM	7.7 dB
128 QAM	8.2 dB
WCDMA downlink carrier	10.6 dB



PAR/Crest Factor

Notes:

- 1. Crest factors specified for QPSK, QAM, WCDMA are typical factors needed for reliable communication, not the theoretical crest factors which can be larger.**
- 2. Waveform factor is the ratio of DC average to RMS and is used to scale resistors for measurements with DC or AC meters. The waveform factor for the half wave rectified sine wave should be 2.22 as the DC average is V_P/π**



Memory-less Linearization Techniques

A generalized look up table can be used for pre-distorter gain/phase correction if no memory effects are taken into consideration

Thus we are able to characterize a PA by:

- 1. Amplitude or AM-to-AM (or Gain Compression)**
- 2. Phase Transfer or AM-to-PM**



Performance Analyses of Efficiency Enhancement Techniques of PA's

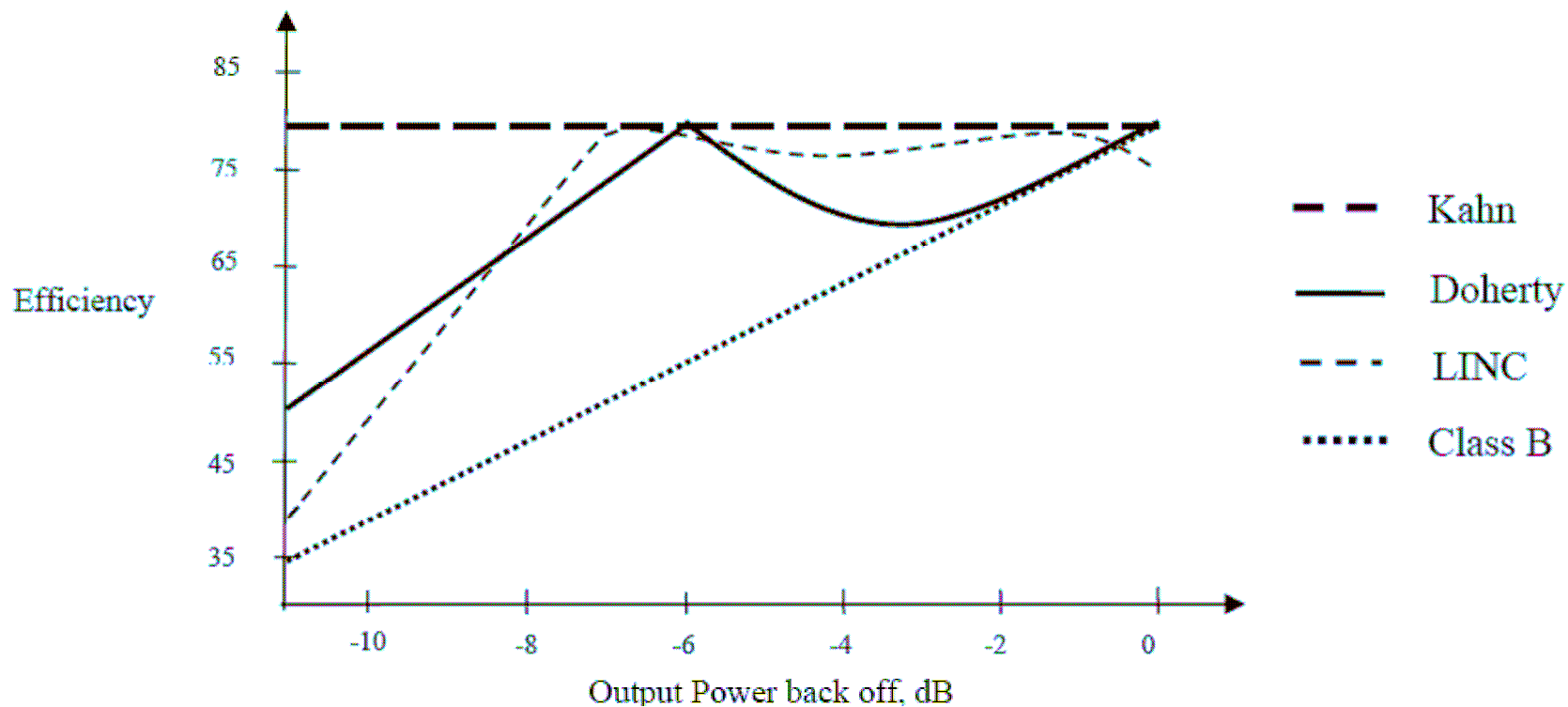
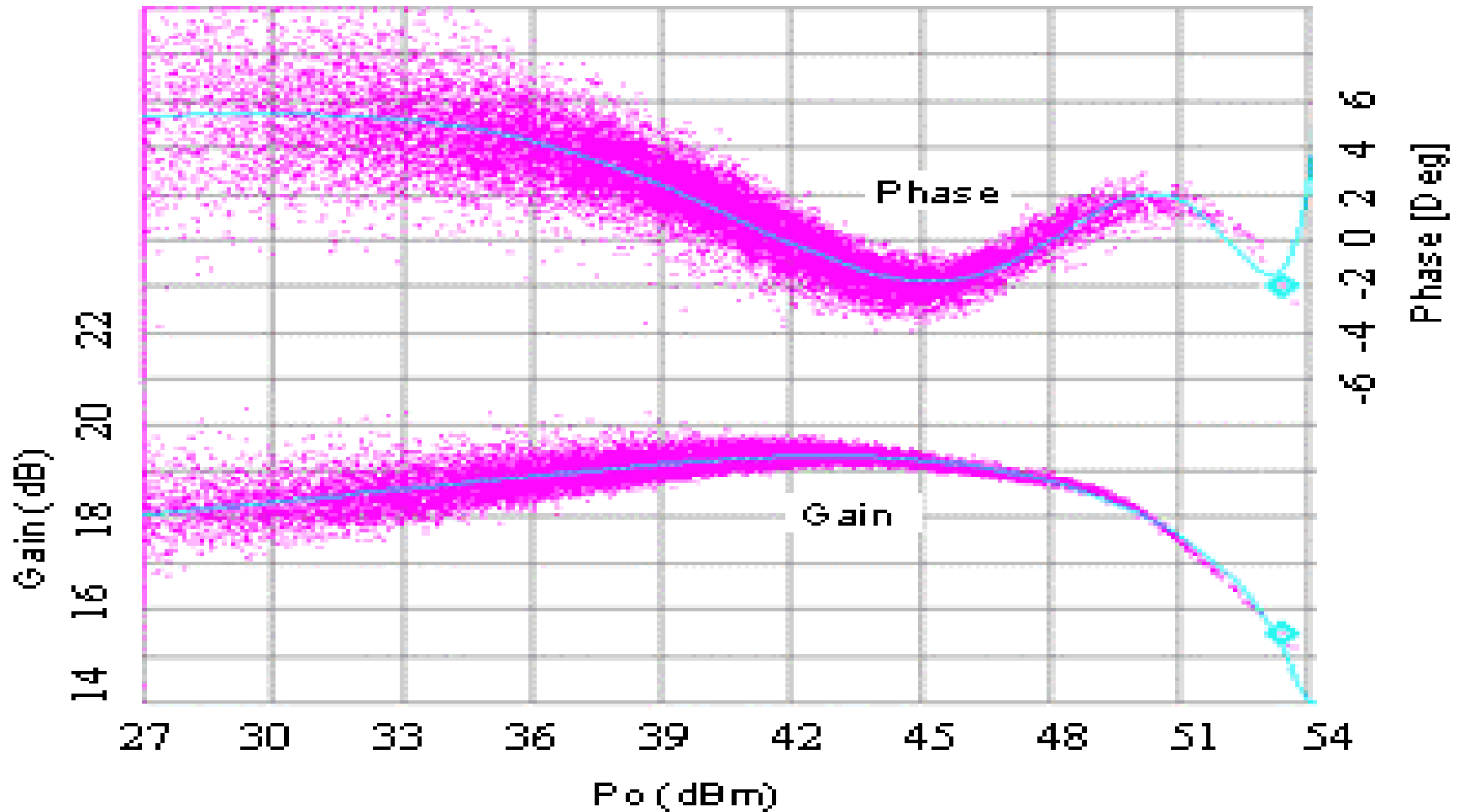
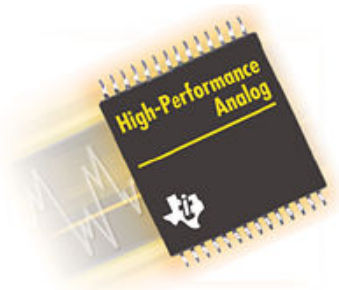




Figure 1: Gain compression and AM-PM characteristics for a typical Doherty PA





A more accurate PA model

Gain and Phase of PA's change with:

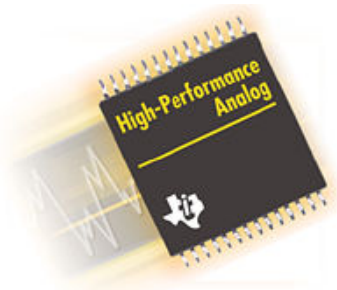
- Temperature
- Voltage
- Component ageing

This requires an adaptive control of look-up tables for effective linearization



Volterra-based DPD Linearizer

- Volterra series and Theorem developed by Vito Volterra in 1887
- It is used to predict non-linear response of a system to a given input
 - Similar to Taylor series but Volterra has ability to capture “memory” effects



Volterra series /Equation 1

$$Y(n) = Y1(n) + Y2(n) + Y3(n) + Y4(n) + Y5(n) + \dots + v(n) \quad (1)$$

Where,

$$Y1(n) = \sum_{i=0:M1} h1(i).x(n-i)$$

$$Y2(n) = \sum_{i1=0:M2} \sum_{i2=0:M2} h2(i1,i2).x(n-i1).x(n-i2)$$

$$Y3(n) = \sum_{i1=0:M3} \sum_{i2=0:M3} \sum_{i3=0:M3} h3(i1,i2,i3).x(n-i1).x(n-i2).x(n-i3)$$

$$Y4(n) = \sum_{i1=0:M4} \sum_{i2=0:M4} \sum_{i3=0:M4} \sum_{i4=0:M4} h4(i1,i2,i3, i4).x(n-i1).x(n-i2).x(n-i3).x(n-i4)$$

$$Y5(n) = \sum_{i1=0:M5} \sum_{i2=0:M5} \sum_{i3=0:M5} \sum_{i4=0:M5} \sum_{i5=0:M5} h5(i1,i2,i3,i4,i5).x(n-i1).x(n-i2).x(n-i3).x(n-i4).x(n-i5)$$



Simplify



WOW!! We need to simplify this!



Memory Polynomial Model

This technique constrains the Volterra Series so that everything except the diagonal terms in the kernels are zero, thus giving a memory polynomial model:

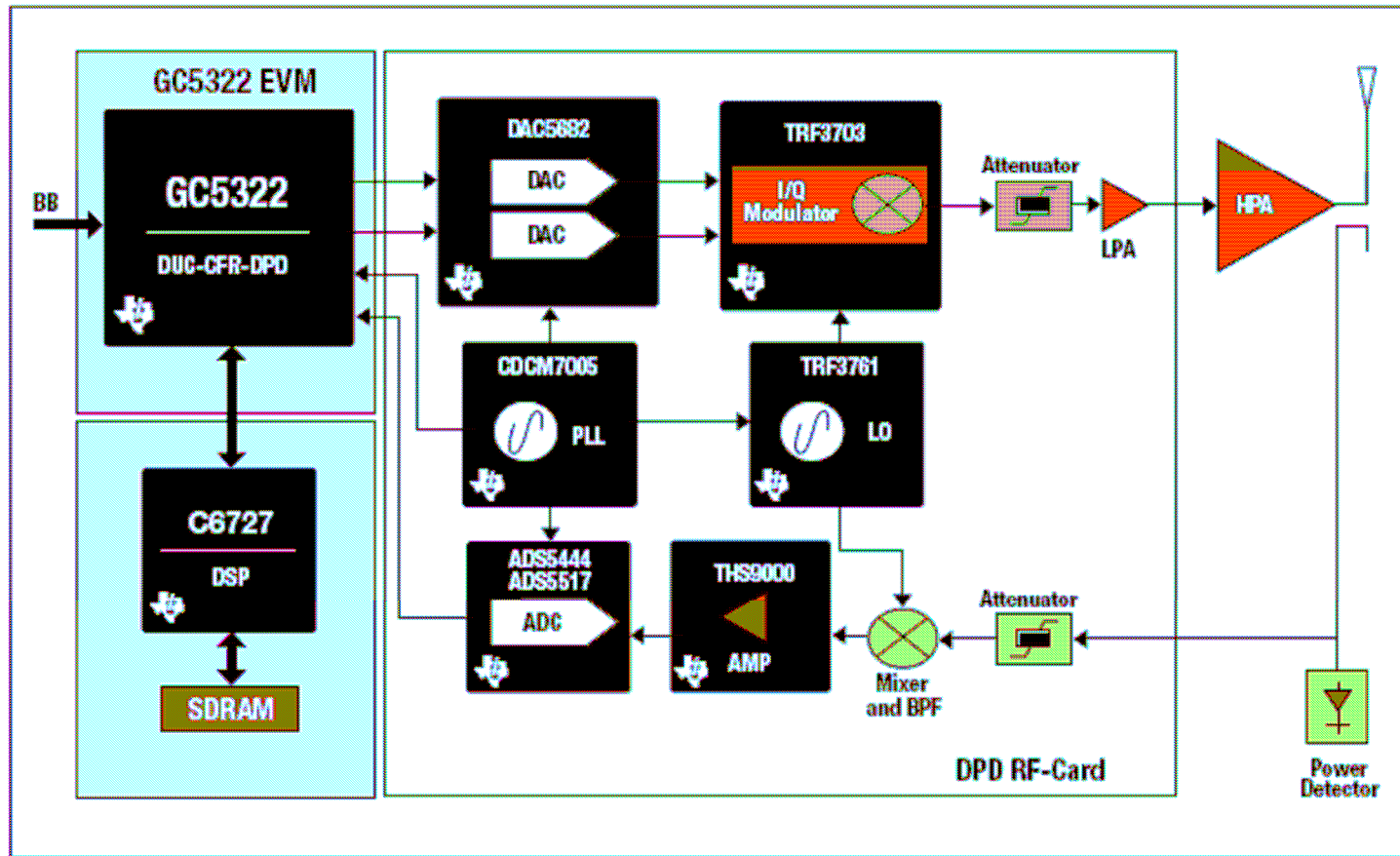
$$Y(n) = \sum_{k=0:K} \sum_{i=0:M} h_k(i) \cdot x(n-i) |x(n-i)|^k$$

This simplification method has been proven to effectively model PA:

- 1. Thermal effects**
- 2. Active matching network**
- 3. Bias circuits due to slowly varying , non-constant amplitude of PA input signal**



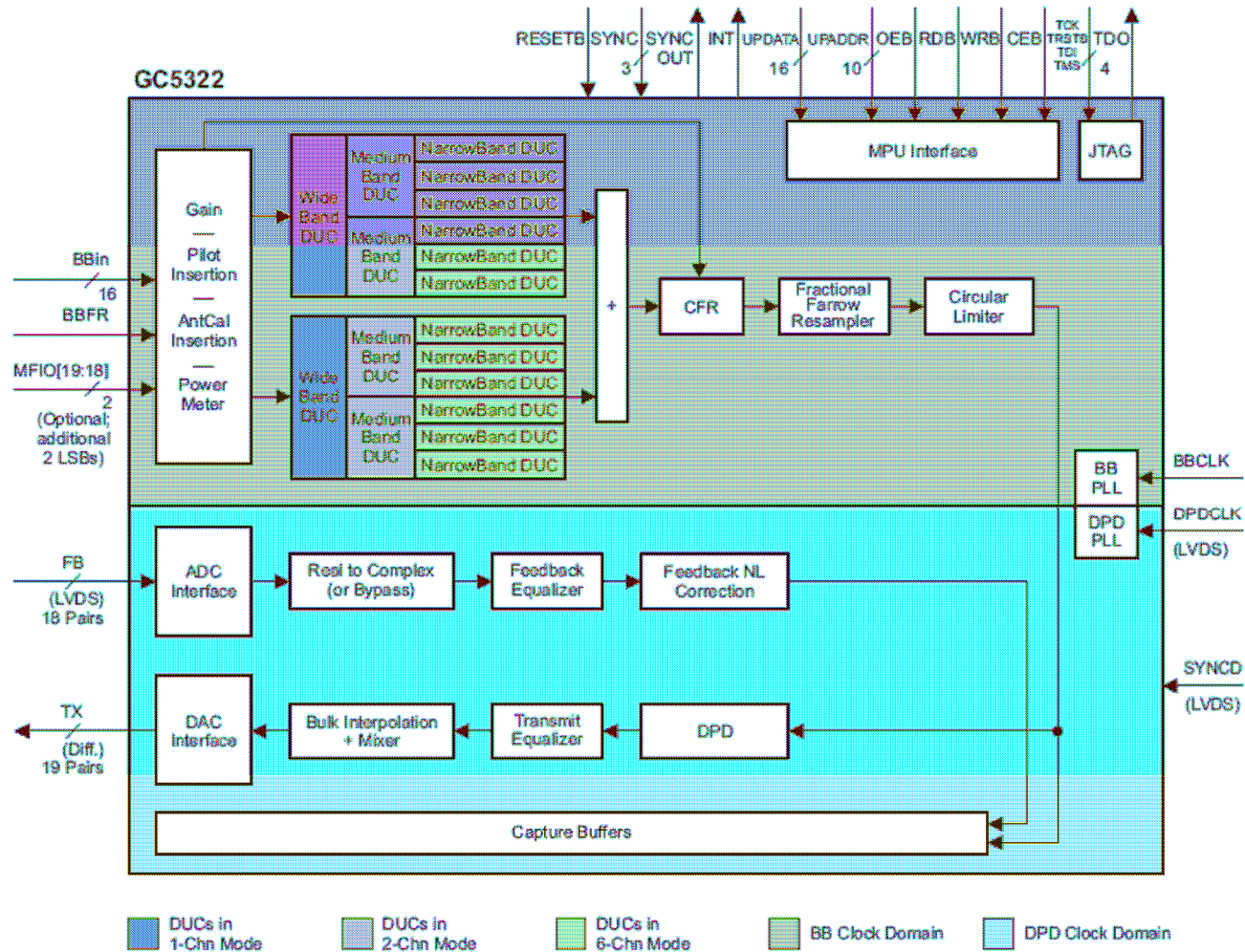
Figure 2: DPD System Diagram



▲ A complete digital pre-distortion transmit signal chain with the GC5322SEK (System Evaluation Kit) based on TI high-speed analog and DSP technology



Figure 2A: GC5322 Diagram





GC5322 DPD blocks

- 1. Linear Equalizer**
- 2. Non-Linear DPD**
- 3. Feedback Non-Linear Compensator and Smart Capture Buffers**



Equation Reduction/Simplification Techniques Used

We used a combination of algorithmic and model reduction approaches:

- 1. The number of terms in (1) significantly reduced by eliminating redundancies associated with various index permutations.**
- 2. Volterra coefficients assumed to be symmetric**
- 3. Real input signal to the PA $x(n)$ expressed in terms of its complex baseband representation significantly reducing the number of terms. For band-limited systems we are only interested in frequency components close to the carrier frequency f_0**
- 4. Even order inter-modulation terms lie far away from frequency band of interest, allowing us to further drop half the terms in (1)**



Equation Reduction/Simplification Techniques Used (cont'd)

We used a combination of algorithmic and model reduction approaches:

- 5. The model is rotationally invariant, this simplifies things since a phase shift on the input of the PA produces exactly the same phase shift on the output. This allows (1) to be reduced to terms involving products of the signal and powers of its magnitude squared.**
- 6. The PA is causal, so we assume the linear portion of the PA is minimum phase. This further restricts Volterra terms**
- 7. Since PA implementations perform the processing in stages, this also helps simplify the model into cascade sections with each matched to the needs of compensating the distortions induced by the particular PA stage.**

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First Stage--- Linear Equalizer ----Equation 2

**We get the model for the Linear Equalizer block
by restricting the Volterra Series to only linear terms with
memory M1:**

$$Y1(n) = \sum_{i=0:M1} h1(i).x(n-i) \quad (2)$$



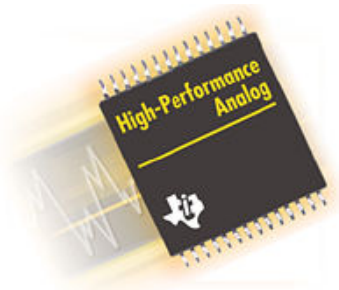
Second Stage-- Non-Linear DPD -----Equation 3

We get the Non-Linear DPD block by restricting the Volterra Series to only the non-linear terms with memory M2, and dropping even terms we get:

$$Y(n) = \sum_{i=0:M2} h3(i,i,i).x(n-i).|x(n-i)|^2 + \sum_{i=0:M2} h5(i,i,i,i,i).x(n-i).|x(n-i)|^4 + \sum_{i=0:M2} h7(i,i,i,i,i,i,i).x(n-i).|x(n-i)|^6$$

+ other higher order terms depending on the polynomial modeling accuracy requirements of the adaptation algorithm. (3)





Rearranging Equation 3



Rearranging terms in Equation 3 gives:

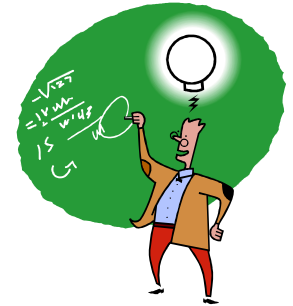
$$\begin{aligned} Y(n) &= \sum_{i=0:M2} \{ h3(i,i,i) \cdot |x(n-i)|^2 + h5(i,i,i,i,i) \cdot [|x(n-i)|^2]^2 + \\ &\quad h7(i,i,i,i,i,i,i) \cdot [|x(n-i)|^2]^3 + \text{higher order terms} \} \cdot x(n-i) \\ &= \sum_{i=0:M2} \text{LUT}(|x(n-i)|^2) \cdot x(n-i) \end{aligned}$$



Equation 4

Simplifying Equation 1 Volterra Series terms:

$$\begin{aligned}
 Y(n) = & \sum_{i=0}^{M3} h3(i,i,0) \cdot |x(n-i)|^2 \cdot x(n-i) + \\
 & \sum_{i=0}^{M3} h5(i,i,0,0,0) \cdot |x(n-i)|^2 \cdot |x(n)|^2 \cdot x(n) + \\
 & \sum_{i=0}^{M3} h5(i,i,i,i,0) \cdot |x(n-i)|^4 \cdot x(n) + \\
 & \sum_{i=0}^{M3}, i \neq j \sum_{j=0}^{M3} h5(i,i,j,j,0) \cdot |x(n-i)|^2 \cdot |x(n-j)|^2 \cdot x(n) + \\
 & \sum_{i=0}^{M3} h7(i,i,0,0,0,0,0) \cdot |x(n-i)|^2 \cdot |x(n)|^4 \cdot x(n) + \\
 & \sum_{i=0}^{M3} h7(i,i,i,i,0,0,0) \cdot |x(n-i)|^4 \cdot |x(n)|^2 \cdot x(n) + \\
 & \sum_{i=0}^{M3} h7(i,i,i,i,i,i,0) \cdot |x(n-i)|^6 \cdot x(n) + \\
 & \sum_{i=0}^{M3}, i \neq j \sum_{j=0}^{M3} h7(i,i,j,j,0,0,0) \cdot |x(n-i)|^2 \cdot |x(n-j)|^2 \cdot |x(n)|^2 \cdot x(n) + \\
 & \sum_{i=0}^{M3}, i \neq j \sum_{j=0}^{M3} h7(i,i,i,i,j,j,0) \cdot |x(n-i)|^4 \cdot |x(n-j)|^2 \cdot x(n) \\
 & + \text{higher order terms} \tag{4}
 \end{aligned}$$





Third Stage---Feedback Non-Linear Compensator and Smart Capture Buffers

Feedback signal from PA used to compute the instantaneous error, which along with reference transmit signal can be captured by a pair of on-chip memories.

DSP processor reads back these captured signals and implements the adaptation algorithms for the pre-distorter blocks.



Pre-Distortion Adaptation Algorithm

A Direct Learning architecture is used in the pre-distortion algorithm implemented on the DSP.

A model of the pre-distorter is maintained in software---its parameters optimized to minimize the error signal captured in the hardware.



Figure 3: GC5322 evaluation platform system diagram

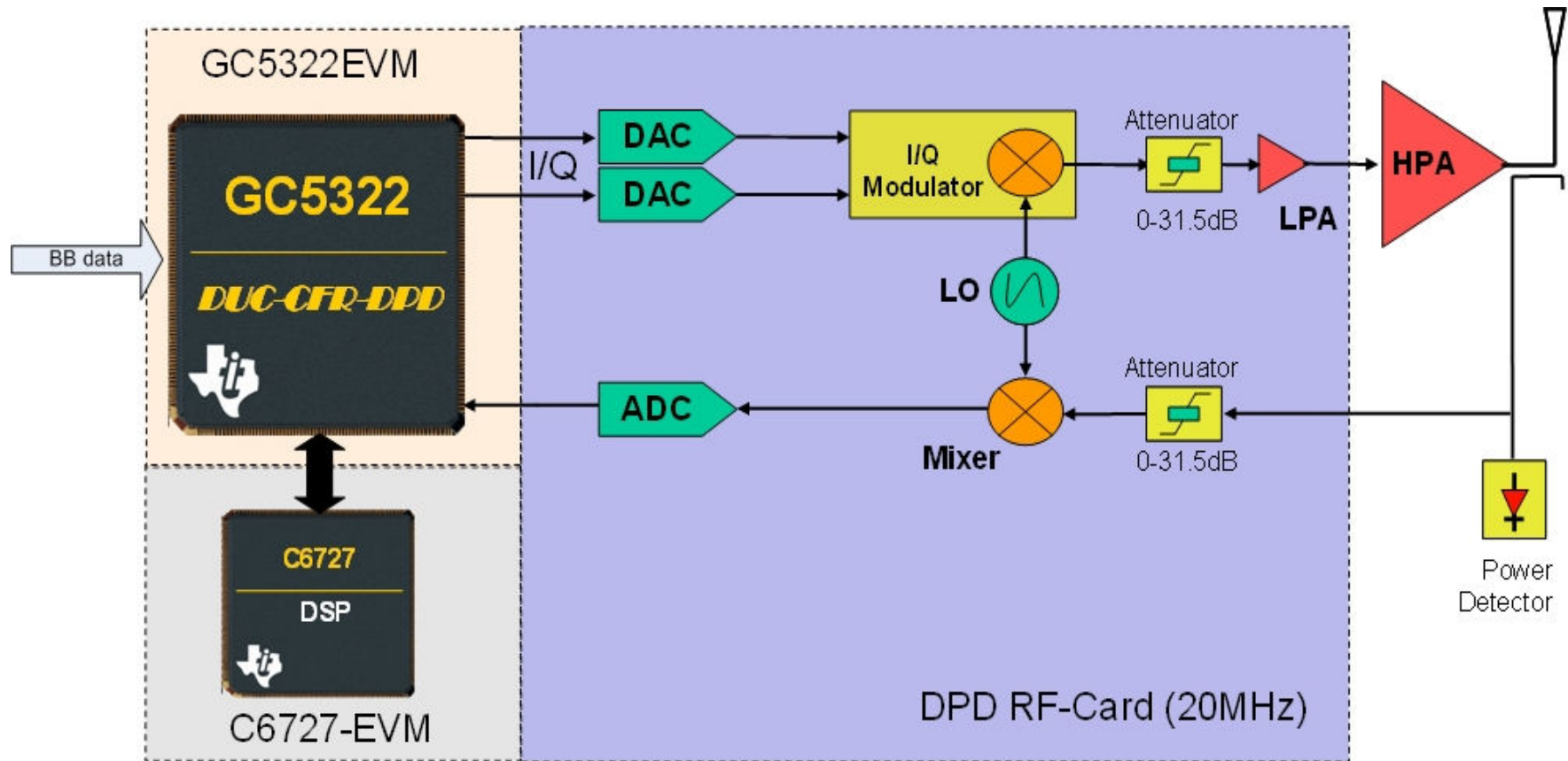




Table 1: GC5322 evaluation platform system parameters

Evaluation System Configuration		
RF Card Version	WiMax	WCDMA
DUC Input Sample Rate	11.2MSPS (WiMax)	3.84MSPS (WCDMA), 1.28MSPS(TD-SCDMA), 4.333MSPS (MC-GSM), 30.72MSPS (LTE)
CFR Sample Rate	67.2MSPS (WiMax)	61.44MSPS (WCDMA, TD-SCDMA, LTE), 69.333MSPS (MC-GSM)
DPD Sample Rate	112MSPS	122.88MSPS
DAC	DAC5682 @ 672MHz Complex	DAC5682 @ 737.28MHz Complex
ADC	ADS5444 @ 224MHz Real	ADS5444 @ 245.76MHz Real
IF Frequency	168MHz	184.32MHz
RF Frequency	2.123GHz	2.139GHz
IQ Modulator	TRF3703	
Mixer	HMC214	
LO	TRF3761	
PLL	CDCM7005	



Figure 4-A: Adjacent channel ACLR Vs. Pout at different PAR levels & test signals, pre & post DPD

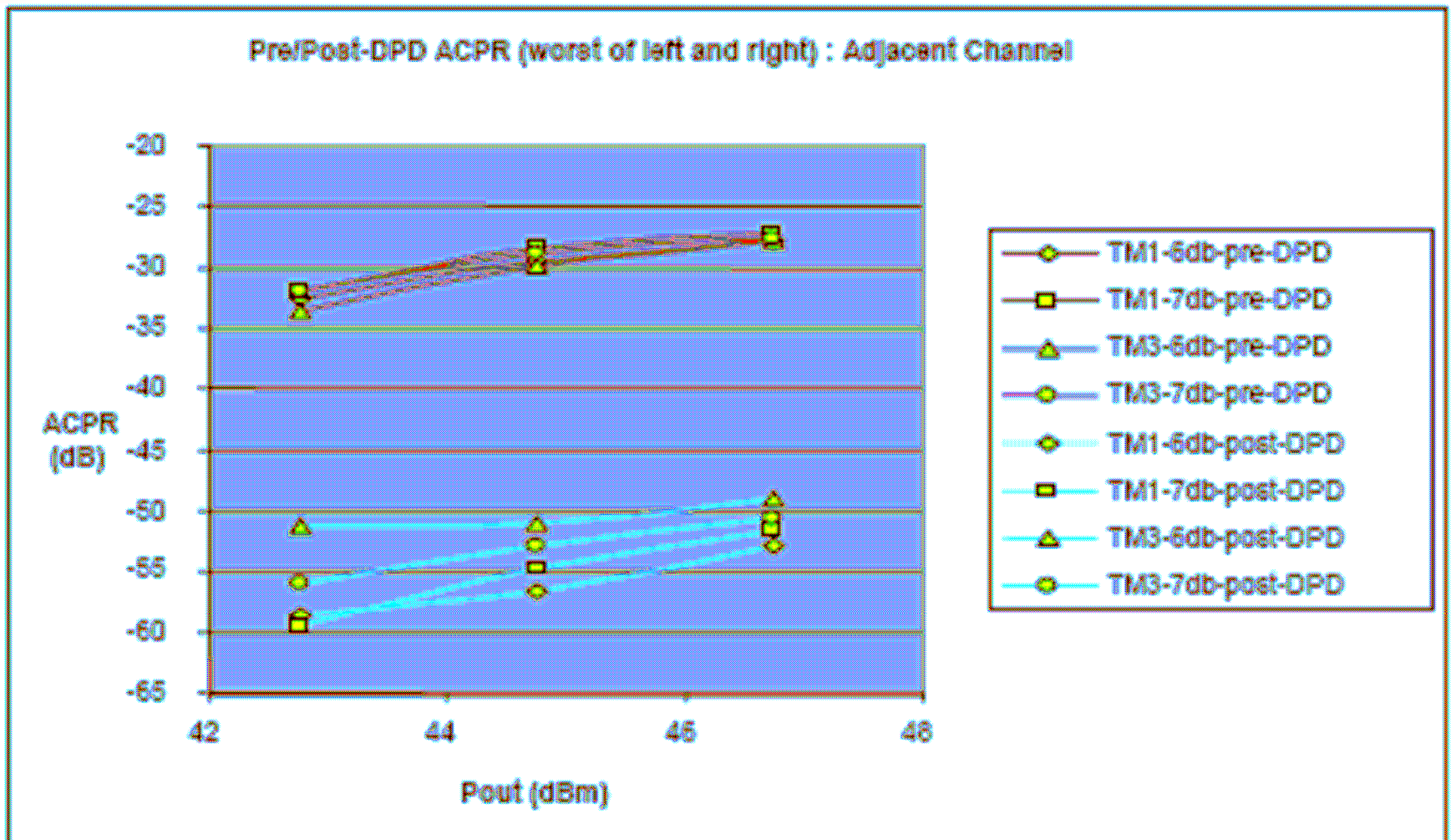




Figure 4-B: Alternate channel ACLR Vs. Pout at different PAR levels & test signals, pre & post DPD

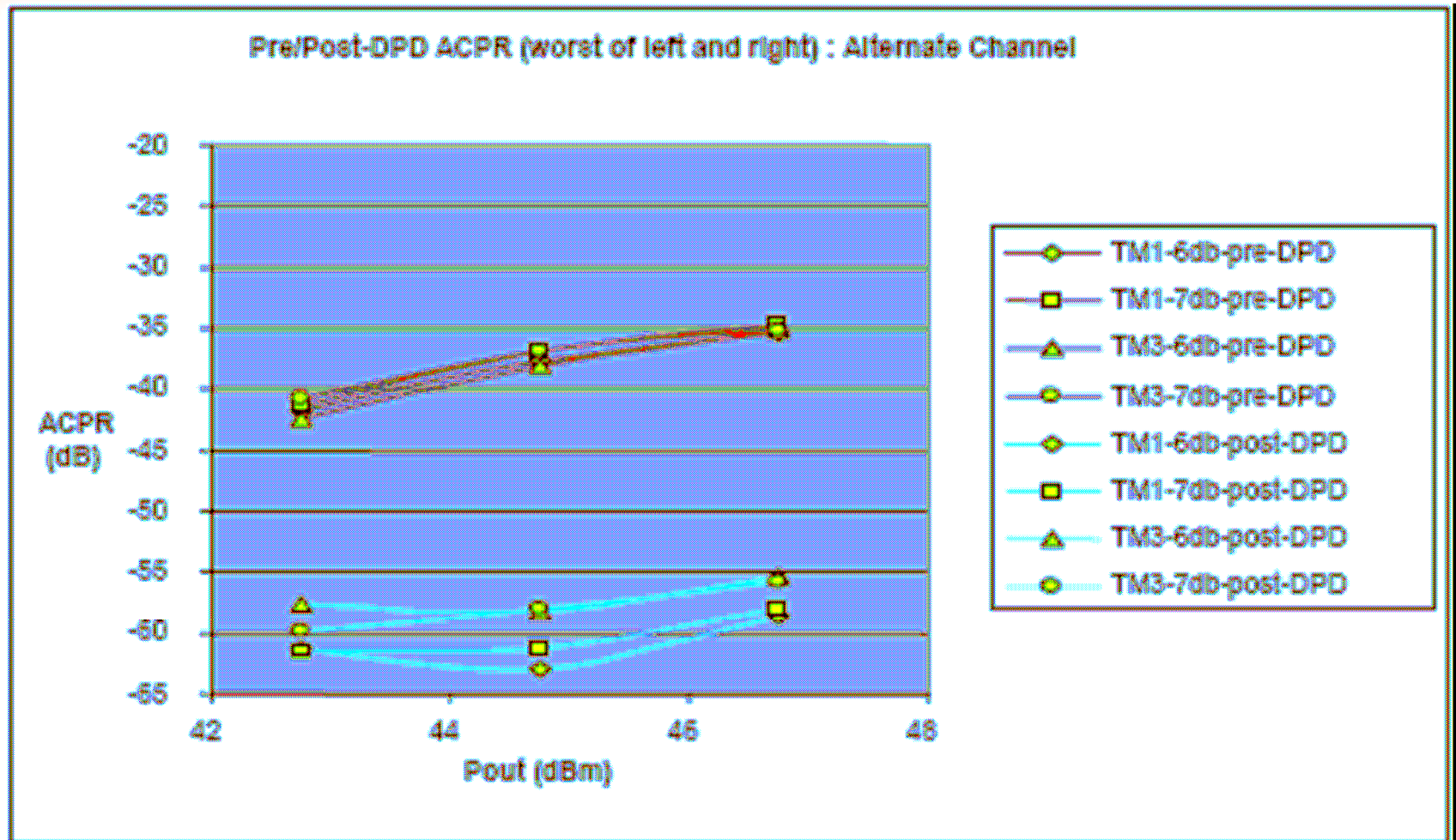




Figure 5-A: Pre-DPD spectrum at 46.75dBm Pout and 6dB PAR (TM1-64 data)

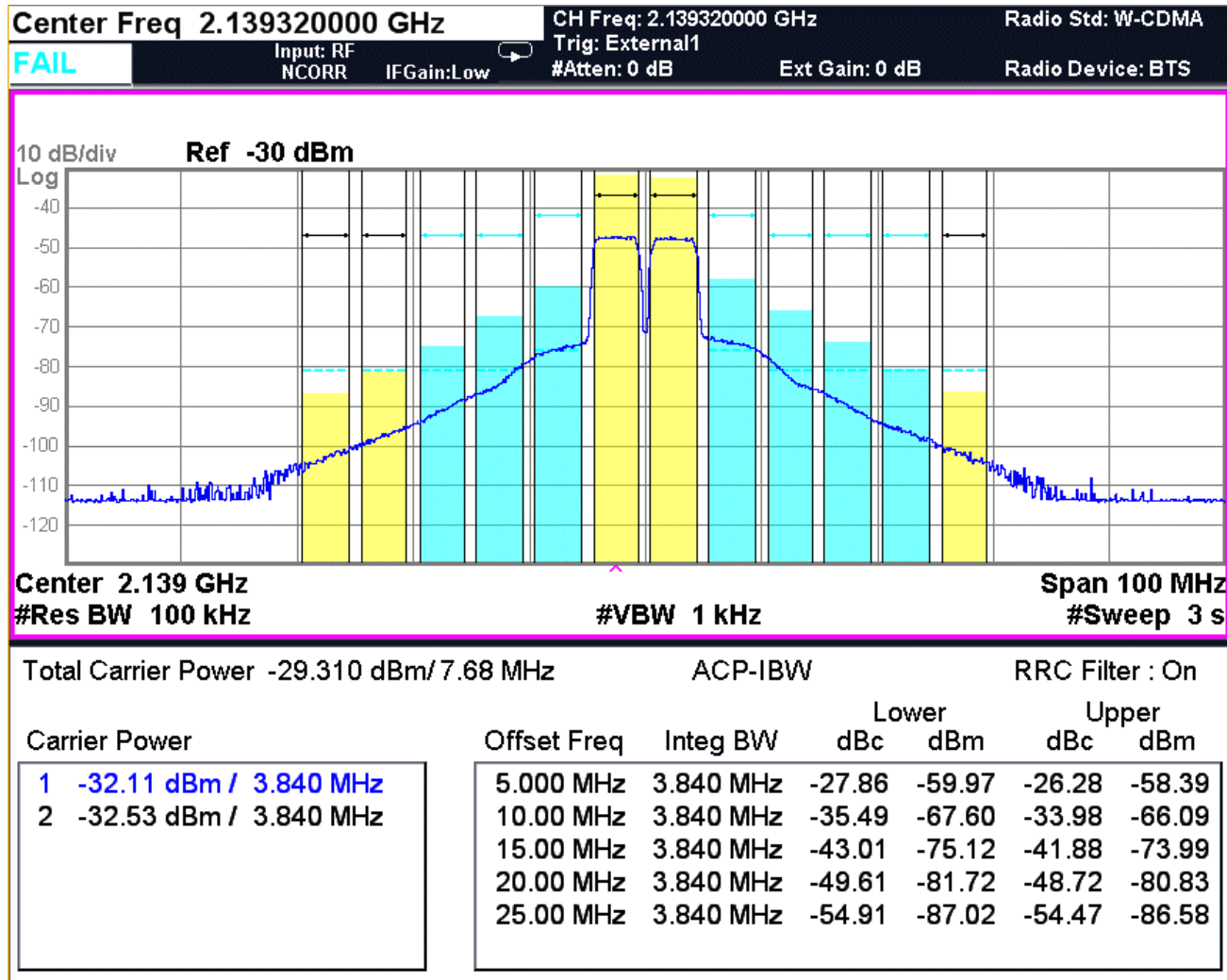




Figure 5-B: Post-DPD spectrum at 46.75dBm Pout and 6dB PAR (TM1-64 data)

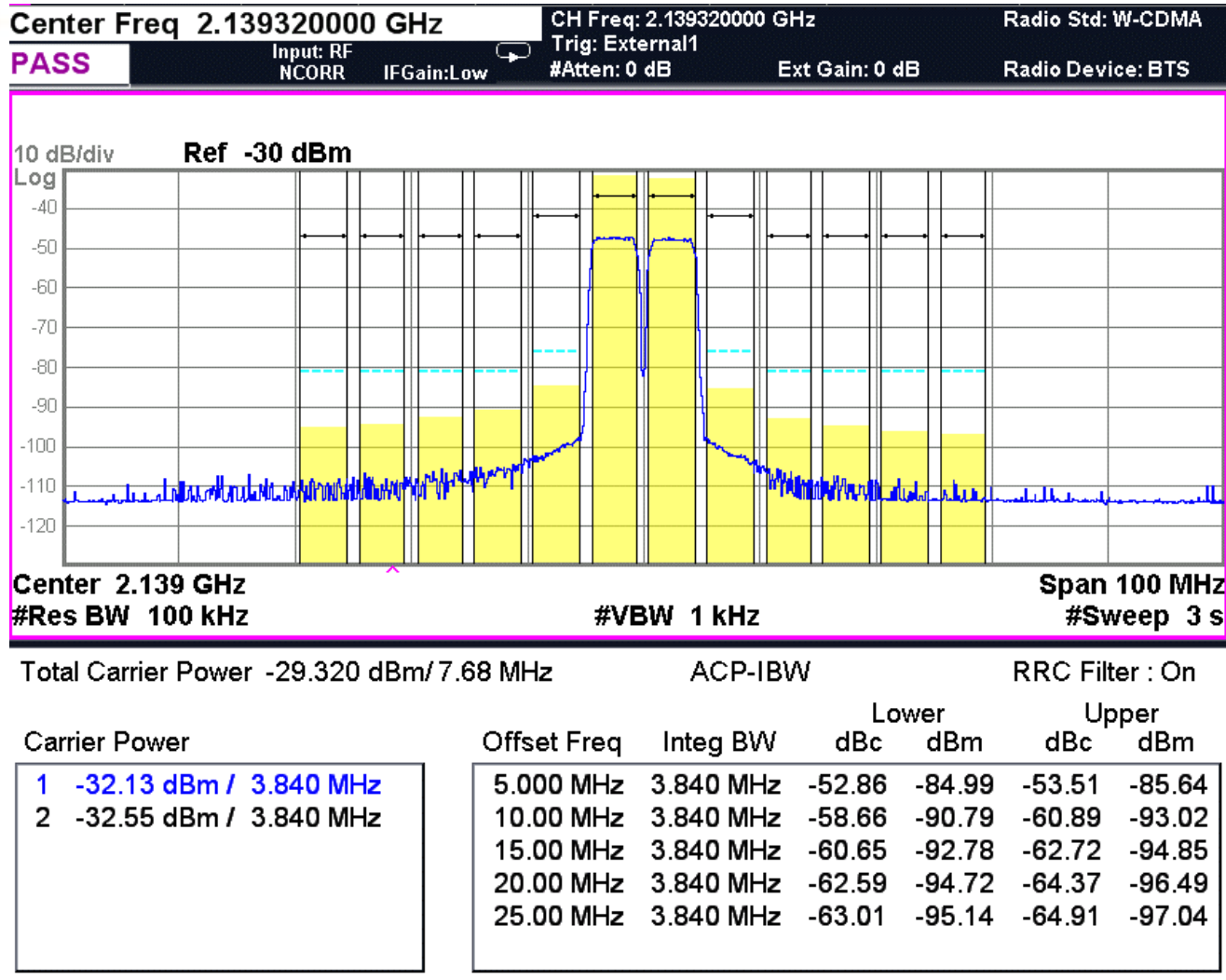




Figure 6-A: PCDE Vs. Pout at different PAR levels and test signals, pre and post DPD

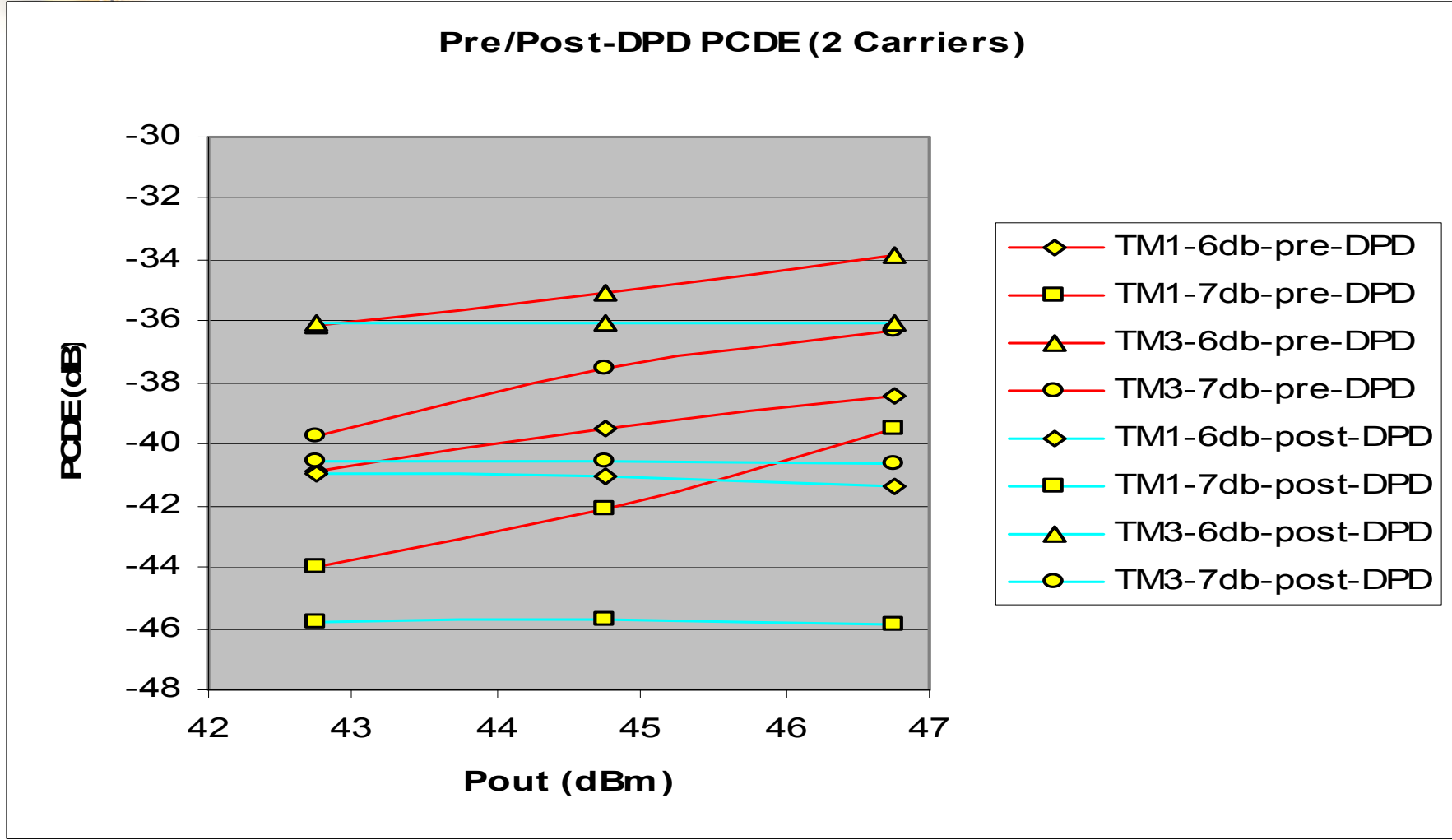
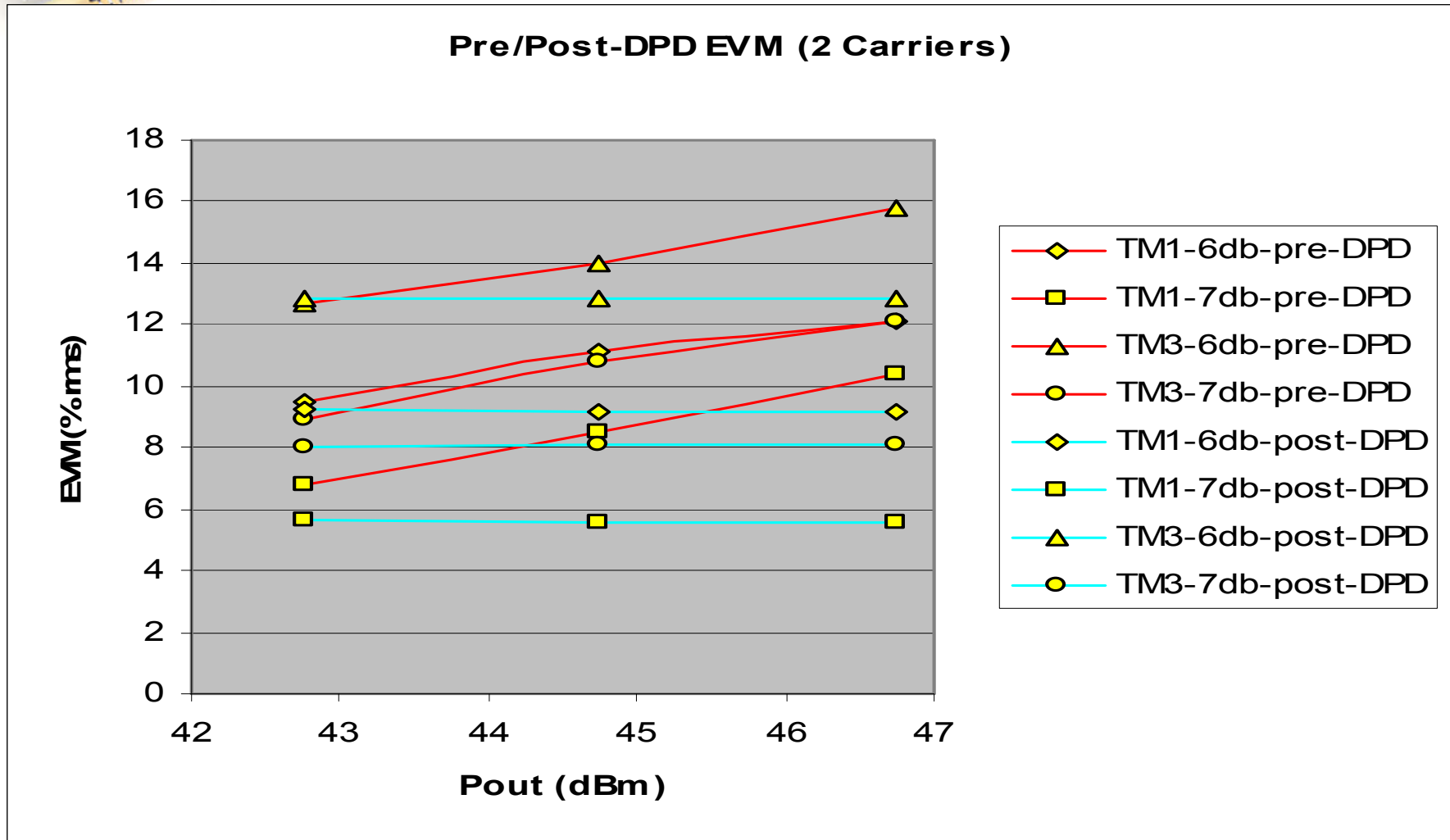




Figure 6-B: EVM Vs. Pout at different PAR levels and test signals, pre and post DPD



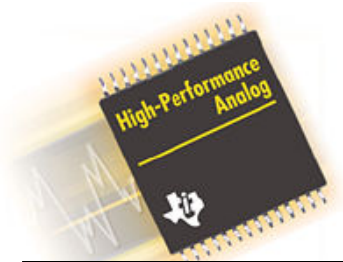


Figure 7: PA drain power efficiency Vs. output power

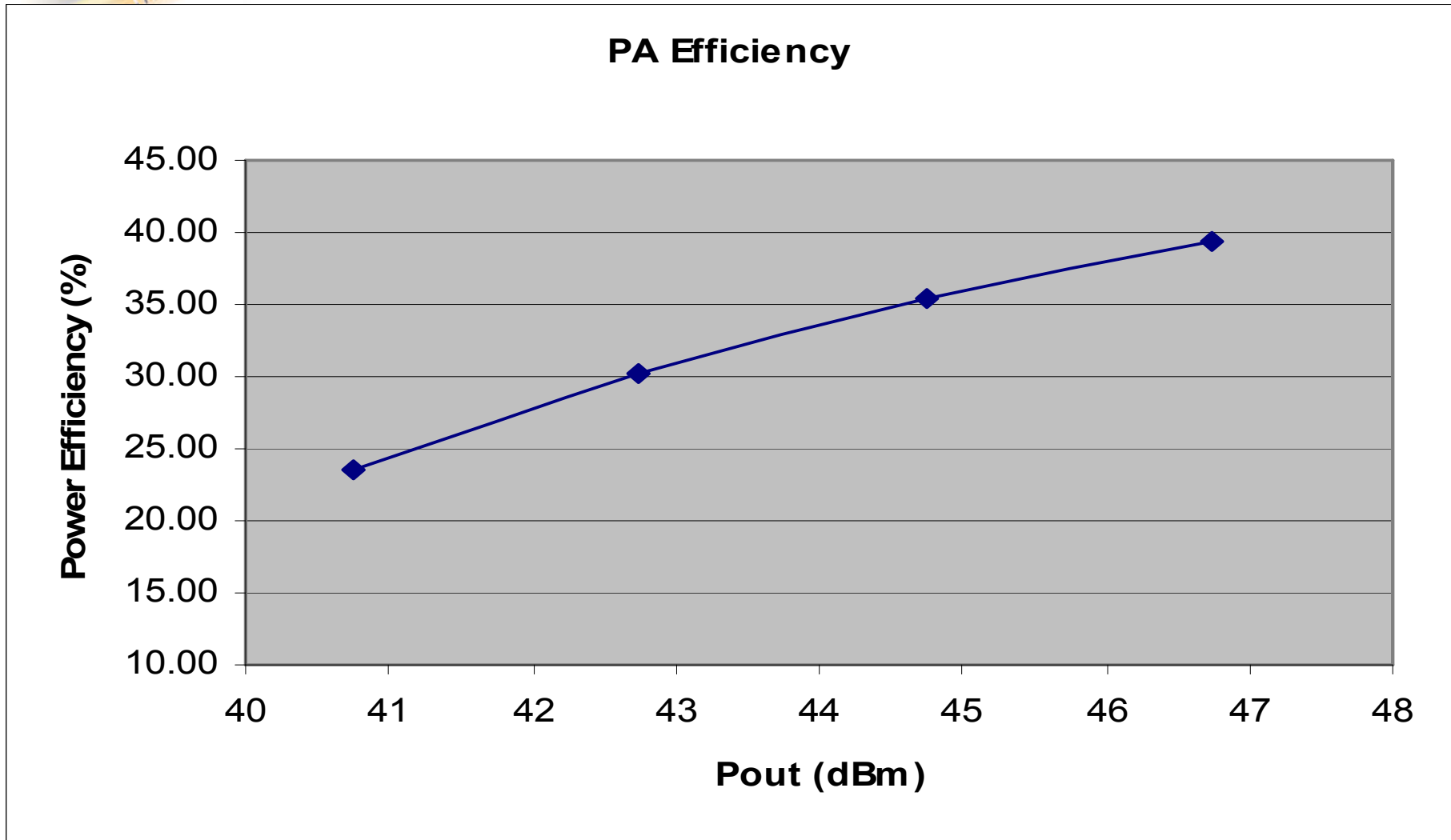




Figure 8-A: WCDMA: Pre-DPD spectrum at 42.75dBm Pout and 6dB PAR (TM1-64 data)

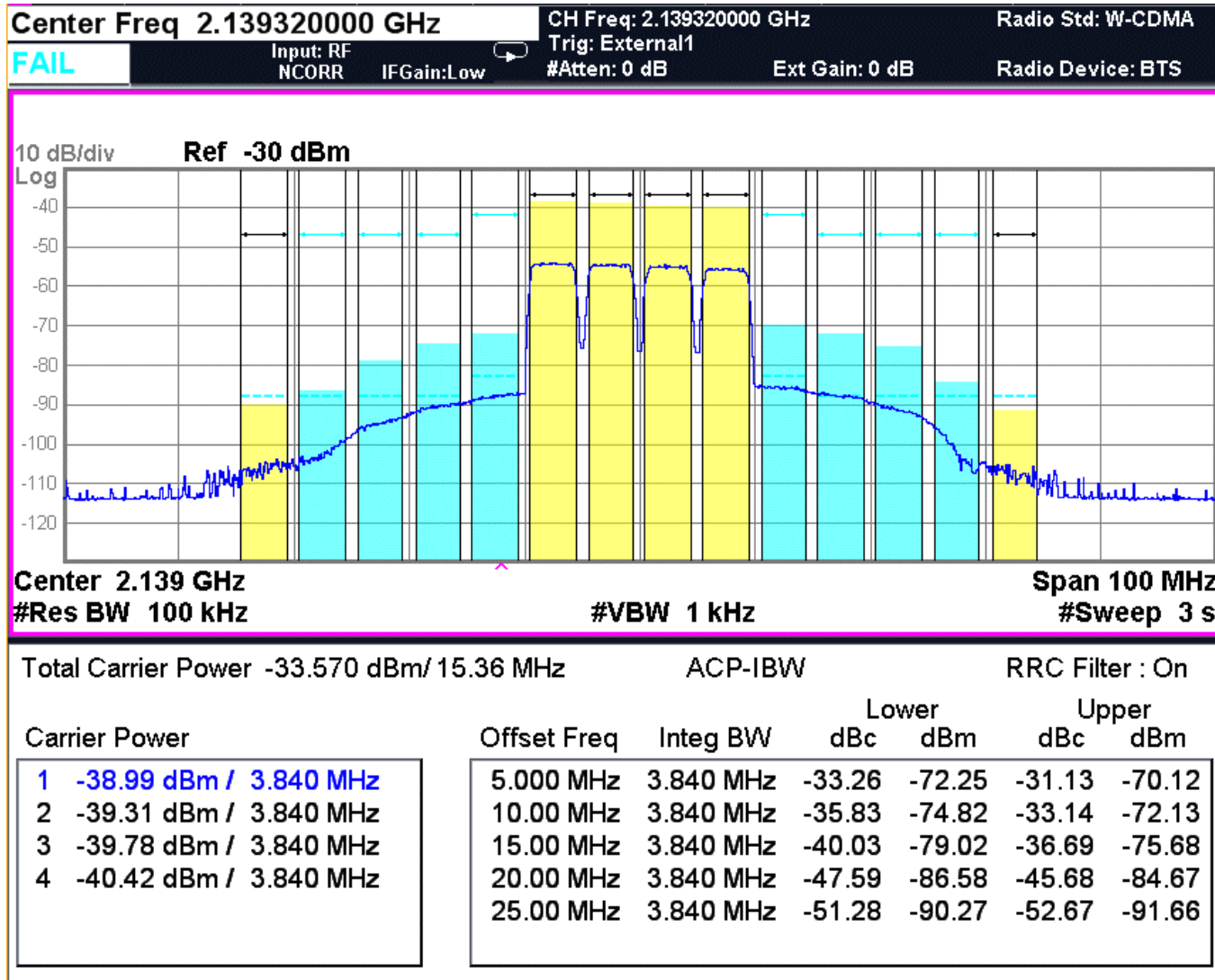




Figure 8-B: WCDMA: Post-DPD spectrum at 42.75dBm Pout and 6dB PAR(TM1-64 data)

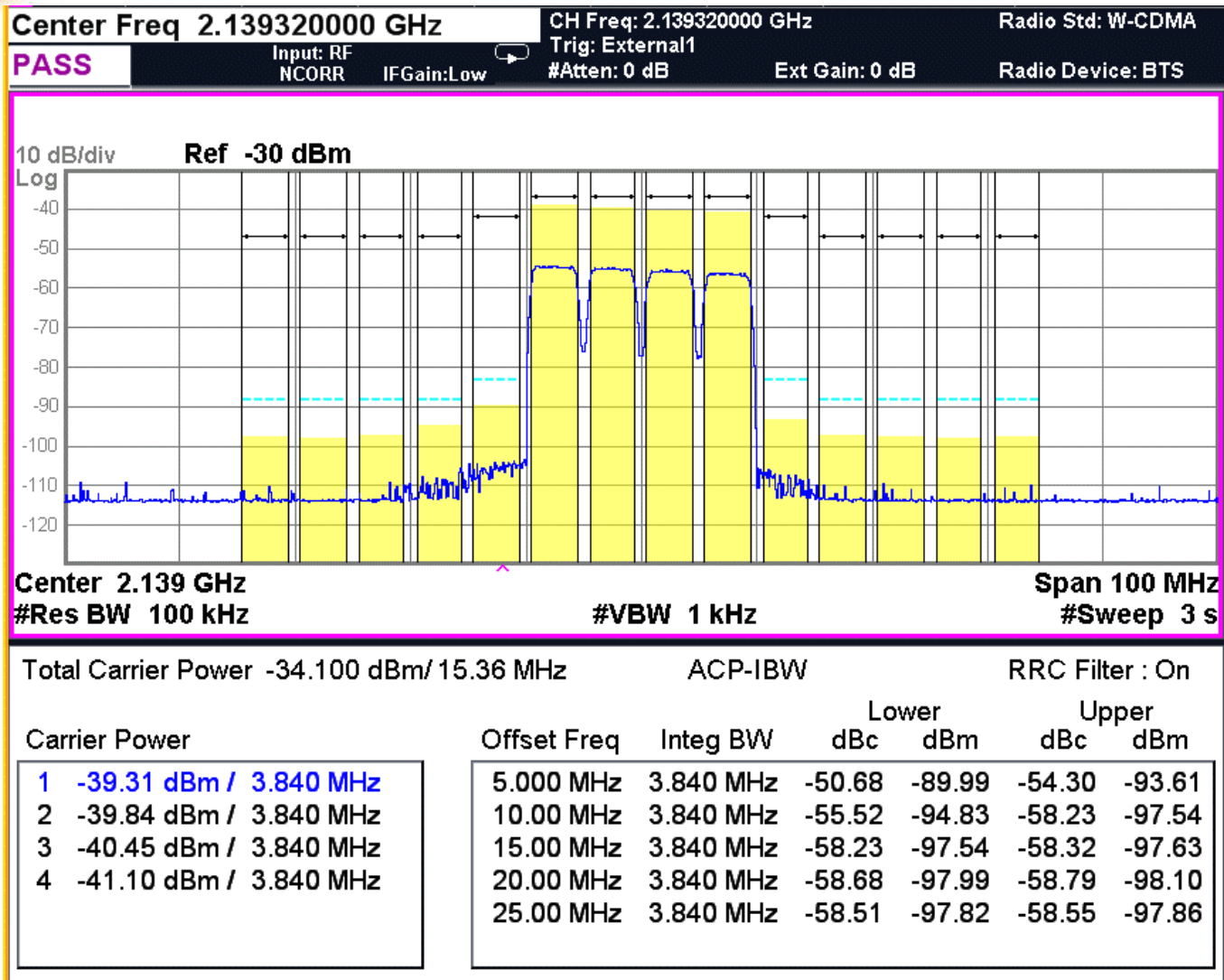
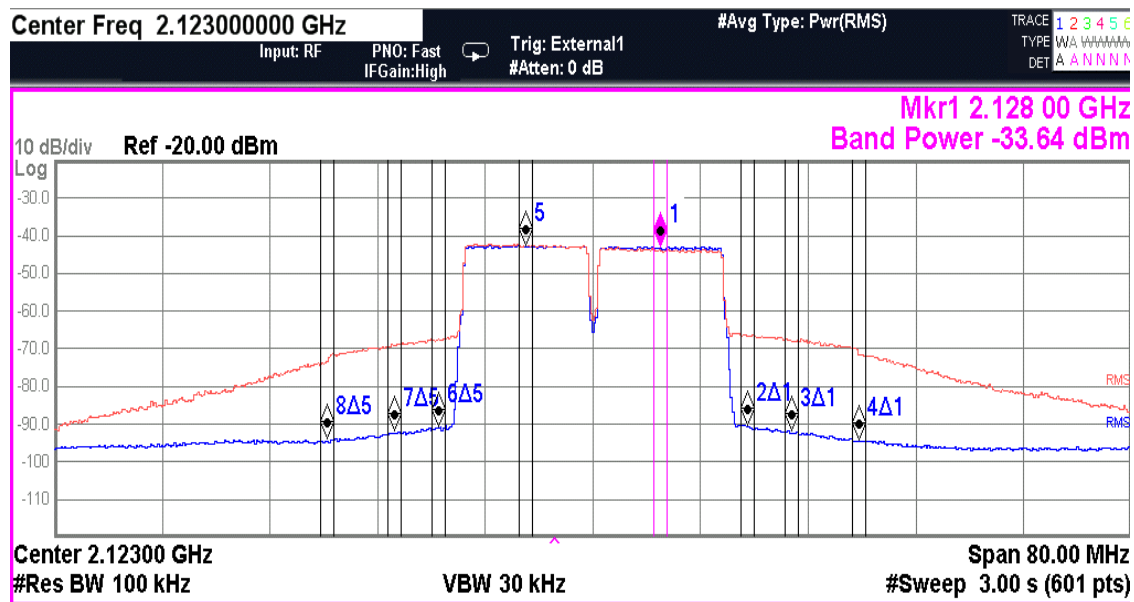




Figure 9-A: WiMax: Pre (red) and post (blue) DPD spectrums at 43.75dBm Pout and 8.5dB PAR



Pre - DPD

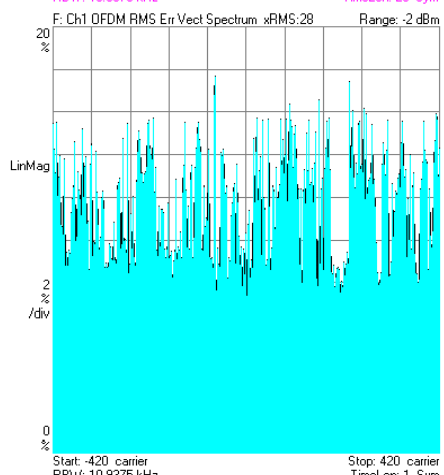
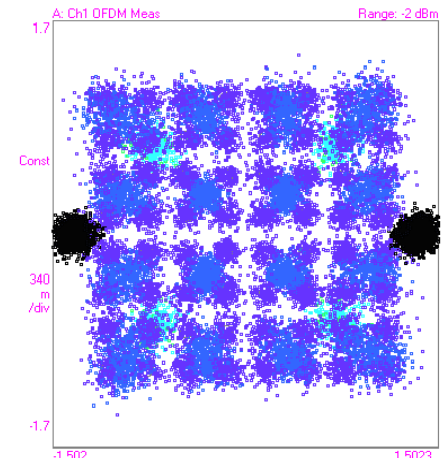
MKR	MODE	TRC	SCL	X	Y	FUNCTION	FUNCTION WIDTH	FUNCTION VALUE
1	N	1	f	2.128 00 GHz	-44.00 dBm	Band Power	1.000 MHz	-34.25 dBm
2	Δ1	1	f (Δ)	6.50 MHz (Δ)	-22.64 dB	Band Power	1.000 MHz (Δ)	-22.55 dB
3	Δ1	1	f (Δ)	9.75 MHz (Δ)	-24.07 dB	Band Power	1.000 MHz (Δ)	-23.80 dB
4	Δ1	1	f (Δ)	14.75 MHz (Δ)	-27.46 dB	Band Power	1.000 MHz (Δ)	-26.76 dB
5	N	1	f	2.118 00 GHz	-42.78 dBm	Band Power	1.000 MHz	-32.95 dBm
6	Δ5	1	f (Δ)	-6.50 MHz (Δ)	-24.70 dB	Band Power	1.000 MHz (Δ)	-24.89 dB
7	Δ5	1	f (Δ)	-9.75 MHz (Δ)	-26.22 dB	Band Power	1.000 MHz (Δ)	-26.37 dB
8	Δ5	1	f (Δ)	-14.75 MHz (Δ)	-30.35 dB	Band Power	1.000 MHz (Δ)	-30.01 dB

Post - DPD

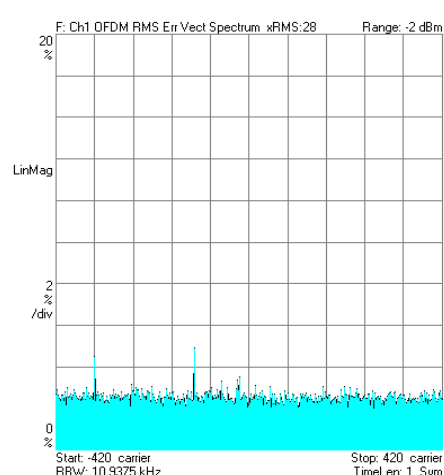
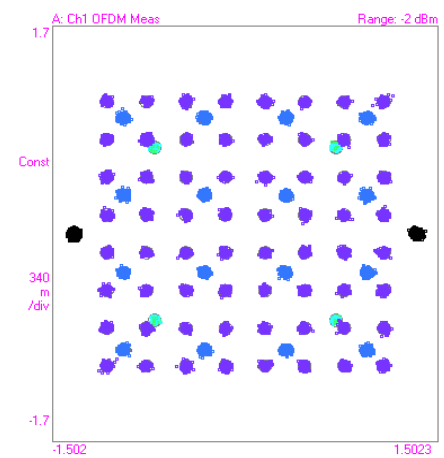
MKR	MODE	TRC	SCL	X	Y	FUNCTION	FUNCTION WIDTH	FUNCTION VALUE
1	N	1	f	2.128 00 GHz	-43.36 dBm	Band Power	1.000 MHz	-33.64 dBm
2	Δ1	1	f (Δ)	6.50 MHz (Δ)	-47.21 dB	Band Power	1.000 MHz (Δ)	-47.33 dB
3	Δ1	1	f (Δ)	9.75 MHz (Δ)	-49.01 dB	Band Power	1.000 MHz (Δ)	-48.82 dB
4	Δ1	1	f (Δ)	14.75 MHz (Δ)	-51.18 dB	Band Power	1.000 MHz (Δ)	-51.15 dB
5	N	1	f	2.118 00 GHz	-42.94 dBm	Band Power	1.000 MHz	-33.21 dBm
6	Δ5	1	f (Δ)	-6.50 MHz (Δ)	-48.04 dB	Band Power	1.000 MHz (Δ)	-48.20 dB
7	Δ5	1	f (Δ)	-9.75 MHz (Δ)	-49.44 dB	Band Power	1.000 MHz (Δ)	-49.43 dB
8	Δ5	1	f (Δ)	-14.75 MHz (Δ)	-51.54 dB	Band Power	1.000 MHz (Δ)	-51.50 dB



**Figure 9-B: WiMax: Clockwise from top left:
Pre-DPD Constellation, Post-DPD Constellation, Post-DPD Error vector spectrum,
Pre-DPD Error Vector Spectrum plots for 43.75dBm Pout, 8.5dB PAR**



RCE (EVM) = -19.756	dB	RCE (EVM) = 10.284	%rms
RCE Pk = 36.824	% pk at sym 7		
DataRCE = -19.205	dB	DataRCE = 10.959	%rms
DataRCE Pk = 36.824	% pk at sym 7		
PilotRCE = -22.534	dB	CPE = 1.4780	%rms
UnmodRCE = -780	dB	RSSI = -10.953	dBm
Freq Err = 557.93	Hz	SymClkErr = 0.16036	ppm
IQ Dllset = -52.945	dB	IQ Skew = 20.922	psec



RCE (EVM) = -32.819	dB	RCE (EVM) = 2.2858	%rms
RCE Pk = 9.5707	% pk at sym 8		
DataRCE = -32.317	dB	DataRCE = 2.4218	%rms
DataRCE Pk = 9.5707	% pk at sym 8		
PilotRCE = -35.14	dB	CPE = 733.63	m%rms
UnmodRCE = -780	dB	RSSI = -10.629	dBm
Freq Err = 568.71	Hz	SymClkErr = 0.22713	ppm
IQ Dllset = -63.038	dB	IQ Skew = 3.5122	psec



Figure 10-A: TD-SCDMA: Pre (blue) and post (green) DPD spectral plots at 46dBm Pout and 8dB PAR

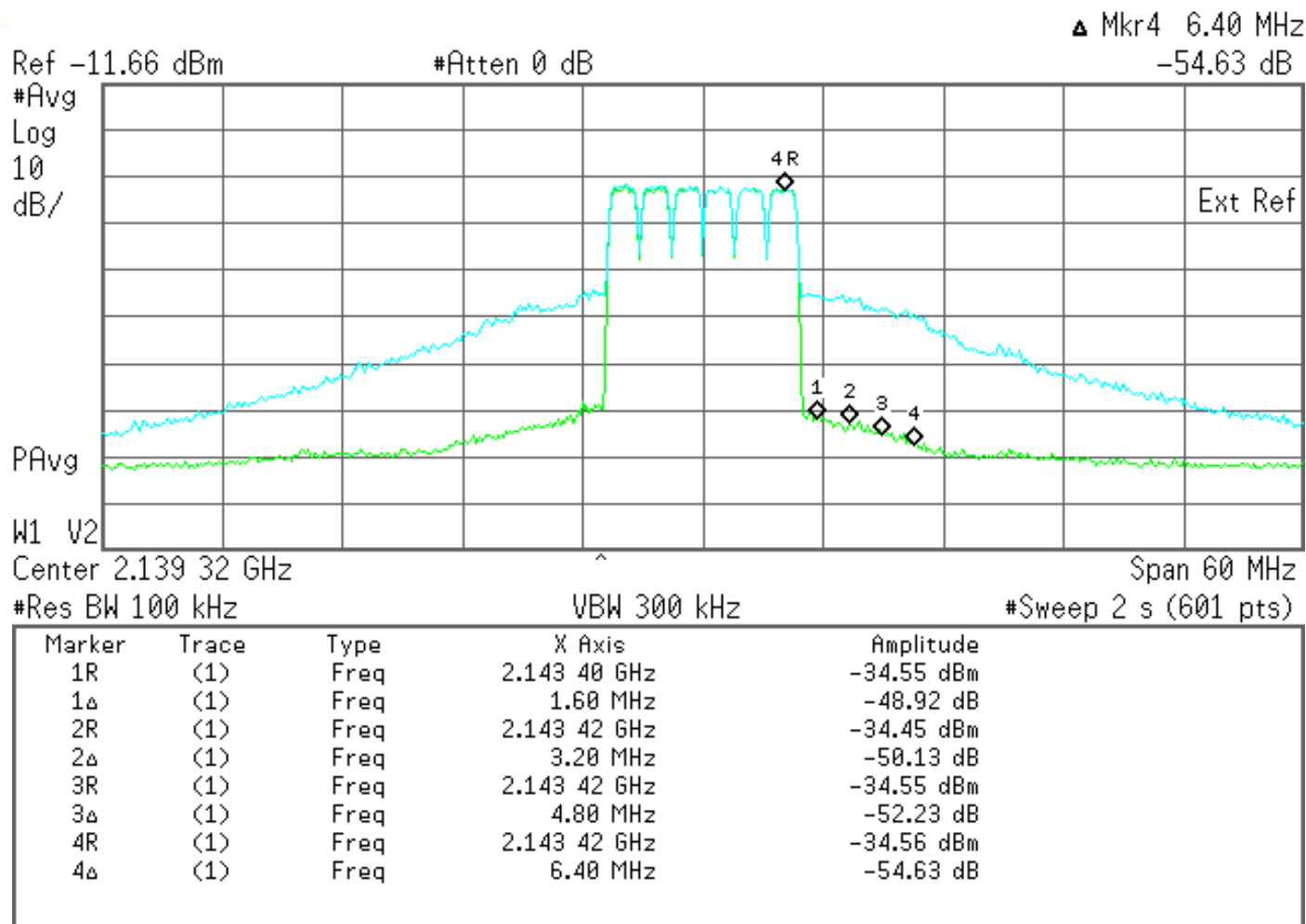
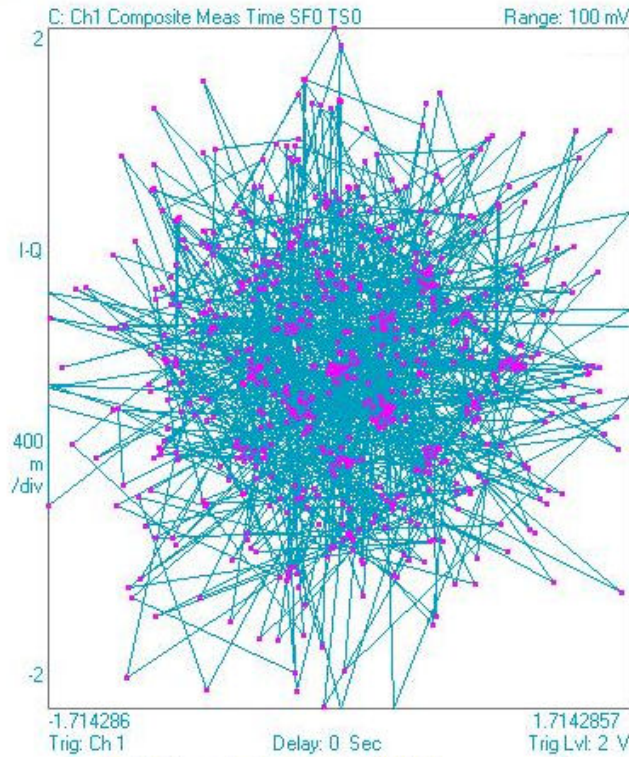


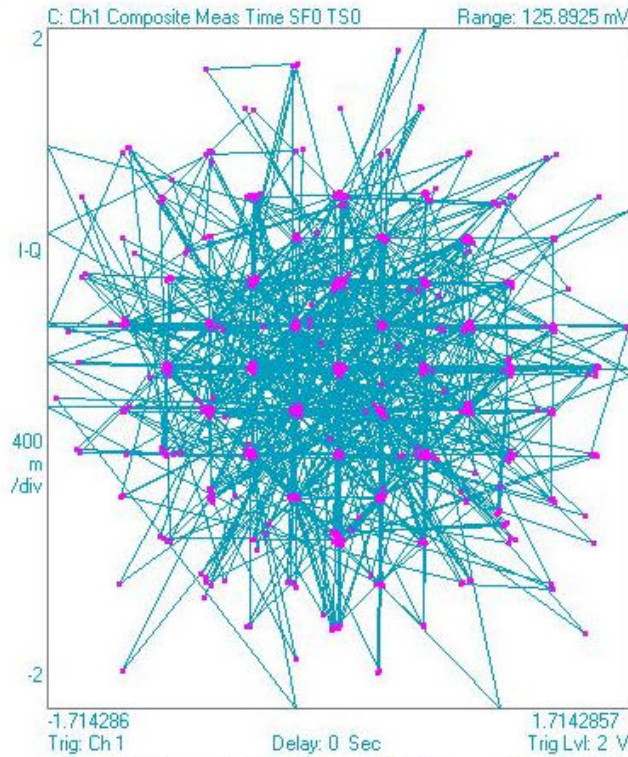


Figure 10-B: TD-SCDMA: Pre-DPD (left) and post-DPD (right) Constellation plots for 46dBm Pout, 8dB PAR



D: Ch1 Composite Error Summary SF0 TS0 Range: 100 mV

Rho	= 0.98641			
EVM	= 11.691	%rms	45.300	% pk at chip 193
Mag Err	= 9.0153	%rms	-43.078	% pk at chip 193
Phase Err	= 22.855	deg	175.63	deg pk at chip 735
Freq Err	= -3.1165	Hz		
Quad Err	= 468.01	mdeg		
			IQ Offset	= -51.867 dB
			Gain Imb	= -0.002 dB
Pk Act CDE	= -33.286	dB		
Pk CDE	= -33.286	dB		



D: Ch1 Composite Error Summary SF0 TS0 Range: 125.8925 mV

Rho	= 0.99716			
EVM	= 5.3293	%rms	31.250	% pk at chip 177
Mag Err	= 4.3263	%rms	-28.240	% pk at chip 504
Phase Err	= 20.149	deg	-173.73	deg pk at chip 156
Freq Err	= -424.62	mHz		
Quad Err	= -824.67	mdeg		
			IQ Offset	= -58.762 dB
			Gain Imb	= 0.026 dB
Pk Act CDE	= -39.392	dB		
Pk CDE	= -39.392	dB		



Figure 11: MC-GSM: Pre (blue) and post (green) DPD spectral plots at 42dBm Pout and 6.3dB PAR

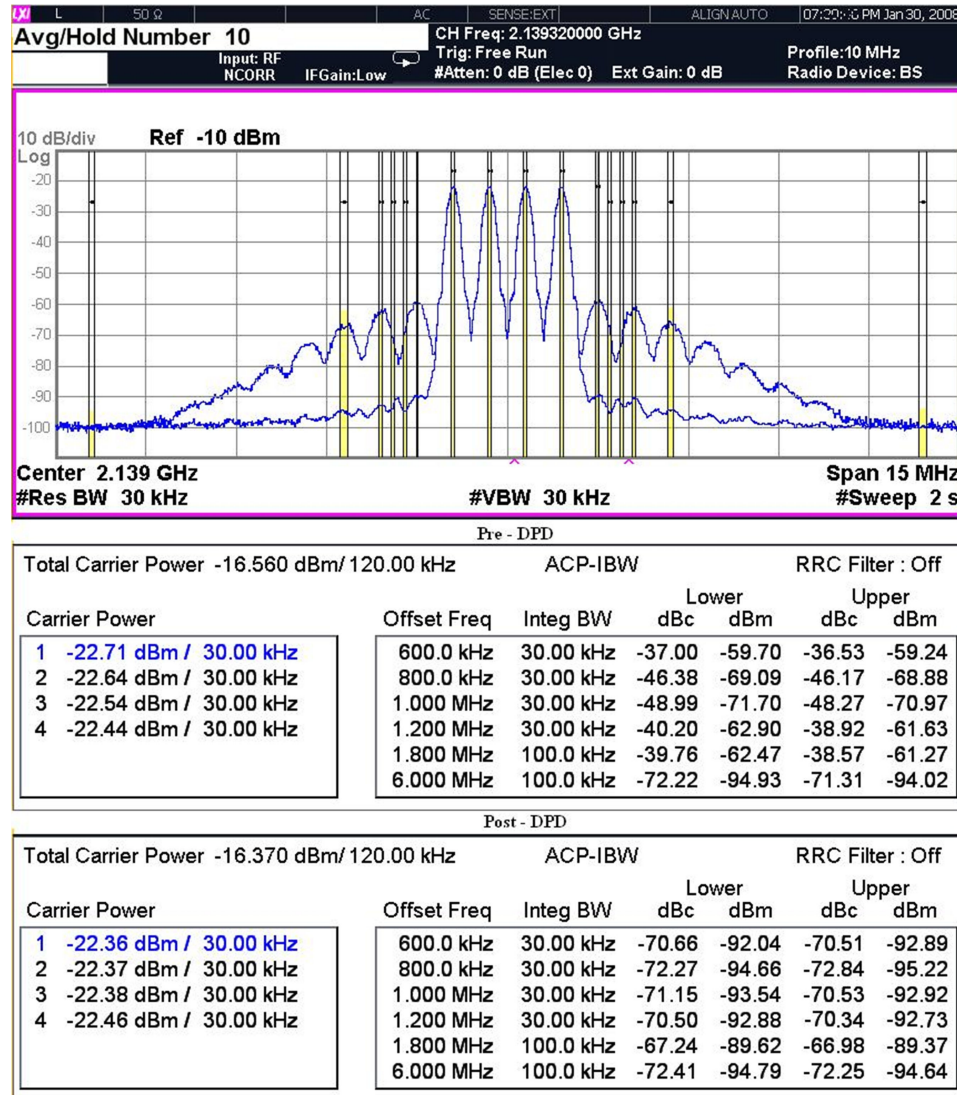
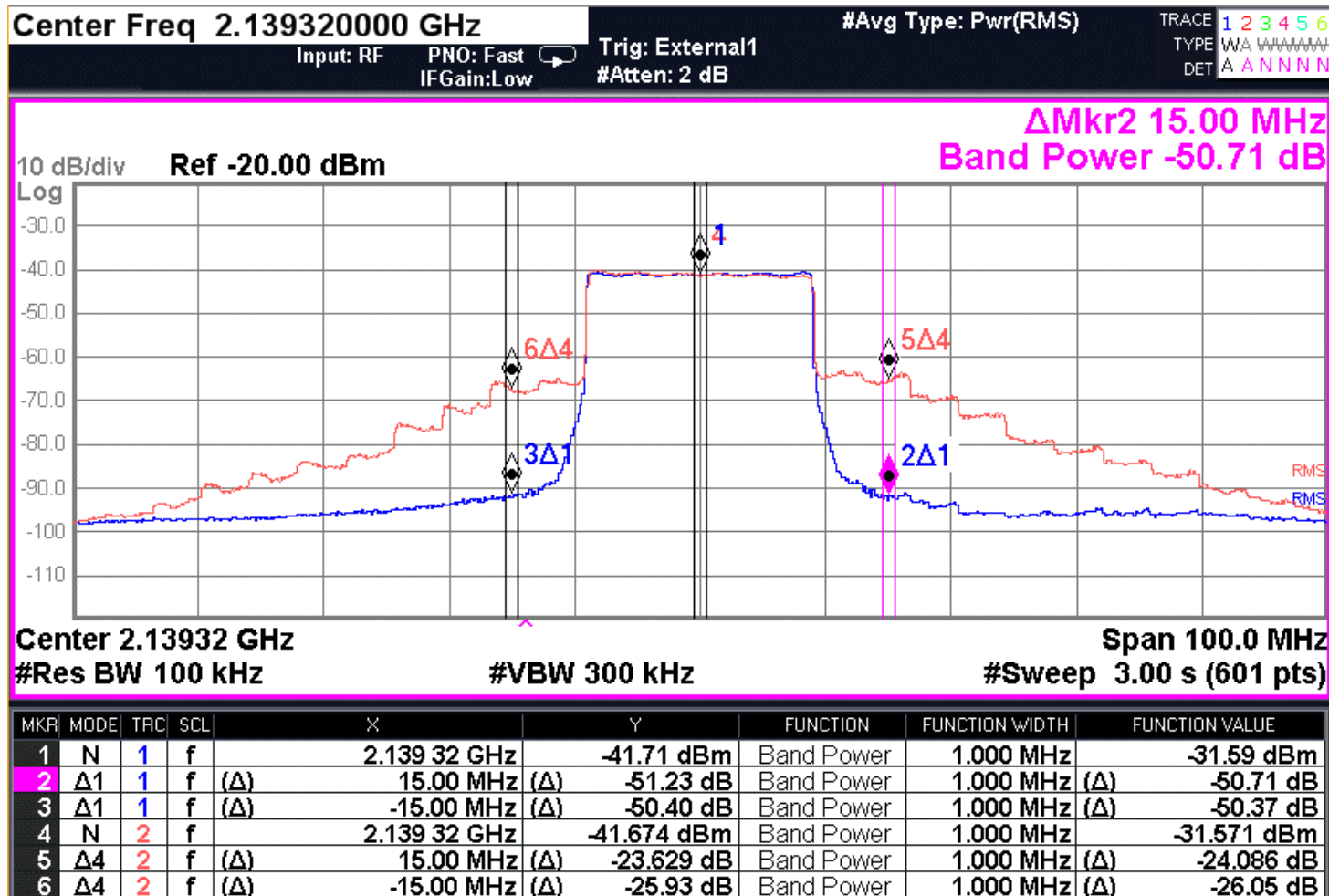




Figure 12: LTE: Pre(red) and post(blue) DPD spectrums at 43.5dBm Pout and 7.5dB PAR





Summary

The pre-distortion scheme presented here is shown to be highly efficient at improving amplifier linearity and power efficiency.

The GC5322 integrated transmit solution presented here not only provides a significant environmental benefit, but also provides a substantial cost savings both in capital expenditure and operational expenditure for next generation base stations.

By providing an integrated DUC-CFR-DPD signal processing hardware solution, along with optimized DSP-based adaptation software and a proven reference RF board design, faster time to market can be achieved.