Establishing the Minimum Reverse Bias for a p-i-n Diode in a High-Power Switch

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Abstract—An important circuit design parameter in a high-power p-i-n diode application is the selection of an appropriate applied dc reverse bias voltage. Until now, this important circuit parameter has been chosen either conservatively, using the magnitude of the peak RF voltage, or by empirical trials to determine a possible lower value. This paper explores the reverse bias requirement for a p-i-n diode operating in a high-power RF and microwave environment. It demonstrates that the minimum reverse bias voltage is equivalent to the p-i-n diode's self-generated dc voltage under similar RF conditions. A concise expression for this self-generated voltage is developed and experimentally verified and will assist the design engineer in more accurately selecting an appropriate minimum value for the applied reverse bias voltage setting.

I. INTRODUCTION

A FUNDAMENTAL property of a p-i-n diode is its ability to control large radio frequency (RF) and microwave signals with much lower values of dc current and voltage. While there are design rules for selecting a minimum level of forward current based on allowable ohmic loss and distortion requirements [1], [2], there are no existing design rules on which to base the selection of the minimum level of applied dc reverse bias voltage.

The instantaneous voltage across the p-i-n diode (both RF and dc) must never exceed its avalanche breakdown voltage (V_{BR} in Fig. 1(a)), where high reverse current densities may cause p-i-n diode failure. Safe operation will result if the instantaneous voltage never forces the p-i-n diode into forward conduction or into avalanche breakdown (Fig. 1(b)). However, this requires that the applied dc voltage be at least equal to the peak RF voltage and that the breakdown voltage be at least twice the peak RF voltage (V_{RF}). In many applications, high applied reverse bias voltages are often not available or are too expensive to implement. Frequently, p-i-n diodes are operated in the so-called conditionally safe region, where an instantaneous excursion of voltage into the forward conducting region may be tolerated (Fig. 1(c)). If a dc reverse bias voltage in this region is chosen, circuit

performance parameters such as loss, distortion, and reliability must not be compromised. It is this conditionally safe region where most high-power (greater than 1 kW) p-i-n diode switches are designed to operate. The applied dc reverse bias voltage must be large enough to prevent excessive conduction during the positive portion of the RF signal. If excessive conduction does occur, the p-i-n diode loss will increase and the diode will be subject to failure.

In the absence of any theory or analytic design guidelines, the design engineer may choose a dc bias voltage equal to the peak RF voltage, resulting in extremely conservative and costly designs; more frequently, however, the design is based on empirically matching a p-i-n diode to an available voltage. This paper presents a guide for the p-i-n diode circuit designer, similar to the forward bias case, for selecting a minimum applied reverse bias voltage based on diode and circuit operating parameters.

The investigation of the relationship of the reverse bias requirement was prompted by experimental observations of p-i-n diode distortion under zero applied bias open circuit conditions, using a test circuit of the type shown in Fig. 2. The 10^9 Ω resistor was inserted in the voltmeter line to increase the effective voltmeter internal resistance from its nominal 10^7 Ω value to better approximate an open circuit across the diode. The voltage read was then approximately 1% of the diode voltage.

A self-generated reverse bias dc voltage was developed across the p-i-n diode that allowed the diode to operate in its high-impedance state with good stability. The magnitude of the self-generated dc voltage was influenced primarily by the peak RF voltage level, the frequency, and the thickness of the i region. Upon application of an equivalent externally applied dc bias, the distortion generated was identical to the self-generated dc voltage. However, when the applied dc voltage was lower than the self-generated voltage, unstable performance would occur, manifested by large increases in distortion signals and by heating of the p-i-n diode, which often led to device failure. Published experimental results by other investigators [3] show similar device and circuit parameters that affect the degree of forward conduction in the p-i-n diode.

An analysis of the p-i-n diode leading to a concise expression for the safe minimum operating dc reverse bias voltage is presented. The expression indicates how the

UNSAFE BIAS
$V_{DC} + |VRF| > V_{BR}$

(a)

SAFE BIAS
$V_{DC} + VRF < V_{BR}$
$V_{DC} \geqslant VRF$

(b)

CONDITIONALLY SAFE BIAS
$V_{DC} + VRF < V_{BR}$
$V_{DC} < VRF$

(c)
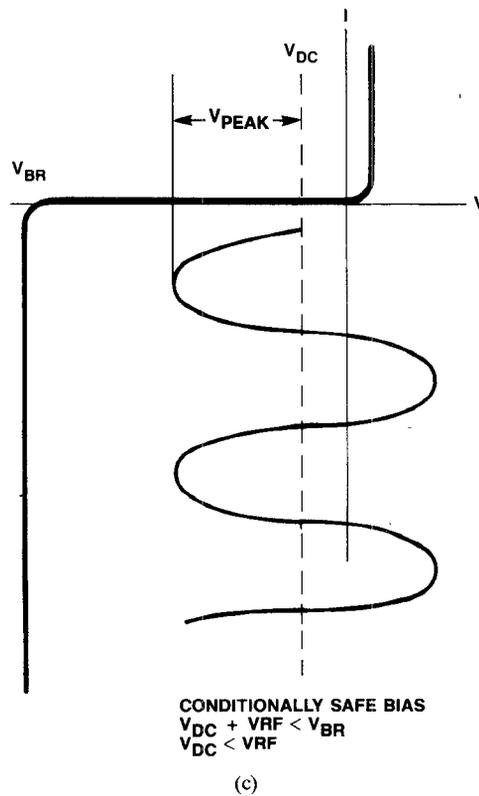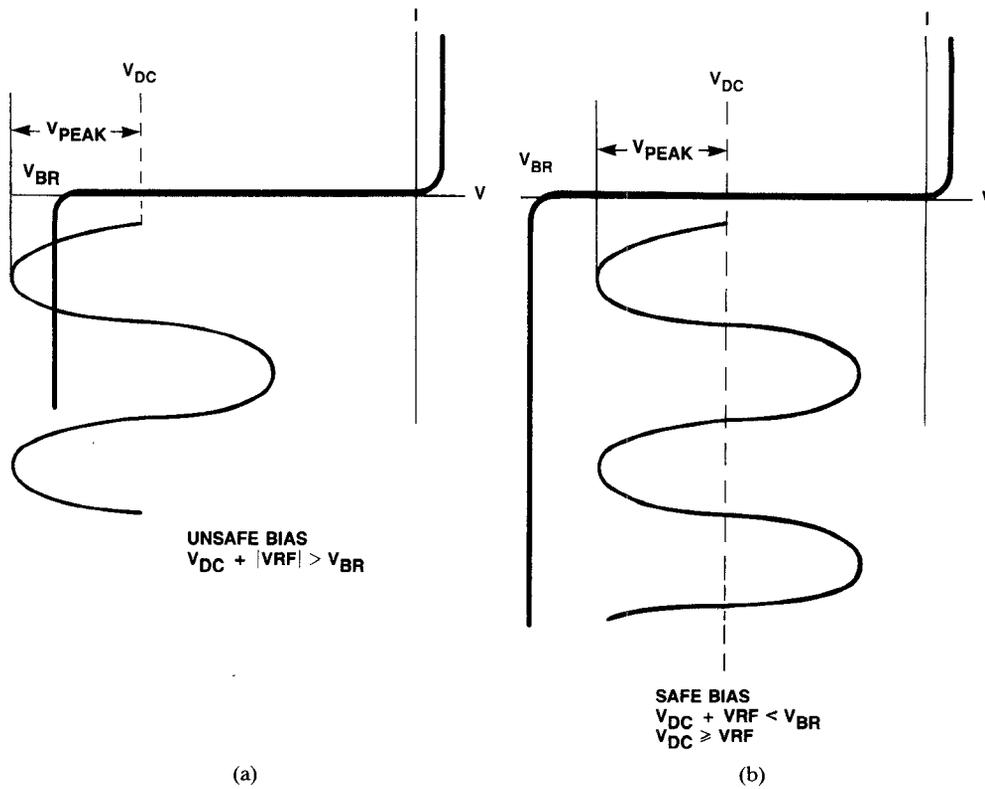
Fig. 1.   (a) Unsafe operating region, (b) safe operating region, and (c) conditionally safe operating region for the reverse-biased p-i-n diode.
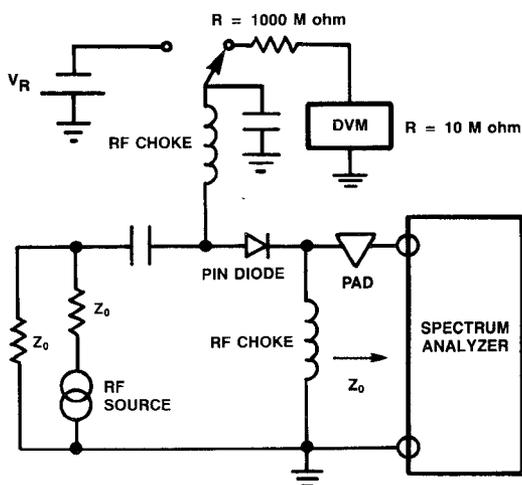
Fig. 2.   Test set used for measurement of the self-generated dc voltage of p-i-n diodes.

p-i-n diode i region and circuit parameters such as frequency, duty factor, and peak RF voltage affect the magnitude of the minimum reverse bias voltage. The derived expression is verified using experimental measurements of the developed open-circuit zero bias voltage across a variety of p-i-n diode geometries and circuit operating conditions. An application example is also presented.

II. ANALYSIS

In the presence of an applied RF or microwave signal, an ideal rectifier diode will instantaneously conduct when the RF voltage places the diode into its forward bias state. In most applications where a reverse-biased p-i-n diode is used, forward conduction in the p-i-n diode can be unconditionally avoided if the diode is reverse biased such that the peak RF voltage swing remains between the device turn-on voltage (typically 0.7 V for silicon diodes) and the reverse bias breakdown voltage. This requirement is the basis for a conservative "worst case" p-i-n diode dc reverse bias point, where $|V_{DC}| = |V_{RF}|$.

In real circuit applications, however, the p-i-n diode does not show the same instantaneous turn-on time as the ideal rectifier diode. Rather, the RF signal must be positive for a finite amount of time before the diode starts conducting in the forward direction. This turn-on time is the time required for the i region to fill with charge carriers (both holes and electrons from the heavily doped end regions) during the forward cycle of the applied RF signal. Depending on the frequency, the peak RF voltage level ($|V_{RF}|$), and the i-region thickness (W), the excursion into the forward direction of the RF signal may be too short to allow sufficient time for the carriers to completely traverse the i region, hence preventing the p-i-n diode from entering its conducting state [4]–[6]. The diode will then act as a lossy capacitor with its capacitance dependent on the i-region thickness and p-i-n diode cross section. In this case no externally applied dc reverse bias voltage is necessary to prevent forward conduction since

the i-region stored charge is never established during the positive portion of the RF signal. The conducting state of the p-i-n diode is therefore never achieved.

Between these two limiting cases lies an operating region for the p-i-n diode where prevention of forward conduction of the diode may be achieved by reverse biasing the diode at a voltage less than the peak RF voltage. Experiments [7] have shown that the dc voltage developed by the p-i-n diode in its open-circuit, zero bias state is directly related to the dc reverse bias voltage needed to prevent significant forward conduction in the p-i-n diode.

The analysis of the developed open-circuit, zero bias voltage in p-i-n diodes is based on the existence of both conduction and displacement currents flowing through the p-i-n diode [8]:

$$J(t) = 2nqv + \epsilon \, dE/dt \qquad (1)$$

where $J(t)$ is the total current density, n is the i-region carrier density (where the density of holes equals the density of electrons to simplify the analysis), q is the elemental electronic charge, v is the drift velocity of the charge carriers (assuming equal hole and electron drift velocities), ϵ is the dielectric permittivity, and E is the electric field. Assuming that the flux density D is uniform through the diode's cross section (A) yields

$$\oint D \, dA = \int \rho \, dV = DA = QA\epsilon E \qquad (2)$$

where Q is the sum of both the RF and dc components of the i-region stored charge and ρ is the total i-region charge density. Substituting the results of (2) into (1) shows that the total current density, $J(t)$, may be written as

$$J(t) = 2nqv + (1/A) \, dQ/dt. \qquad (3)$$

A p-i-n diode with i-region thickness W then, using (3), has a total diode current of

$$I = I_{RF} + I_{dc} = Q/T + dQ/dt \qquad (4)$$

where the i-region transit time, T, is defined as $W/2v$ [8]. If a time variation of the form $e^{j\omega t}$ for all quantities is assumed, the RF component of the total diode current may be written as

$$I_{RF} = Q_{RF}(1 + j\omega T)/T \qquad (5)$$

and the dc component of the total diode current may be written as

$$I_{dc} = Q_{dc}/T. \qquad (6)$$

The resistance (or conductance) of the p-i-n diode can be computed from the amount of stored charge in the i region [3]. The RF and dc voltages are determined from these resistances and the corresponding currents:

$$V_{RF} = \left(\frac{W^2}{2\mu Q_{RF}} \right) I_{RF} = \left(\frac{W^2}{2\mu} \right) \frac{1 + j\omega T}{T} \qquad (7a)$$

and

$$V_{dc} = \left(\frac{W^2}{2\mu Q_{dc}} \right) I_{dc} = \left(\frac{W^2}{2\mu T} \right) \qquad (7b)$$

where μ is the mobility (again, assuming equal hole and electron mobility values for simplicity). The magnitude of the ratio of these two voltages may be written using (7) and the definition for the transit time as

$$\left|\frac{V_{dc}}{V_{RF}}\right| = \frac{1}{\left[1+(\pi fW/v)^2\right]^{1/2}}. \quad (8)$$

The transit time, T, is a function of the carrier drift velocity, v, and, in turn, a function of the electric field. In semiconductors such as silicon, the carrier velocity increases approximately linearly with applied electric field for only relatively low values of electric field (Fig. 1). At higher electric field values, the interaction of the charge carriers with the semiconductor lattice atoms serves to limit the velocity of the carriers to a value termed the saturation velocity, v_{sat}. This velocity varies with carrier type, semiconductor material, and temperature, but is approximately 10^7 cm/s for electrons in silicon at 290 K [9]. An approximation of the electric field dependence on velocity which includes the effects of velocity saturation may be written as [10]

$$v(E) = \frac{2\mu E}{\left[1+\sqrt{1+\left(\dfrac{2\mu E}{v_{sat}}\right)^2}\right]} \quad (9)$$

where the term μ is the low-field carrier mobility.

The p-i-n diode is often used in high-pulsed-power applications and is able to handle kilowatts of power operating in this mode. The rms value of the electric field under these conditions is needed to estimate the carrier drift velocity (9) and may be computed assuming a half-wave-rectified pulsed RF waveform where the carrier frequency (f) is much larger than the inverse of either the pulse period (T_p) or the pulse duration (T_D). Assuming that the electric field across the i region of the p-i-n diode may be approximated by $E = V_{RF}/W$, then the rms value of the electric field, E, may be calculated as

$$E = V_{RF}\sqrt{D} \sqrt{\left[\frac{1}{\pi^2}+\frac{1}{8}\right]} \Big/ W \quad (10)$$

where $D = T_D/T_P$ is the RF pulse duty cycle. The dc voltage developed across the p-i-n diode may be written using (8), (9), and (10) as

A further simplification may be used on (12) if the applied RF voltage is low enough so that velocity saturation does not occur:

$$|V_{dc}| = \frac{|V_{RF}|}{\left[1+\left(0.0285f_{MHz}W_{mil}^2/V_{RF}\sqrt{D}\right)^2\right]^{1/2}}. \quad (13)$$

At low frequency and/or for diodes with thin i regions, the developed dc voltage, $|V_{dc}|$, approaches the peak RF voltage, approximating the ideal behavior of a pn junction diode. For higher frequencies or thicker i regions, however, the dc voltage developed decreases as $1/f$ for a given RF voltage. The developed dc voltage will then decrease by increasing the i-region thickness. Increasing the i-region thickness effectively increases the transit time proportionally since at high RF voltages the carrier velocity is limited to its saturation value, v_{sat}. Fig. 3 illustrates the dependence of the ratio $|V_{dc}|/|V_{RF}|$ on the rms value of the applied RF electric field ($E = 0.475|V_{RF}|\sqrt{D}/W$) with the factor $fW^2/D^{1/2}$ as a parameter. A significant reduction in the developed dc voltage is indicated for low peak RF electric fields (low applied $|V_{RF}|$), high-frequency operation, large i-region widths (W), and short duty cycles. At large RF voltages, the dc voltage developed approaches the limiting factor

$$|V_{dc}| = \frac{|V_{RF}|}{\sqrt{1+\left(\dfrac{\pi fW}{v_{sat}}\right)^2}}. \quad (14)$$

III. EXPERIMENTAL RESULTS

Experimental measurements of the dc self-generated voltage were performed using a test set similar to that shown in Fig. 2. This test set simulates the isolating arm (reverse bias p-i-n diode) of a SP2T p-i-n diode in each arm. Measurements were made at power levels up to 100 W at frequencies from 1 to 60 MHz and duty factors from 0.07 to 1.0. The p-i-n diode specimens selected had i-region widths ranging from 50 to 200 μm and encompassed various cross sections and carrier lifetime values. Fig. 4 graphically illustrates a comparison between experimental measurements of the ratio of the peak RF voltage

$$|V_{dc}| = \frac{|V_{RF}|}{\left[1+\left[\pi fW^2/0.95\mu V_{RF}\sqrt{D}\left[1+\sqrt{1+\left[0.95\mu V_{RF}\sqrt{D}/Wv_{sat}\right]^2}\right]\right]^2\right]^{0.5}}. \quad (11)$$

Equation (11) may be simplified if one assumes a carrier mobility of $\mu = 0.15$ cm^2/V-s and the previously mentioned value of v_{sat}:

$$|V_{dc}| = \frac{|V_{RF}|}{\left[1+\left[0.0142f_{MHz}W_{mil}^2/V_{RF}\sqrt{D}\left[1+\sqrt{1+\left[0.056V_{RF}\sqrt{D}/W_{mil}\right]^2}\right]\right]^2\right]^{0.5}}. \quad (12)$$
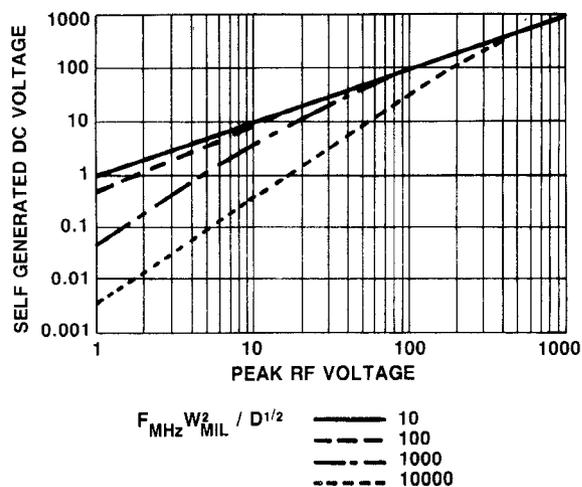
Fig. 3. Graph of the magnitude of the self-generated dc voltage versus the magnitude of the peak RF voltage with the term $f_{MHz}W_{mil}^2/\sqrt{D}$ as a parameter.
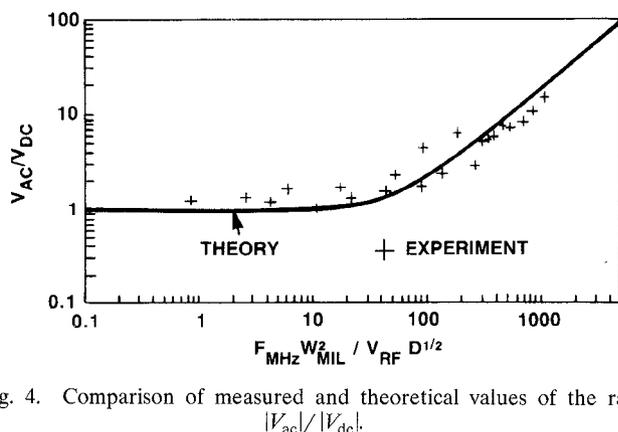
Fig. 4. Comparison of measured and theoretical values of the ratio $|V_{ac}|/|V_{dc}|$.

to self-generated dc voltage ($|V_{RF}|/|V_{dc}|$) and the expression for the ratio indicated by (12).

A significant experimental observation indicates that the p-i-n diode may be operated at high RF power without applying any external dc bias. The p-i-n diode here is operating in a zero bias open-circuit mode where the self-generated voltage becomes the reverse bias. To operate in the open-circuit mode, any external resistance across the diode must be very high, generally higher than 10^8 Ω. Typical levels of harmonic distortion in this mode were approximately 20 dB below the carrier.

Upon application of an external dc reverse bias at identical values of the self-generated dc voltage, the distortion measured was identical. When the applied dc reverse bias was increased slightly, often as little as 10 V higher than the self-generated voltage, the distortion improved significantly, by as much as 60 dB below carrier. If the applied reverse voltage was lower that the self-generated dc voltage, the distortion would degrade and the loss would increase, often leading to p-i-n diode failure. The dependence of reverse bias distortion on increasing reverse bias is consistent with observations and experiments
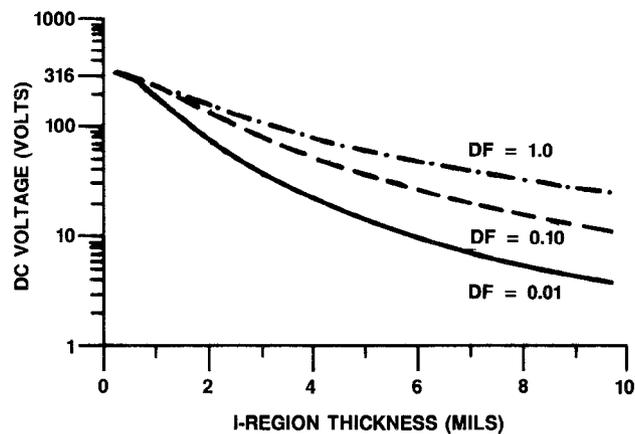
Fig. 5. Calculated generated dc reverse bias voltage versus i-region thickness and duty cycle for a 1 kW signal at 1 GHz.

previously reported by the authors [11]. It was also observed that the time it took the self-generated voltage to reach it final value was virtually instantaneous upon the initial application of RF power. However, when the RF power was changed, there appeared a time lag of as much as several seconds until the self-generated dc voltage stabilized and reached its new final value.

IV. APPLICATIONS EXAMPLE

As a result of this study, the designer may now analytically determine the minimum dc reverse bias requirement for a p-i-n diode in a high-power RF environment. It also affirms that the value of the dc voltage may be significantly lower than the peak RF voltage. The following example will illustrate this. Consider a p-i-n diode operating as a switch element at 1 GHz with a 1 kW signal ($|V_{RF}| = 316.2$ V across 50 Ω). Fig. 5 shows the calculated value (using (12)) of the generated reverse bias voltage as a function of i-region thickness and RF duty cycle. For p-i-n diodes with i-region thicknesses less that approximately 1 mil (25 μm), an external dc reverse bias equal to the peak RF voltage is required, regardless of duty cycle. This reverse bias requirement is relaxed, however, for thicker p-i-n diodes and low RF duty cycles (D) so that a 10 mil (250 μm) diode requires at most 35 V reverse bias to keep within the conditionally safe reverse bias region under any duty cycle. The figure shows that, in general, p-i-n diodes with thicker i regions require lower dc reverse voltages and would therefore appear preferable to thinner diodes. It should be noted, however, that thicker p-i-n diodes may also have higher forward resistance and will switch at a slower speed.

V. CONCLUSIONS

In many situations, the design engineer is unsure of the exact RF voltage stress on the p-i-n diode or its i-region width. The experimental method described in this paper may also be used to measure the self-generated dc voltage. This value may then be considered as the minimum

applied reverse bias voltage that will bias the diode in the "conditionally safe" region. In many situations the dc voltage established must be able to support RF signals where the SWR of the load termination may increase to a large value. Under this situation, the RF voltage will be double that of a perfectly matched circuit. In applying (12) or (13) the inserted value of RF voltage must reflect the peak value at maximum voltage stress.

Another benefit of biasing a p-i-n diode in the conditionally safe region may be used in the screening of devices. Depending on the desired application, the devices may be screened at a voltage level significantly below the avalanche breakdown voltage, increasing the reliability and lowering the cost of p-i-n diodes.

It would be a valuable contribution if a circuit technique could be devised that would make it possible, by applying only a small incremental dc reverse voltage to the self-generated voltage, to obtain distortion performance similar to that obtained when applying the full dc reverse voltage. This would significantly simplify the design and lower the cost of the higher voltage p-i-n diode drivers now being used in higher power switches and phase shifters.

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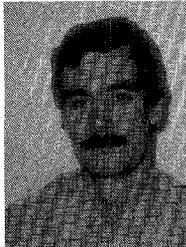
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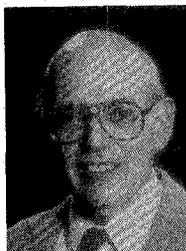
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