

**IT MAY SEEM LIKE A SIMPLE TASK TO MODIFY YOUR OP-AMP DESIGN TO WORK FROM A SINGLE VOLTAGE POWER SUPPLY, BUT THE CHANGE IN PERFORMANCE WILL SURPRISE YOU.**

# Demystifying single-supply op-amp design

**B**ATTERY-POWERED OP-AMP applications, such as those found in automotive and marine equipment, have only a single available power source. Other applications, such as computers, may operate from the ac power lines but still have only a single polarity power source, such as 5 or 12V dc. Therefore, it is often a practical necessity to power op-amp circuits from a single polarity supply. But single-supply operation has its drawbacks: It requires additional passive components in each stage and, improper execution of the design can lead to serious instability problems.

Single-supply applications have inherent problems that dual-supply op-amp circuits often overcome. The fundamental problem is that an op amp is a dual-supply device, so you must employ biasing using external components to center the op amp's output voltage at midsupply. This approach allows the maximum input and output voltage swing for a given supply voltage. In some low-gain applications having low input signals, the op amp's output can be only 2 or 3V above ground. But in most cases, you must avoid clipping, and thus you must center the output around midsupply.

The circuit of **Figure 1** shows a simple single-supply biasing method. This noninverting, ac-coupled, amplifier circuit uses a resistor divider with two biasing resistors,  $R_A$  and  $R_B$ , to set the voltage on the noninverting input equal to  $V_S/2$ . The input signal,  $V_{IN}$ , is capacitively coupled to the noninverting input terminal.

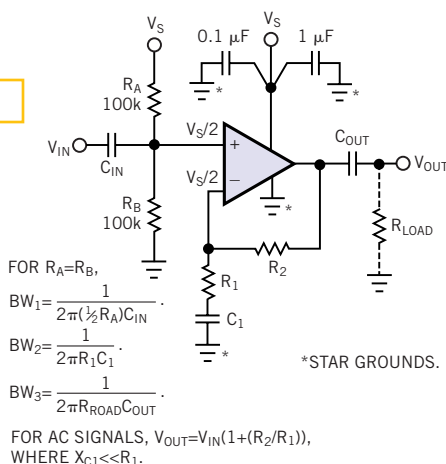
This simple circuit has some serious limitations. The first limitation is that the op amp's power-supply rejection is almost entirely missing, because any change in supply voltage directly changes the  $V_S/2$  biasing voltage, which the resistor divider sets. Power-supply rejection is an important and frequently overlooked op-amp characteristic. Normally high power-supply rejection that any modern op amp provides greatly reduces the problem of ac signals and power-supply hum feeding into the op amp via

its supply line. Because a 1V change on the supply line causes a 0.5V change at the output of the divider, the circuit's power-supply rejection is only 6 dB. Even worse, instability often occurs in circuits in which the op amp must supply large output currents into a load. Unless the power supply is well-regulated and well-bypassed, large signal voltages appear on the supply line. With the op amp's noninverting input referenced directly off the supply line, these signals will feed directly back into the op amp, often initiating instability. The use of careful layout, multicapacitor-power-supply bypassing, star grounds, and a pc-board power plane may provide circuit stability. However, it is easier to reintroduce some reasonable amount of power-supply rejection into the design.

## RESISTOR-DIVIDER BIASING

One way to increase power-supply rejection is to modify the circuit (**Figure 2**). Capacitor  $C_2$  now bypasses the tap point on the voltage divider, restor-

**Figure 1**



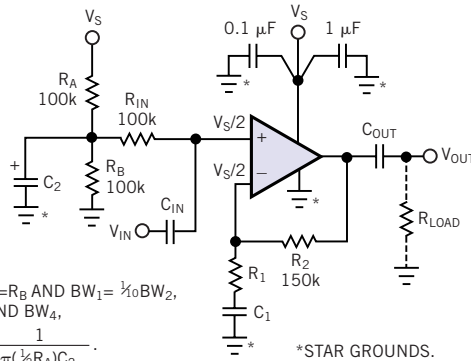
**A first-cut single-supply op-amp design yields a potentially unstable circuit.**

ing some ac power-supply rejection. Resistor  $R_{IN}$  provides a dc return path for the  $V_S/2$  reference voltage and sets the circuit's ac input impedance. Many published applications circuits show a 100/100-k $\Omega$  voltage divider for  $R_A$  and  $R_B$  with a 0.1- $\mu$ F or similar capacitance value for  $C_2$ . However, the parallel combination of  $R_A$  and  $R_B$  and  $C_2$  set the -3-dB bandwidth of this network, which is equal to:

$$-3\text{dB BW} = 1/2\pi (50,000) (0.1 \times 10^{-6}\text{F}) = 30 \text{ Hz.}$$

Instability can still occur, because the circuit has essentially no power-supply rejection for low frequencies. So, any signals lower than 30 Hz on the supply line can easily find their way back to the positive input of the op amp. A practical solution to this

**Figure 2**



FOR  $R_A=R_B$  AND  $BW_1 = \frac{1}{2} BW_2$ ,  
 $BW_3$ , AND  $BW_4$ ,

$$BW_1 = \frac{1}{2\pi(\frac{1}{2}R_A)C_2}.$$

$$BW_2 = \frac{1}{2\pi R_{IN}C_{IN}}.$$

$$BW_3 = \frac{1}{2\pi R_1 C_1}.$$

$$BW_4 = \frac{1}{2\pi R_{LOAD}C_{OUT}}.$$

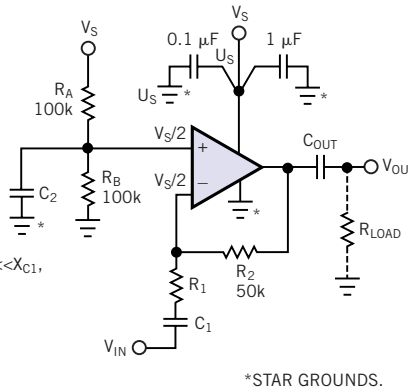
FOR AC SIGNALS,  $V_{OUT} = V_{IN}(1 + (R_2/R_1))$ ,  
 WHERE  $X_{C1} \ll R_1$ .

TO MINIMIZE INPUT-BIAS-CURRENT ERRORS,  
 $R_2$  SHOULD EQUAL  $R_{IN} + (\frac{1}{2}R_A)$ .

\*STAR GROUNDS.

**One way to increase power-supply rejection is to modify the circuit using a decoupled op-amp-biasing circuit.**

**Figure 3**



FOR  $R_A=R_B$  AND  $X_{C2} \ll X_{C1}$ ,

$$BW_1 = \frac{1}{2\pi(\frac{1}{2}R_A)C_2}.$$

$$BW_2 = \frac{1}{2\pi R_1 C_1}.$$

$$BW_3 = \frac{1}{2\pi R_{LOAD}C_{OUT}}.$$

FOR AC SIGNALS,  $V_{OUT} = V_{IN}(R_2/R_1)$ ,

WHERE  $X_{C1} \ll R_1$ .

TO MINIMIZE INPUT-BIAS-CURRENT ERRORS,  
 $R_2$  SHOULD EQUAL  $\frac{1}{2}R_A$ .

\*STAR GROUNDS.

**You can also add decoupling to a single-supply inverting amplifier circuit.**

and other factors can become complex. However, you can greatly simplify the design by using a “cookbook” approach. For a common voltage-feedback op amp operating from a single 15 or 12V supply, a resistor divider using two 100-k $\Omega$  resistors is a reasonable compromise between supply-current consumption and input-bias current errors. You can reduce the resistors for a 5V supply to a lower value, such as 42 k $\Omega$ . In addition, some applications need to operate from the new 3.3V standard. For 3.3V applications, the op amp must be a rail-to-rail device, and you must bias it close to midsupply. You can further reduce the biasing resistors to approximately 27 k $\Omega$ .

Current-feedback op amps typically target high-frequency use; the lowpass filter that  $R_2$  and stray circuit capacitance form can severely reduce the circuit's 3-dB bandwidth. Therefore, current-feedback op amps normally need to use a low resistance value for  $R_2$ . An op amp such as the AD811, which targets use in video applications, typically will have optimum performance using a 1-k $\Omega$  resistor for  $R_2$ . Therefore, these high-speed applications need to use smaller resistor values in the  $R_A/R_B$  voltage divider to minimize input-bias-current errors. Unless the circuit must operate over

problem is to increase the value of capacitor  $C_2$ . It needs to be large enough to effectively bypass the voltage divider at all frequencies within the circuit's pass-band. A good rule of thumb is to set this pole at one-tenth the -3-dB input bandwidth, set by  $R_{IN}/C_{IN}$  and  $R_1/C_1$ . Even though the dc circuit gain is unity, you need to consider the op amp's input-bias currents. The  $R_A/R_B$  voltage divider adds considerable resistance in series with the op amp's positive input terminal, equal to the parallel combination of the two resistors. Maintaining the op amp's output close to midsupply requires balancing this resistance by increasing the resistance in the negative input terminal by an equal amount. Current-feedback op amps often have unequal input-bias currents, which further complicates the design.

A single-supply op-amp circuit design that considers input-bias current errors as well as power-supply rejection, gain, input- and output-circuit bandwidth,

**TABLE 1—TYPICAL COMPONENT VALUES FOR THE CIRCUIT OF FIGURE 2**

Gain	Input bandwidth (Hz)	Output bandwidth (Hz)	$C_{IN}$ ( $\mu$ F)	$R_1$ (k $\Omega$ )	$C_1$ ( $\mu$ F)	$C_2$ ( $\mu$ F)	$C_{OUT}$ ( $\mu$ F)	$R_{LOAD}$ (k $\Omega$ )
10	10	10	0.3	16.5	1.5	3	0.2	100
20	10	10	0.3	7.87	3	3	0.2	100
10	50	50	0.1	16.5	0.3	0.6	0.05	100
101	20	20	0.2	1.5	6.8	2	0.1	100

Notes:  $R_A=R_B=100 \text{ k}\Omega$ ,  $R_{IN}=100 \text{ k}\Omega$ , and  $R_2=150 \text{ k}\Omega$ .

Capacitance values are rounded off to next highest common value. Because the  $C_{IN}/R_{IN}$  pole and  $C_1/R_1$  poles are at the same frequency and both affect the input bandwidth, each capacitor is  $\sqrt{2}$  larger than it would otherwise be for a single pole RC-coupled input. The table lists a  $C_2$  value that provides a corner frequency of one-tenth that of the input bandwidth.

a wide temperature range, you can use a modern FET-input op amp instead of a bipolar device to reduce input-bias-current errors. In any case, balancing the resistance in the op amp's input terminals is still a wise precaution. Tables 1 and 2 provide typical component values for the circuits in figures 2 and 3 for several gains and 3-dB bandwidths.

**ZENER-DIODE BIASING**

Although the resistor-divider-biasing technique is low-cost and keeps the op amp's output voltage at  $V_S/2$ , the op amp's common-mode rejection depends entirely upon the RC time constant that  $R_A$ ,  $R_B$ , and  $C_2$  form. Using a  $C_2$  value that provides at least 10 times the RC time constant of the input RC coupling network,  $R_1/C_1$  and  $R_{IN}/C_{IN}$ , helps to ensure a reasonable common-mode-rejection ratio. With 100-k $\Omega$  resistors for  $R_A$  and  $R_B$ , you can keep practical values of  $C_2$  fairly small as long as the circuit bandwidth is high enough. However, another way to provide the necessary  $V_S/2$  biasing for single-supply operation is to use a zener-diode regulator (Figure 4). Current flows through resistor  $R_Z$  to the zen-

**TABLE 2—TYPICAL COMPONENT VALUES FOR THE CIRCUIT OF FIGURE 3**

Gain	Input bandwidth (Hz)	Output bandwidth (Hz)	$R_1$ (k $\Omega$ )	$C_1$ ( $\mu$ F)	$C_2$ ( $\mu$ F)	$C_{OUT}$ ( $\mu$ F)	$R_{LOAD}$ (k $\Omega$ )
10	10	10	2	8.2	0.5	0.2	100
20	10	10	1	20	0.5	0.2	100
10	50	50	2	2	0.1	0.05	100
100	20	20	1	8.2	0.3	0.1	100

Notes:  $R_Z=50$  k $\Omega$ , and  $R_A=R_B=100$  k $\Omega$ .

Capacitance values are rounded off to next highest common value. Because the  $C_1/R_1$  pole and  $C_2/R_A/R_B$  poles are at the same frequency, and both affect the input bandwidth, each capacitor is  $\sqrt{2}$  larger than it would otherwise be for a single-pole, RC-coupled input.

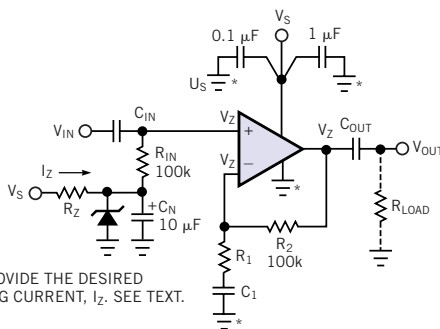
er diode. Capacitor  $C_N$  helps prevent any zener-generated noise from feeding into the op amp. Low-noise circuits may need to use a larger value for  $C_N$  than the specified 10  $\mu$ F.

Choose a zener diode that has an operating voltage close to  $V_S/2$ . Select resistor  $R_Z$  to provide a high enough zener current to operate the diode at its stable rated voltage and to minimize the zener output noise. It is also important to minimize power consumption and heating and to prolong the diode's life. Because the op amp's input current is essentially zero, it's a good idea to choose a low-power zener. A 250-mW device is best, but the more common 500-mW types are also acceptable. The ideal zener current varies with each manufacturer, but practical levels of 5  $\mu$ A for a 250-mW

diode and 5 mA for a 500-mW version are usually a good compromise for this application.

Within the operating limits of the zener diode, the circuit of Figure 4 basically restores the op amp's power-supply rejection. But this restoration comes at a price: The op amp's output is now at the zener voltage rather than at  $V_S/2$ . If the power-supply voltage drops, nonsymmetrical clipping can occur on large signals. Furthermore, the circuit now consumes more power. You also still need to consider input-bias currents. Resistors  $R_{IN}$  and  $R_Z$  should be close to the same value to prevent input bias currents from creating a large offset-voltage error. Figure 5 shows an inverting-amplifier circuit using the same zener-biasing method. You can use Table 3 with the cir-

**Figure 4**



SELECT  $R_Z$  TO PROVIDE THE DESIRED ZENER OPERATING CURRENT,  $I_Z$ . SEE TEXT.

$$R_Z = \frac{V_S - V_{ZENER}}{I_Z}$$

$$BW_1 = \frac{1}{2\pi R_{IN} C_{IN}}$$

$$BW_2 = \frac{1}{2\pi R_1 C_1}$$

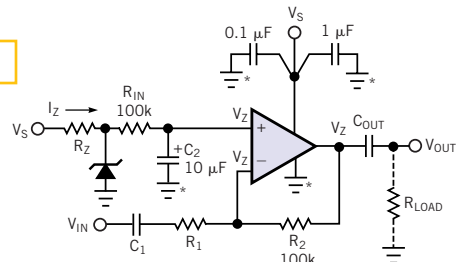
$$BW_3 = \frac{1}{2\pi R_{LOAD} C_{OUT}}$$

FOR AC SIGNALS,  $V_{OUT} = V_{IN}(1 + (R_2/R_1))$ , WHERE  $X_{C1} \ll R_1$ ,

TO MINIMIZE INPUT-BIAS-CURRENT ERRORS,  $R_Z$  SHOULD EQUAL  $R_{IN}$ .

**Zener-diode biasing also improves the power-supply rejection of this noninverting amplifier.**

**Figure 5**



SELECT  $R_Z$  TO PROVIDE THE DESIRED ZENER OPERATING CURRENT,  $I_Z$ . SEE TEXT.

FOR AC SIGNALS,  $V_{OUT} = V_{IN}(R_2/R_1)$ , WHERE  $X_{C1} \ll R_1$ ,

$$R_Z = \frac{V_S - V_{ZENER}}{I_Z}$$

$$BW_1 = \frac{1}{2\pi R_1 C_1}$$

$$BW_2 = \frac{1}{2\pi R_{IN} C_2}$$

$$BW_3 = \frac{1}{2\pi R_{LOAD} C_{OUT}}$$

TO MINIMIZE INPUT-BIAS-CURRENT ERRORS,  $R_Z$  SHOULD EQUAL  $R_{IN}$ .

**The same zener-diode-biasing arrangement also improves an inverting amplifier design.**

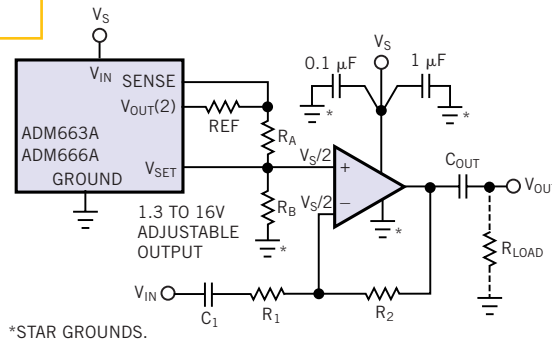
cuits in figures 4 and 5 to provide practical  $R_z$  resistor values for use with some common zener diodes. Note that for the lowest possible circuit noise, select the zener-diode current by referring to the zener product data sheet. Tables 4 and 5 provide practical component values for figures 4 and 5 for several circuit gains and bandwidths.

A 1.65V biasing voltage is necessary for op-amp circuits operating from the new 3.3V standard; however, zener diodes are commonly available only with voltages as low as 2.4V. The easiest way to provide this biasing voltage is to use a linear voltage regulator, such as the ADM663A or ADM666A devices (Figure 6). Although a zener diode is usually the cheapest voltage regulator available, a linear voltage regulator has lower drift over temperature and less noise than a zener. Select resistors  $R_A$  and  $R_B$  to provide the desired  $V_s/2$  voltage reference, which the AD663A data sheet describes.

**BATTERY-POWERED, DC-COUPLED CIRCUITS**

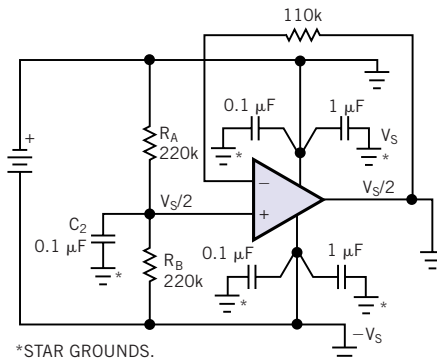
With the use of suitably large input and output coupling capacitors, an ac-coupled circuit can operate at frequencies well below 1 Hz, but some applications require a true dc response. Battery-powered applications permit the use of a “phantom-ground” circuit (Figure 7). This circuit provides dual-supply voltages, both positive and negative with respect to ground, from a single battery. An op amp buffers the output of a  $V_s/2$  voltage divider. If you use a low-voltage battery, such as 3.3V, the op amp should be a rail-to-rail device and able to operate effectively

**Figure 6**



You can use a linear-voltage-regulator-biasing circuit for low-voltage op-amp designs.

**Figure 7**



An op amp provides a “phantom ground” for battery-powered, dc-coupled applications.

from this supply voltage. The op amp also must be able to supply an output current large enough to power the load circuit. Capacitor  $C_2$  bypasses the voltage-divider output enough to prevent any resistor noise from feeding into the op amp. This capacitor need not provide power-supply rejection because the load current flows directly to ground, so any signal currents flow equally from both sides of the battery. Select resistors  $R_A$

and  $R_B$  to provide the desired  $V_s/2$  voltage reference that the AD663A data sheet shows.

**NOISE AND TURN-ON TIME**

Some op-amp applications need a low-noise amplifier, and low-noise-amplifier circuits require low resistance values in the signal path. Johnson (resistor) noise equals 4 nV times the square root of the resistance value in kilohms. Although the Johnson noise of a 1-k $\Omega$  resistor is only 4 nV/ $\sqrt{\text{Hz}}$ , this amount increases to 18 nV/ $\sqrt{\text{Hz}}$  for a 20-k $\Omega$  resistor and 40 nV/ $\sqrt{\text{Hz}}$  for a 100-k $\Omega$  resistor. Even though  $C_2$  bypasses the  $R_A/R_B$  resistor divider to ground, these resistors set a limit on the minimum value that you can use for the op amp’s feedback resistor, and, the larger this value is, the greater the Johnson noise. So, low-noise applications need to use much smaller op-amp-biasing-resistor values than 100 k $\Omega$ . However, lower value resistors in the divider mean higher power-supply current and reduced battery life.

Fortunately, the zener-diode biasing method supplies  $V_s/2$  without the need for large resistors. As long as you bypass the zener to keep its noise out of the circuit, you can reduce both noise and supply current. The use of a linear voltage regulator is even better, because both its noise and its output impedance are low.

You also need to consider circuit turn-on time. The approximate turn-on time equals the RC time constant of the lowest bandwidth filter you use. The circuits call for the  $R_A/R_B$  and  $C_2$  voltage-divider network to have a 10-times-longer time constant than that of the input or output circuit. This longer time constant simplifies the circuit design because as many as three RC poles set the input bandwidth. This long time constant also helps keep the biasing network

**TABLE 3—RECOMMENDED  $R_z$  VALUES AND MOTOROLA PART NUMBERS FOR FIGURES 4 AND 5**

Supply voltage (V)	Zener voltage (V)	Zener type	Zener current ( $I_z$ )	$R_z$ value ( $\Omega$ )
15	7.5	1N4100	500 $\mu$ A	15k
15	7.5	1N4693	5 mA	1.5k
12	6.2	1N4627	500 $\mu$ A	11.5k
12	6.2	1N4691	5 mA	1.15k
9	4.3	1N4623	500 $\mu$ A	9.31k
9	4.3	1N4687	5 mA	931
5	2.4	1N4617	500 $\mu$ A	5.23k
5	2.7	1N4682	5 mA	464

**TABLE 4—TYPICAL COMPONENT VALUES FOR THE CIRCUIT OF FIGURE 4**

Gain	Input bandwidth (Hz)	Output bandwidth (Hz)	$C_{IN}$ ( $\mu$ F)	$R_1$ (k $\Omega$ )	$C_1$ ( $\mu$ F)	$C_{OUT}$ ( $\mu$ F)	$R_{LOAD}$ (k $\Omega$ )
10	10	10	0.3	11	2	0.2	100
20	10	10	0.3	5.23	4.7	0.2	100
10	50	50	0.1	11	0.47	0.05	100
101	20	20	0.2	1	15	0.1	100

Notes:  $R_{IN}=R_2 = 100$  k $\Omega$ , and  $C_N=0.1$   $\mu$ F. Select  $R_2$  from Table 3.

Capacitance values are rounded off to next highest common value. Because the  $C_{IN}/R_{IN}$  pole and  $C_1/R_1$  poles are at the same frequency, and both affect the input bandwidth, each capacitor is  $\sqrt{2}$  larger than it would otherwise be for a single-pole, RC-coupled input.

**TABLE 5—TYPICAL COMPONENT VALUES FOR THE CIRCUIT OF FIGURE 5**

Gain	Input bandwidth (Hz)	Output bandwidth (Hz)	$R_1$ (k $\Omega$ )	$C_1$ ( $\mu$ F)	$C_2$ ( $\mu$ F)	$C_{OUT}$ ( $\mu$ F)	$R_{LOAD}$ (k $\Omega$ )
10	10	10	10	2.7	0.2	0.2	100
20	10	10	5	4.7	0.2	0.2	100
10	50	50	10	0.5	0.05	0.05	100
100	20	20	1	12	0.1	0.1	100

Notes:  $R_{IN}=R_2=100$  k $\Omega$ . Select  $R_2$  from Table 3.

Capacitance values are rounded off to next highest common value. Because the  $C_1/R_1$  pole and  $C_2/R_{IN}$  poles are at the same frequency, and both affect the input bandwidth, each capacitor is  $\sqrt{2}$  larger than it would otherwise be for a single-pole, RC-coupled input.

from turning on before the op amp’s input and output networks, and, therefore, the op amp’s output gradually climbs from 0V to  $V_s/2$  without “railing” to the positive-supply line. **Table 1** supplies a value for a 3-dB corner frequency that is one-tenth that of  $R_1/C_1$  and  $R_{LOAD}/C_{OUT}$ . For example, in **Figure 2**, for a circuit bandwidth of 10 Hz and a gain of 10, **Table 1** recommends a  $C_2$  value of 3  $\mu$ F, which provides a 3-dB bandwidth of 1 Hz. The parallel combination of  $R_A$  and  $R_B = 50$  k $\Omega \times 3$   $\mu$ F = 0.15-sec RC time constant. So, the op amp’s output will take approximately 0.15 sec to settle to  $V_s/2$ . The input and output RC networks charge as much as 10 times faster. In applications in which the circuit’s  $-3$ -dB, low-frequency bandwidth is low, the circuit turn-on time may become excessively long. In that case, a zener-biasing method may be a better choice.

**INPUT-HEADROOM CONSIDERATIONS**

Some specialty op amps are designed for low-voltage operation. Powering these op amps from a low-voltage single supply, such as 5 or 3.3V, may introduce input-headroom limitations. This scenario can happen if the amplifier’s input stage does not limit symmetrically. For example, the AD8061 op amp has an input-common-mode-voltage range that extends to ground or the negative-supply line. However, its inputs can swing to

within only 1.8V of the positive-supply voltage without introducing dc errors or limiting device bandwidth. So, if you operate this amplifier from a single 5V supply and bias the amplifier’s positive input at  $V_s/2$ , 2.5V, the input voltage can swing in the negative direction a full 2.5 to 0V. But, in the positive direction, it can swing only 1V before clipping.

This situation is not a problem if the amplifier operates at a gain of 2.5 or higher, because it will reach its maximum output swing of  $\pm 2.5$ V before the input stage limits. However, if the amplifier operates at a lower gain, you must bias the positive input below  $V_s/2$  to allow symmetrical input stage limiting. In the case of the AD8061, biasing the positive input at 1.5V allows a 3V p-p input swing without clipping. Refer to the individual product data sheets to determine the optimum single-supply biasing voltage. □

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