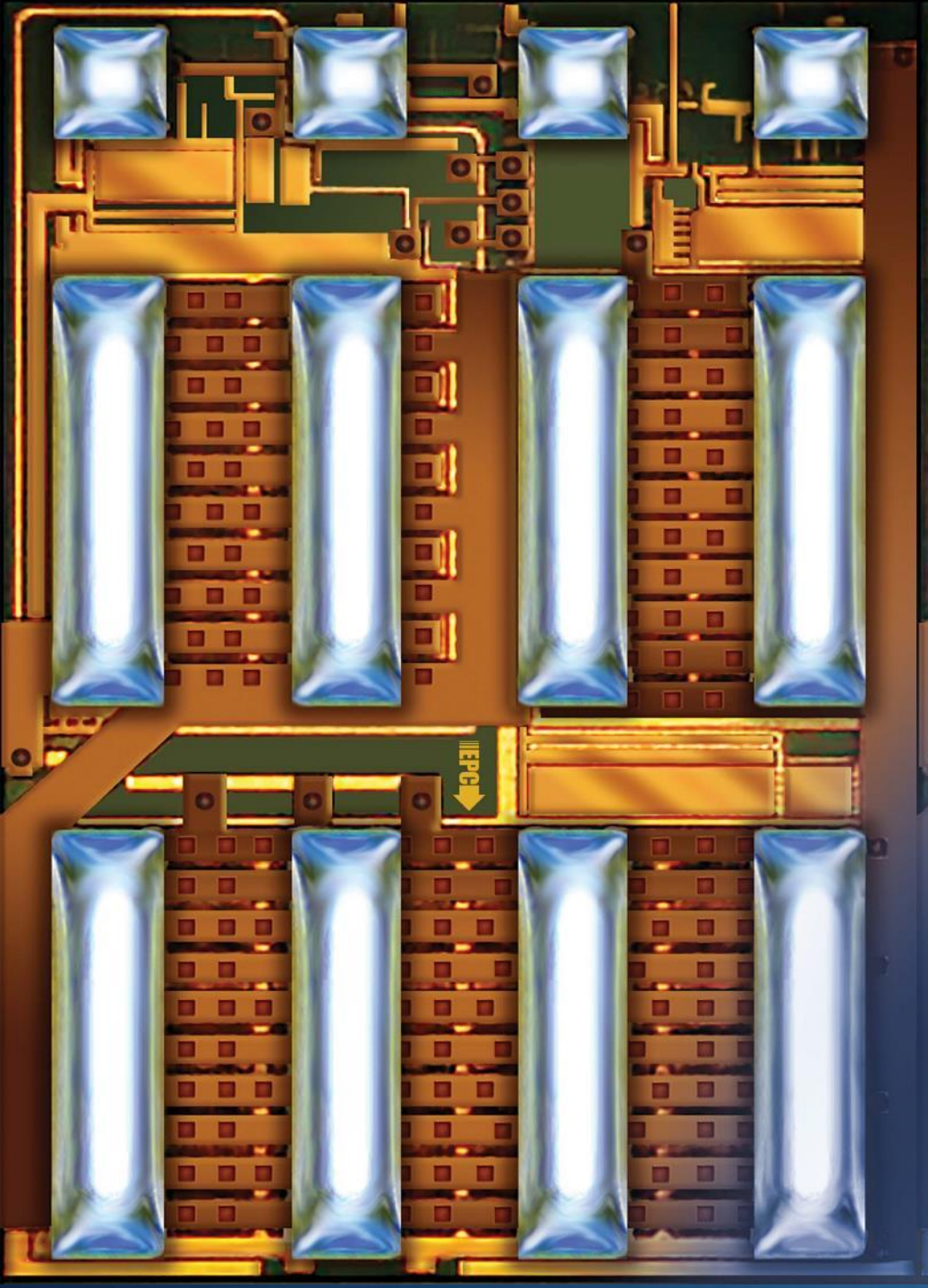

Advances in GaN Devices

November 2022

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EFFICIENT POWER CONVERSION

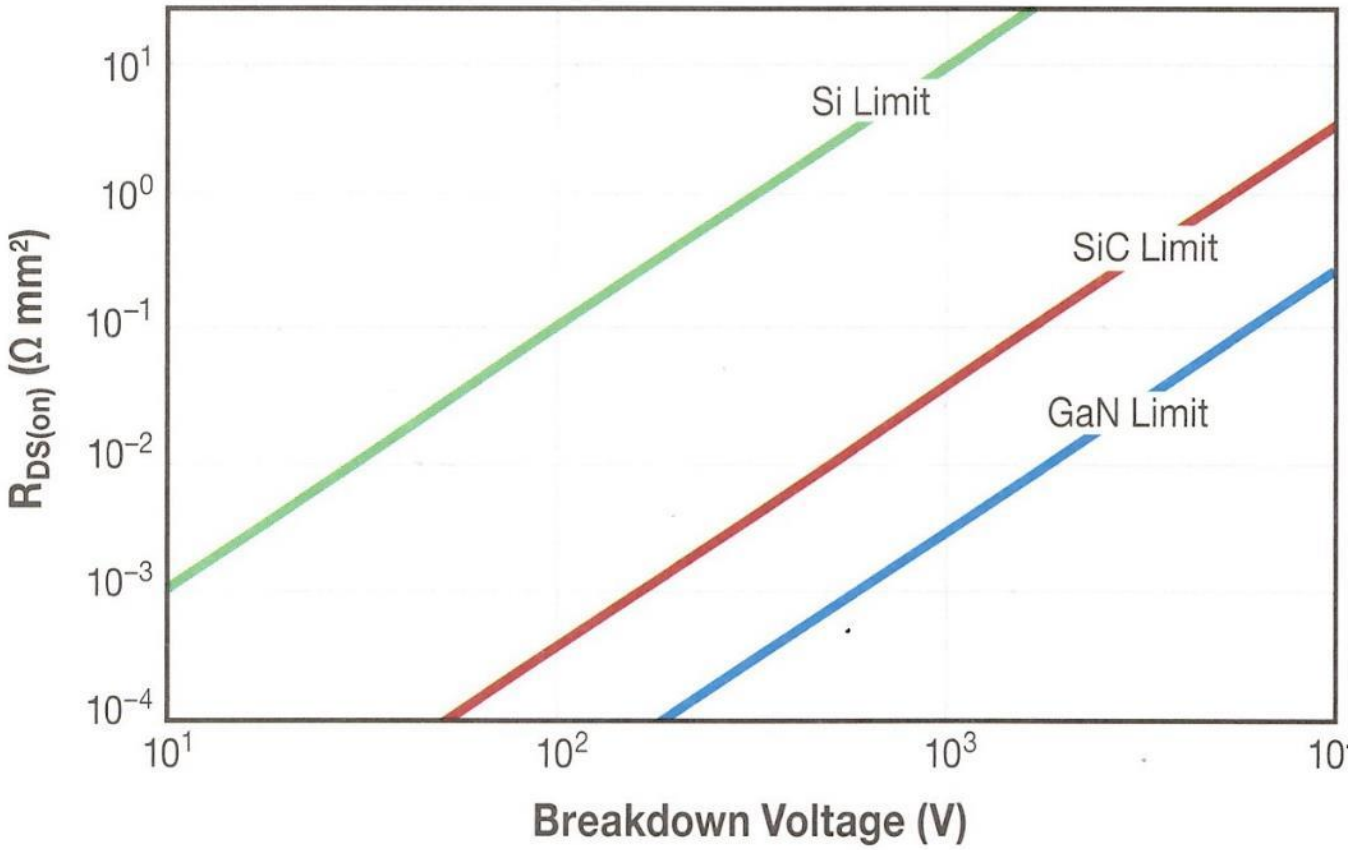
Advances in GaN Devices

- Motivation for GaN power devices
  - Structure review
  - Characteristics review
- Advances:
  - Die shrinkage, and its advantages
  - Reliability Advances
  - Packaging
  - Board layout advances
  - Thermal
  - Monolithic GaN ICs
- A look forward

Motivation for Wide Band Gap Devices

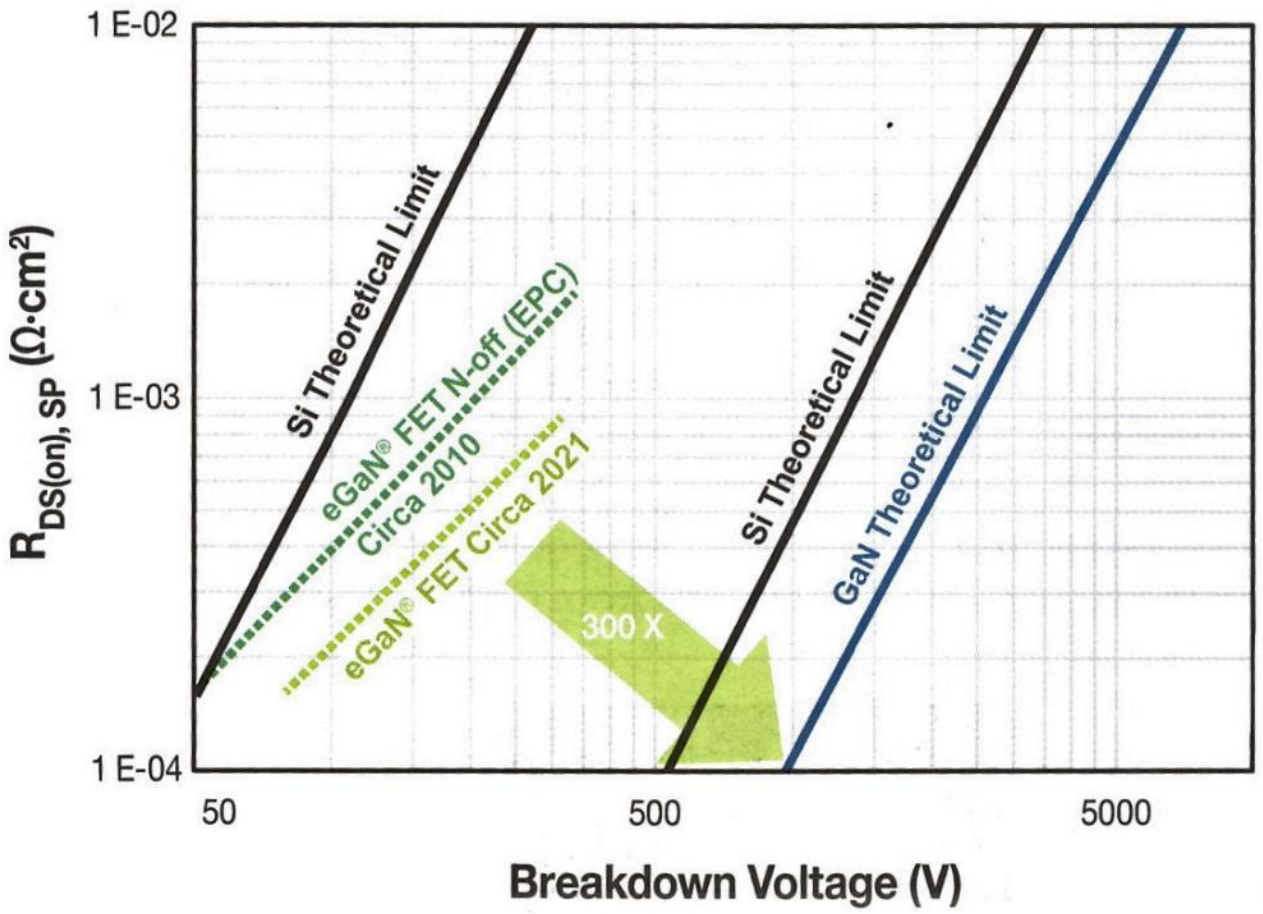
The potential of wide band gap

- SiC and GaN: theoretical much smaller size for a given Rds(on)
- Can this potential be realized?
  - Silicon MOSFETs **have** reached their potential. Real-world devices match the green line
  - What about GaN FETs? What advancement is seen?



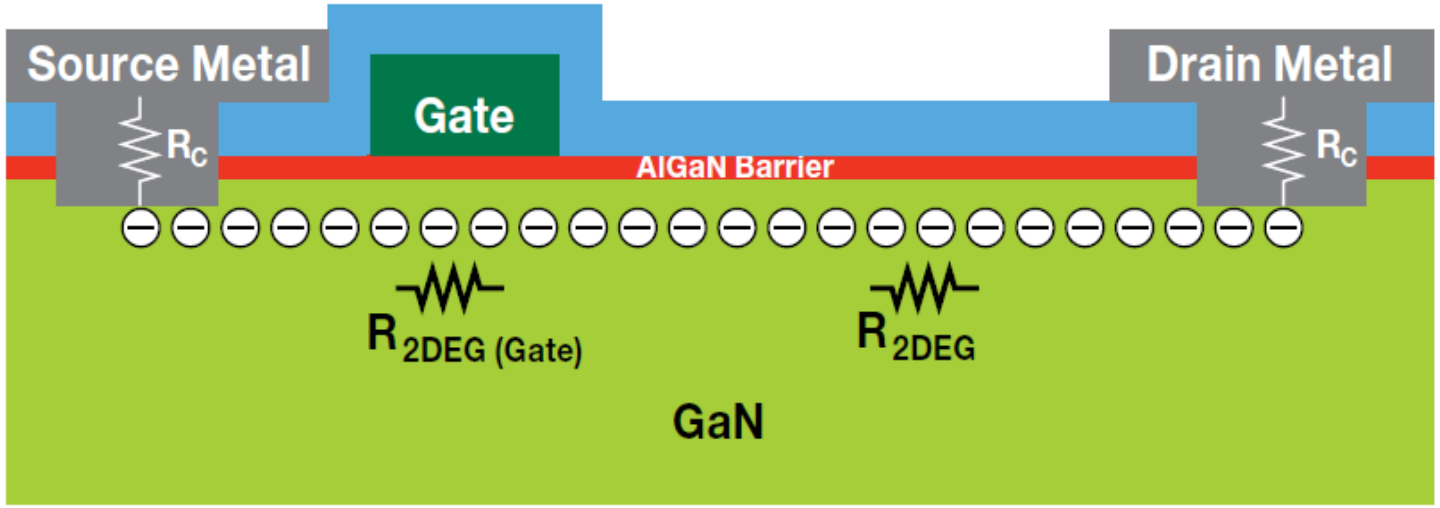
Motivation for Wide Band Gap Devices

- GaN Advances so far:
  - Progress from 2010 to 2021: ~ 2x
  - Still 300 x from theoretical limit
- GaN and SiC future advances are expected/planned
- Why is further size reduction important?
  - Affects cost
  - Affects many parasitics
  - Smaller allows improved board layout



GaN Structure

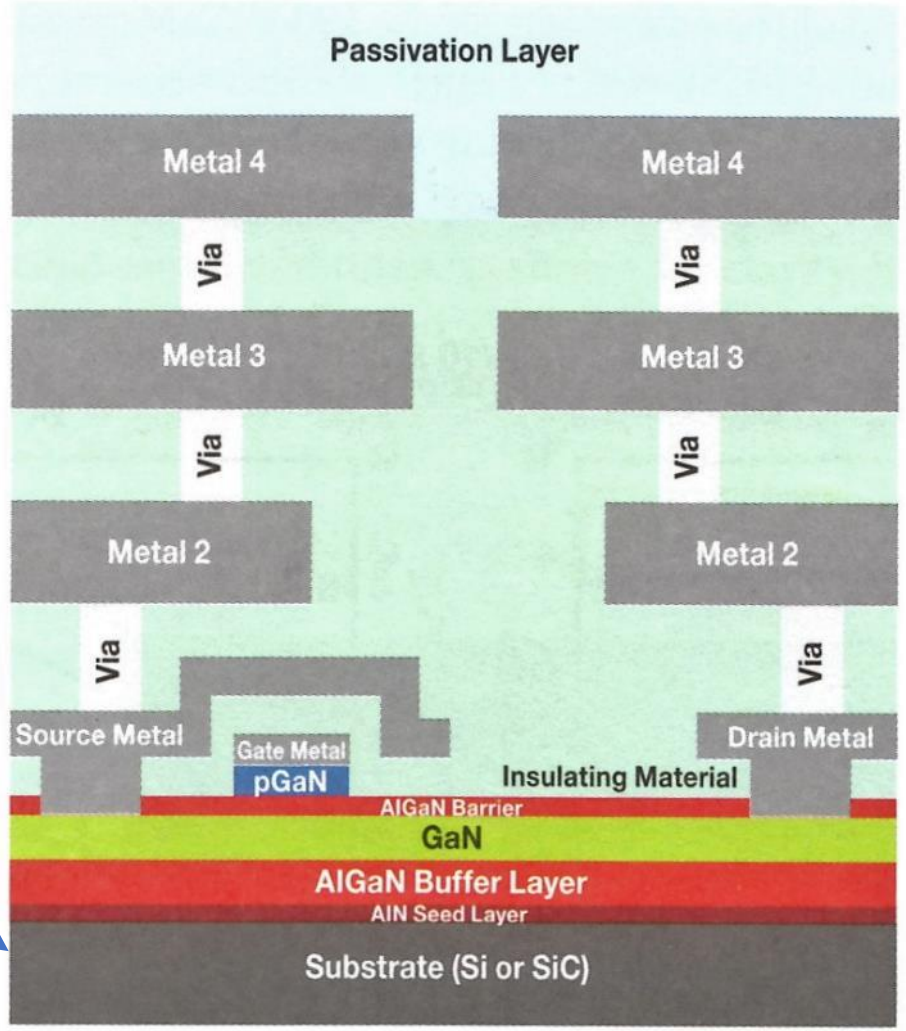
- GaN devices can be lateral or vertical
- Some High-Voltage GaN devices use vertical GaN… for kV
- Low voltage GaN typically are lateral (as diagram)



GaN Structure

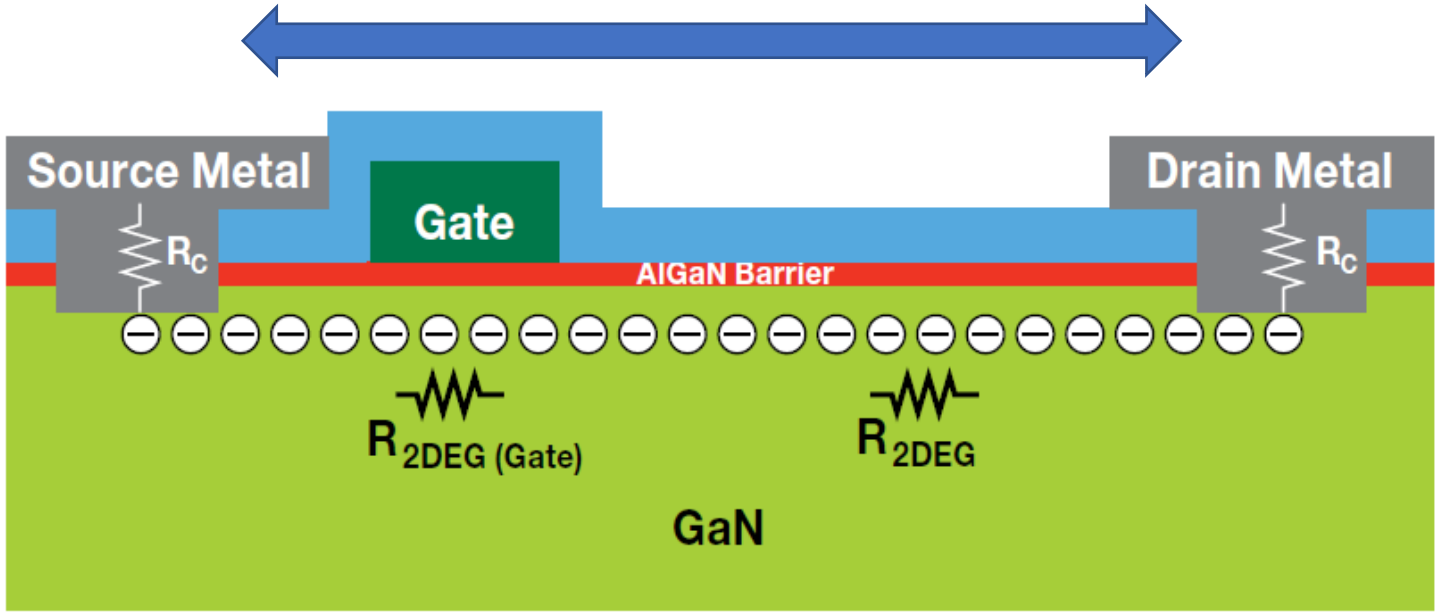
Lateral GaN FET diagram, detail

- Advancements
  - More layers
    - Metal 3 & Metal 4
    - Helps for low Rds, on
  - Thinner Substrate
    - Lower height
    - Improved thermal conductivity



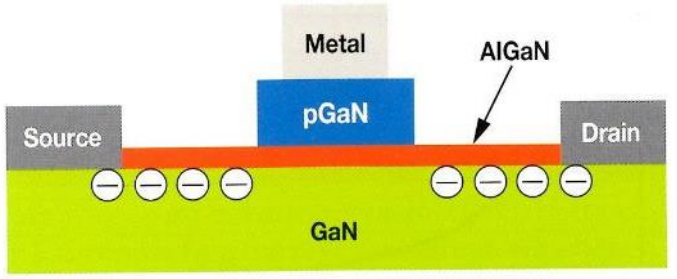
Die Size Reduction

- Die Size:
  - Drain to Source distance, vs. voltage
  - To shrink: reduce Drain to Source distance
  - But: electric field *increases*
    - A challenge to make it reliable
  - Motivation:
    - Die size
    - Less width for same R

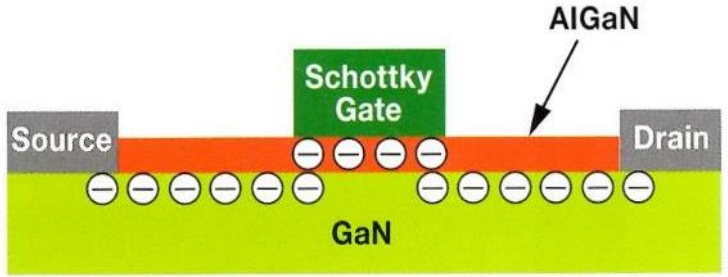


GaN Structure: Gate

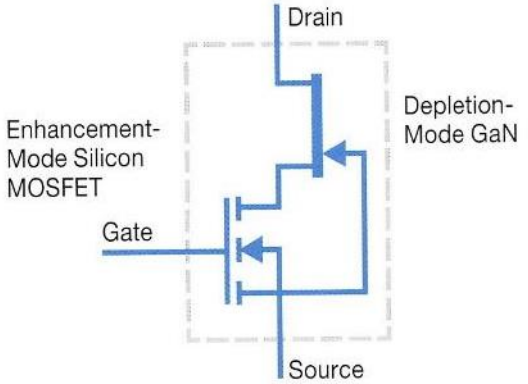
- GaN gate: many possible varieties!
- Goal for all: enhancement mode operation
  - Depletion-mode: ON at Vgs = 0V
    - not desirable for power FETs, in general
  - P-type gate: typically 5-7 V on, 0 V off
  - Schottky gate: a few variations
  - Cascode: good for higher voltage



P-type GaN gate



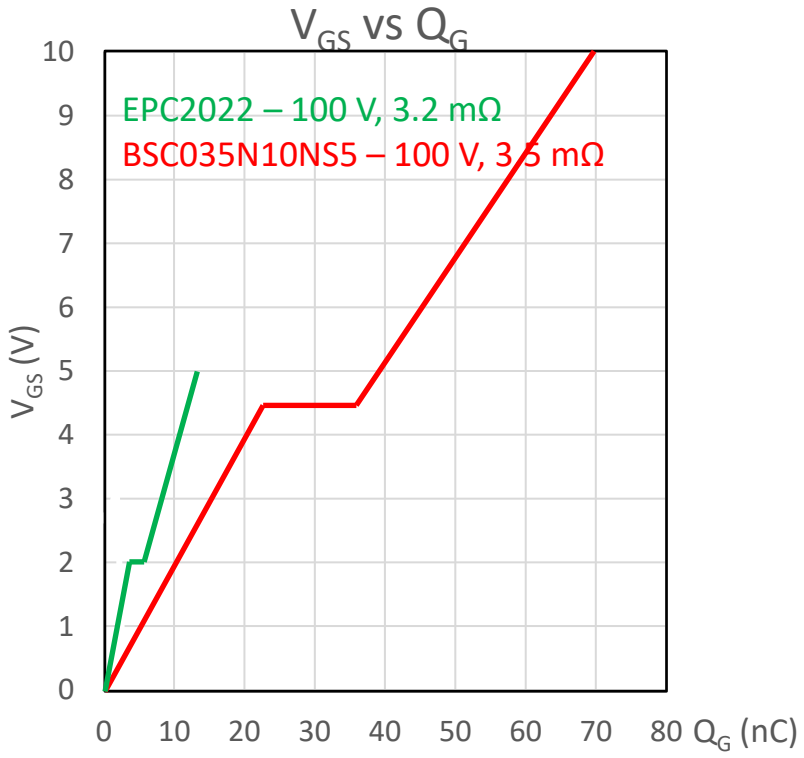
Schottky GaN gate



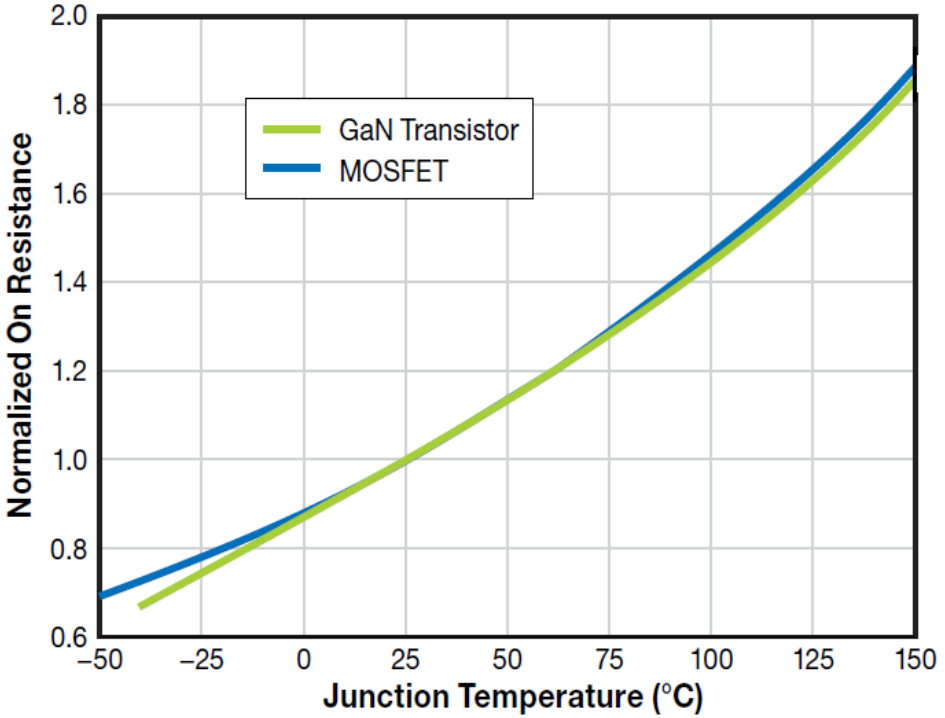
Cascode, GaN + MOSFET

GaN Characteristics

Some characteristics are similar to silicon MOSFETs:



Gate Voltage vs. Gate Charge

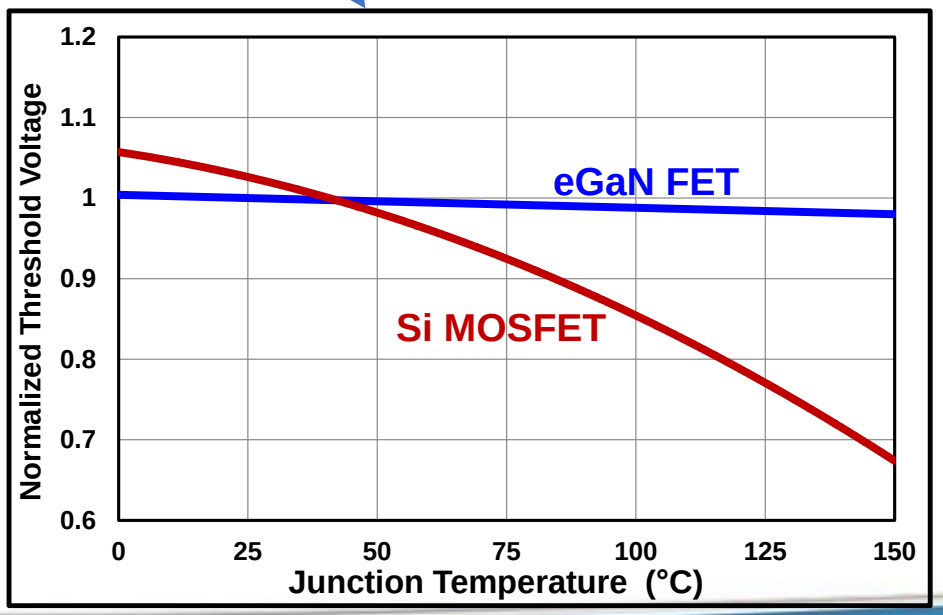


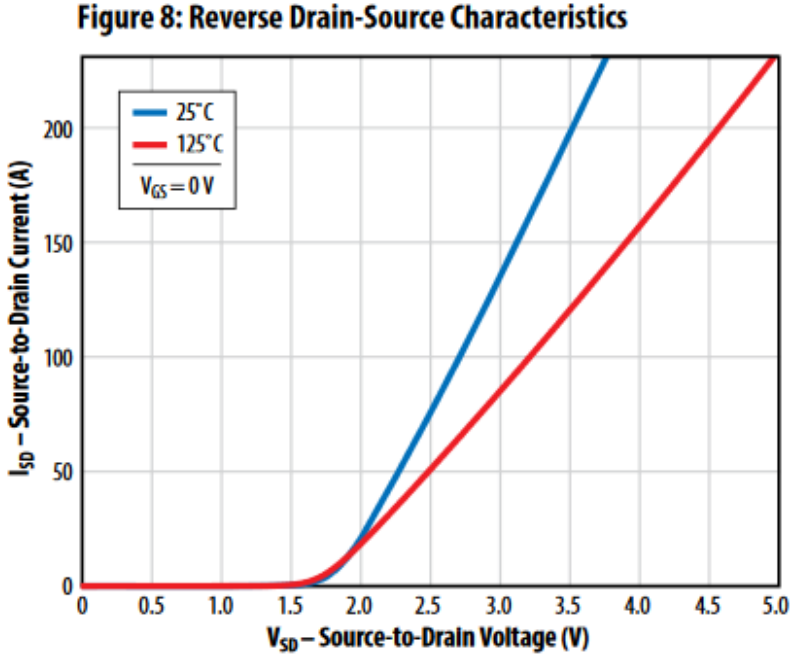
Rds,on vs. temperature

GaN Characteristics

Some characteristics are different from silicon MOSFETs:

- No Reverse Recovery (Qrr)
  - No parasitic p-n diode
- Higher reverse “diode” voltage
- Vth (gate threshold): very small temperature variation





GaN Characteristics

Optimization differences vs. silicon MOSFETs:

- ***Dead time***: Can use very short dead times
  - 5-15 ns
  - No Reverse Recovery (Qrr), so no active dead time management needed
- ***Diode***: Limit high-current /time in diode mode
  - Due to heat… OK electrically
  - Can use small parallel Schottky if needed
- ***Upper Gate Drive***: Observe Vgs max limit
  - Boost often floats higher

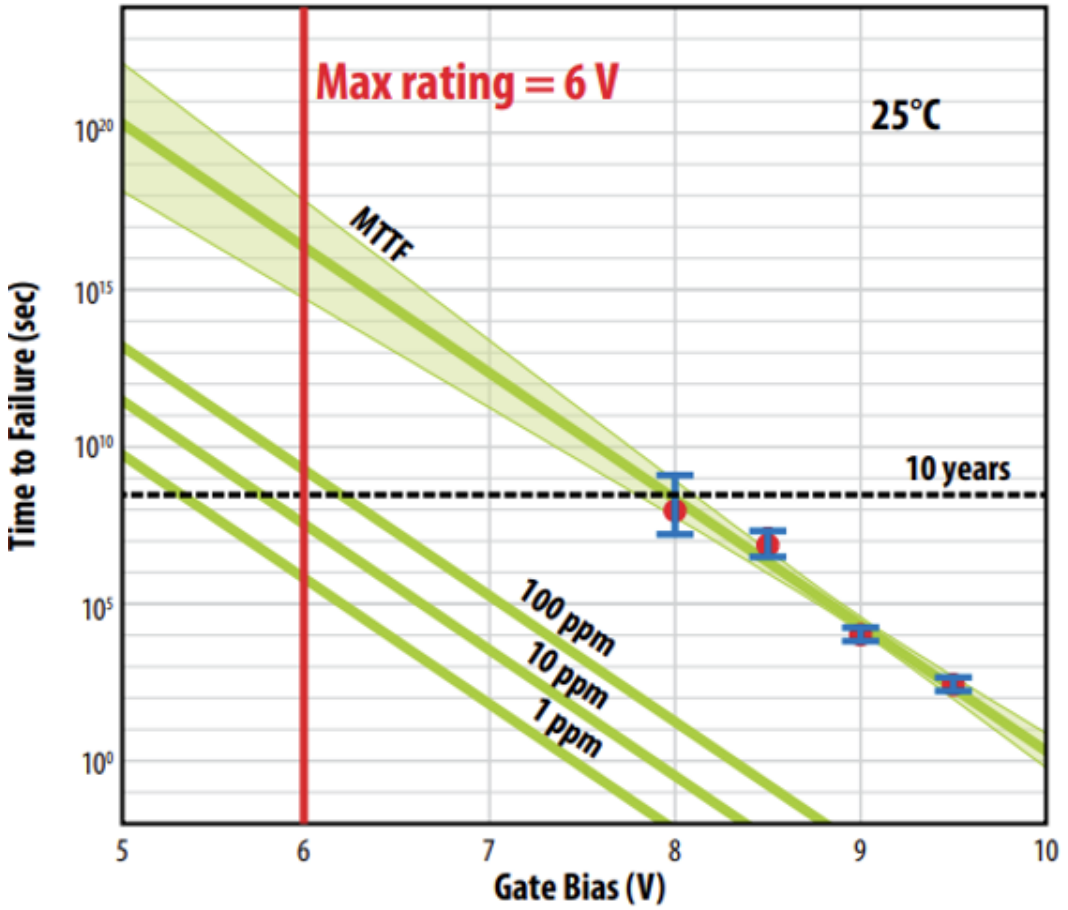
GaN Reliability: test to failure

Gate Reliability

- How does a GaN FET gate fail?
  - Suddenly? Or gradual degradation?
  - Below 10 V: gradual failure
- For this example GaN FET: gate typical = 5V, absolute max = 6V.

- Time to Failure vs. Gate Bias Voltage.

- 25 years = 7.9 x 10^8 seconds.



Source: EPC, Phase 12 and Phase 14 Reliability Reports

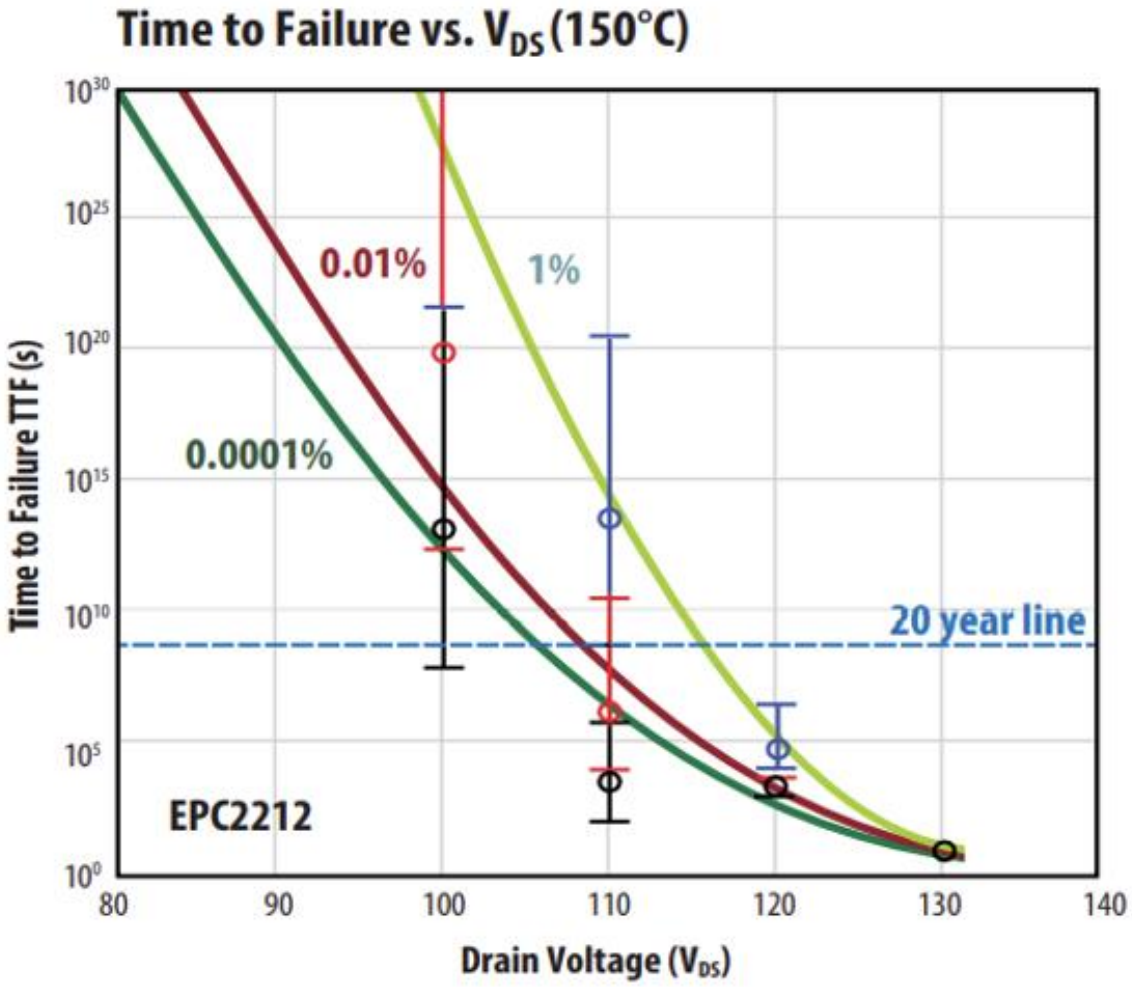
GaN Reliability: test to failure

Drain Voltage Reliability

- 100 V GaN FET
- High Temp. Reverse Bias
- Time to Failure vs. Drain Voltage

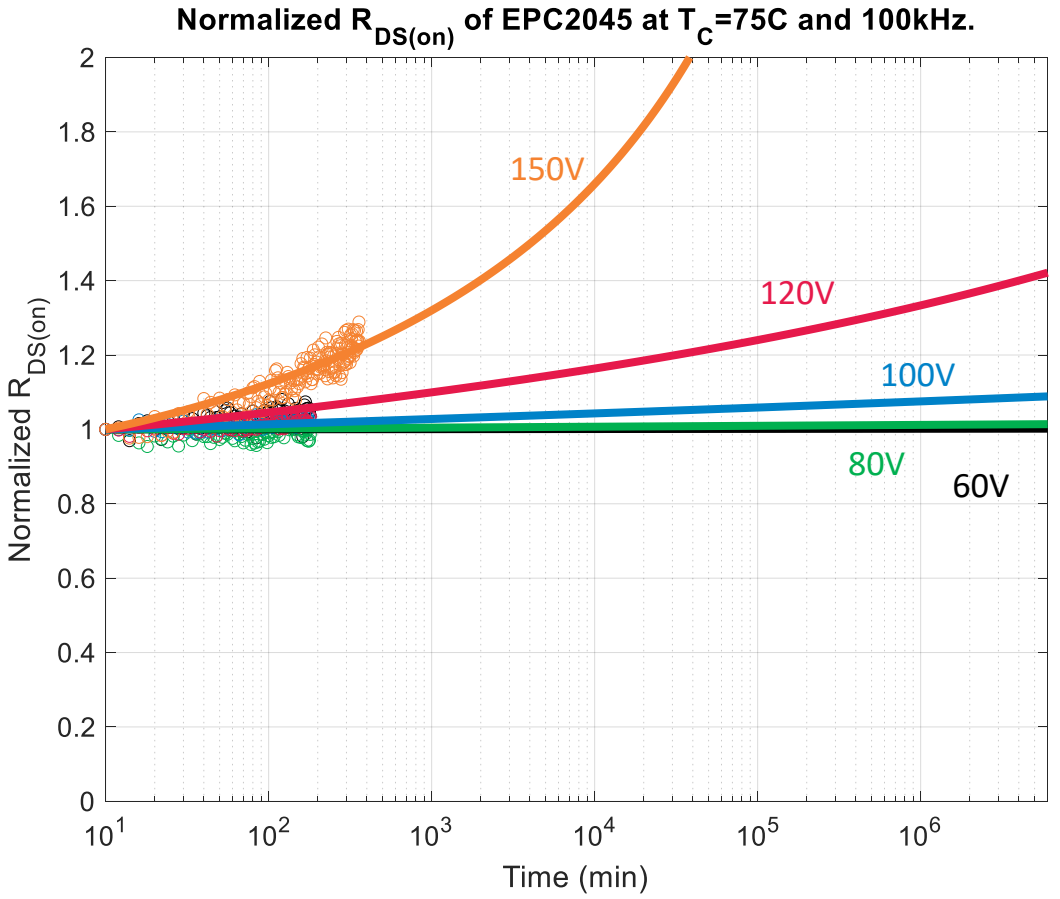
- Conclusion: voltage is a strong accelerator of failure

- 25 years = 7.9 x 108 seconds



GaN Reliability: Voltage Tests

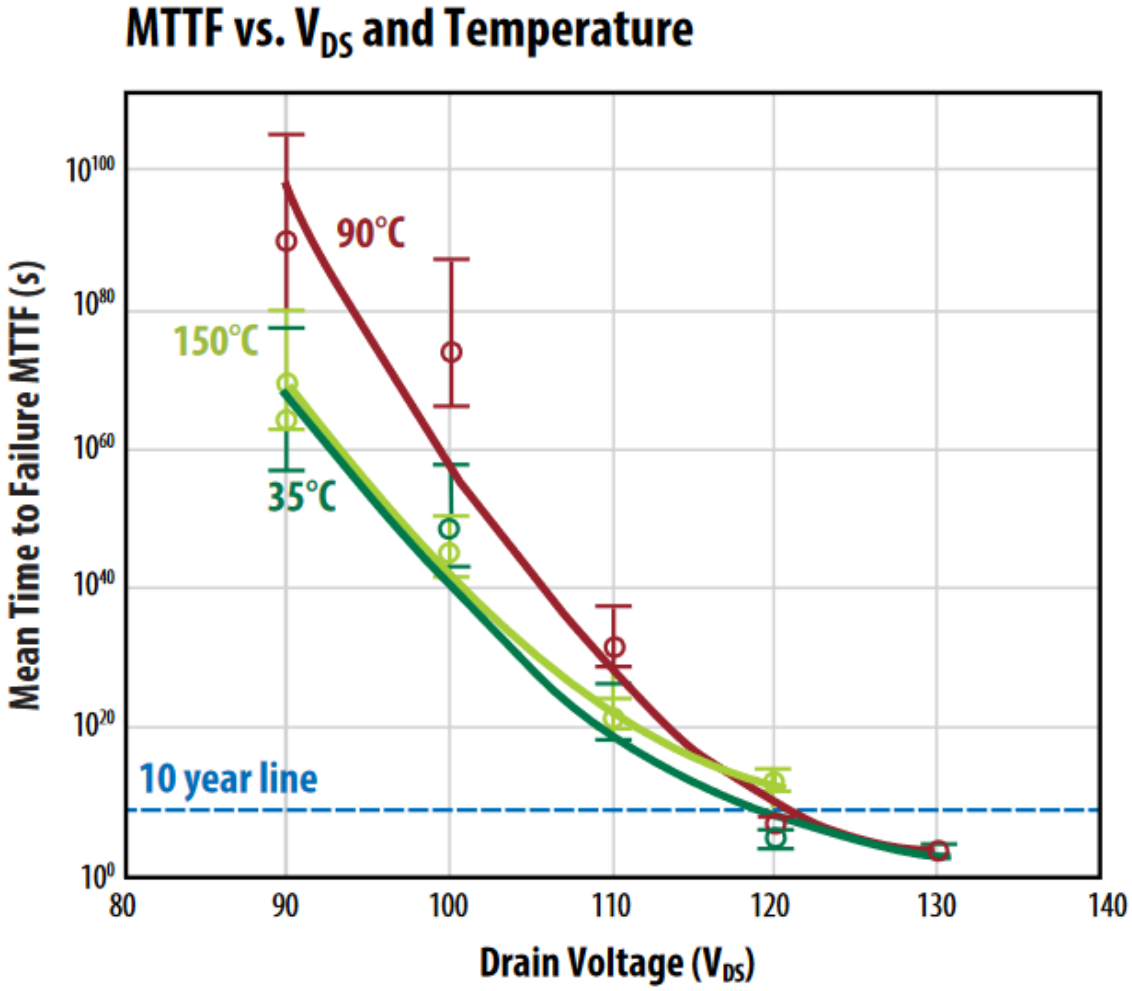
- Test a 100 V GaN FET at various voltages
  - Including 120% and 150% of rated
  - For this case, failure = Rds, on



GaN Reliability: Temperature

Testing a 100 V GaN FET at various temperatures

- Voltage = 150% of rated = 150 V
- Temperatures: 35 C (dark green), 90 C (red), and 150 C (light green)
- Note the reliability at 90 C > reliability at 35 C & 150 C. For < 100 V.



Temperature Cycling Advances

Advances in studying thermo-mechanical reliability

- Temperature Cycling: FETs mounted on board, -40°C to 125°C
- Performance depends on die size, assembly, underfill, etc.
  - Right-hand graph is for a large die. 13.9 mm^2
- Underfill can help (or hurt!) chip-scale TC performance

Underfill comparison for an example GaN FET

Product/DOE	EPC2053									
Stress condition: -40°C to 125°C	Status	300 cycles	550 cycles	850 cycles	1000 cycles	1250 cycles	1550 cycles	1750 cycles	1950 cycles	2150 cycles	2450 cycles
No Underfill	Completed	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	2/32 fails	3/32 fails	3/32 fails	3/32 fails
Henkels UF1137_H	On-going	0/40 fail	0/40 fail	0/40 fail	0/40 fail	0/40 fail					
Masterbond EP3UF_M	On-going	1/40 fails	7/40 fails	15/40 fails	25/40 fails	39/40 fails					
MC7685-UFS	Completed	0/32 fail	0/32 fail	0/32 fail	1/32 fails	17/32 fails	32/32 fails	32/32 fails			
MC7885-UF	Completed	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	1/32 fails	1/32 fails	1/32 fails
Namics 8410-406B	Completed	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail
Namics U8437-2_N	Completed	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail	0/32 fail
	On-going	0/40 fail	0/40 fail	0/40 fail	0/40 fail	0/40 fail					

Table 10: –40°C to 125°C Temperature Cycling results for EPC2053.

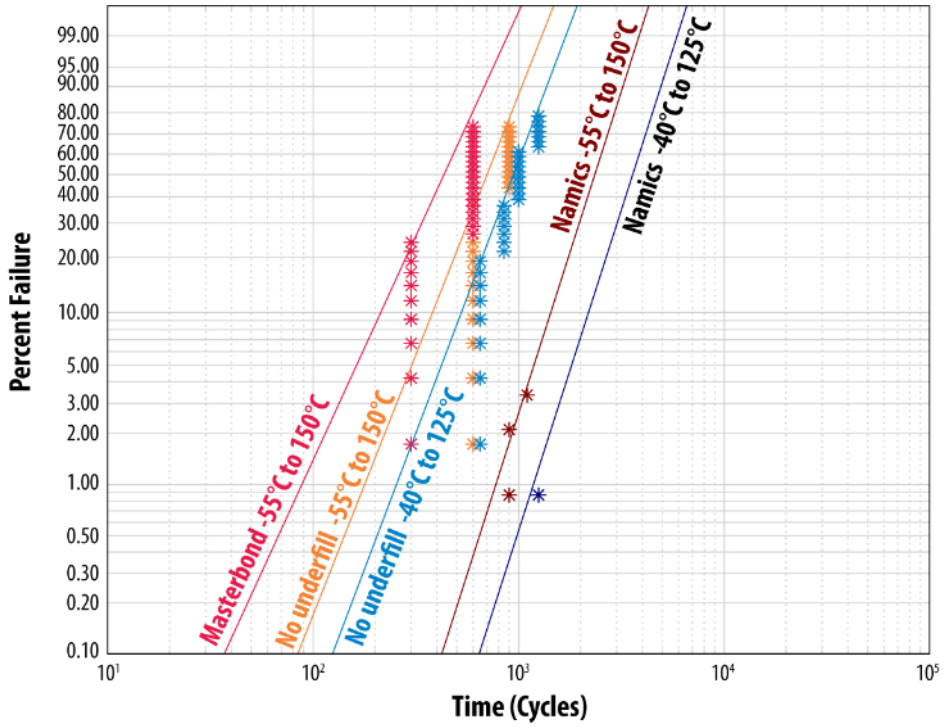
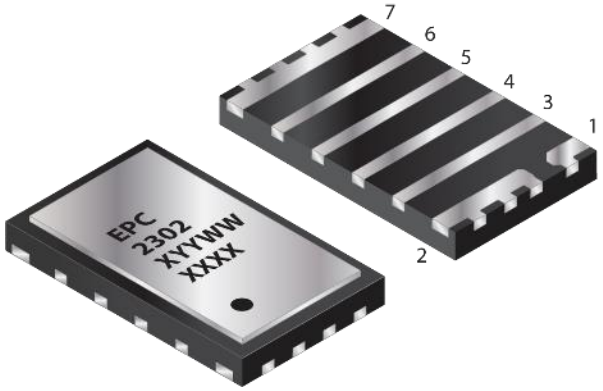


Figure 48: Weibull plots of Temperature Cycling results of EPC2206

GaN Packaging Advances



Exposed-die-top QFN, EPC

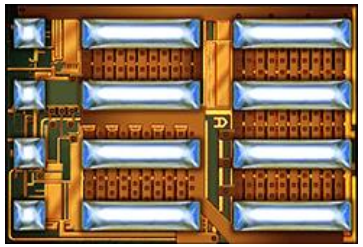
- *Familiar assembly of QFN*
- *Top-side thermal conduction*
- *Discrete FET & IC versions*

Advanced package, GaN Systems

- *Low inductance*
- *Top-side thermal conduction*

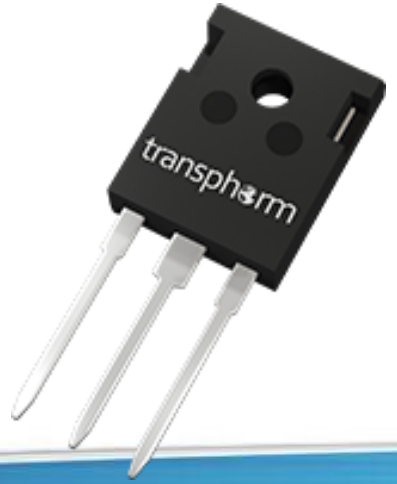
IC package, Navitas Semi

- *Low inductance*
- *Top-side thermal conduction*



Chip-scale GaN IC, EPC

- *Minimum size*
- *Top-side thermal conduction*
- *IC & discrete FETs*



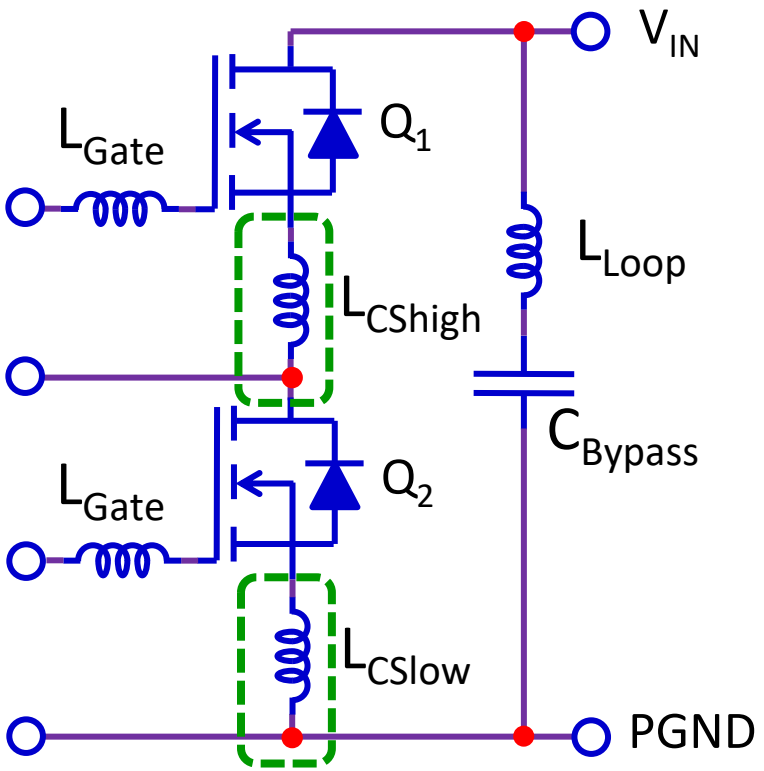
TO-247 GaN, Transphorm

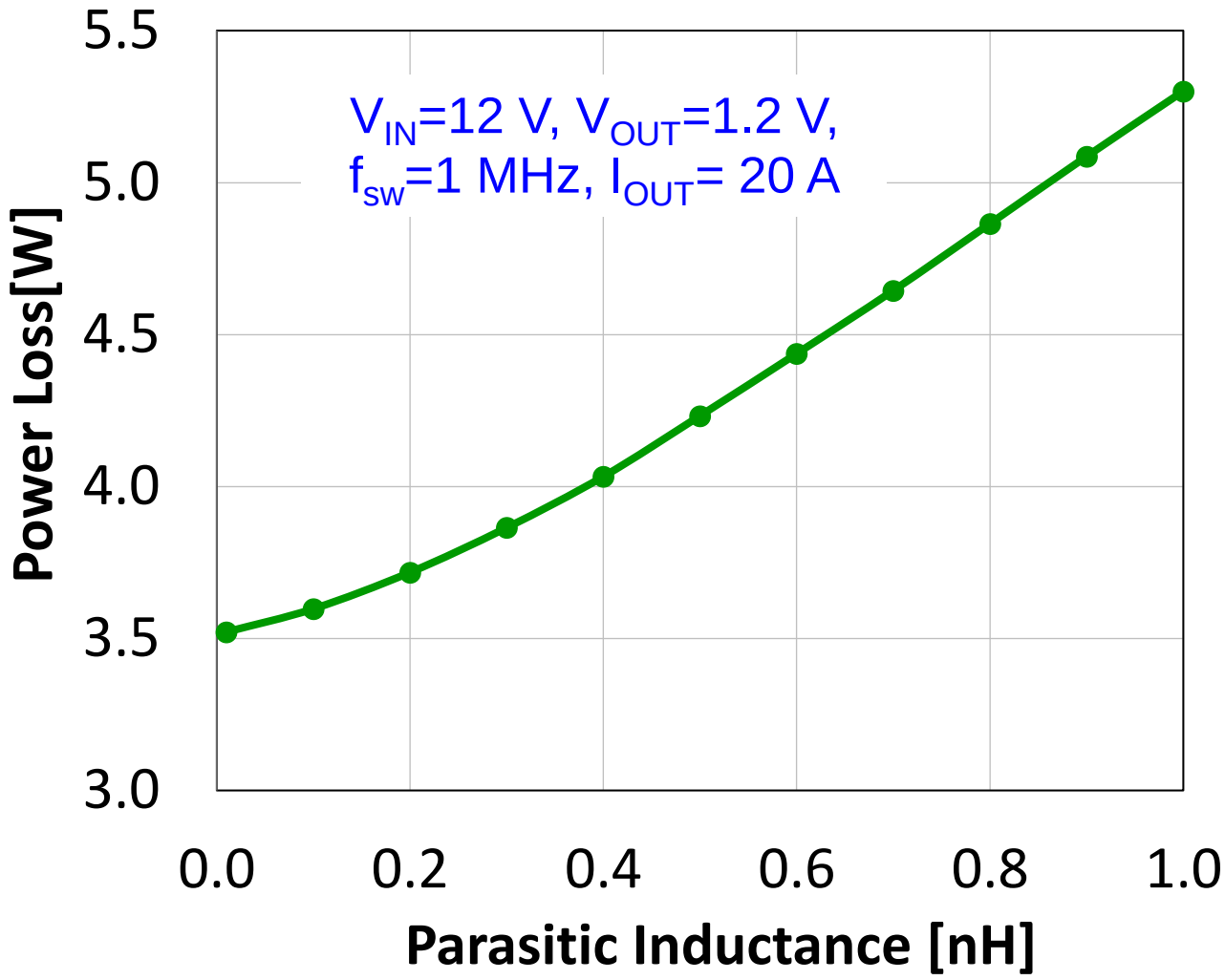
- *Familiar TO-247, plus QFN*
- *Screw to traditional heat sinks*
- *Up to 900 V, 63 m-ohms*

Layout Advances

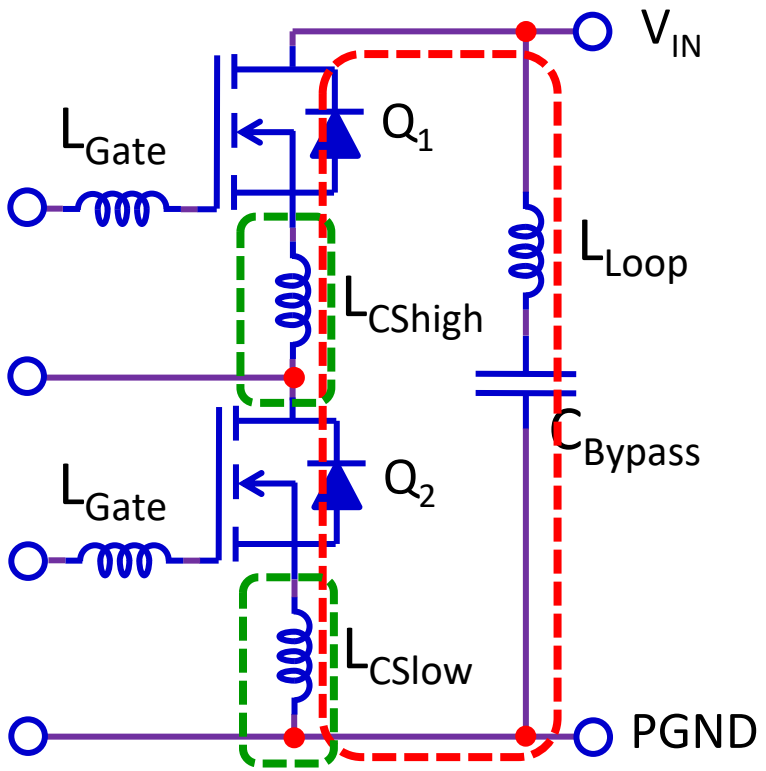
- GaN FETs are faster than Silicon MOSFETs
- Good layout needed… or layout can limit performance!
  - GaN FETs' speed "forces" focus on layout
- Goal: minimizing inductances.
  - Let's review…

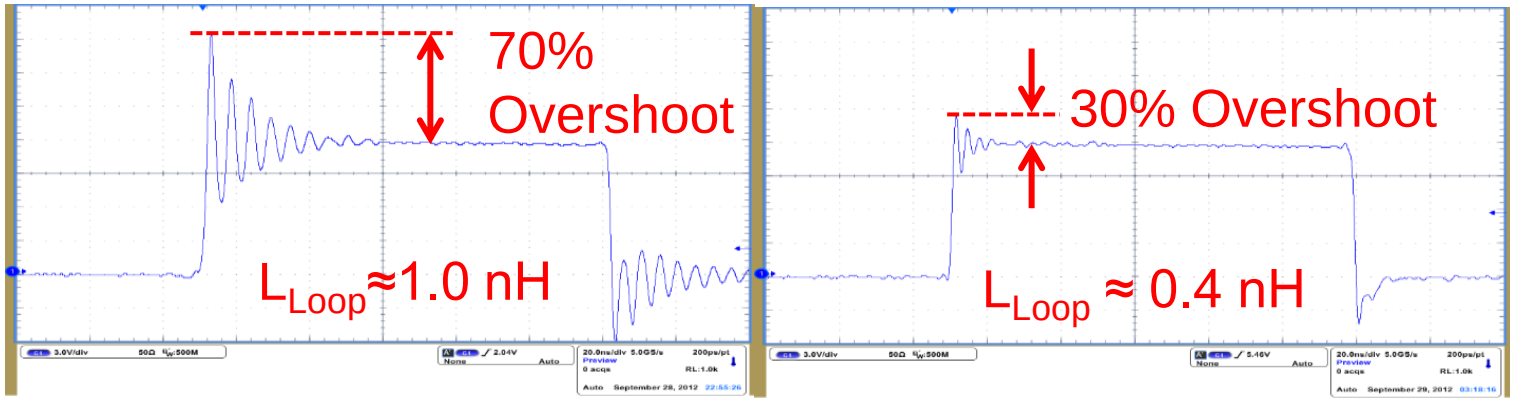
Impact of Common Source Inductance

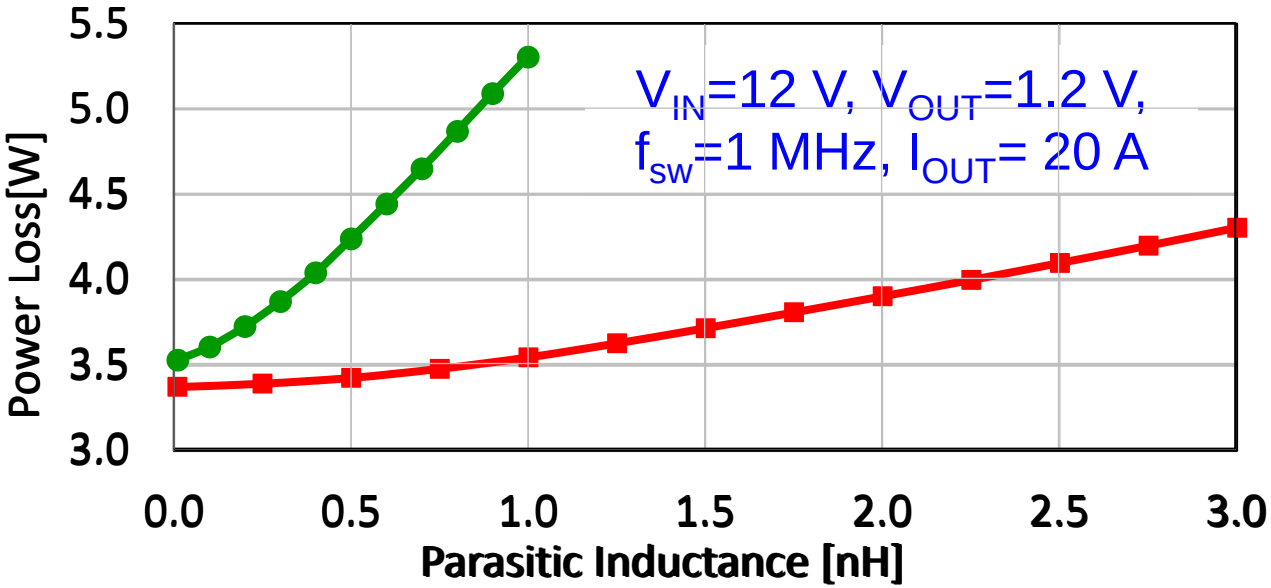




Impact of Power Loop Inductance

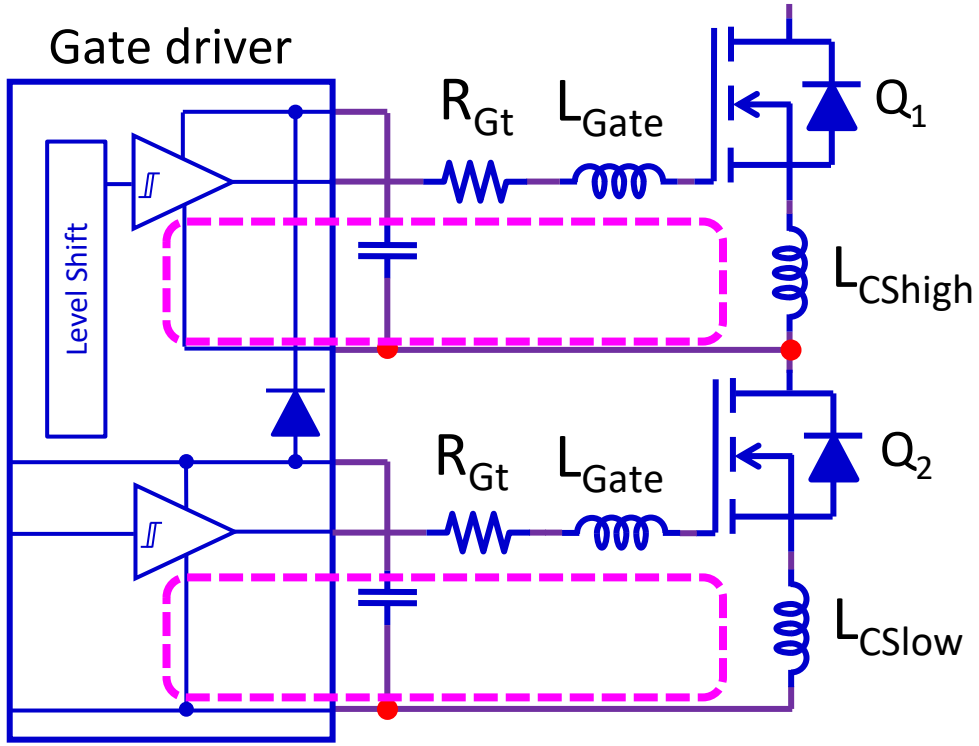




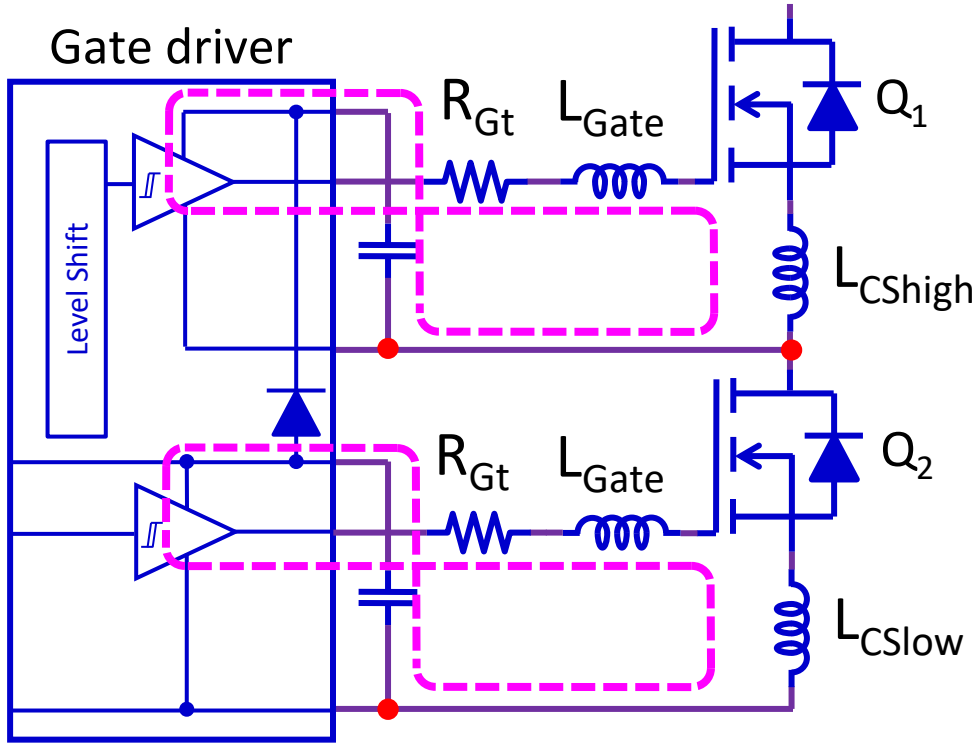


Impact of Gate Loop Inductance

- Two loops to consider: Turn-on & Turn-off
- L_{Gate} requires R_{Gt} to damp ringing overshoot
  - slows transition

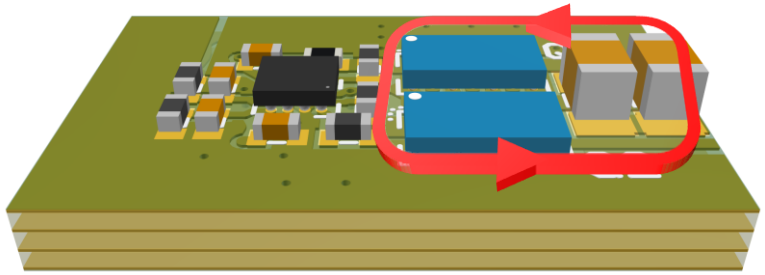


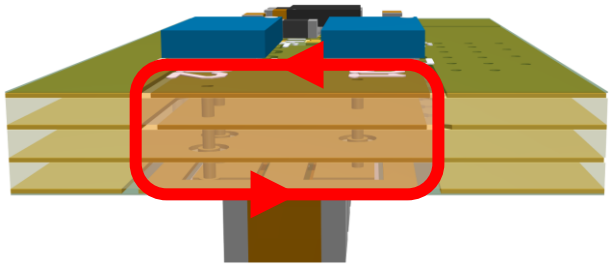
Turn Off

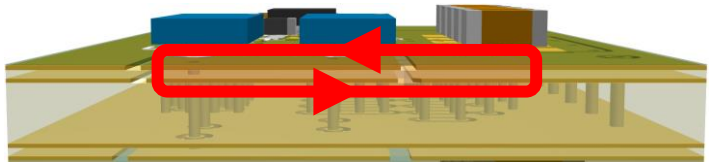


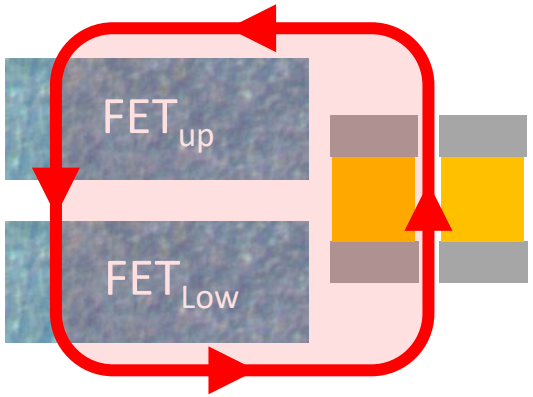
Turn On

Layout Comparisons



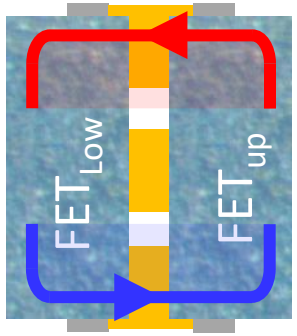






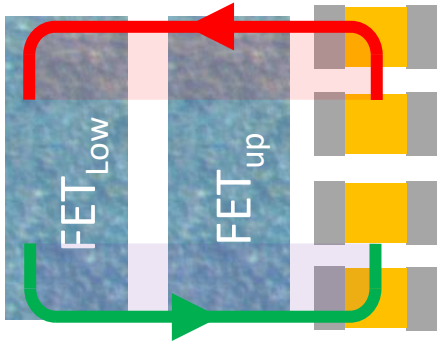
Top Layer

Lateral



Top Layer Bottom Layer

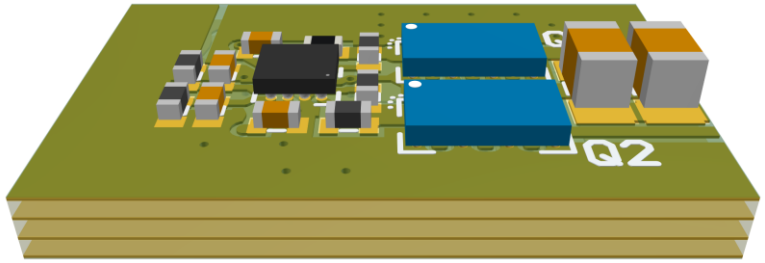
External Vertical



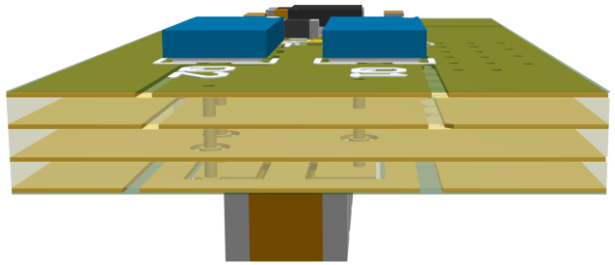
Top Layer Inner Layer 1

Internal Vertical

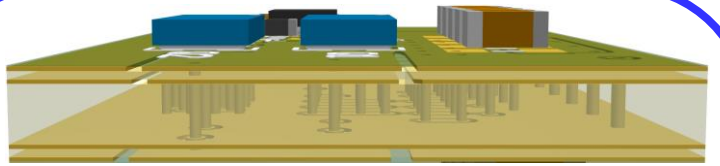
Layout Inductance Comparison



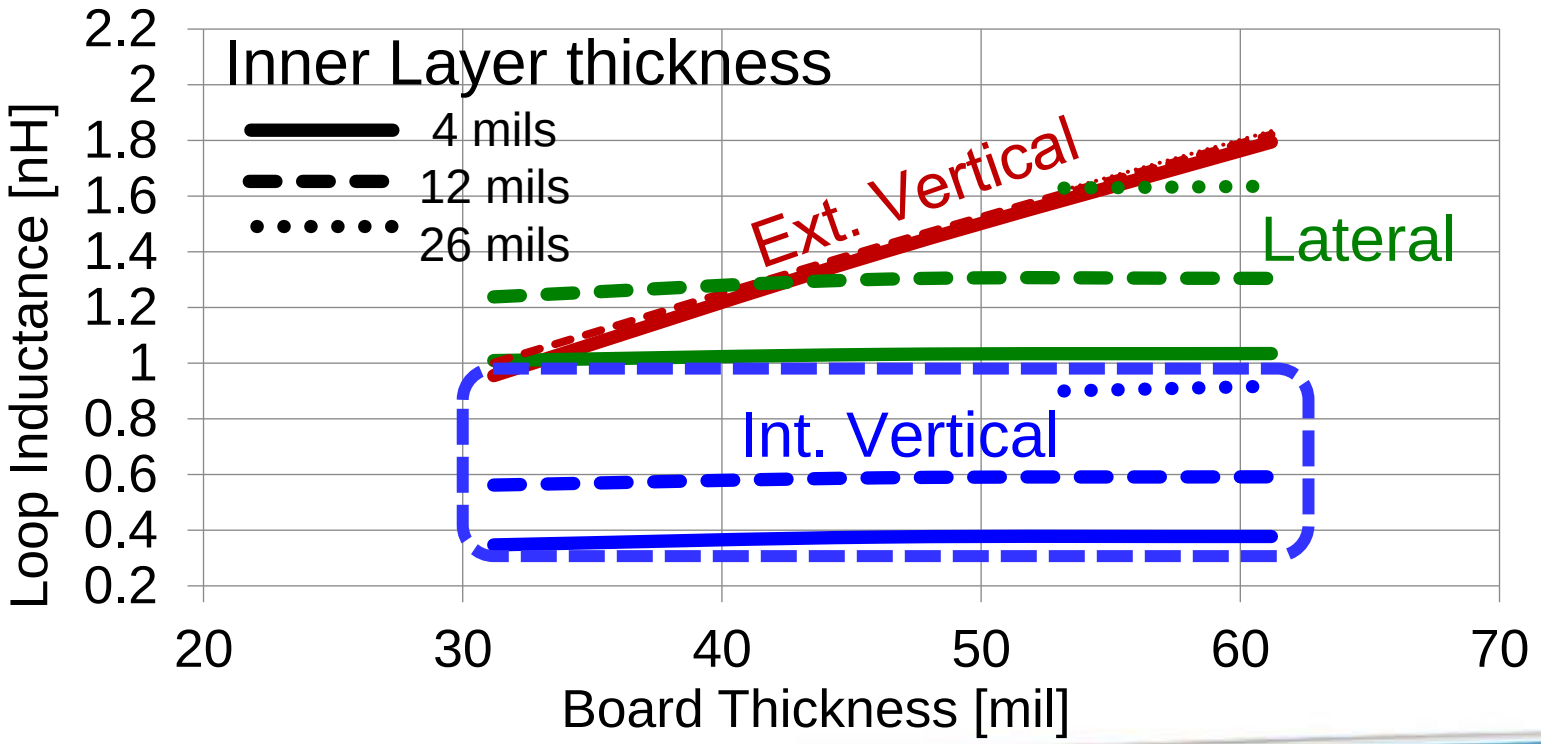
Lateral

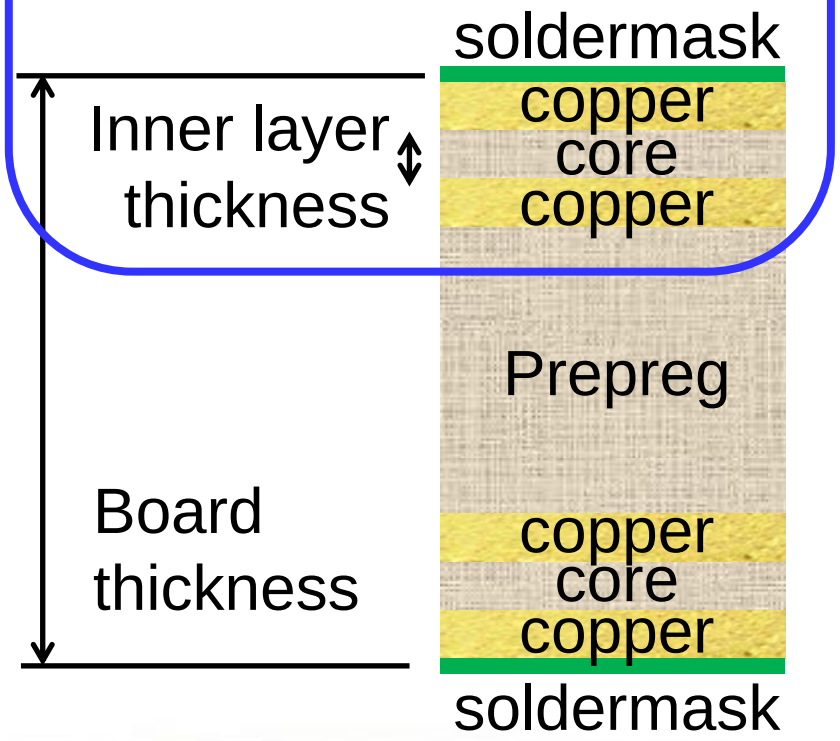


Ext. Vertical



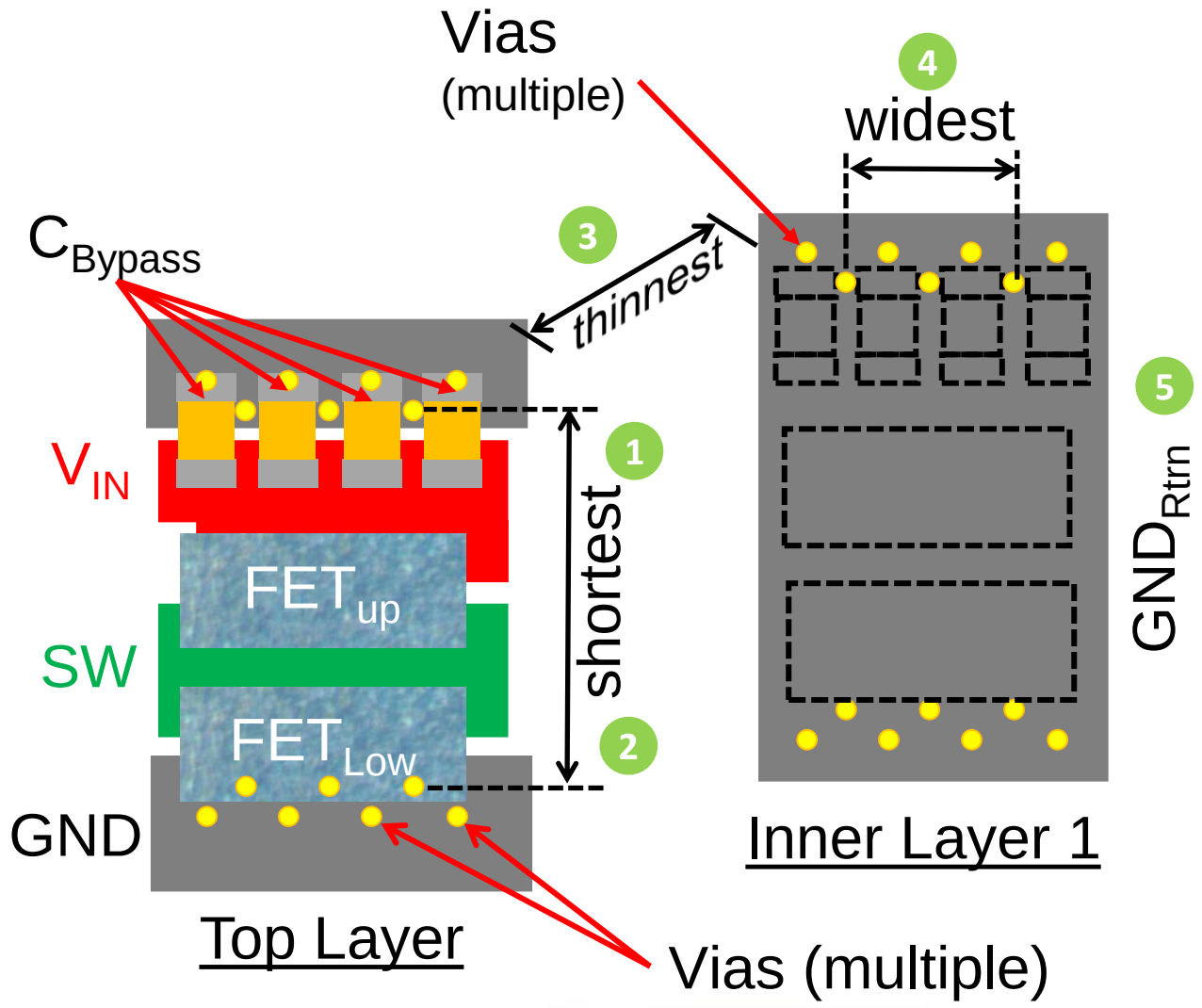
Int. Vertical
Best Choice





Getting to a Low Inductance Layout

1. Components: Vertically close
2. Vias: Close to the innermost electrical connection
3. Substrate: Thinnest permissible thickness between outer and first inner layer
4. Via Connections: Spread out at innermost connect
5. Ground Return: doesn't need to carry full current

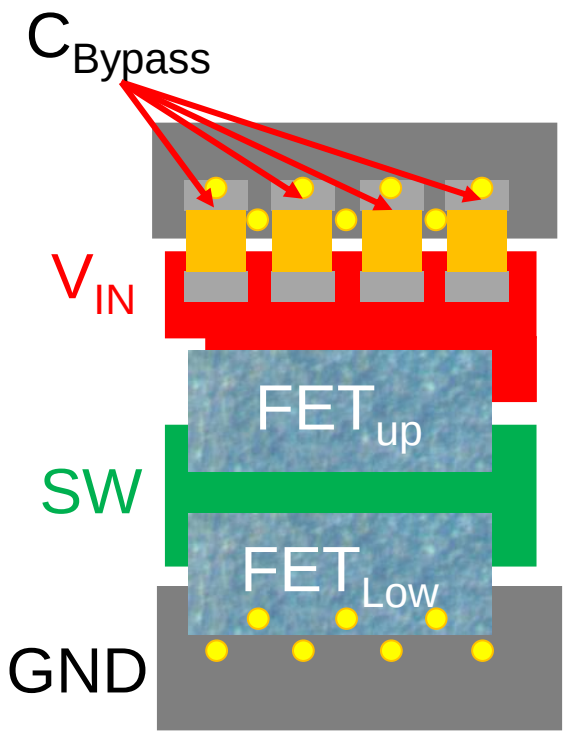


Getting to a Low Inductance Layout

Variations: vertically rotate caps & FETs

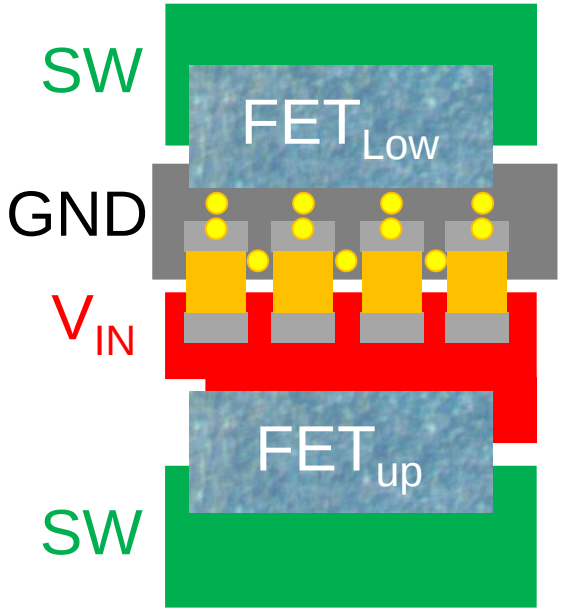
- Original: Caps → top FET → bottom FET
  - Ground on 2nd layer
- Variation 1: top FET → bottom FET → caps
  - Vin on 2nd layer
- Variation 2: bottom FET → caps → top FET
  - Switch node on 2nd layer.. Buried
  - FETs a bit separated, better for thermals

Original



Top Layer

Variation 2

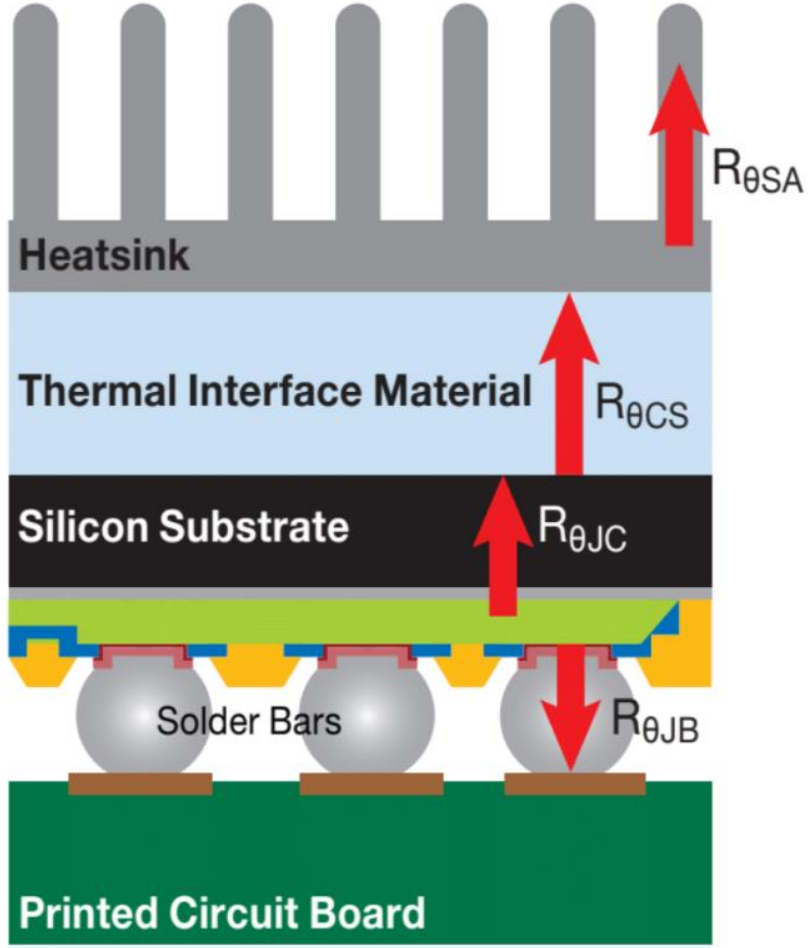


Top Layer

Thermal Management

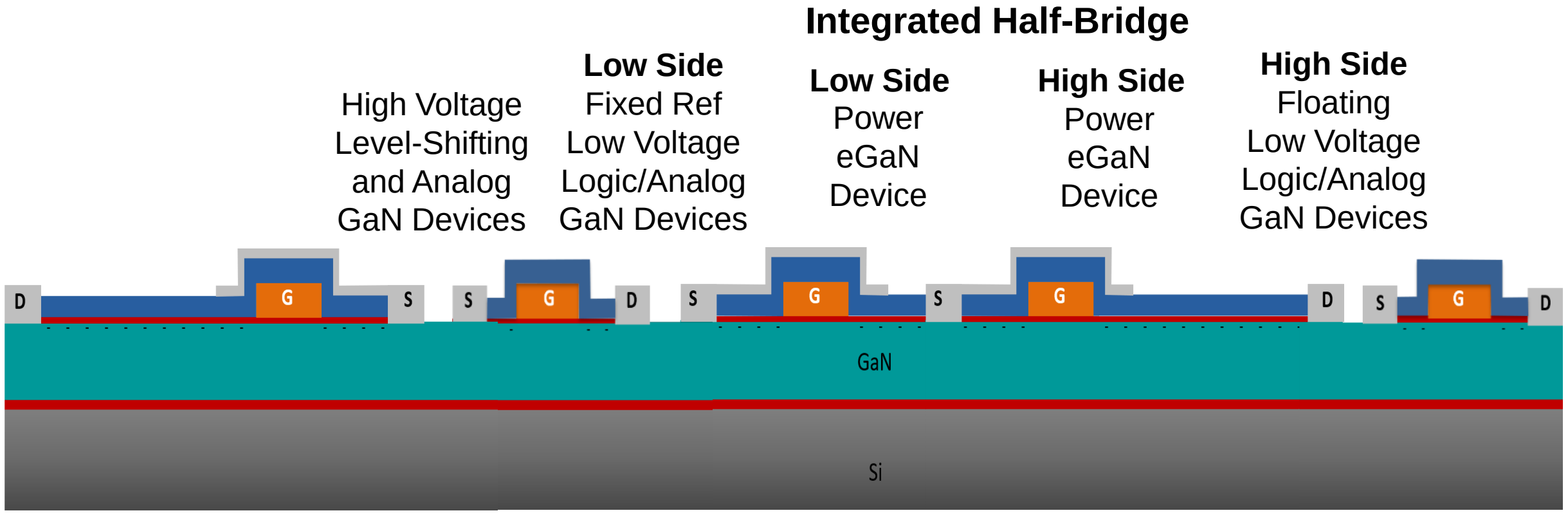
- GaN FETs are smaller than Silicon MOSFETs
  - Thus the concern: how to get the heat out?
- Thermal advantages for GaN FETs:
  - Lateral
    - no lead frame needed, so thermal connection direct to die
  - Less heat generated, due to improved switching losses
  - Many FETs have thermal connections at Source potential
  - Conduction top & bottom

- Examples
  - GaN Systems, 650 V: 0.27 deg. C/W (GS-065-060-3-T)
  - EPC, 100 V: QFN, 0.2 deg. C/W (EPC2302)
  - Transphorm, 650 V, 0.8 deg C/W (TP65H035G4WS)
  - Navitas, 650 V IC, QFN: 1.2 deg C/W (NV6128)



GaN Integration

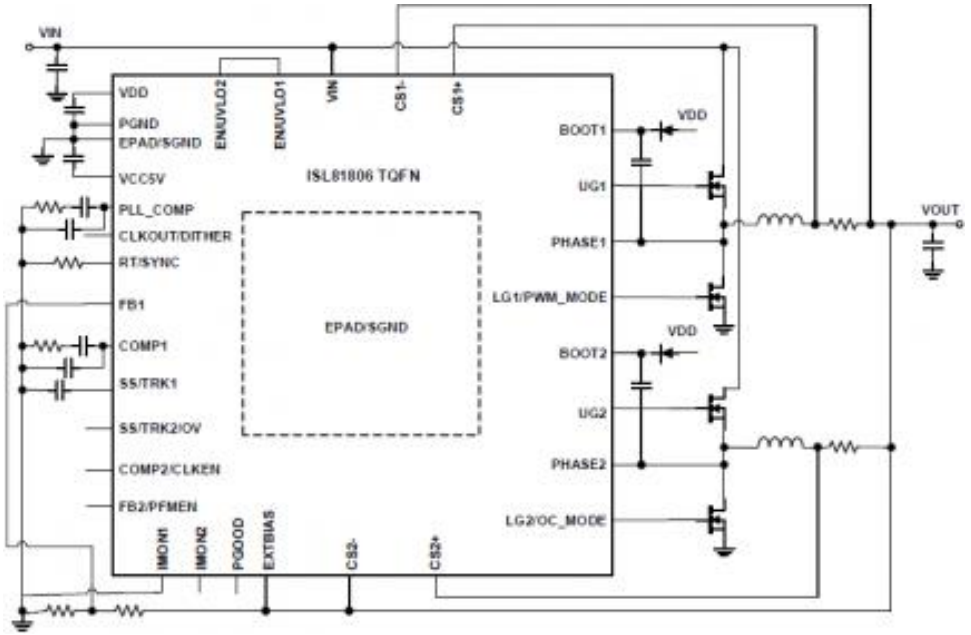
Lateral FETs allow various voltages and Rds,on FETs on one die:

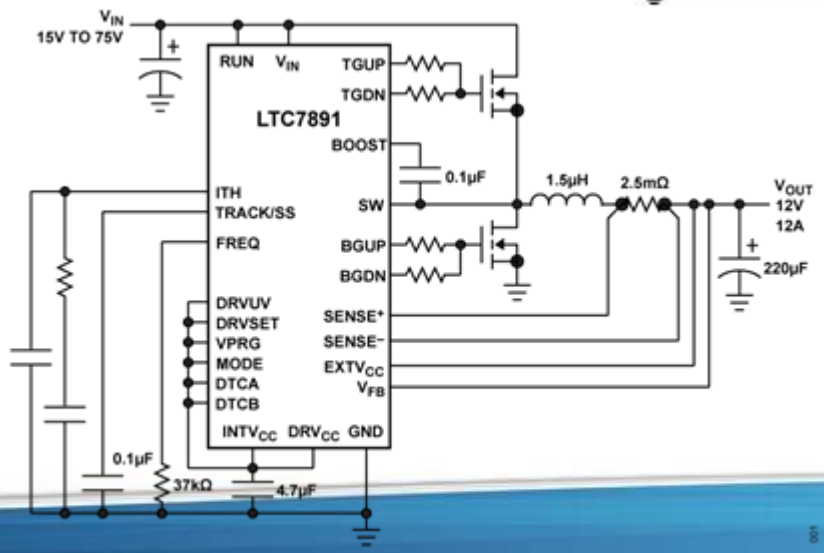


GaN Controller Advances

GaN FET-compatible analog controllers

- First step was adapting existing controllers
  - But non-optimum dead time, gate clamp, etc.
- Now, controllers made-for-GaN:
  - Renesas: 2-phase buck (ISL81806), 2-phase boost (ISL81807)
  - Analog Devices: buck (LTC7891)





A look at future GaN advancements

GaN future advancements coming:

- Generational Improvement
  - 2021: GaN FETs are 300x away from theoretical performance limit
  - 2023: Approaching a 2x improvement vs. 2021
  - This leaves 150x for future years
- GaN power ICs
  - Now: Power FETs + gate drivers
  - Future: other functions, higher voltage, etc.
  - Leading to wider adaption

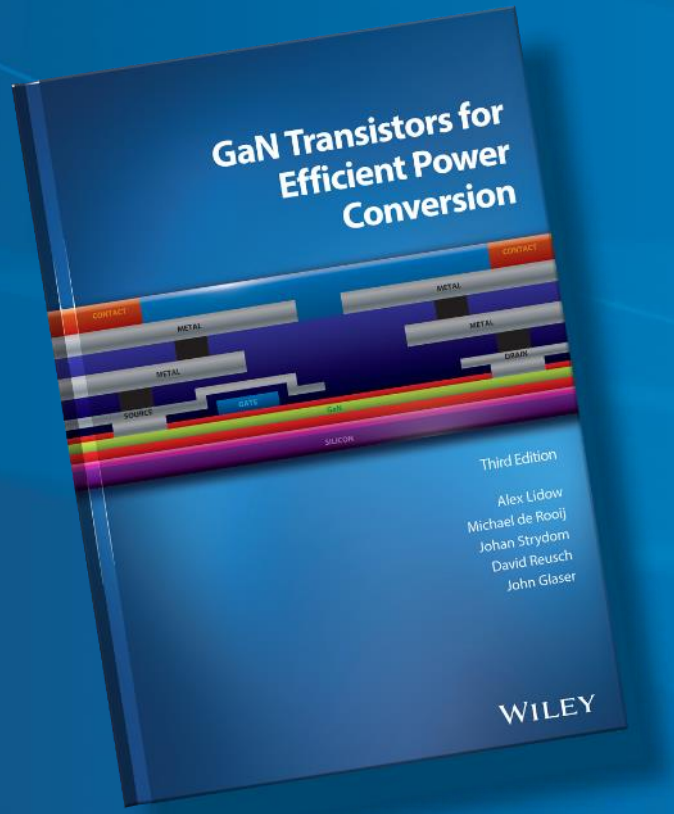
A look at future GaN advancements

GaN future advancements coming:

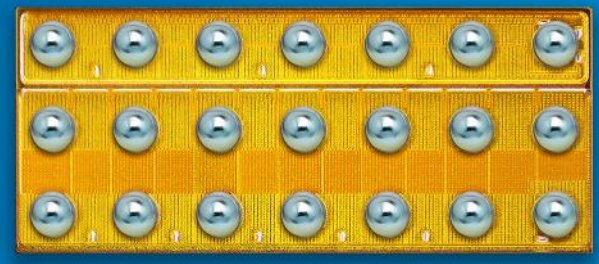
- Other future potential advancements…
  - Made-for-GaN controllers and drivers
    - DC-DC, Motor drivers, synchronous rectification, etc.
  - New packaging
  - Automotive-approved GaN FETs and GaN ICs
    - To standard AEC-Q101 and –Q100
  - Radiation Hardened GaN FETs & GaN ICs

EFFICIENT POWER CONVERSION

How To GaN Video Series

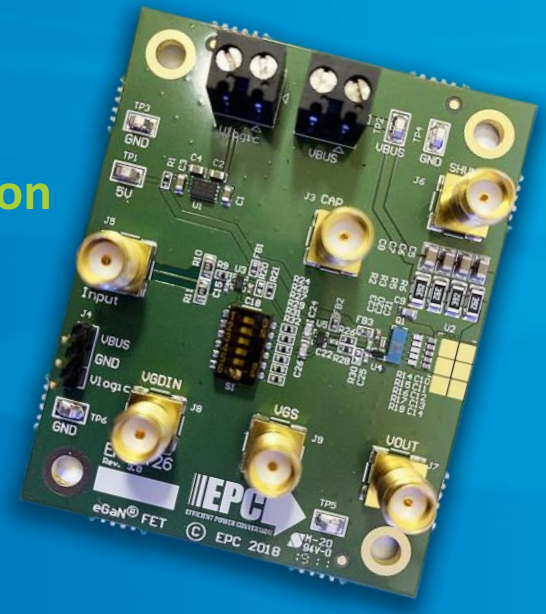


3rd Edition Textbook



eGaN® FETs and ICs

Evaluation Kits



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