



LI IEEE 2022

Louis Diana SMTS

Avoid Design Problems Using Worst Case Analysis Calculations

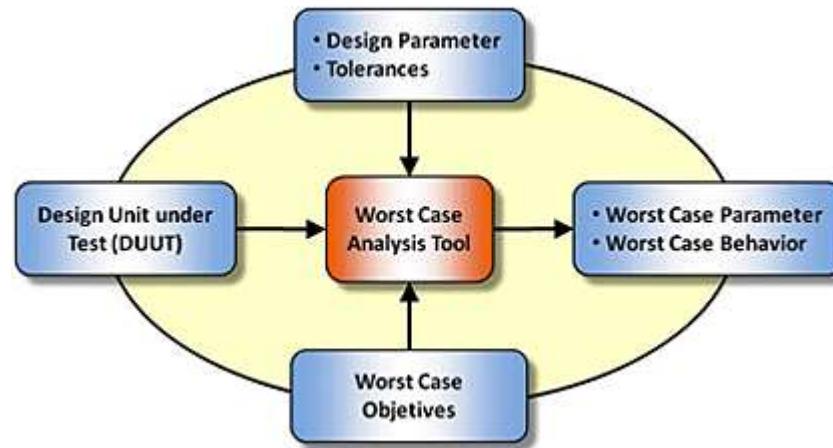
2nd Edition

Agenda

- Discussion on what is worst case analysis
- Different types of worst case analysis – i.e.: Extreme value, RSS
- Discussion on electronic component tolerances – resistors, capacitors, and Inductors, with an inductor saturation example.
- Example 1: Output voltage regulation. Reference and IC tolerance included.
- Example 2: Feedback loop stability WCA.
- Example 3: MOSFET Power dissipation. FET and Diode tolerances included.

Worst Case Analysis Definition

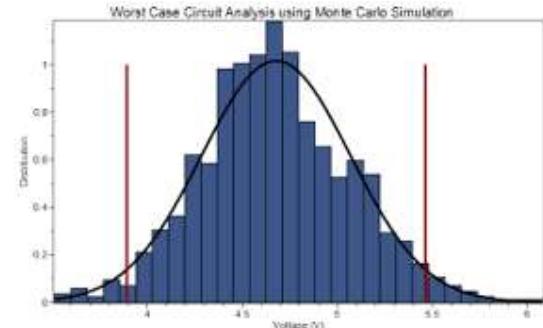
- A worst-case analysis is an assessment of a circuits functional performance, accounting for tolerances, such as **Beginning of life (BOL)**, environmental (**Temperature**), aging **End of Life (EOL)**, and, in the case of Space applications, radiation tolerances.



Worst Case Analysis Method Types

- **Extreme Value Analysis (EVA)** This is an estimate of the most extreme limits of the circuit's components and function.
- **Root Sum Square (RSS)** method works on a statistical approach. It assumes that most of the components fall to the mid of the tolerance zone rather than at the extreme ends.
- **Monte Carlo analysis**, in which parameters are randomly selected from a distribution, and the circuit simulated, anywhere from 1000 to 100000 times.

$$\Delta Y = \sqrt{\sum_{i=1}^n \delta_i^2}$$



Worst Case Analysis component Tolerances

Resistor Tolerances

$\text{deLT} := 75$

$\text{tol_rd1_bol} := 0.1\%$

$\text{tol_rd2_bol} := 1\%$

$\text{tol_rd3_bol} := 1\%$

$\text{tol_rd4_bol} := 10\%$

$\text{tol_rd1_eol} := 0.5\%$

$\text{tol_rd2_eol} := 0.5\%$

$\text{tol_rd3_eol} := 0.5\%$

$\text{tol_rd4_eol} := 0.5\%$

EOL obtained from component manufacturer,
or engineering APL

$\text{tol_rd1_temp} := 25 \cdot 10^{-6} \cdot \text{deLT}$ ppm /C

$\text{tol_rd2_temp} := 100 \cdot 10^{-6} \cdot \text{deLT}$ ppm/C

$\text{tol_rd3_temp} := 250 \cdot 10^{-6} \cdot \text{deLT}$ ppm /C

$\text{tol_rd4_temp} := 2000 \cdot 10^{-6} \cdot \text{deLT}$ ppm /C

Variations

$k1 := (\text{tol_rd1_bol} + \text{tol_rd1_eol} + \text{tol_rd1_temp})$

$k1 = 7.875 \cdot 10^{-3}$

$k2 := (\text{tol_rd2_bol} + \text{tol_rd2_eol} + \text{tol_rd2_temp})$

$k2 = 0.023$

$\text{xr23} := 53.6 \cdot k$

$\text{xr23min} := \text{xr23} \cdot (1 - k1)$

$\text{xr23max} := \text{xr23} \cdot (1 + k1)$

$$\text{xr23min} = 5.318 \cdot 10^4$$

$$\text{xr23max} = 5.402 \cdot 10^4$$

Worst Case Analysis component Tolerances

Capacitor Tolerances

$\text{deltT} := 75$

$\text{tol_npo_bol} := 5\%$

$\text{tol_npo_eol} := 0.5\%$

$\text{tol_npo_temp} := 30 \cdot 10^{-6} \cdot \text{deltT}$

$\text{tol_bx_bol} := 10\%$

$\text{tol_bx_eol} := 21\%$

$\text{tol_bx_temp} := 15\%$

$\text{tol_x7r_bol} := 10\%$

$\text{tol_x7r_eol} := 21\%$

$\text{tol_x7r_temp} := 15\%$

Variations

$k3 := (\text{tol_npo_bol} + \text{tol_npo_eol} + \text{tol_npo_temp})$

$k3 = 0.057$

$k4 := (\text{tol_bx_bol} + \text{tol_bx_eol} + \text{tol_bx_temp})$

$k4 = 0.46$

$k5 := (\text{tol_x7r_bol} + \text{tol_x7r_eol} + \text{tol_x7r_temp})$

$k5 = 0.46$

$a1c12 := 39 \cdot p$

$a1c12min := a1c12 \cdot (1 - k3)$

$a1c12max := a1c12 \cdot (1 + k3)$

EOL obtained from component manufacturer,
or engineering APL

BX characteristics are identical
to X7R dielectric, with the added
restriction that the Temperature-
Voltage Coefficient (TVC) is not
to exceed $-25\% \Delta C$ at rated
voltage, over the operating
temperature range ($-55^\circ C$ to
 $125^\circ C$).

$$a1c12min = 3.833 \cdot 10^{-11}$$

$$a1c12max = 3.967 \cdot 10^{-11}$$

Worst Case Analysis component Tolerances

Inductor Tolerances

Part number ¹	Inductance ² ±20% (μH)	DCR (mOhms) ³		SRF typ ⁴ (MHz)	Isat ⁵ (A)	Irms (A) ⁶	
		typ	max			20°C rise	40°C rise
XAL7030-161ME	0.16	1.15	1.26	158	60.0	24.9	32.5
XAL7030-301ME	0.30	1.75	1.92	101	41.0	21.0	27.6
XAL7030-601ME	0.60	3.00	3.30	72	36.0	18.0	23.0
XAL7030-102ME	1.0	4.55	5.00	52	28.0	16.1	21.8
XAL7030-152ME	1.5	7.60	8.36	39	23.5	11.9	15.0
XAL7030-222ME	2.2	13.7	15.07	29	18.0	10.0	12.9
XAL7030-272ME	2.7	15.7	17.30	32	12.8	9.2	11.4
XAL7030-332ME	3.3	19.5	21.45	25	12.3	8.0	10.0
XAL7030-472ME	4.7	26.1	30.00	21	10.1	6.9	9.0
XAL7030-562ME	5.6	28.1	32.32	17	9.8	5.3	7.3
XAL7030-682ME	6.8	45.0	51.75	15	8.7	4.4	6.8
XAL7030-822ME	8.2	53.0	60.94	13	8.4	2.9	5.9
XAL7030-103ME	10	60.4	69.46	12	7.7	2.6	5.3

5. DC current at 25°C that causes an inductance drop of 30% (typ) from its value without current.

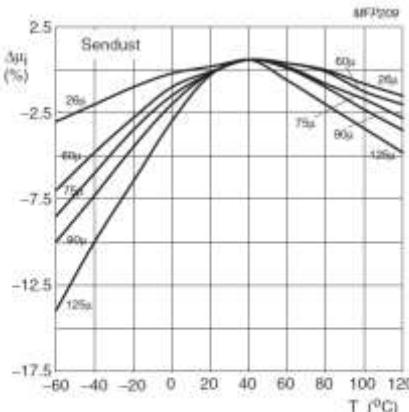
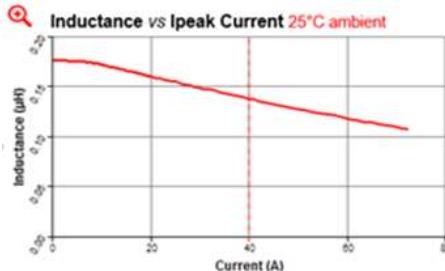
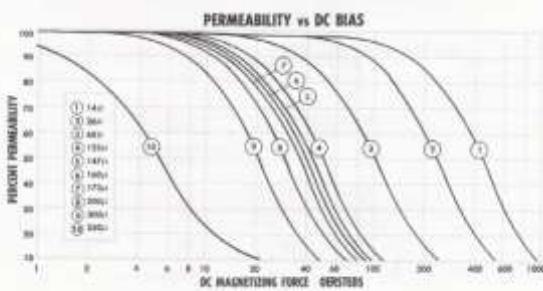


Fig.2 Initial permeability as a function of temperature.



$$L_{\text{mm}} := \frac{4 \cdot 3.14 \cdot u \cdot \text{turns}^2 \cdot (Ae)}{le \cdot 10^8}$$

Where:

Linductance = Henry's

μ = core permeability

N = number of turns

A_e = core cross-section (mm^2)

le = core magnetic path length (mm)

Worst Case Analysis Inductance rolloff example

Example of saturation current

$V_{in} = 12V$ $V_o = .9V$
 $V_{inmax} = 13.2V$ $I_{omax} = 40A$
 $V_{inmin} = 10.8V$ $I_{omin} = 4A$
 $f = 650\text{khz}$

Now what happens if I push I_{omax} to 60A and reduce the inductance by 30%

$V_{in} = 12V$ $V_o = .9V$
 $V_{inmax} = 13.2V$ $I_{omax} = 60A$
 $V_{inmin} = 10.8V$ $I_{omin} = 4A$
 $f = 650\text{khz}$

$$L_{out} = 160\text{nH}$$

$$L_{out} = 112\text{nH}$$

$$I_{peak} = 45.6A$$

Peak inductor current

$$I_{peak} = 68.7A$$

Peak inductor current

Rule of thumb derate I_{sat} by 30 to 40%

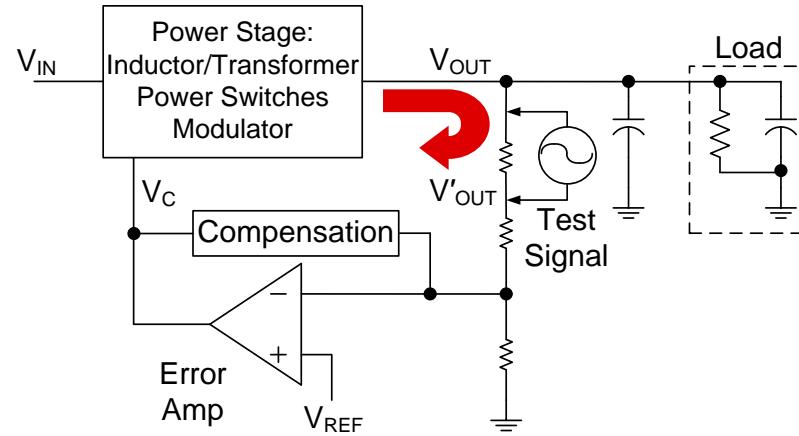
Worst Case Analysis Output regulation example

Problem statement

- What is my worst case output voltage regulation

Procedure

- Find tolerances for Vref, error-amp, and resistor divider.
- Write equation for feedback regulation
- Calculate sensitivity of variables.
- Solve equation



Worst Case Analysis Output regulation example

Reference tolerance

$$\text{tol_TL431_bol} := 0.5\%$$

$$\text{tol_TL431_eol} := .25\%$$

$$\text{tol_TL431_temp} := 60 \cdot 10^{-6} \cdot \Delta T$$

- Reference Voltage Tolerance at 25°C
 - 0.5% (B Grade)
 - 1% (A Grade)
 - 2% (Standard Grade)

Reference Variation

$$V_{ref} := 2.495$$

$$\text{TL431vrefmin} := V_{ref} \cdot (1 - \text{tol_TL431_bol}) \cdot (1 - \text{tol_TL431_eol}) \cdot (1 - \text{tol_TL431_temp})$$

$$\text{TL431vrefmin} = 2.465$$

$$\text{TL431vrefmax} := V_{ref} \cdot (1 + \text{tol_TL431_bol}) \cdot (1 + \text{tol_TL431_eol}) \cdot (1 + \text{tol_TL431_temp})$$

$$\text{TL431vrefmax} = 2.525$$

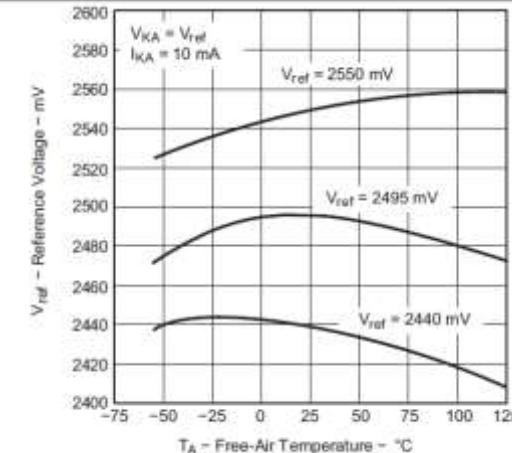


Figure 1. Reference Voltage vs Free-Air Temperature

Worst Case Analysis Output regulation example

Op-amp tolerance

Op-amp dc error sources include:

- Input offset voltage VOS
 - Input bias current IB
 - Input offset current IOS
 - Open loop gain

From LM158 Data sheet:

V_{os} bol = 7mV from -55c to 125c

Vos temp = 15uV/c

Vos eol = hard to find check with Manufacturer

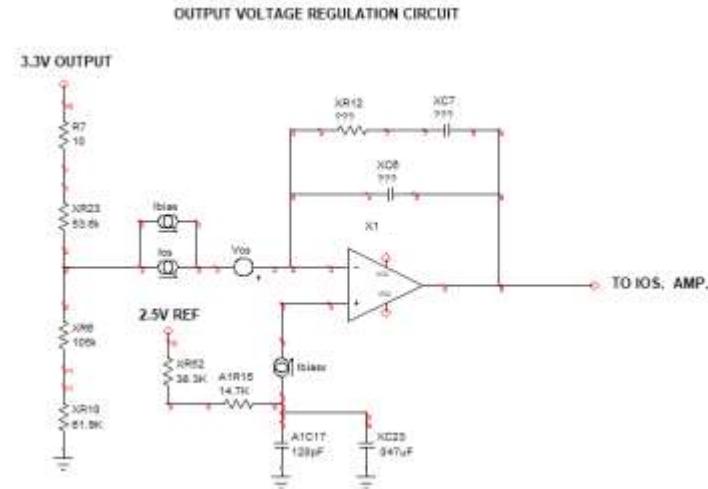
Ib_bol = 300nA from -55c to 125c,

Ios bol = 100nA from -55c to 125c

`los_temp = 200pA/c, los_eol = hard to find check with Manufacturer`

Open loop gain min = 35V/mV =35000

Open loop gain typ = 140V/mV = 140000



Worst Case Analysis Output regulation example

Below is a sensitivity calculation to show which parts should be minimized or maximized

$$V_{\text{nom}}(V_{\text{ref}}, V_{\text{os}}, V_{\text{bias nom}}, V_{\text{bias gain nom}}, \text{xr23}, \text{r7}, \text{xr10}, \text{xr6}) := \left(\begin{array}{l} V_{\text{ref}} + V_{\text{os}} \dots \\ + V_{\text{bias nom}} \dots \\ + V_{\text{bias gain nom}} \end{array} \right) \cdot \frac{(\text{xr23} + \text{r7} + \text{xr10} + \text{xr6})}{\text{xr10} + \text{xr6}}$$

$$\frac{d}{dV_{\text{ref}}} V_{\text{nom}}(V_{\text{ref}}, V_{\text{os}}, V_{\text{bias nom}}, V_{\text{bias gain nom}}, \text{xr23}, \text{r7}, \text{xr10}, \text{xr6}) = 1.321$$

$$\frac{d}{dV_{\text{bias gain nom}}} V_{\text{nom}}(V_{\text{ref}}, V_{\text{os}}, V_{\text{bias nom}}, V_{\text{bias gain nom}}, \text{xr23}, \text{r7}, \text{xr10}, \text{xr6}) = 1.321$$

$$\frac{d}{dV_{\text{os}}} V_{\text{nom}}(V_{\text{ref}}, V_{\text{os}}, V_{\text{bias nom}}, V_{\text{bias gain nom}}, \text{xr23}, \text{r7}, \text{xr10}, \text{xr6}) = 1.321$$

$$\frac{d}{dxr23} V_{\text{nom}}(V_{\text{ref}}, V_{\text{os}}, V_{\text{bias nom}}, V_{\text{bias gain nom}}, \text{xr23}, \text{r7}, \text{xr10}, \text{xr6}) = 1.504 \cdot 10^{-5}$$

$$\frac{d}{dV_{\text{bias nom}}} V_{\text{nom}}(V_{\text{ref}}, V_{\text{os}}, V_{\text{bias nom}}, V_{\text{bias gain nom}}, \text{xr23}, \text{r7}, \text{xr10}, \text{xr6}) = 1.321$$

$$\frac{d}{dr7} V_{\text{nom}}(V_{\text{ref}}, V_{\text{os}}, V_{\text{bias nom}}, V_{\text{bias gain nom}}, \text{xr23}, \text{r7}, \text{xr10}, \text{xr6}) = 1.504 \cdot 10^{-5}$$

$$\frac{d}{dxr10} V_{\text{nom}}(V_{\text{ref}}, V_{\text{os}}, V_{\text{bias nom}}, V_{\text{bias gain nom}}, \text{xr23}, \text{r7}, \text{xr10}, \text{xr6}) = -4.83 \cdot 10^{-6}$$

$$\frac{d}{dxr6} V_{\text{nom}}(V_{\text{ref}}, V_{\text{os}}, V_{\text{bias nom}}, V_{\text{bias gain nom}}, \text{xr23}, \text{r7}, \text{xr10}, \text{xr6}) = -4.83 \cdot 10^{-6}$$

Worst Case Analysis Output regulation example

Resistor divider tolerance

$$\text{Reqmax} := \frac{1}{\left(\frac{1}{\text{xr23max} + \text{r7max}} + \frac{1}{\text{xr10min} + \text{xr6min}} \right)}$$

$$\text{Reqmax} = 4.074 \cdot 10^4$$

$$\text{a1r15max} = 1.503 \cdot 10^4$$

$$\text{Reqmin} := \frac{1}{\left(\frac{1}{\text{xr23min} + \text{r7min}} + \frac{1}{\text{xr10max} + \text{xr6max}} \right)}$$

$$\text{Reqmin} = 4.041 \cdot 10^4$$

$$\text{a1r15min} = 1.437 \cdot 10^4$$

Worst Case Analysis Output regulation example

Voltage error due to the offset current, bias current, A1r15 and Req

$$V_{bias\ min} := R_{eq\ min} \cdot (I_{bias} - I_{os}) - I_{bias} \cdot (a_{1r15\ max} + x_{r52\ max}) \quad V_{bias\ min} = -6.685 \cdot 10^{-4}$$

$$V_{bias\ max} := R_{eq\ max} \cdot (I_{bias} + I_{os}) - I_{bias} \cdot (a_{1r15\ min} + x_{r52\ min}) \quad V_{bias\ max} = 1.748 \cdot 10^{-4}$$

$$V_{bias\ nom} := \frac{V_{bias\ max} + V_{bias\ min}}{2} \quad V_{bias\ nom} = -2.469 \cdot 10^{-4}$$

Voltage error due to the gain in the error amplifier

$$V_{out} = (V_{pos} - V_{neg}) \times A_v$$

$$V_{in} = V_{pos} - V_{neg}$$

$$V_{bias\ gain} = V_{in}$$

$v_{oh} := 5$ **v_{oh} is the V_{dd} voltage on the error amp. therefore the maximum output voltage on the error amp.**

$$V_{bias_gain\ max} := \frac{v_{oh}}{O_{LG\ min}} \quad V_{bias_gain\ max} = 1.429 \cdot 10^{-4}$$

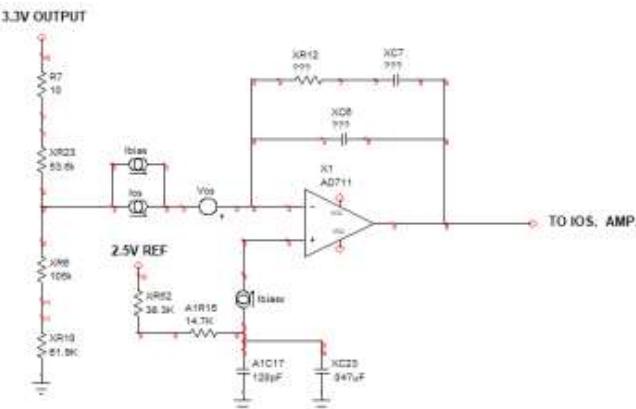
This is the min. and max. voltage required for op-amp

$$V_{bias_gain\ min} := \frac{v_{oh}}{O_{LG\ max}} \quad V_{bias_gain\ min} = 3.571 \cdot 10^{-5}$$

operation

$$V_{bias_gain\ nom} := \frac{V_{bias_gain\ max} + V_{bias_gain\ min}}{2} \quad V_{bias_gain\ nom} = 8.929 \cdot 10^{-5}$$

OUTPUT VOLTAGE REGULATION CIRCUIT



Worst Case Analysis Output regulation example

The total output voltage error due to Vref, Vos, Vbias, Req, and A1r15

$$V_{omax} := (v_{refmax} + V_{os} + V_{biasmax} + V_{bias_gainmax}) \cdot \frac{(x_{r23max} + r7max + x_{r10min} + x_{r6min})}{x_{r10min} + x_{r6min}} \quad V_{omax} = 3.37$$

$$V_{omin} := (v_{refmin} - V_{os} + V_{biasmin} + V_{bias_gainmin}) \cdot \frac{(x_{r23min} + r7min + x_{r10max} + x_{r6max})}{x_{r10max} + x_{r6max}} \quad V_{omin} = 3.236$$

The percent delta for Vout is as follows

$$\text{V}_{onom} := 3.3$$

$$V_{odelta\%pos} := \frac{V_{omax} - \text{V}_{onom}}{\text{V}_{onom}} \cdot 100 \quad V_{odelta\%pos} = 2.126$$

$$V_{odelta\%neg} := \frac{\text{V}_{onom} - V_{omin}}{\text{V}_{onom}} \cdot 100 \quad V_{odelta\%neg} = 1.926$$

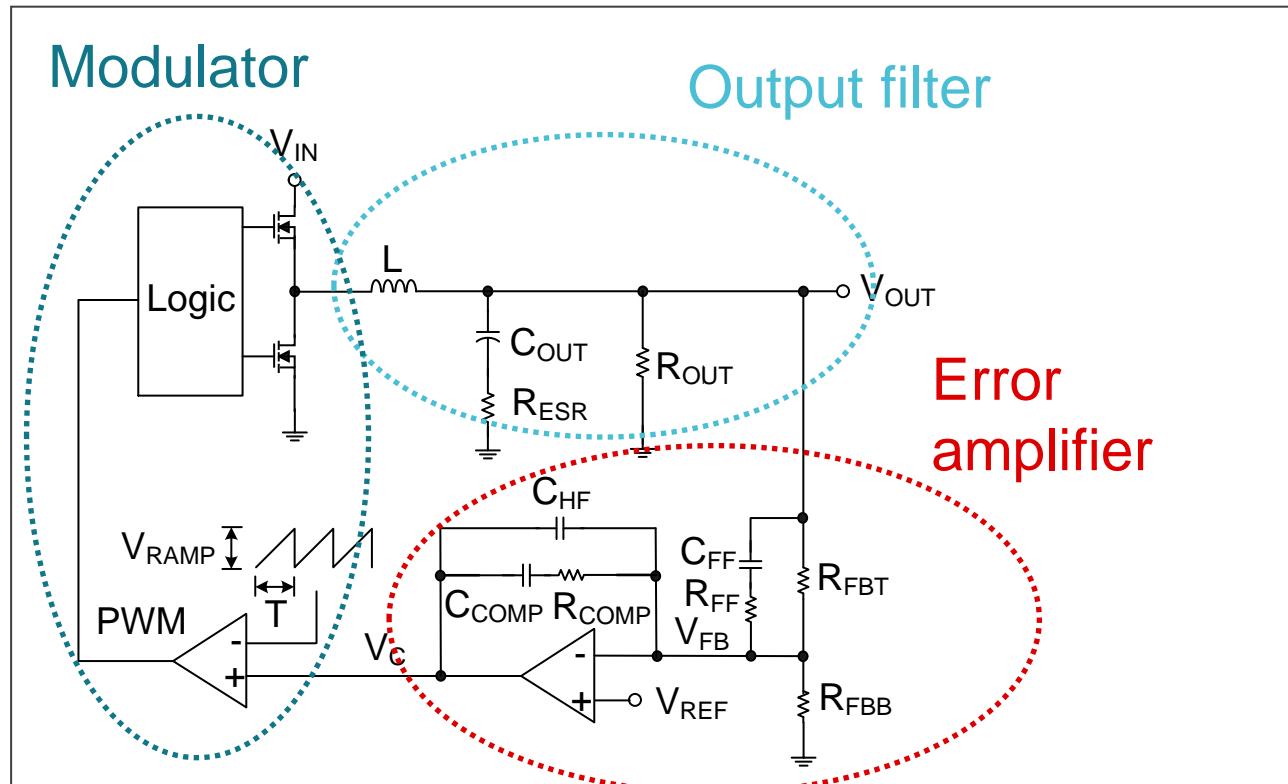
Voltage-mode buck loop stability worst case

Problem statement

- What is my worst case loop stability

Procedure

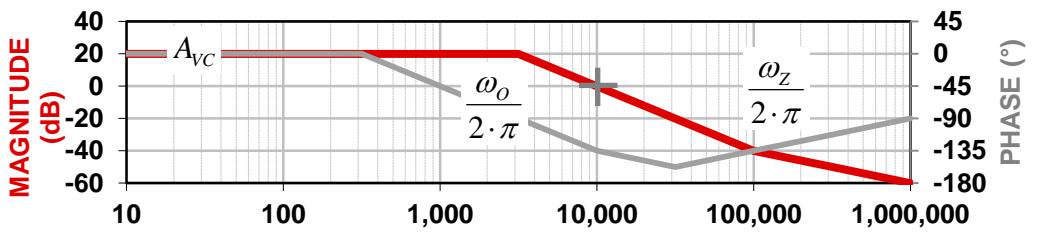
- Find tolerances for L, Cout, and compensation components.
- Write equation for the power stage, and the type 3 error amp
- Plot the bode plot for each section
- Plot the loop bode plot



Voltage-mode buck loop stability worst case

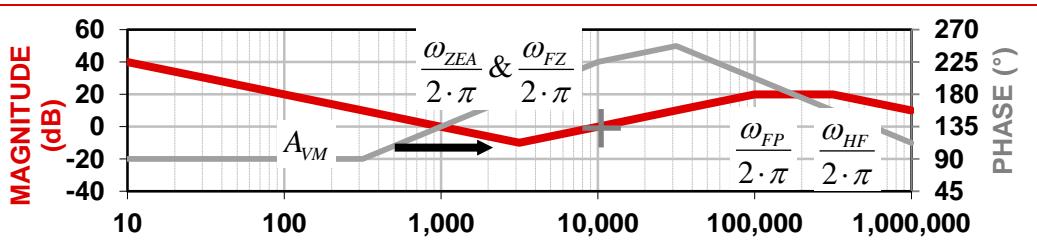
Power stage

$$\frac{\hat{v}_{OUT}}{\hat{v}_C} \approx A_{VC} \cdot \frac{1 + \frac{s}{\omega_Z}}{1 + \frac{s}{Q_O \cdot \omega_O} + \frac{s^2}{\omega_O^2}}$$



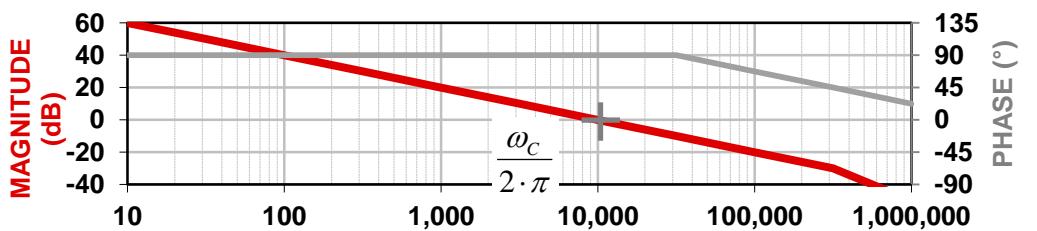
Error amplifier

$$\frac{\hat{v}_C}{\hat{v}'_{OUT}} \approx -A_{VM} \cdot \frac{\left(1 + \frac{\omega_{ZEA}}{s}\right) \cdot \left(1 + \frac{s}{\omega_{FZ}}\right)}{\left(1 + \frac{s}{\omega_{FP}}\right) \cdot \left(1 + \frac{s}{\omega_{HF}}\right)}$$

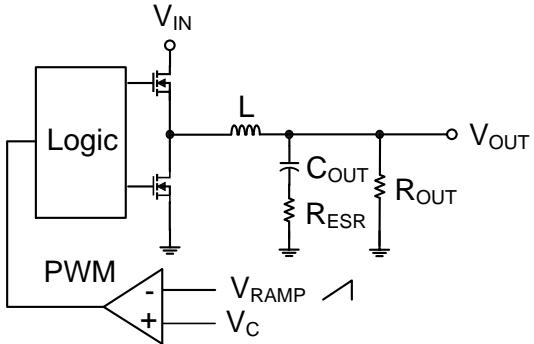


Control loop

$$\frac{\hat{v}_{OUT}}{\hat{v}'_{OUT}} = \frac{\hat{v}_{OUT}}{\hat{v}_C} \cdot \frac{\hat{v}_C}{\hat{v}'_{OUT}}$$



Voltage-mode buck power stage

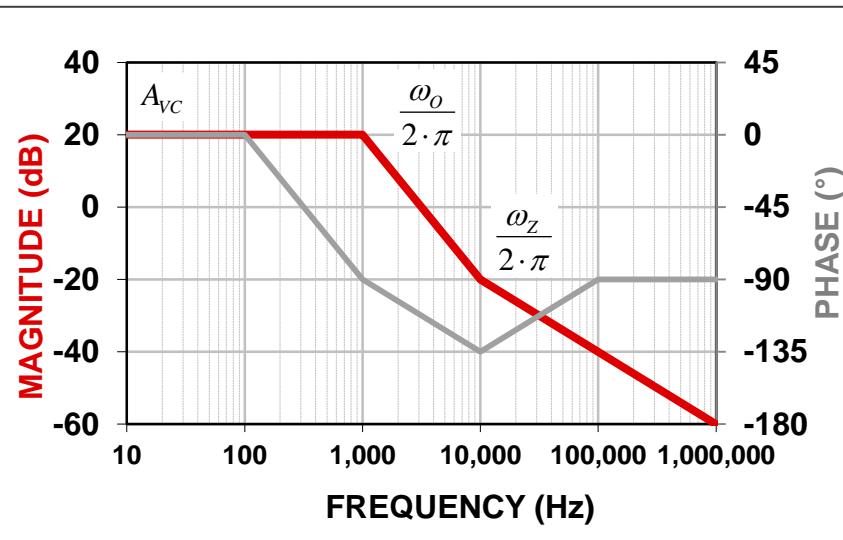


$$A_{VC} = \frac{V_{IN}}{V_{RAMP}}$$

$$\omega_o = \frac{1}{\sqrt{L \cdot C_{OUT}}}$$

$$Q_o = \frac{R_{OUT}}{\sqrt{L/C_{OUT}}}$$

$$\omega_z = \frac{1}{R_{ESR} \cdot C_{OUT}}$$



$$\frac{\hat{v}_{OUT}}{\hat{v}_C} = A_{VC} \cdot \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{Q_o \cdot \omega_o} + \frac{s^2}{\omega_o^2}}$$

Loop stability worst case

$$\text{Vinmin} := 26\text{V}$$

$$\text{Vrampmin} := 1.8\text{V}$$

$$\text{gainmin} := \frac{\text{Vinmin}}{\text{Vrampmax}}$$

$$\text{gainmax} := \frac{\text{Vinmax}}{\text{Vrampmin}}$$

$$\text{Loutmin} := \text{Lout_act} - \text{Lout_act} \cdot 20\%$$

$$\text{Loutmax} := \text{Lout_act} + \text{Lout_act} \cdot 20\%$$

$$\text{Coutmin} := \text{Cout1} \cdot (1 - \text{K5})$$

$$\text{Coutmax} := \text{Cout1} \cdot (1 + \text{K5})$$

$$\text{ESRCoutmax} := \text{RCout1} \cdot (1 + 20\%)$$

$$\text{ESRCoutmin} := \text{RCout1} \cdot (1 - 20\%)$$

$$R_{Lmin} := 75 \cdot \Omega$$

$$R_{Lmax} := 5 \cdot \Omega$$

$$\text{Vinmax} := 30\text{V}$$

$$\text{Vrampmax} := 2.2\text{V}$$

$$\text{gainmin} = 11.818$$

$$\text{gainmax} = 16.667$$

$$\text{Loutmin} = 1.76 \times 10^{-5} \text{H}$$

$$\text{Loutmax} = 2.64 \times 10^{-5} \text{H}$$

$$\text{Coutmin} = 2.538 \times 10^{-4}$$

$$\text{Coutmax} = 6.862 \times 10^{-4}$$

$$\text{ESRCoutmax} = 0.06$$

$$\text{ESRCoutmin} = 0.04$$

$$\text{K5} := .46$$

$$\omega := (100, 200.. 6400000)$$

$$\text{Cout1} := 470 \cdot 10^{-6}$$

$$\text{RCout1} := 0.05$$

$$\text{H}$$

$$fzeromax := \frac{1}{\text{ESRCoutmin} \cdot \text{Coutmin}}$$

$$fpolemax := \frac{1}{\sqrt{\frac{\text{Loutmin}}{\text{H}} \cdot \text{Coutmin}}}$$

$$Qomax := \frac{\frac{\Omega}{\text{R}_{Lmax}}}{\sqrt{\frac{\text{Loutmin}}{\text{H}}}}$$

$$\text{PSmin}(\omega) := \text{gainmin} \cdot \frac{1 + \frac{i \cdot \omega}{fzeromax}}{1 + \frac{i \cdot \omega}{\text{Qomin} \cdot fpolemin} + \frac{\omega^2}{fpolemin^2}}$$

$$fzeromin := \frac{1}{\text{ESRCoutmax} \cdot \text{Coutmax}}$$

$$fpolemin := \frac{1}{\sqrt{\frac{\text{Loutmax}}{\text{H}} \cdot \text{Coutmax}}}$$

$$Qomin := \frac{\frac{\Omega}{\text{R}_{Lmin}}}{\sqrt{\frac{\text{Loutmax}}{\text{H}}}}$$

$$\text{PSmax}(\omega) := \text{gainmax} \cdot \frac{1 + \frac{i \cdot \omega}{fzeromax}}{1 + \frac{i \cdot \omega}{\text{Qomax} \cdot fpolemax} + \frac{\omega^2}{fpolemax^2}}$$

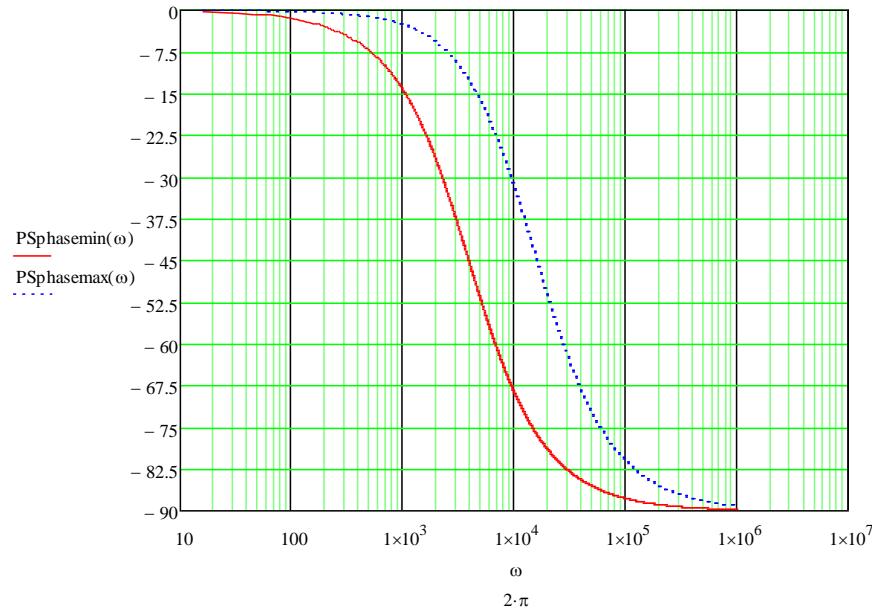
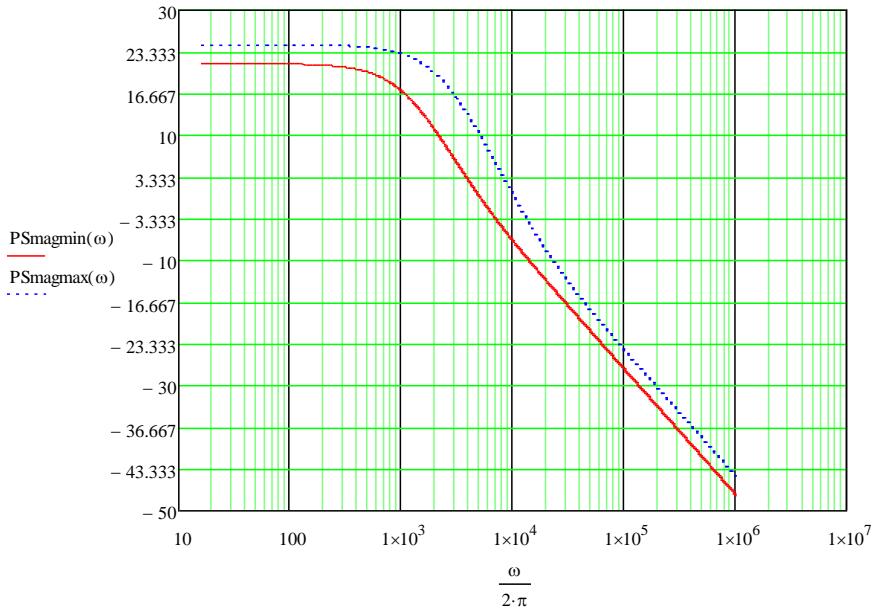
$$\text{PSmagmin}(\omega) := 20 \cdot \log(|\text{PSmin}(\omega)|)$$

$$\text{PSmagmax}(\omega) := 20 \cdot \log(|\text{PSmax}(\omega)|)$$

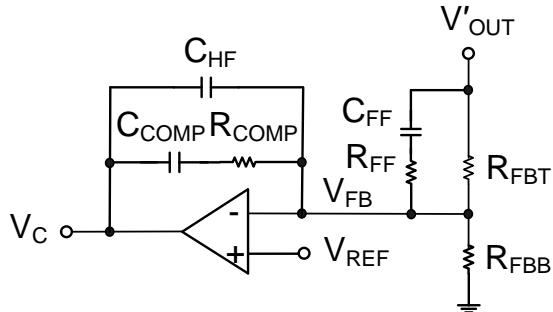
$$\text{PSphasemin}(\omega) := -\frac{180}{\pi} \cdot \arg(\text{PSmin}(\omega))$$

$$\text{PSphasemax}(\omega) := -\frac{180}{\pi} \cdot \arg(\text{PSmax}(\omega))$$

Loop stability worst case



Type III error amplifier



$$A_{VM} \approx \frac{R_{COMP}}{R_{FBT}}$$

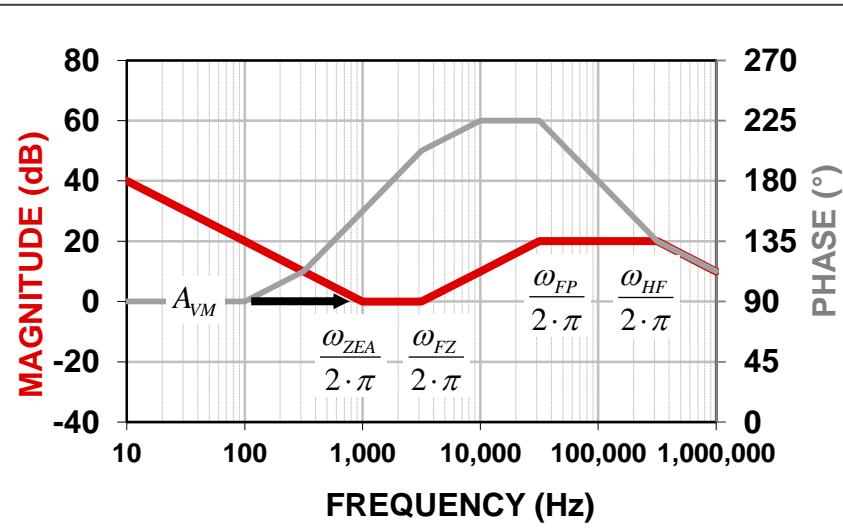
$$\omega_{ZEA} = \frac{1}{R_{COMP} \cdot C_{COMP}}$$

$$\omega_{FP} = \frac{1}{R_{FF} \cdot C_{FF}}$$

Assumptions: $C_{COMP} \gg C_{HF}$ & $R_{FBT} \gg R_{FF}$

$$\omega_{FZ} \approx \frac{1}{R_{FBT} \cdot C_{FF}}$$

$$\omega_{HF} \approx \frac{1}{R_{COMP} \cdot C_{HF}}$$



$$\frac{\hat{v}_c}{\hat{v}'_{OUT}} = -A_{VM} \cdot \frac{\left(1 + \frac{\omega_{ZEA}}{s}\right) \cdot \left(1 + \frac{s}{\omega_{FZ}}\right)}{\left(1 + \frac{s}{\omega_{FP}}\right) \cdot \left(1 + \frac{s}{\omega_{HF}}\right)} = -\frac{A_{VM} \cdot \omega_{ZEA}}{s} \cdot \frac{\left(1 + \frac{s}{\omega_{ZEA}}\right) \cdot \left(1 + \frac{s}{\omega_{FZ}}\right)}{\left(1 + \frac{s}{\omega_{FP}}\right) \cdot \left(1 + \frac{s}{\omega_{HF}}\right)}$$

Loop stability worst case

$$k1 := .007875$$

$$Rfbt := 51.1K$$

$$Rfbtmin := Rfbt \cdot ((1 - k1))$$

$$Rfbtmax := Rfbt \cdot ((1 + k1))$$

$$Rcomp := 100K$$

$$Rcompmin := Rcomp \cdot ((1 - k1))$$

$$Rcompmax := Rcomp \cdot ((1 + k1))$$

$$Chf := 2200 \cdot 10^{-12}$$

$$Chfmin := Chf \cdot (1 - K3)$$

$$Chfmax := Chf \cdot (1 + K3)$$

$$Ccomp := 1800 \cdot 10^{-12}$$

$$Ccompmin := Ccomp \cdot (1 - K3)$$

$$Ccompmax := Ccomp \cdot (1 + K3)$$

$$Cff := 1800 \cdot 10^{-12}$$

$$Cffmin := Cff \cdot (1 - K3)$$

$$Cffmax := Cff \cdot (1 + K3)$$

$$K3 := .057$$

$$Rfbfb := 10K$$

$$Rfbfbmin := Rfbfb \cdot ((1 - k1))$$

$$Rfbfbmax := Rfbfb \cdot ((1 + k1))$$

$$Rff := 26.12K$$

$$Rffmin := Rff \cdot ((1 - k1))$$

$$Rffmax := Rff \cdot ((1 + k1))$$

$$Chfmin = 2.075 \times 10^{-9}$$

$$Chfmax = 2.325 \times 10^{-9}$$

$$Ccompmin = 1.697 \times 10^{-9}$$

$$Ccompmax = 1.903 \times 10^{-9}$$

$$Cffmin = 1.697 \times 10^{-9}$$

$$Cffmax = 1.903 \times 10^{-9}$$

$$Avmin := \frac{Rcompmin}{Rfbtmax}$$

$$Avmax := \frac{Rcompmax}{Rfbtmin}$$

$$Wzeamin := \frac{1}{Rcompmax \cdot Ccompmax}$$

$$Wzeamax := \frac{1}{Rcompmin \cdot Ccompmin}$$

$$Wfzmin := \frac{1}{Rfbtmax \cdot Cffmax}$$

$$Wfzmax := \frac{1}{Rfbtmin \cdot Cffmin}$$

$$Wfpmin := \frac{1}{Rffmax \cdot Cffmax}$$

$$Wfpmax := \frac{1}{Rffmin \cdot Cffmin}$$

$$Whfmin := \frac{1}{Rcompmax \cdot Chfmax}$$

$$Whfmax := \frac{1}{Rcompmin \cdot Chfmin}$$

$$Avmin = 1.926$$

$$Avmax = 1.988$$

$$Wzeamin = 5.215 \times 10^3$$

$$Wfzmin = 1.021 \times 10^4$$

$$Wfzmax = 1.162 \times 10^4$$

$$Wfpmin = 1.997 \times 10^4$$

$$Wfpmax = 2.273 \times 10^4$$

$$Whfmin = 4.267 \times 10^3$$

$$Whfmax = 4.858 \times 10^3$$

$$G_{cmin}(\omega) := -\frac{Avmin \cdot Wzeamin}{i \cdot \omega} \cdot \left[1 + \frac{(i \cdot \omega)}{Wzeamin} \right] \cdot \left(1 + \frac{i \cdot \omega}{Wfzmin} \right)$$

$$G_{cmax}(\omega) := -\frac{Avmax \cdot Wzeamax}{i \cdot \omega} \cdot \left[1 + \frac{(i \cdot \omega)}{Wzeamax} \right] \cdot \left(1 + \frac{i \cdot \omega}{Wfzmax} \right)$$

$$Wfzmin = 1.021 \times 10^4$$

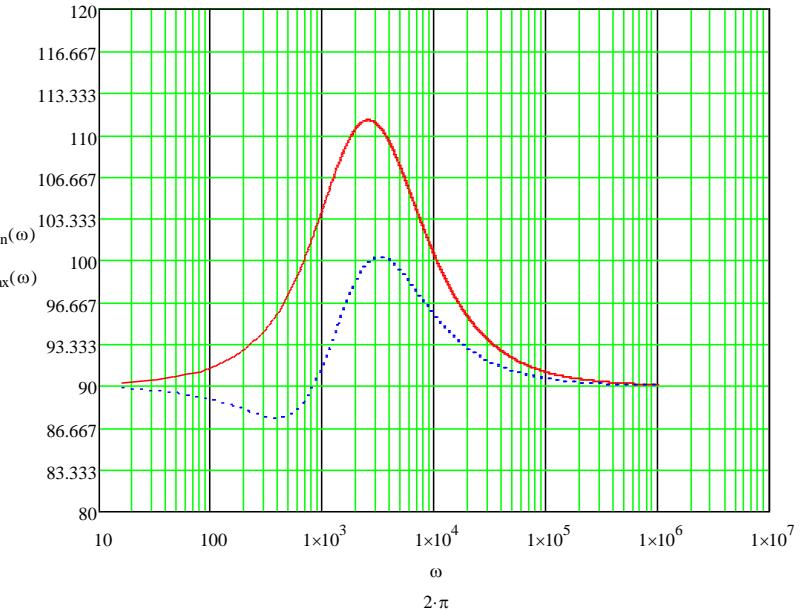
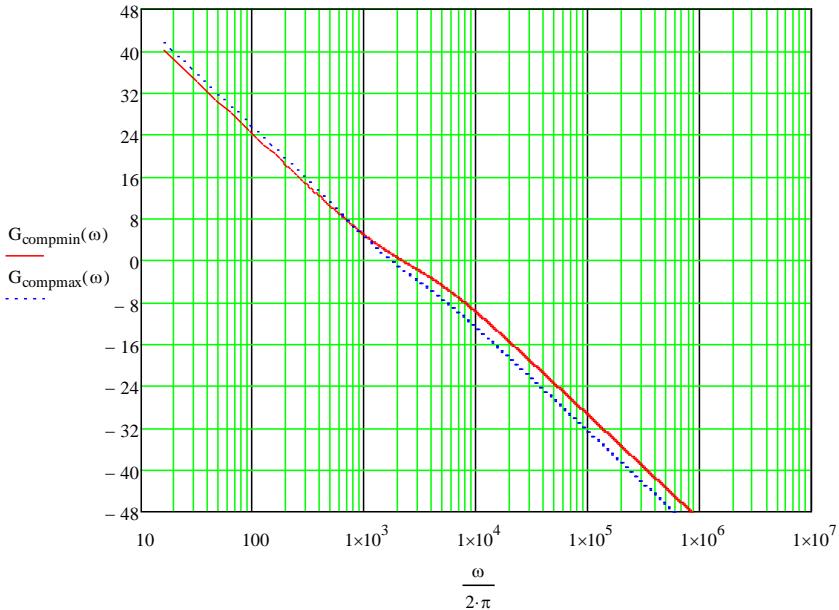
$$G_{compmin}(\omega) := 20 \cdot \log(|G_{cmin}(\omega)|)$$

$$G_{compmax}(\omega) := 20 \cdot \log(|G_{cmax}(\omega)|)$$

$$G_{comphmin}(\omega) := \frac{180}{\pi} \cdot \arg(G_{cmin}(\omega))$$

$$G_{comphmax}(\omega) := \frac{180}{\pi} \cdot \arg(G_{cmax}(\omega))$$

Loop stability worst case



Loop stability worst case

Open Loop Response:

$$Gloopmin(\omega) := -PSmin(\omega) \cdot G_{cmin}(\omega)$$

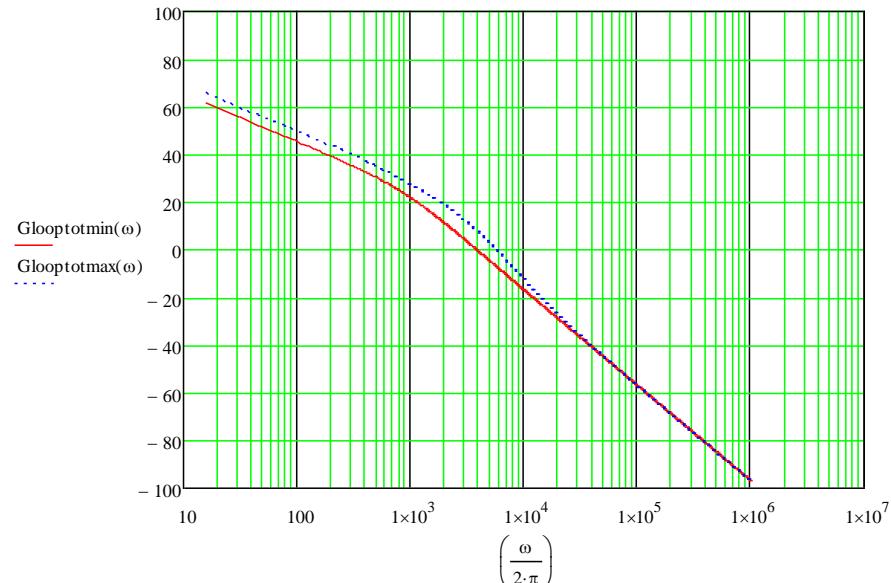
$$Gloopmax(\omega) := -PSmax(\omega) \cdot G_{cmax}(\omega)$$

$$Glooptotmin(\omega) := 20 \cdot \log(|Gloopmin(\omega)|)$$

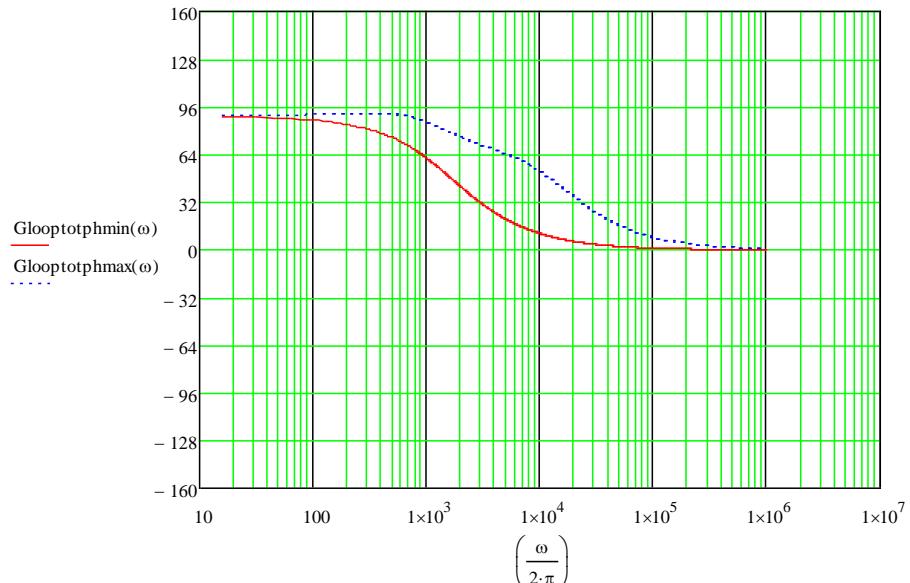
$$Glooptotphmin(\omega) := -\frac{180}{\pi} \cdot \arg(Gloopmin(\omega))$$

$$Glooptotmax(\omega) := 20 \cdot \log(|Gloopmax(\omega)|)$$

$$Glooptotphmax(\omega) := -\frac{180}{\pi} \cdot \arg(Gloopmax(\omega))$$



TI Information – Selective Disclosure



Worst Case Analysis MOSFET Power Dissipation Example

Problem statement

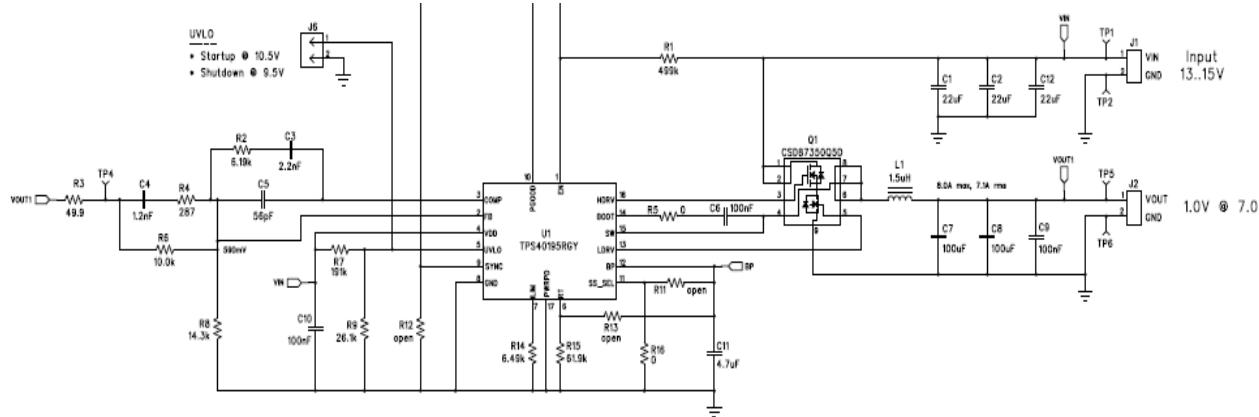
- The FET's in my PS are getting hot

Possible causes

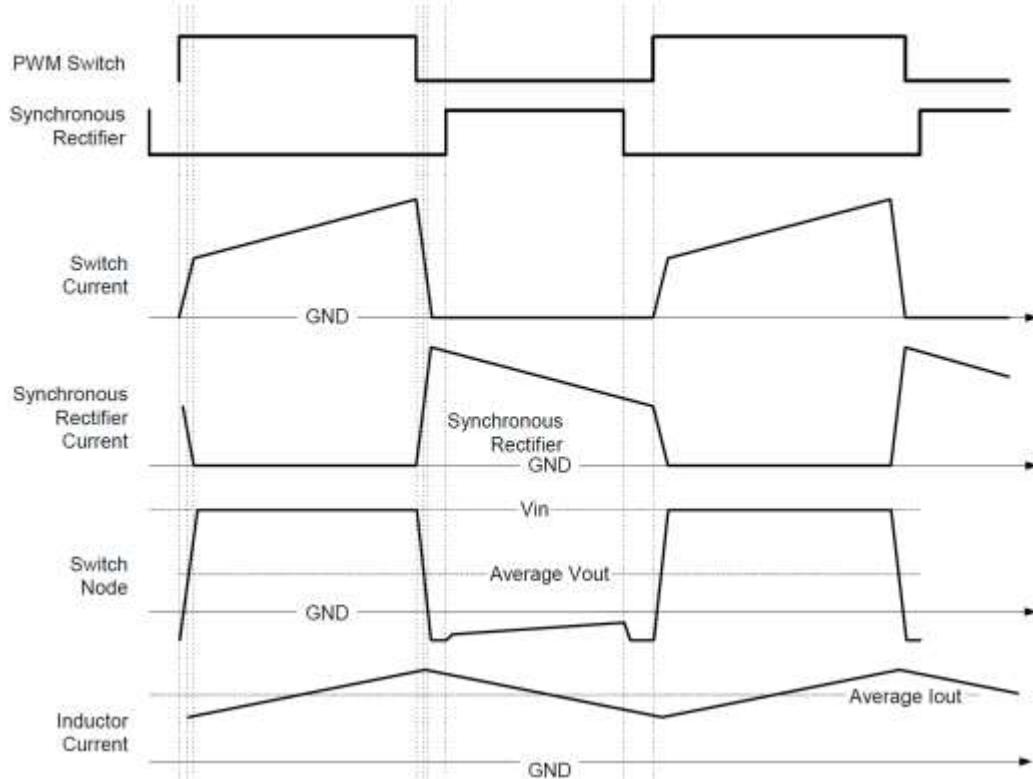
- Not enough heat sink
 - Shoot through

Solution

- WCA on FET power dissipation



Worst Case Analysis MOSFET Power Dissipation Example



Procedure

- Find tolerances for R_{ds} , Q_g total gate charge, Q_{gs} charge gate to source, Q_{gd} charge gate to drain, Q_{oss} output charge, body drain diode forward voltage, and controller dead time.
- Write equation and Analyze R_{ds} conducted losses, switching loss, and gate drive loss for top FET.
- Write equation and Analyze R_{ds} conducted losses, body drain diode loss, and gate drive loss for bottom FET
- Add up all losses

Worst Case Analysis component Tolerances

MOSFET tolerance

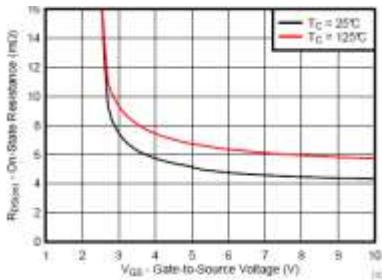


Figure 20. Control MOSFET $R_{DS(on)}$ vs V_{GS}

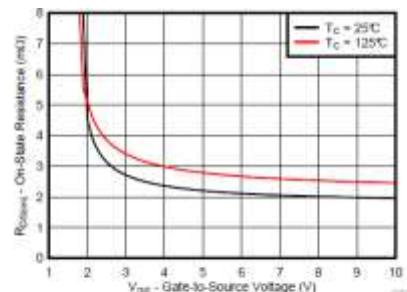


Figure 21. Sync MOSFET $R_{DS(on)}$ vs V_{GS}

CSD87350Q5D Synchronous Buck NexFET™ Power Block

Rds goes up as temp goes up

$$R_{ds_bol} = 20\%$$

$$R_{ds_tempmax} = 63\%$$

$$R_{ds_tempmin} = -40\%$$

$$R_{dson_top} := 5 \cdot 10^{-3} \cdot \Omega$$

$$R_{dson_bot} := 1.2 \cdot 10^{-3} \cdot \Omega$$

$$R_{dsmin_top} = 2.4 \times 10^{-3} \Omega$$

$$R_{dsmin_bot} = 5.76 \times 10^{-4} \Omega$$

$$R_{dsmax_top} = 9.78 \times 10^{-3} \Omega$$

$$R_{dsmax_bot} = 2.347 \times 10^{-3} \Omega$$

Total gate charge

$$q_{total_top} := 8.4 \text{nC}$$

$$q_{total_bol} := 30\%$$

$$q_{total_bot} := 20 \text{nC}$$

$$q_{total_min_top} = 5.88 \times 10^{-9} \text{ C}$$

$$q_{total_min_bot} = 1.4 \times 10^{-8} \text{ C}$$

$$q_{total_max_top} = 1.092 \times 10^{-8} \text{ C}$$

$$q_{total_max_bot} = 2.6 \times 10^{-8} \text{ C}$$

Gate charge gate to drain and gate to source

$$Q_{gd_top} := 1.6 \text{nC}$$

$$Q_{gd_bol} := 30\%$$

$$Q_{gs_top} := 2.6 \text{nC}$$

$$Q_{gs_bol} := 30\%$$

$$Q_{gd_min_top} = 1.12 \times 10^{-9} \text{ C}$$

$$Q_{gs_min_top} = 1.82 \times 10^{-9} \text{ C}$$

$$Q_{gd_max_top} = 2.08 \times 10^{-9} \text{ C}$$

$$Q_{gs_max_top} = 3.38 \times 10^{-9} \text{ C}$$

Worst Case Analysis component Tolerances

MOSFET tolerance

Qoss output charge

$$Q_{oss_bol} := 30\%$$

$$Q_{oss_top} := 9.7\text{nC}$$

$$Q_{oss_min_top} = 6.79 \times 10^{-9}\text{ C}$$

$$Q_{oss_bot} := 28\text{nC}$$

$$Q_{oss_min_bot} = 1.96 \times 10^{-8}\text{ C}$$

$$Q_{oss_max_top} = 1.261 \times 10^{-8}\text{ C}$$

$$Q_{oss_max_bot} = 3.64 \times 10^{-8}\text{ C}$$

Body drain diode forward voltage

$$V_{body} := .8\text{V}$$

$$V_{body_bol} := 25\%$$

$$V_{body_tempphot} := 30\% \text{ At } 125\text{C}$$

$$V_{body_tempcold} := 22.5\% \text{ At } -50\text{C}$$

$$V_{body_max} = 1.3\text{ V}$$

$$V_{body_min} = 0.42\text{ V}$$

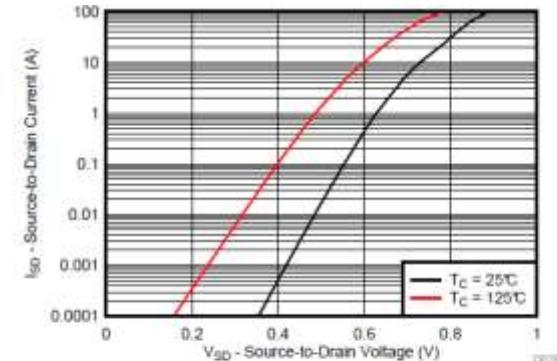


Figure 25. Sync MOSFET Body Diode

Worst Case Analysis component Tolerances

TPS40190 Controller dead time tolerance for body diode PWR calculation

Deadtime_HSoft_LSon := 50ns Deadtime_LSoft_HSon := 25ns DT_bol := 20%

$$\text{Deadtime_HSoft_LSon_min} = 4 \times 10^{-8} \text{ s}$$

$$\text{Deadtime_LSoft_HSon_min} = 2 \times 10^{-8} \text{ s}$$

$$\text{Deadtime_HSoft_LSon_max} = 6 \times 10^{-8} \text{ s}$$

$$\text{Deadtime_LSoft_HSon_max} = 3 \times 10^{-8} \text{ s}$$

Power block delay time tolerance for body diode PWR calculation

Td_FET_bol := 30% Turnon_dly_HS := 7ns Turnon_dly_LS := 8ns Turnoff_dly_HS := 13ns Turnoff_dly_LS := 33ns

$$\text{Trise_HS} := 17\text{ns}$$

$$\text{Trise_LS} := 10\text{ns}$$

$$\text{Tfall_HS} := 2.3\text{ns}$$

$$\text{Tfall_LS} := 4.7\text{ns}$$

$$\text{Turnon_dly_HSmin} = 4.9 \times 10^{-9} \text{ s}$$

$$\text{Trise_HSmin} = 1.19 \times 10^{-8} \text{ s}$$

$$\text{Turnoff_dly_HSmin} = 9.1 \times 10^{-9} \text{ s}$$

$$\text{Tfall_HSmin} = 1.61 \times 10^{-9} \text{ s}$$

$$\text{Turnon_dly_HSmax} = 9.1 \times 10^{-9} \text{ s}$$

$$\text{Trise_HSmax} = 2.21 \times 10^{-8} \text{ s}$$

$$\text{Turnoff_dly_HSmax} = 1.69 \times 10^{-8} \text{ s}$$

$$\text{Tfall_HSmax} = 2.99 \times 10^{-9} \text{ s}$$

$$\text{Turnon_dly_LSmin} = 5.6 \times 10^{-9} \text{ s}$$

$$\text{Trise_LSmin} = 7 \times 10^{-9} \text{ s}$$

$$\text{Turnoff_dly_LSmin} = 2.31 \times 10^{-8} \text{ s}$$

$$\text{Tfall_LSmin} = 3.29 \times 10^{-9} \text{ s}$$

$$\text{Turnon_dly_LSmax} = 1.04 \times 10^{-8} \text{ s}$$

$$\text{Trise_LSmax} = 1.3 \times 10^{-8} \text{ s}$$

$$\text{Turnoff_dly_LSmax} = 4.29 \times 10^{-8} \text{ s}$$

$$\text{Tfall_LSmax} = 6.11 \times 10^{-9} \text{ s}$$

Worst Case Analysis MOSFET Power Dissipation Example

1) First calculate conducted loss

$$I_{rms_top_fet} = 10.462 \text{ A}$$

$$P_{fet_cond_topmax} := I_{rms_top_fet}^2 \cdot R_{dsmax_top} \quad P_{fet_cond_topmax} = 1.07 \text{ W} \quad (\text{Cond losses})$$

$$P_{fet_cond_topmin} := I_{rms_top_fet}^2 \cdot R_{dsmin_top} \quad P_{fet_cond_topmin} = 0.263 \text{ W} \quad (\text{Cond losses})$$

$$I_{rms_bot_fet} = 38.677 \text{ A}$$

$$P_{fet_cond_botmax} := I_{rms_bot_fet}^2 \cdot R_{dsmax_bot} \quad P_{fet_cond_botmax} = 3.511 \text{ W} \quad (\text{Cond losses})$$

$$P_{fet_cond_botmin} := I_{rms_bot_fet}^2 \cdot R_{dsmin_bot} \quad P_{fet_cond_botmin} = 0.862 \text{ W} \quad (\text{Cond losses})$$

2) Calculate top FET switching loss

$$I_g := 1 \text{ A}$$

$$P_{sw_fet_top} := V_{inmax} \cdot f_{max} \left[\frac{I_{pfet_top} \cdot (Q_{gd_max_top} + Q_{gs_max_top})}{I_g} + \frac{Q_{oss_max_top} + Q_{oss_max_bot}}{2} \right] \quad P_{sw_fet_top} = 1.502 \text{ W} \quad (\text{Switching losses})$$

$$T_{sw} := 18 \cdot \text{ns}$$

$$P_{d_SW_FET} := 2 \left[\frac{1}{T_{min}} \cdot \int_0^{T_{sw}} \left(V_{inmax} \cdot \frac{t}{T_{sw}} \right) \cdot \left[I_{pfet_top} \cdot \left(1 - \frac{t}{T_{sw}} \right) \right] dt \right] \quad P_{d_SW_FET} = 1.517 \text{ W} \quad (\text{Switching losses})$$

Bottom FET has body diode voltage across it at turn on/off therefore loss is in the body diode

Worst Case Analysis MOSFET Power Dissipation Example

3) Calculate gate drive losses

PARAMETER	TEST CONDITIONS	Q1 CONTROL FET			Q2 SYNC FET			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
R _G	Series gate resistance			1.3	3	0.8	2	Ω
OUTPUT DRIVERS								
R _{HDI}	High-side driver pull-up resistance	V _{BOOT} - V _{SW} = 4.5 V, I _{HDRV} = -100 mA			3	6	Ω	
R _{HDO}	High-side driver pull-down resistance	V _{BOOT} - V _{SW} = 4.5 V, I _{HDRV} = 100 mA			1.5	3	Ω	
R _{LH}	Low-side driver pull-up resistance	I _{LDRV} = -100 mA			2.5	5	Ω	
R _{LD}	Low-side driver pull-down resistance	I _{LDRV} = 100 mA			0.8	1.5	Ω	

V_{gate} := 8V

$$P_{g_dr_top} := f \cdot q_{total_max_top} \cdot V_{gate} \quad P_{g_dr_top} = 0.028 \text{ W} \quad (\text{Gate losses})$$

$$Act_{gate_drive_pwr_top} := \frac{1.3}{3} \cdot P_{g_dr_top} \quad Act_{gate_drive_pwr_top} = 0.012 \text{ W}$$

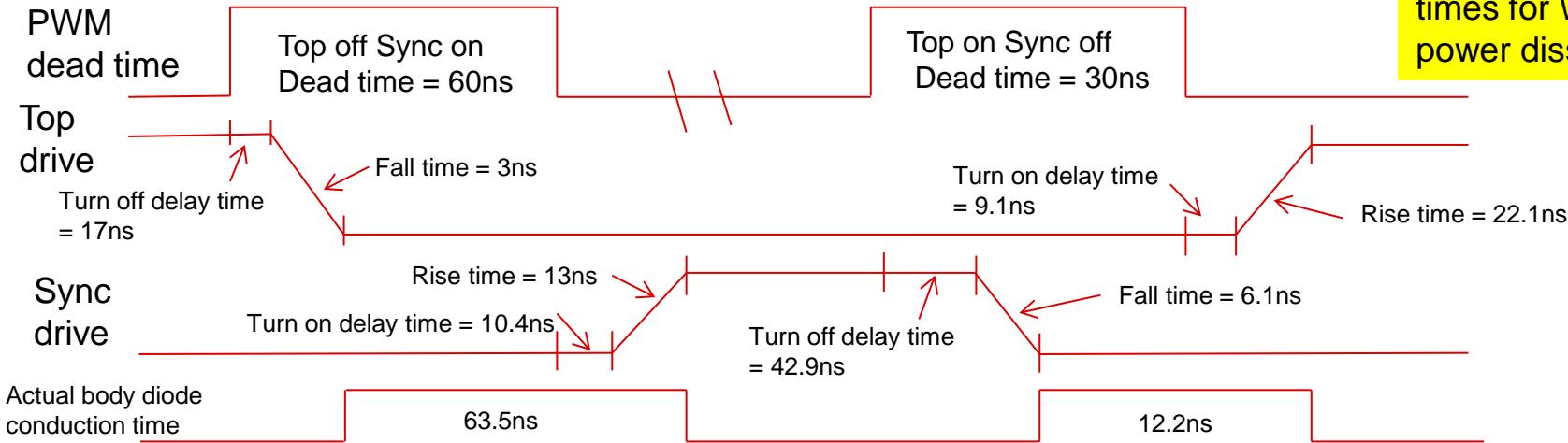
$$P_{g_dr_bot} := f \cdot q_{total_max_bot} \cdot V_{gate} \quad P_{g_dr_bot} = 0.068 \text{ W} \quad (\text{Gate losses})$$

$$Act_{gate_drive_pwr_LS} := \frac{.8}{2.5} \cdot P_{g_dr_bot} \quad Act_{gate_drive_pwr_LS} = 0.022 \text{ W}$$

Worst Case Analysis MOSFET Power Dissipation Example

3) Calculate body diode losses

Used maximum times for WC power dissipation



$$Tdelay1 := \text{Deadtime_HSoff_LSon_max} - \text{Turnoff_dly_HSmax} - \text{Tfall_HSmax} + \text{Turnon_dly_LSmax} + \text{Trise_LSmax}$$

$$Tdelay1 = 6.351 \times 10^{-8} \text{ s}$$

$$Tdelay2 := \text{Deadtime_LSoff_HSon_max} - \text{Turnoff_dly_LSmax} - \text{Tfall_LSmax} + \text{Turnon_dly_HSmax} + \text{Trise_HSmax}$$

$$Tdelay2 = 1.219 \times 10^{-8} \text{ s}$$

$$P_{body_diode_max} := V_{body_min} \cdot I_{omax} \cdot \frac{Tdelay1 + Tdelay2}{Tmin}$$
$$P_{body_diode_max} = 0.475 \text{ W}$$

Worst Case Analysis MOSFET Power Dissipation Example

4) Add up all the top and bottom FET losses

$P_{fet_tot_top_min} := P_{fet_cond_topmin} + P_{sw_fet_top} + A_{ct_gate_drive_pwr_top}$

$P_{fet_tot_top_min} = 1.777 \text{ W}$

(Total top FET losses Cond min)

$P_{fet_tot_top_max} := P_{fet_cond_topmax} + P_{sw_fet_top} + A_{ct_gate_drive_pwr_top}$

$P_{fet_tot_top_max} = 2.584 \text{ W}$

(Total top FET losses max)

$P_{fet_tot_bot_min} := P_{fet_cond_botmin} + A_{ct_gate_drive_pwr_LS} + P_{body_diode_max}$

$P_{fet_tot_bot_min} = 1.359 \text{ W}$

(Total bottom FET losses cond min)

$P_{fet_tot_bot_max} := P_{fet_cond_botmax} + A_{ct_gate_drive_pwr_LS} + P_{body_diode_max}$

$P_{fet_tot_bot_max} = 4.008 \text{ W}$

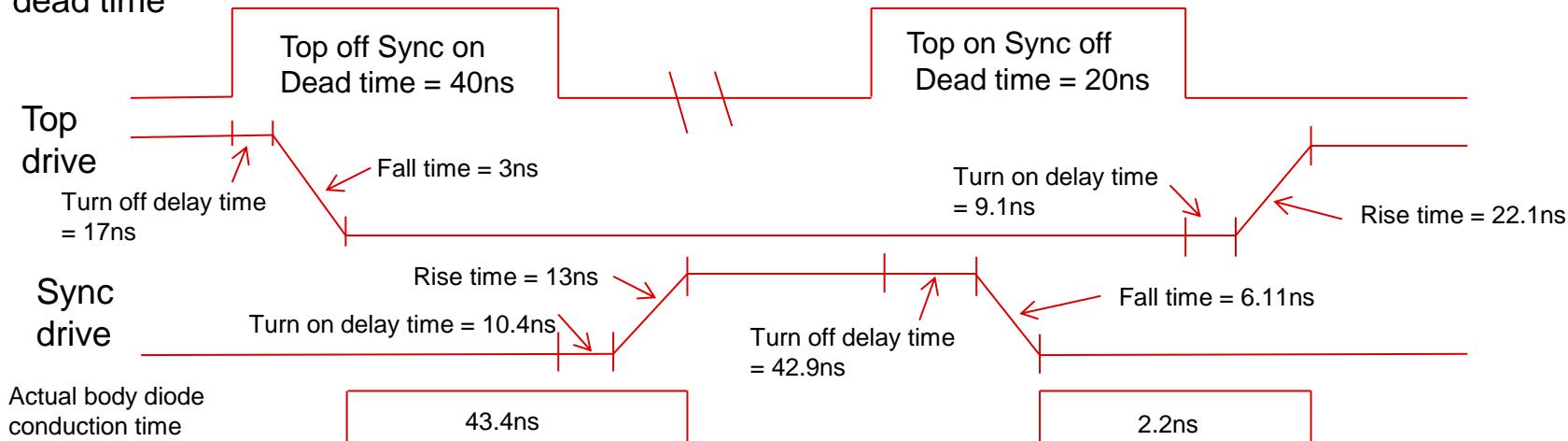
(Total bottom FET losses max)

Worst Case Analysis MOSFET

Cross conduction and Timing issues

Look at what happens
when dead time is minimum
and delay times are maximum

PWM
dead time



Summary

- Analyze the circuit to determine potential issues in the design
- Decide what type of analysis needs to be performed - EV, RSS, Monte Carlo
- Write an equation for the potential issues you found
- Determine the variables in each equation
- Determine the BOL, EOL, and temp tolerances for each variable from the manufactures DS or company APL
- Calculate the tolerances for each
- Calculate the behavioral equations using the variable tolerances to determine the worst case parameters for your design

References

- Brian Lynch and Kurt Hesse, "Under the Hood of Low-Voltage DC/DC Converters," Texas Instruments Power Supply Design Seminar 2002, SEM1500, Topic 5, TI Literature number: SLUP206.
- Louis Diana, "Practical Magnetic Design: Inductors and Coupled Inductors," SEM-2000, Topic 5, 2012, SLUP304
- Robert Sheehan and Louis Diana, "Switch-Mode Power Converter Compensation Made Easy," Topic 3, SEM-2200, SLUP340.
- Lloyd H. Dixon, "Magnetics Design for Switching Power Supplies." Sections 1-7. TI literature Nos. SLUP123, SLUP124, SLUP125, SLUP126, SLUP127, SLUP128, and SLUP129.
- Lloyd H. Dixon, Control Loop Cookbook, SEM-1100 Unitrode Power Supply Design Seminar, 1996. Topic V, TI Literature No. SLUP113
- Laszlo Balogh, A design and Application Guide for High Speed Power MOSFET Gate Driver Circuits, SEM-1400, Unitrode Power Supply Design Seminar, 2001. Topic II, TI Literature No. SLUP169
- Brian King and Michael O'Loughlin, "Common Mistakes in Flyback Power Supply Design and How to Fix Them," SEM-2400, Topic 4, 2020, SLUP392