Designing Switched-Mode Power Supplies in the High di/dt Era

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2018.11.08

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Trends in Switched-mode Power Supplies (SMPSs)

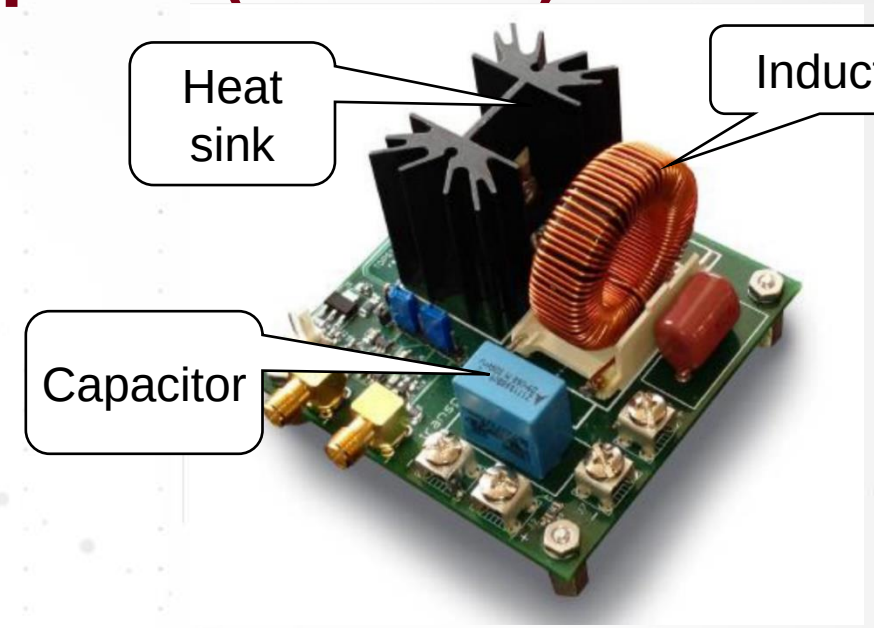


Image courtesy of Transphorm

Consumer demand for:

- lower cost
- smaller size
- lighter weight

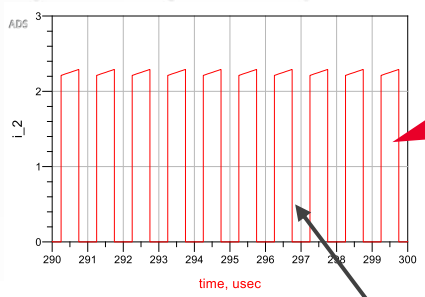
…is driving the industry to higher switching speeds “high di/dt”

Traditional (cut-and-try) design methods don’t work for high di/dt

- $V_{spike} = L_{parasitic}\ di/dt$
- Need to add a field solver to extract layout parasitics into an EM-based model

Switched-Mode Power Supply (SMPS)

SIMPLE EXAMPLE: HARD-SWITCHED BUCK CONVERTER



Rectangle wave duty cycle, D

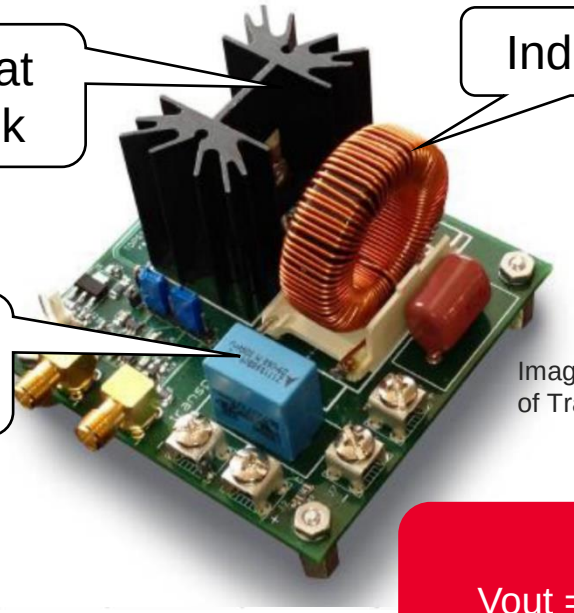
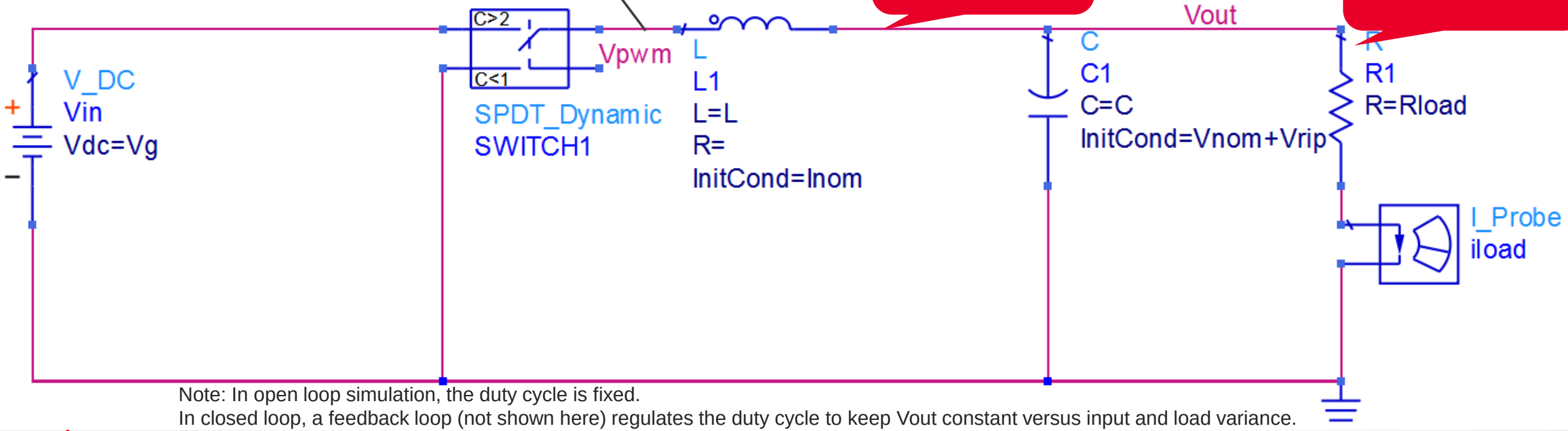


Image courtesy of Transphorm

LC low pass filter
f_{knee} = sqrt(1/LC)/2π

Vout = D * Vg

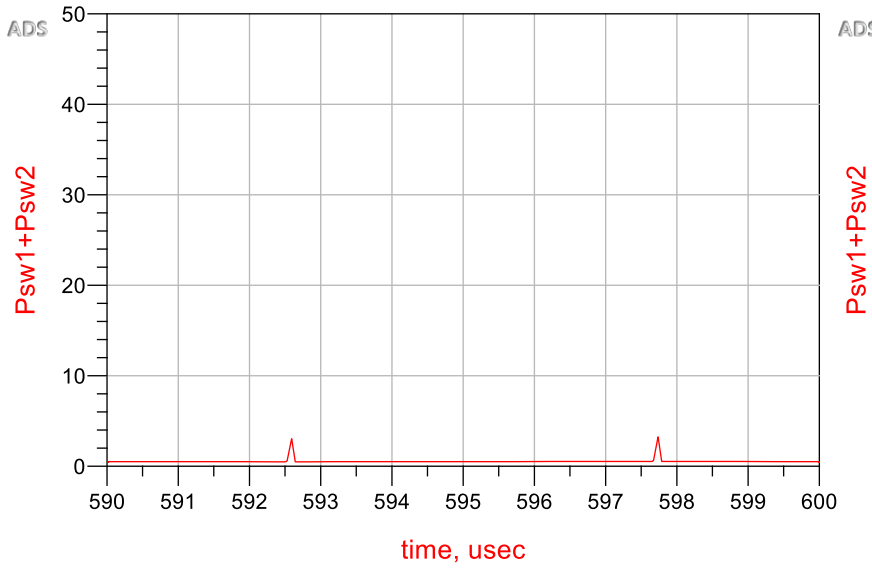


Note: In open loop simulation, the duty cycle is fixed.
In closed loop, a feedback loop (not shown here) regulates the duty cycle to keep Vout constant versus input and load variance.

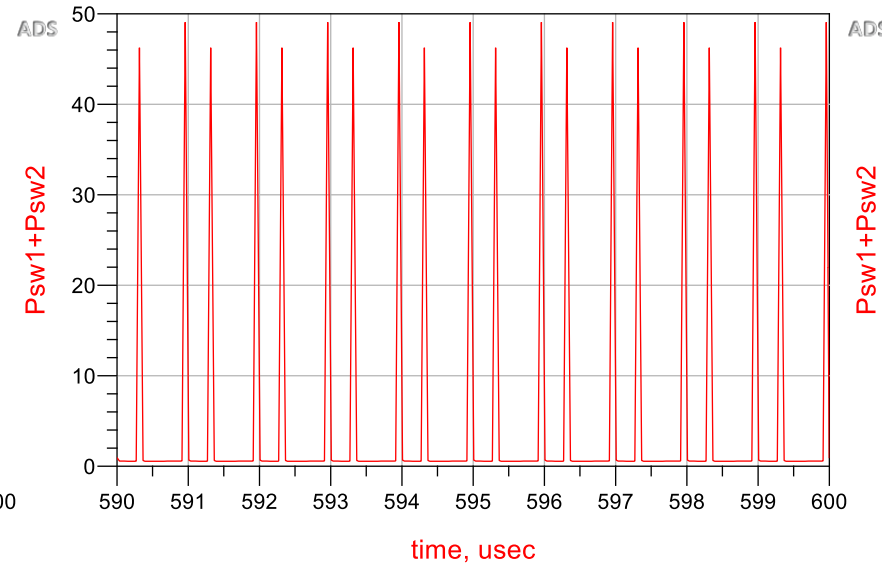
Higher Frequency Can Lead to Higher Switching Loss

UNLESS THE EDGE SPEED IS INCREASED AS WELL

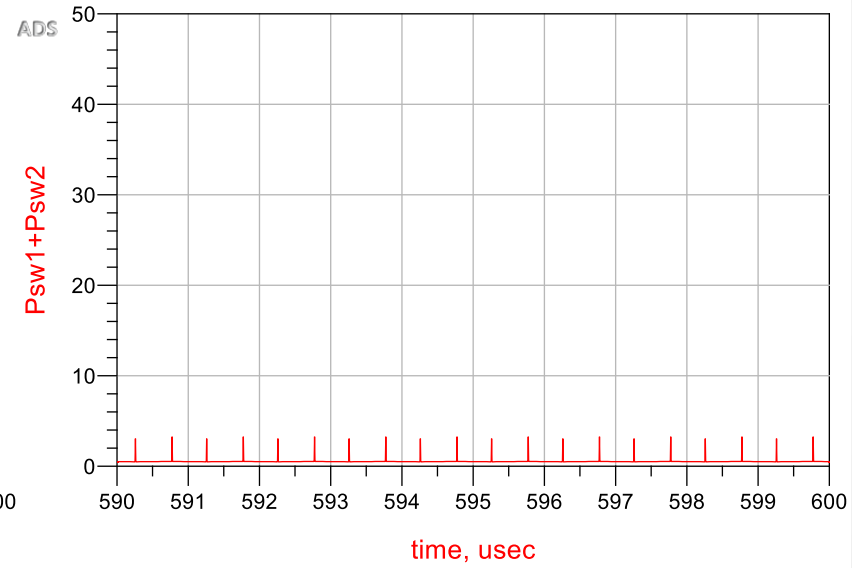
Low frequency
Slow edges
Switching loss 3.5%



Higher frequency
Same slow edges
Switching loss 15.3%

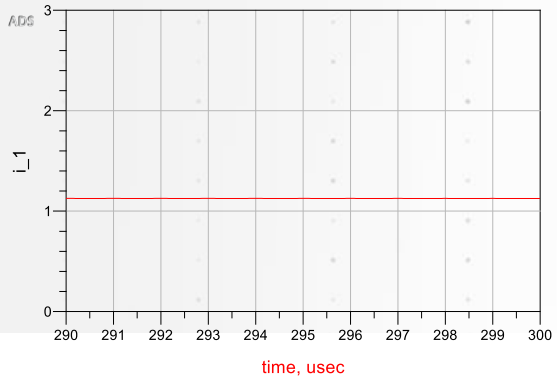


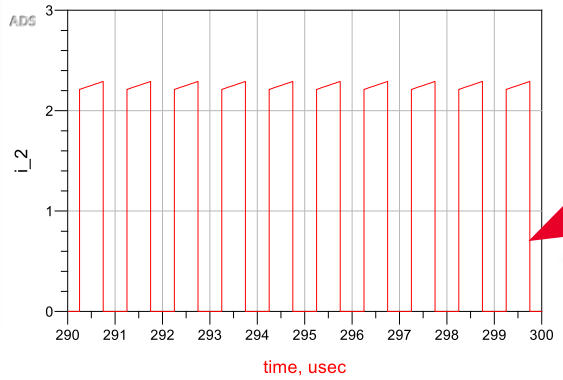
Higher frequency
Faster edges
Switching loss 3.3%



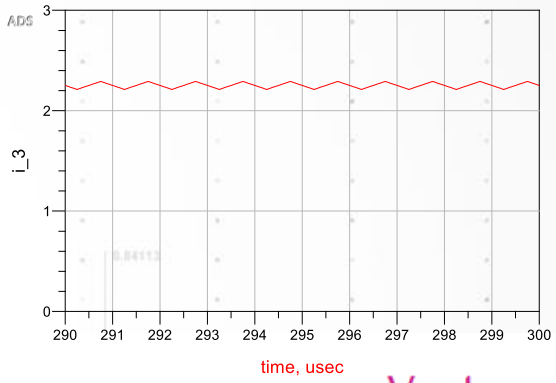
If you want to *reduce* switching loss, you have to improve the edge speed *even more dramatically* than improving the switching frequency

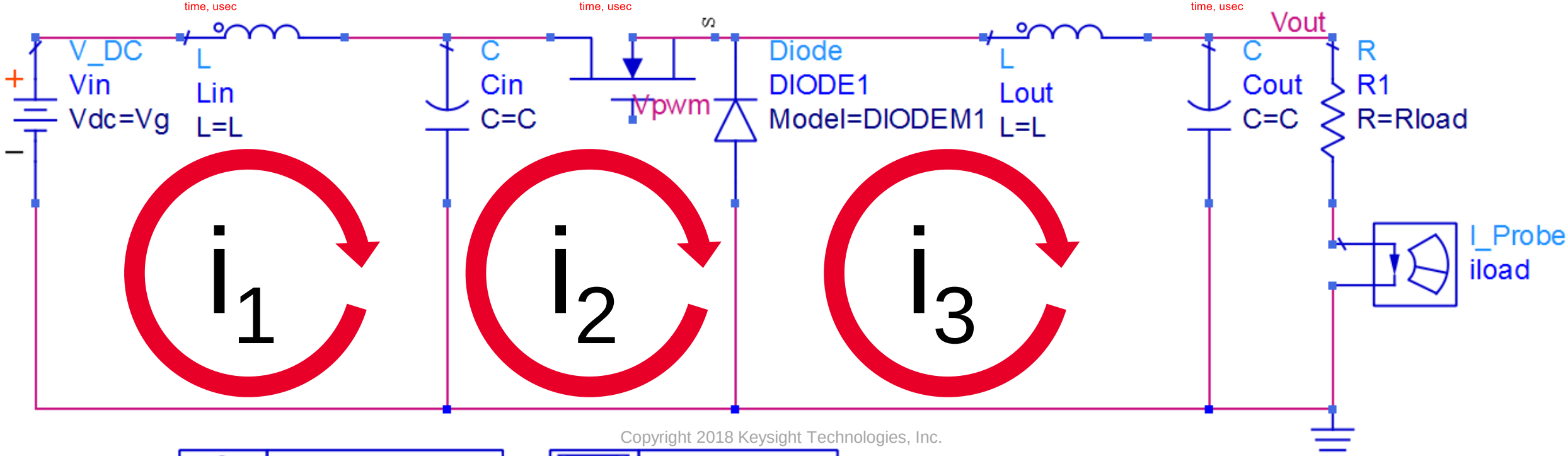
Current Loops: Schematic View





High di/dt in switched loop





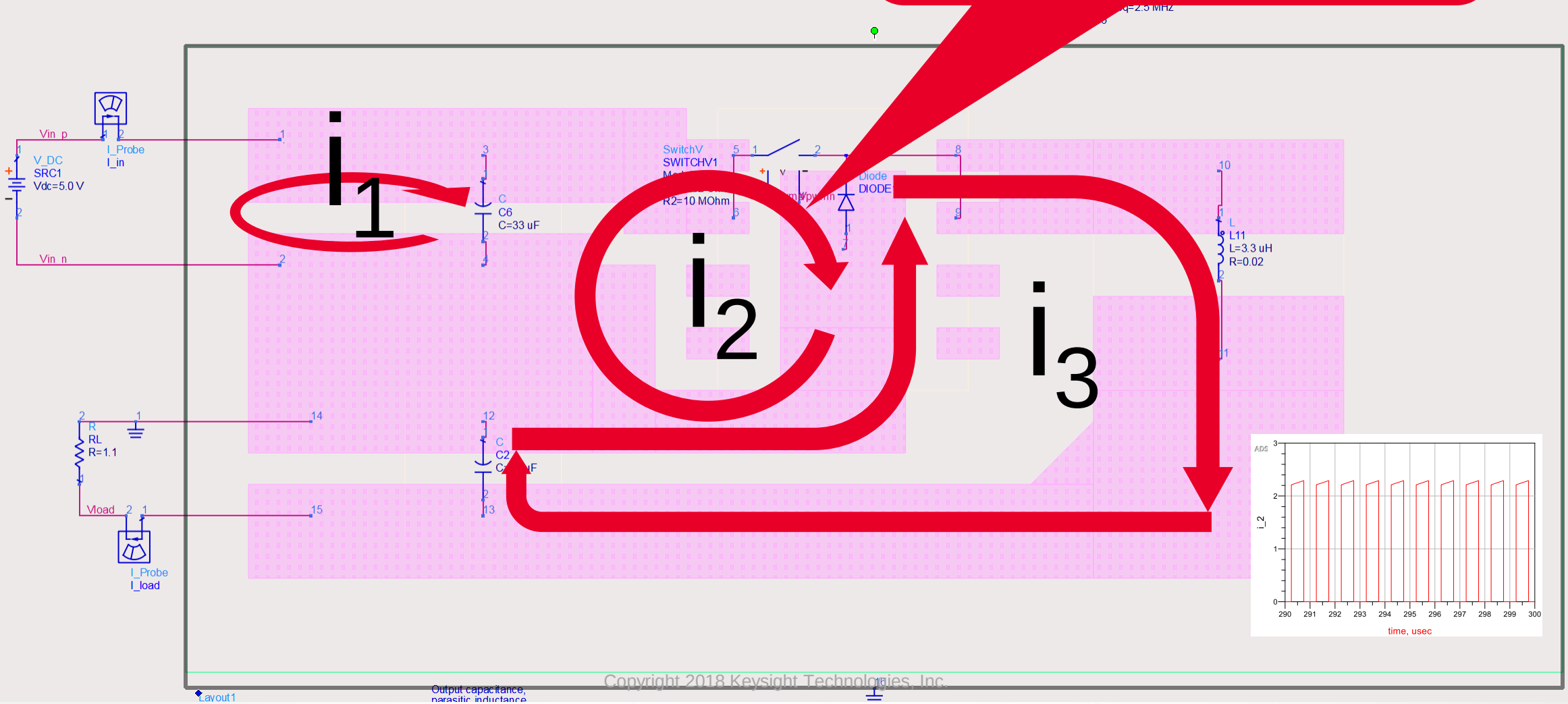
TRANSIENT OPTIONS

Current Loops: Layout View

When does the layout of the switched loop become important?

$V_{spike} = L_{parasitic} * di/dt$

$V_{spike} = L_{parasitic} * I_{on}/\tau$



$$V_{spike} = L_{parasitic} \frac{I_{on}}{\tau}$$

Definition of inductance
Linear ramp di/dt

$$\frac{V_{spike}}{V_{off}} = L_{parasitic} \frac{I_{on}}{\tau V_{off}}$$

Divide both sides by Voff

$$10\% = L_{10\%} \frac{I_{on}}{\tau V_{off}}$$

What inductance will give us a overstress spike that is, say, 10% of Voff?

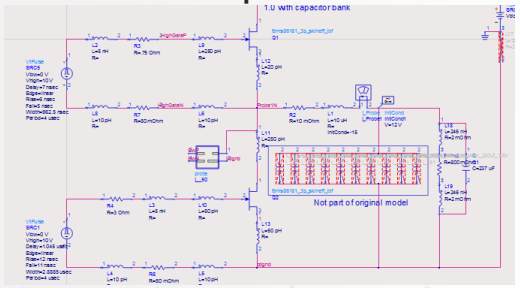
$$L_{10\%} = \frac{0.1 \tau V_{off}}{I_{on}}$$

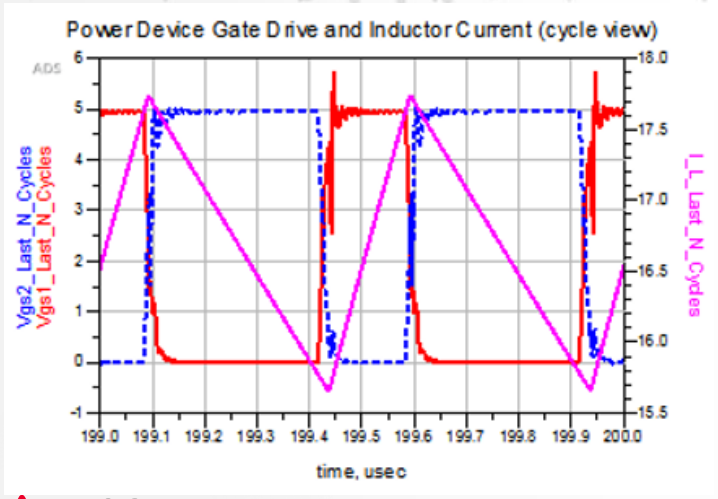
Rearrange, plug in some numbers
10 ns, 20V, 4A answer is 5 nH
Few mm of wire is 5 nH!

Traditional Low Speed Design Approach

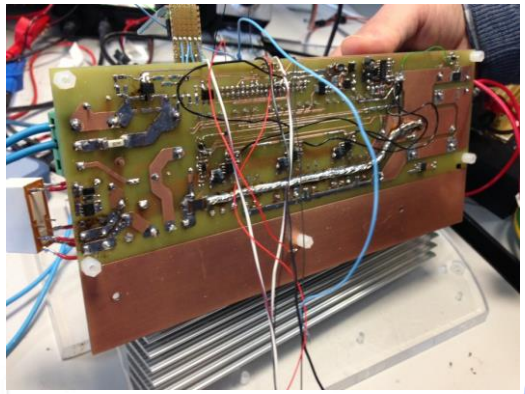
PRE-LAYOUT SPICE, THEN "CUT AND TRY"

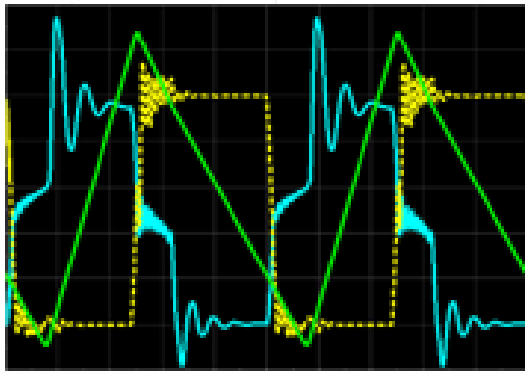
Pre-layout schematic
SPICE simulation:
"Best Case" performance





First prototype has some excess ringing. Cut-and-try until "best case" approached





2-6 spins
$6k-$60k/spin
3-8 weeks slip/spin

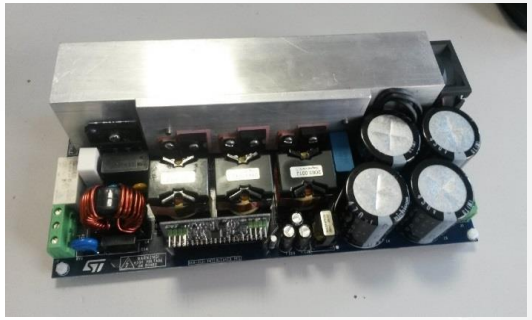
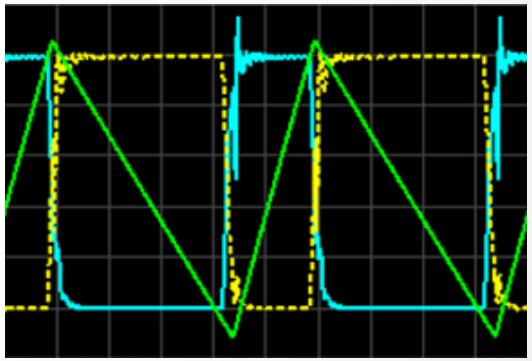


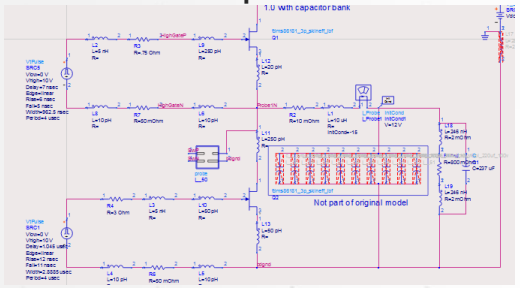
Image courtesy of ST Microelectronics

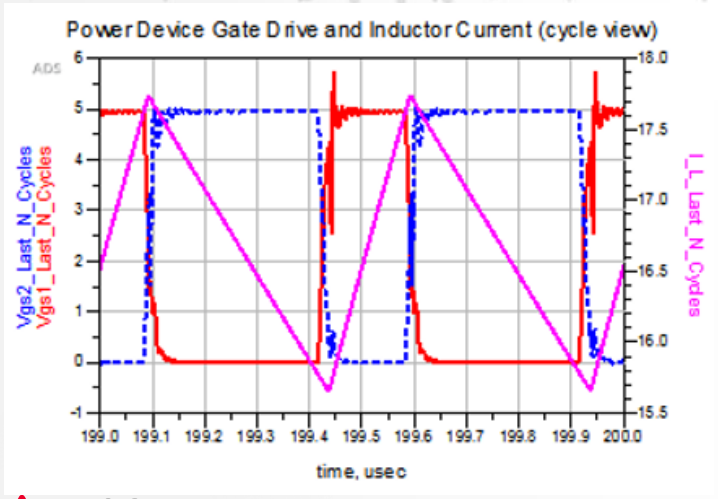


Traditional Design Approach Applied to High Speed

PRE-LAYOUT SPICE, THEN "CUT AND TRY"

Pre-layout schematic SPICE simulation: "Best Case" performance





First prototype has destructive failure.

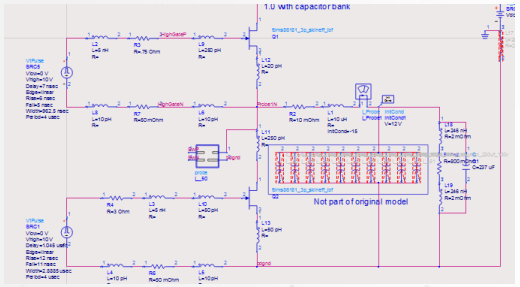
What next?

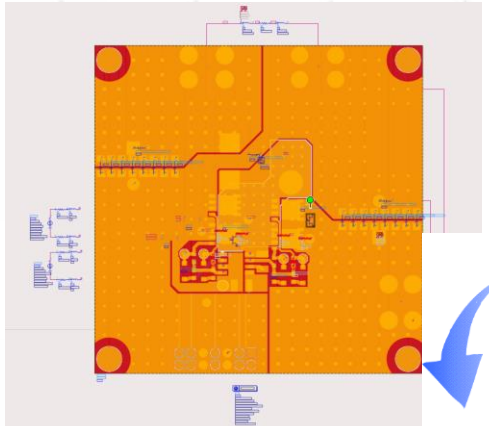
Recommended High Speed Design Approach

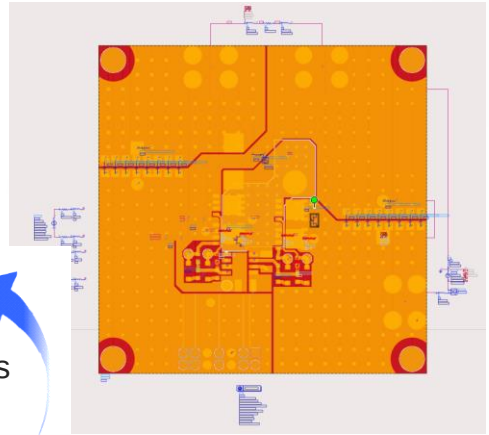
Pre-layout schematic
SPICE simulation:
“Best Case” performance

Post-layout: Integrated EM-circuit co-sim
First “virtual” prototype has some excess ringing.
“White box” – data display – 3D visualization
Explore design space until “best case” approached

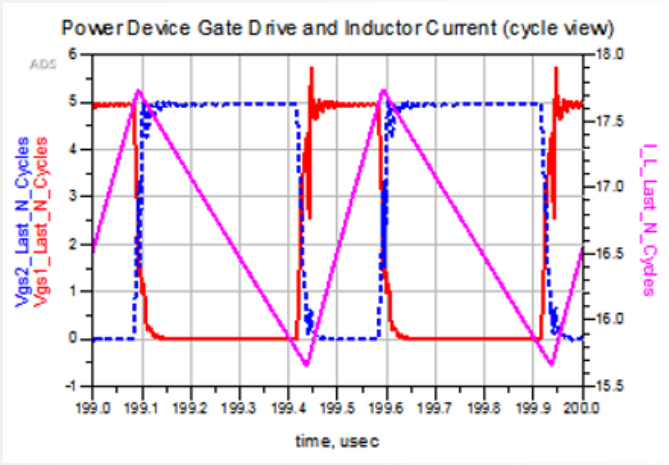
First pass success

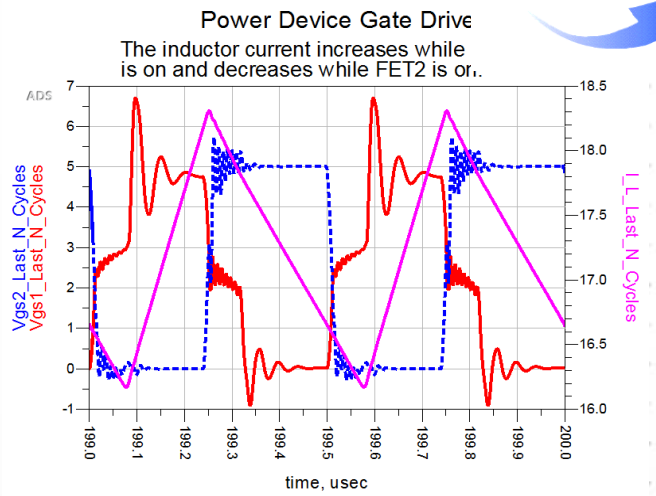


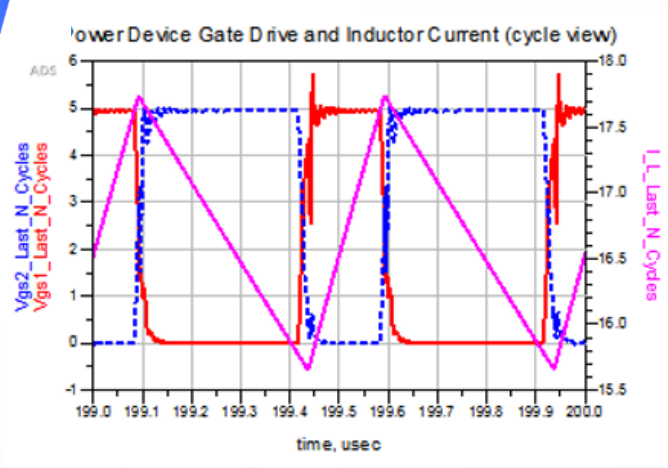


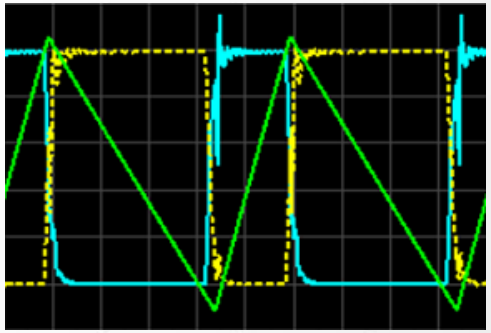


1-5 hours
/spin







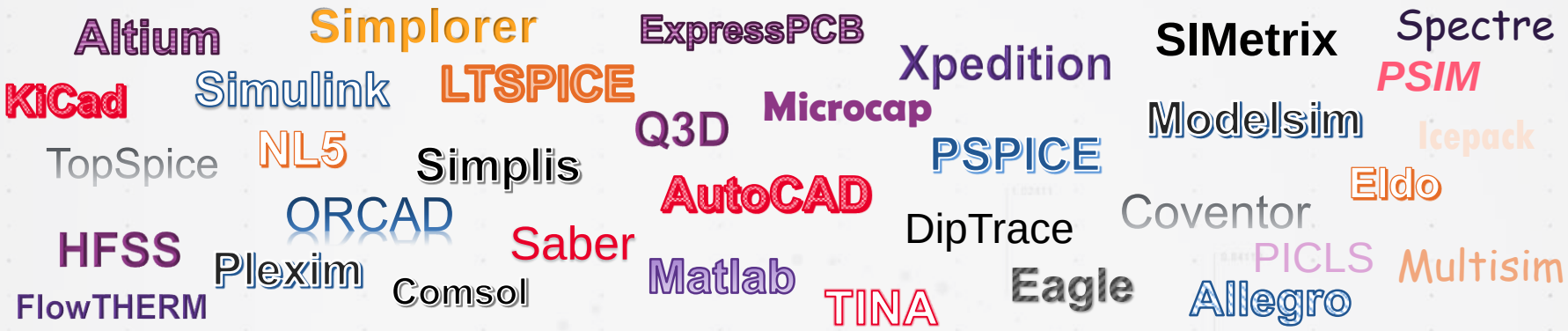


Today's Modern EDA Solutions

NEW PROBLEMS REQUIRE DIFFERENT TOOLS

State of the EDA Industry for PE

LARGELY A COLLECTION OF POINT TOOLS

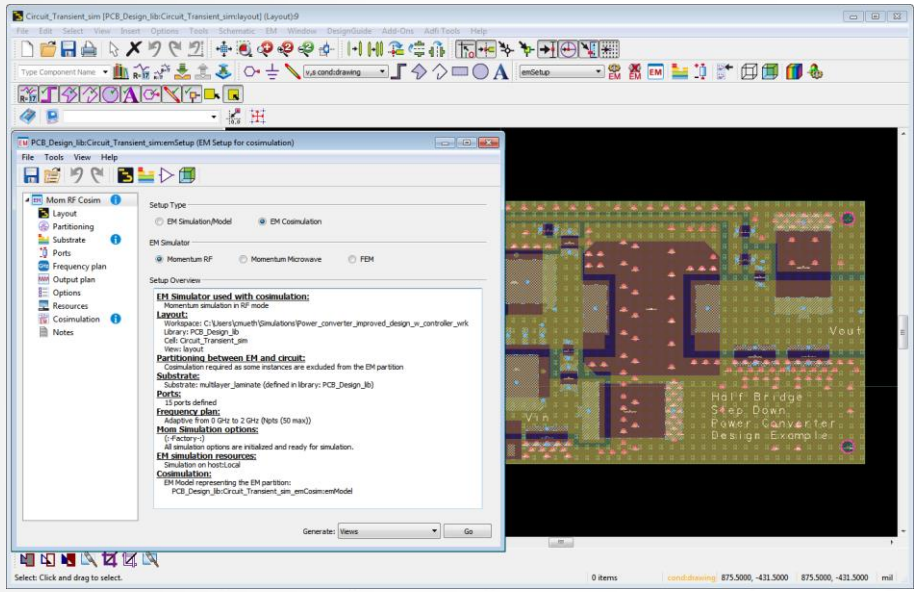


- A myriad of “point tools” exist, each fixed on a piece of the design process
- The biggest EDA tool issues power electronics designers mention:
  - Being limited on what they can analyze
  - Having to know and move among multiple tools to work

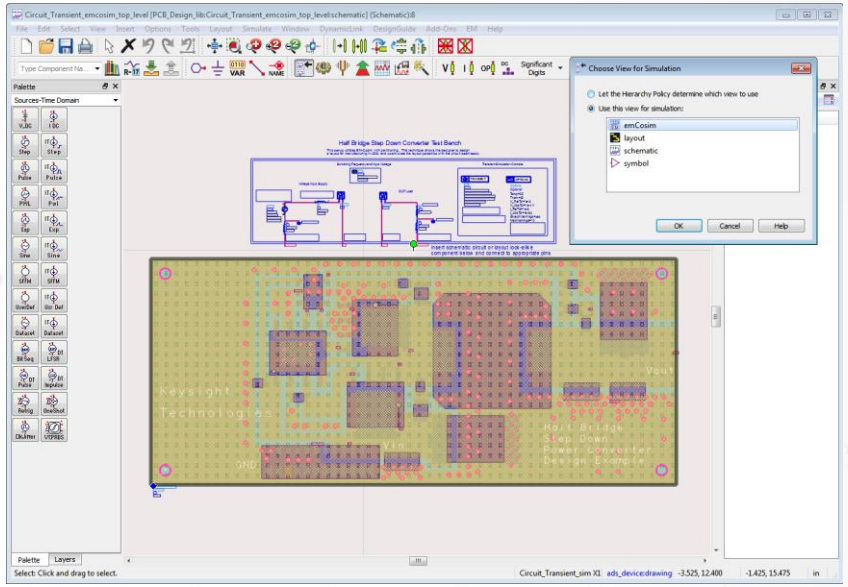
High Speed Power Converter Tool Requirements:

1) Integrated schematic and layout
2) Integrated circuit simulator (SPICE/Harmonic Balance)
3) Integrated EM engine

Using ADS for EM-circuit Co-simulation



Layout and schematic are tied together

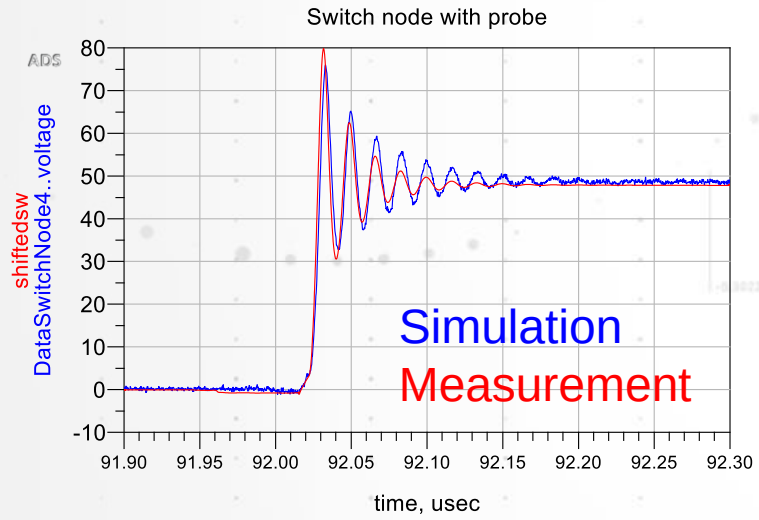


- Field solver extracts EM-based model of the layout parasitics
- Method of Moments provides the best balance of speed and accuracy for PCB/packages

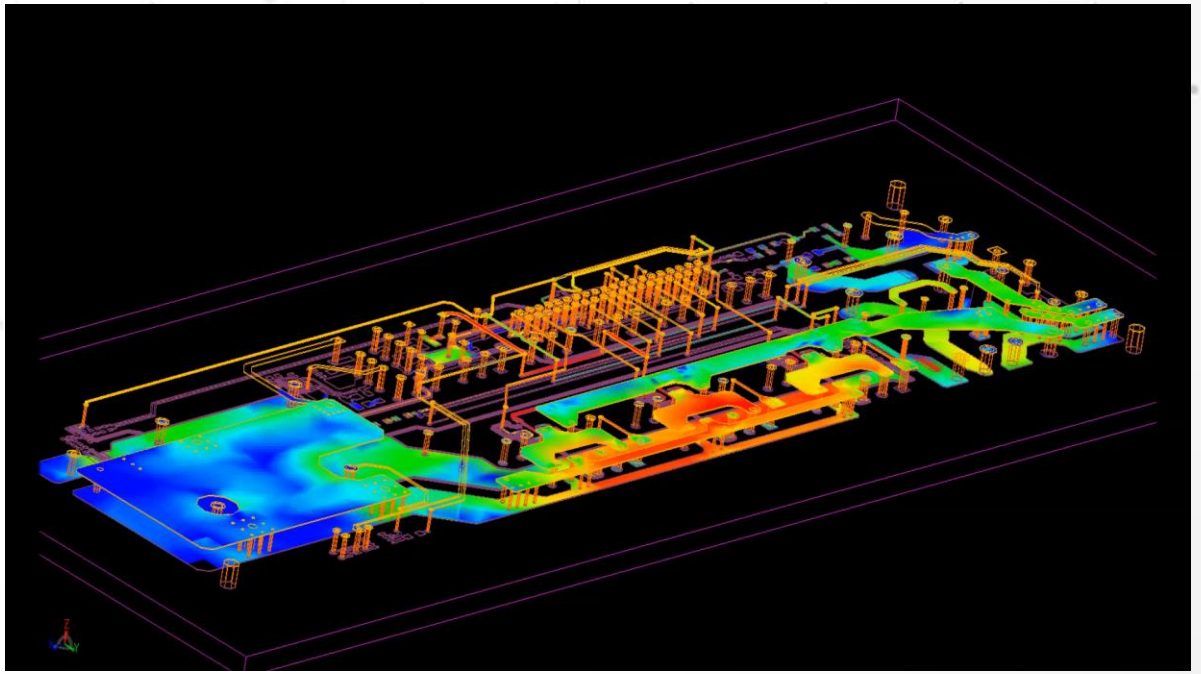
- Compact, EM-based model of layout parasitics is added to the familiar transient (SPICE-like) circuit sim

Results from EM-circuit Co-simulation

- EM-model informs the circuit simulation



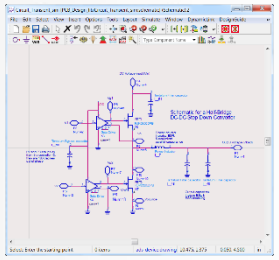
- Circuit excitation informs the EM post-simulation visualization display



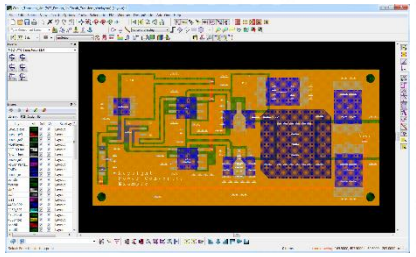
Keysight Integrated Power Electronics Solution

ADVANCED DESIGN SYSTEM (ADS)

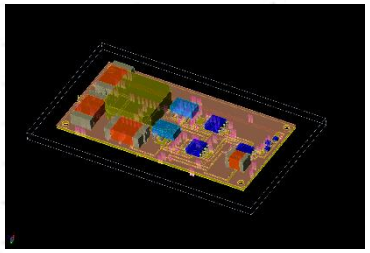
W2240 Power Electronics Bundle



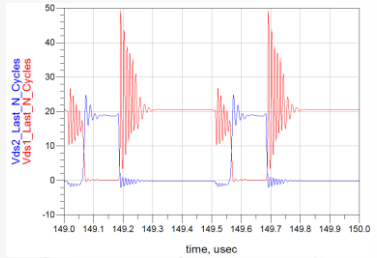
Schematic



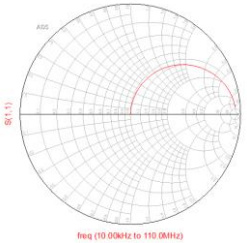
Layout



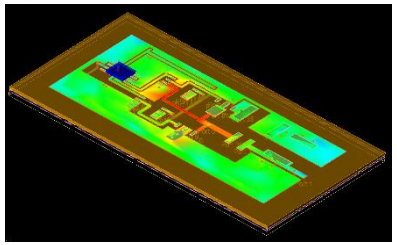
3D viewer



Transient/convolution

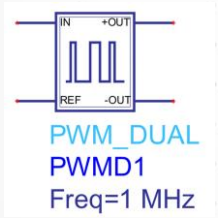


Linear simulator

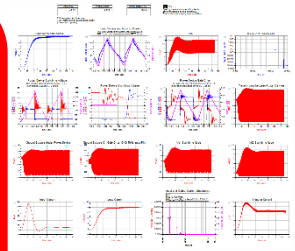


Momentum

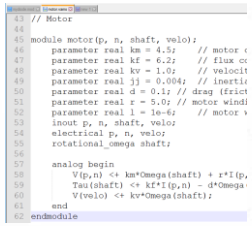
New!



Power Electronics Library

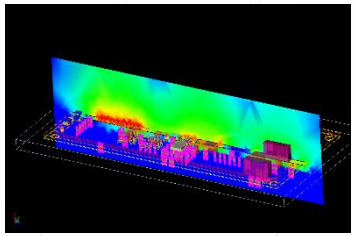


Data display

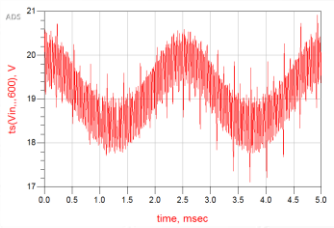


Verilog-A

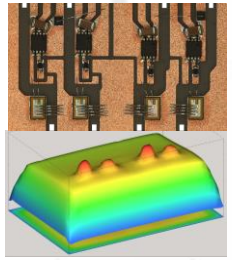
Product Options



W2342 FEM Simulator



W2300 Harmonic Balance Simulator

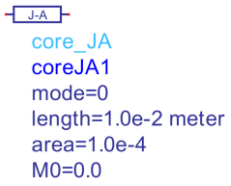


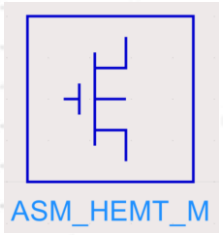
W2349 Electro-Thermal Simulator

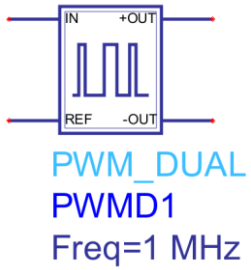
W2375 Power Electronics Library

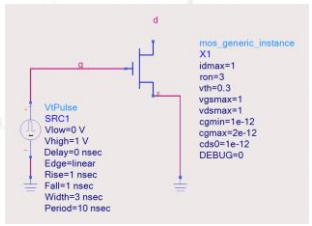
NEW IN ADS 2017 UPDATE 1

- Non-linear magnetics
  - MMF-flux circuits
  - Jiles-Atherton saturation/hysteresis core
- Power device models
  - ASM GaN
  - PowerMOS SiC
  - Si IGBT
- “Pre-selection” components
  - PWM
  - Gate Driver
  - Generic MOSFET









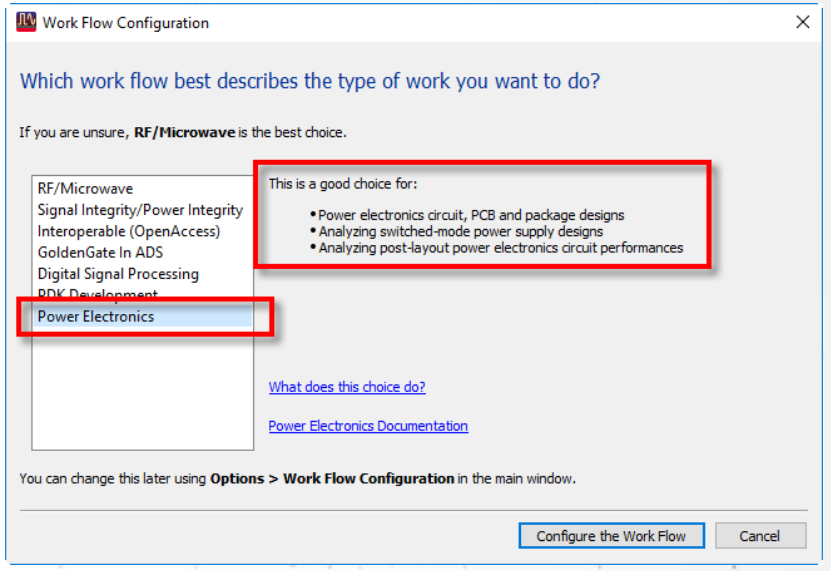
Power Electronics Library Etc. in ADS 2019

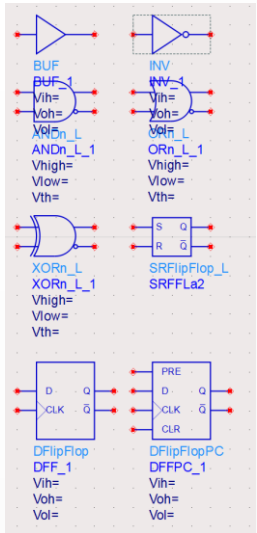
ADDITIONAL CAPABILITY SCHEDULED FOR NOV 1ST RELEASE

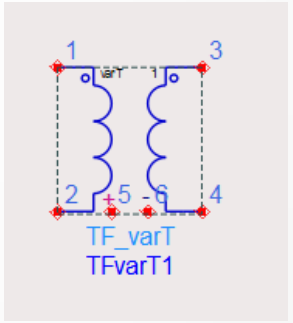
- Power Electronics “personally” in ADS:
  - [ADS Main Window]➔Options➔Work Flow Configurations➔ Power Electronics
  - Examples library (see next slide)
- Analog behavior of logic gates for digital loop compensators
  - BUF, INV, AND, OR, XOR, NAND, NOR, NXOR, D/SR Flip-flops, Schmitt
  - Compatible with equivalent components in LTspice and PSpice
- “Pre-selection” components
  - Voltage-controlled ideal transformer for “circuit average” abstraction method – duty cycle varies turns ratio in closed loop
  - 5-pin opamp: pwr/gnd rail noise, slew, bandwidth, etc.

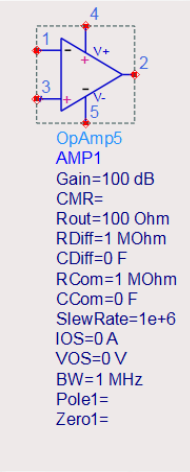
Note: Please preview and influence future releases by joining our beta program (“Early Access Program” EAP)

Contact your local Field Engineer or Application Engineer for details

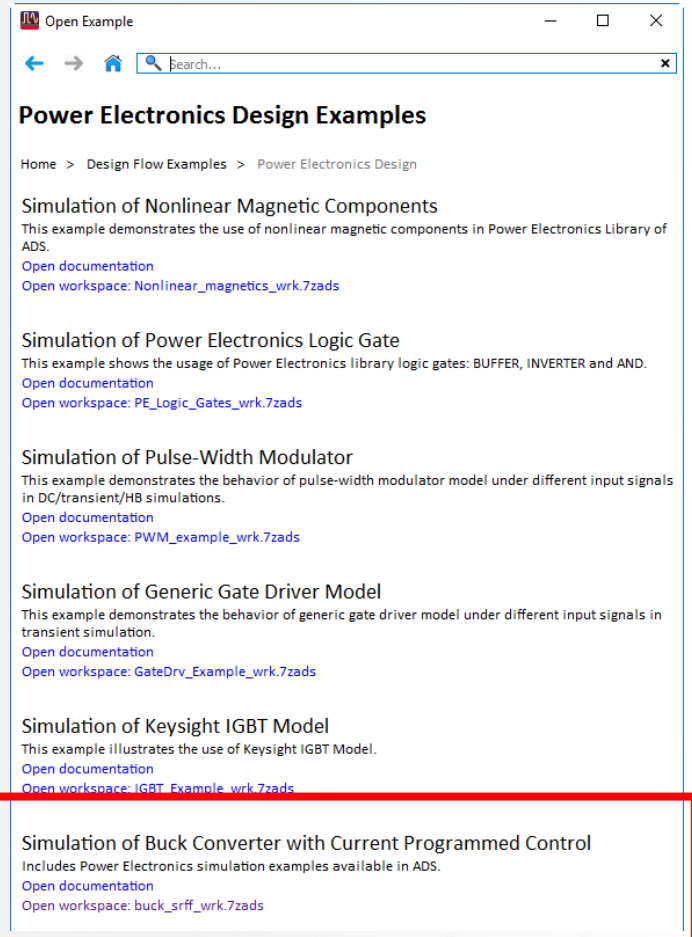


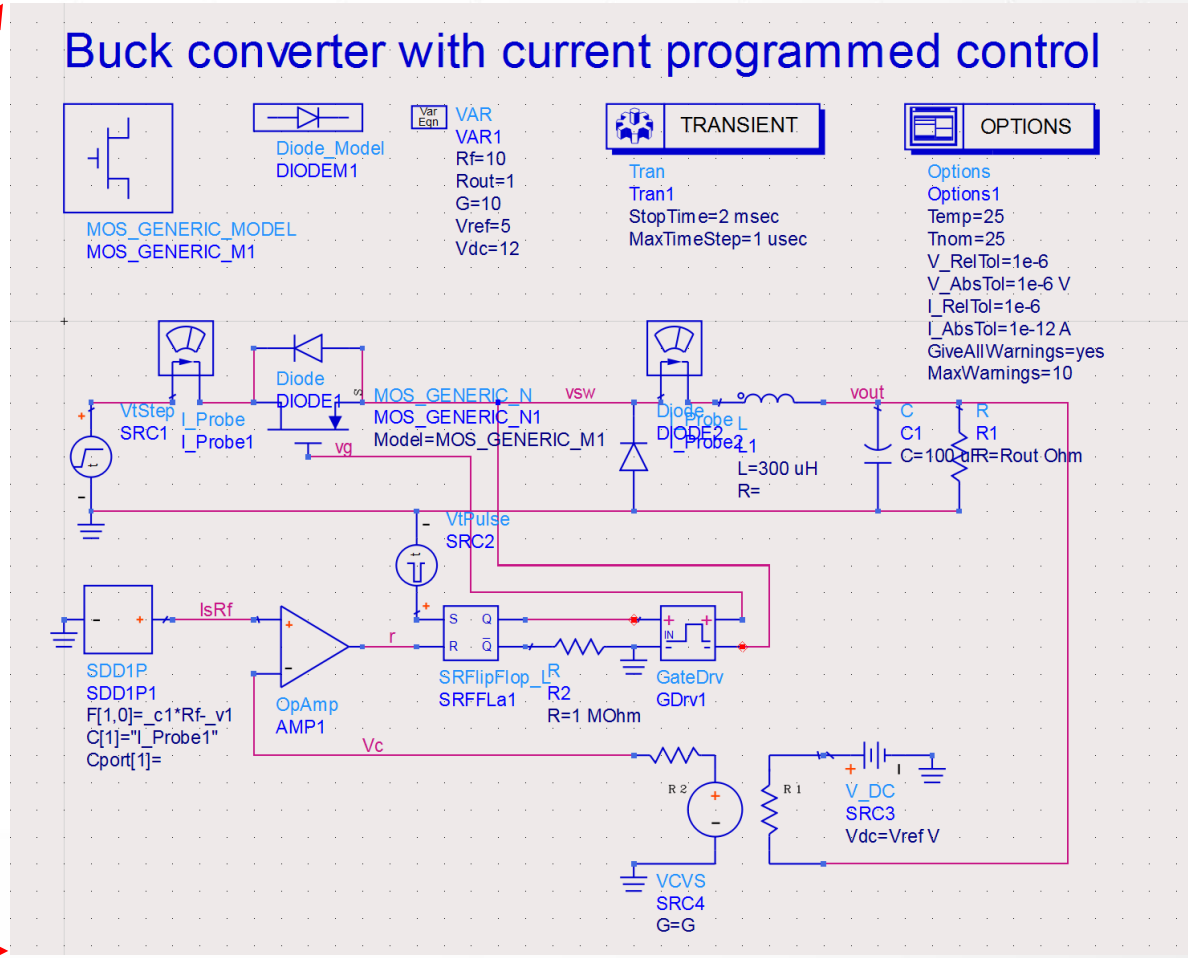




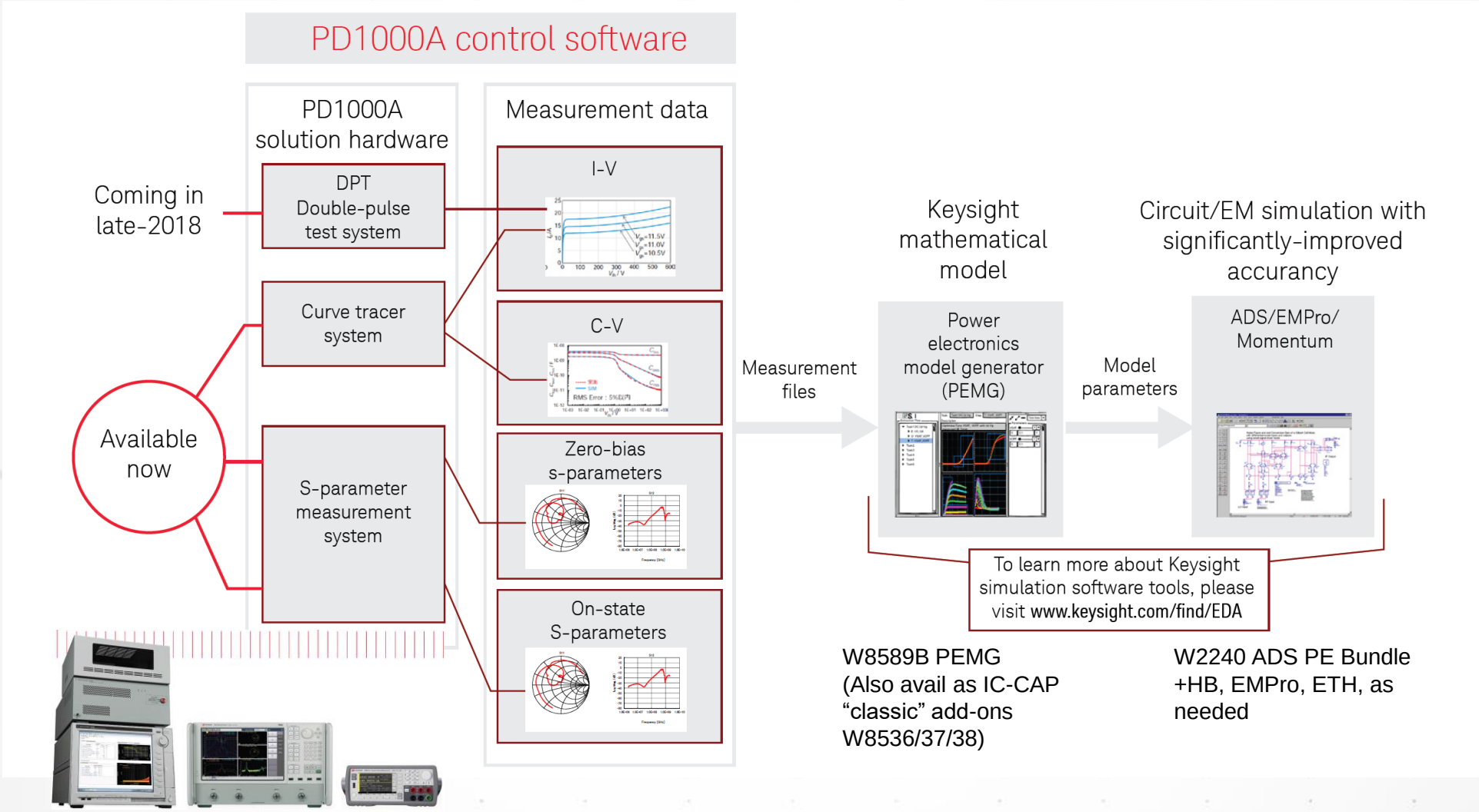


Examples Library Expanded in ADS 2019





Complete Work Flow



Switched-Mode Power Supply (SMPS)

WE GO WHEREVER THE POWER/ENERGY GOES

Sub-circuit simulation

Native ADS gate driver, analog/digital control loop incl. PWM

Electrothermal

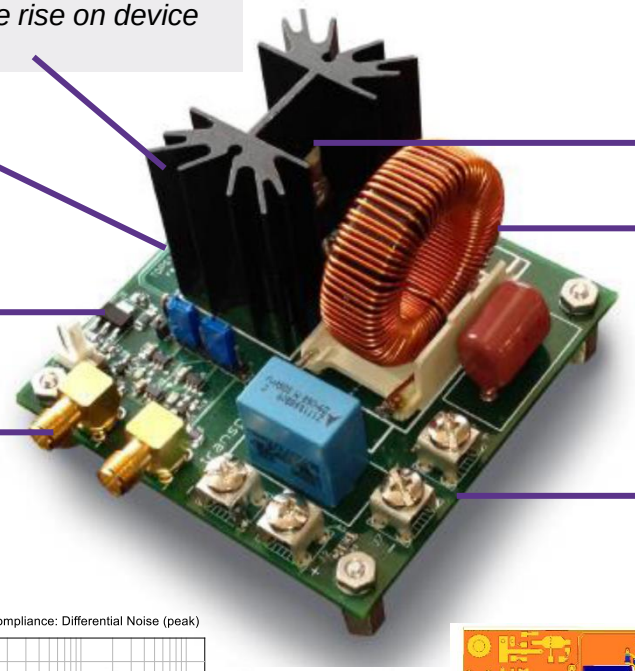
Solves for interaction of temperature rise on device heat output

Power Device Model Generation And Simulation

IGBT, PowerMOS incl. SiC, ASM GaN

Device and sub-circuit models for third-party tools

Import SPICE decks in non-ADS dialects: PSPICE, LTspice, etc.

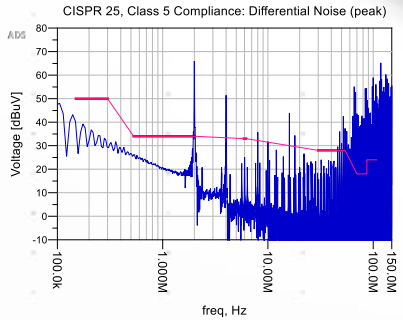


Non-linear magnetics

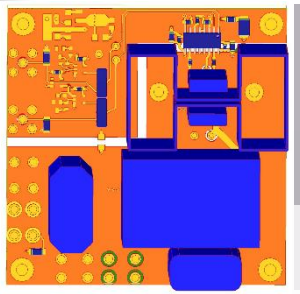
MMF-flux magnetic circuits
Jiles-Atherton saturation/hysteresis model

Connector simulation

Finite Element Method
Finite-Difference Time-Domain Technology



EMI/EMC



EM-based models: Package and board level parasitic extraction

Method-of-Moments Technology

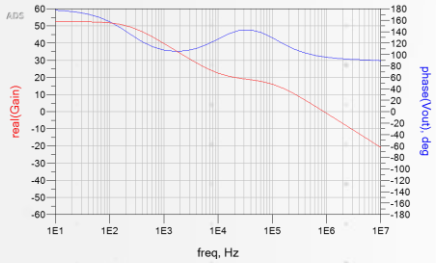
Center image credit: Transphorm

Keysight EDA Power Electronics Key Investment Areas

```
.MODEL mydiode D
+ RS=1.0000E-3
+ CJO=1.0000E-12
+ M=.3333
+ VJ=.75
+ ISR=100.00E-12
+ BV=100
+ IBV=100.00E-6
+ TT=5.0000E-9
```

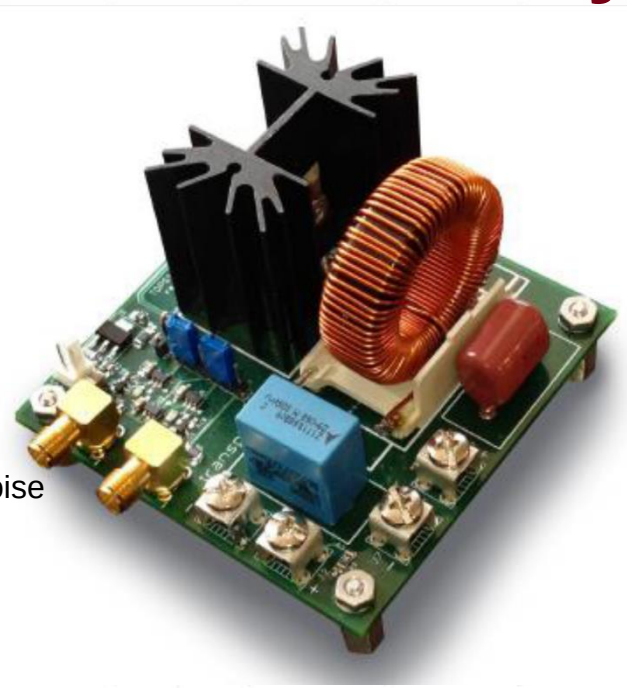
Multi-lingual model import

- Dialects of SPICE
- Verilog-AMS
- VHDL-AMS



Closed-loop analysis

- Bode plot
- Impedance analysis
- Stability in the presence of noise

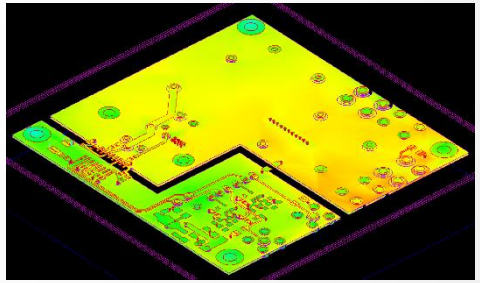


PathWave

- Connect device measurement, device modeling, circuit design, simulation, prototype characterization test, and manufacturing pass/fail test

Post-layout EM extraction

- PEPro (application-specific EM)
- Momentum (general purpose EM)
- EMI/EMC analysis

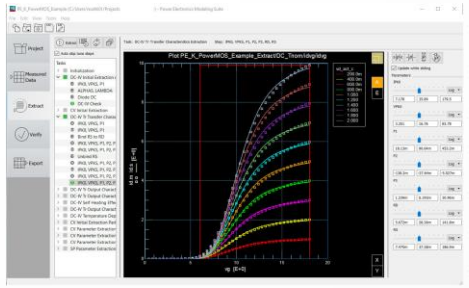


Multi-discipline, multi-nature support for motor control etc.

- Electrical: voltage/current
- Magnetic: MMF/flux
- Kinematic: position/velocity/force or velocity/force
- Rotational: angle/angular v./torque
- Thermal: temperature/power
- Logic: discrete or analog behavioral

Power device model generation

- IC-CAP: Full featured for device modelers
- PEMG: Simplified flow for circuit designers, models from a PDF datasheet



Center image credit: Transphorm

Case Studies

WIDE-BAND GAP POWER DEVICES ENABLE HIGH DI/DT

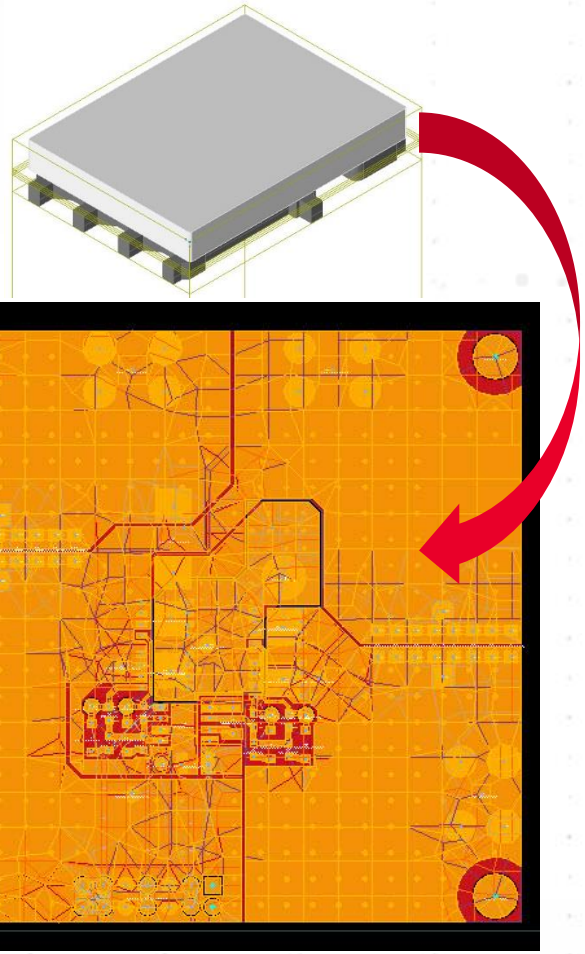
Predictive Results Can Be Obtained

On Semiconductor

REFERENCE DESIGN: POWER MOS + PACKAGE + PCB

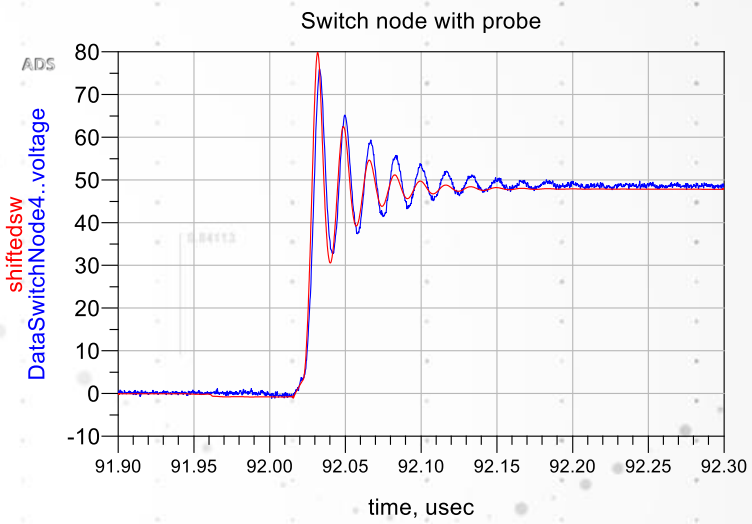
On Semiconductor Test Board

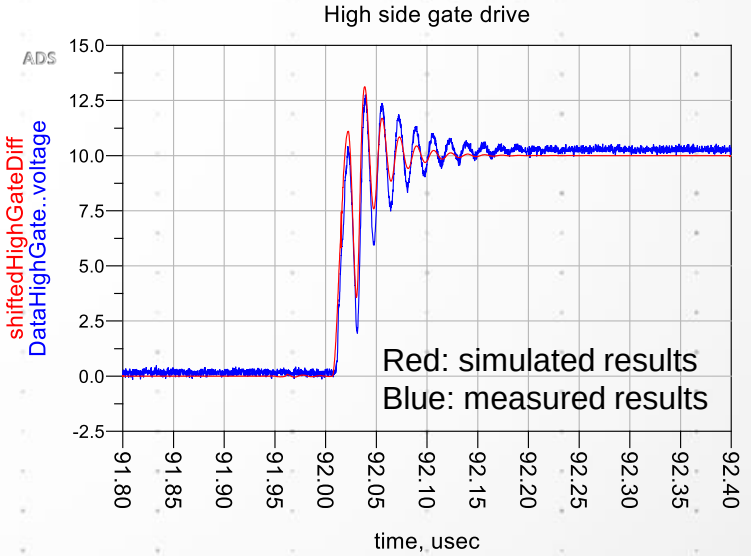
FDMS86181
PowerTrench® MOSFET
ADS package model



Customers often do not believe they can obtain predictive results. They Can!

Image courtesy of ON Semiconductor





Enabling Semiconductor Technologies

POWER SEMICONDUCTOR FIGURE OF MERIT (FOM)

Switching loss dominates conduction loss in high speed converters

Power Device Switching Loss:

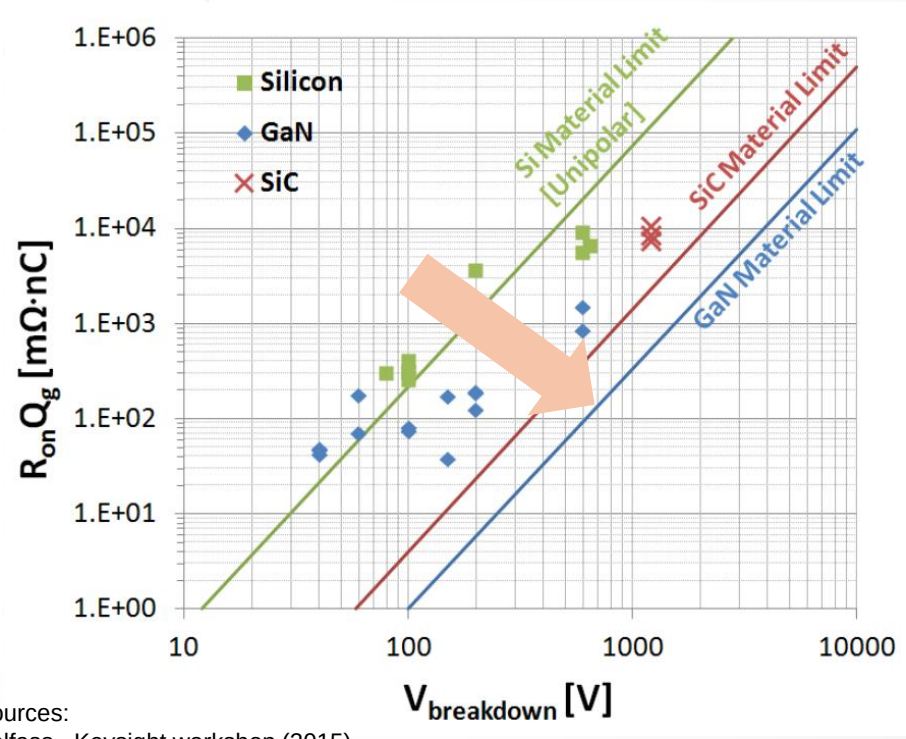
$Ploss = Rds(on)\ (ID)^2\ (rms) + ID\ VD\ (Qsw/IG)\ fs + 1/3\ Qds\ VD\ fs$

Transistor FOM:

On resistance (Ron) x gate charge (Qg)

- *Low Ron = low transistor loss*
- *Low Qg allows the device to switch on and off faster*

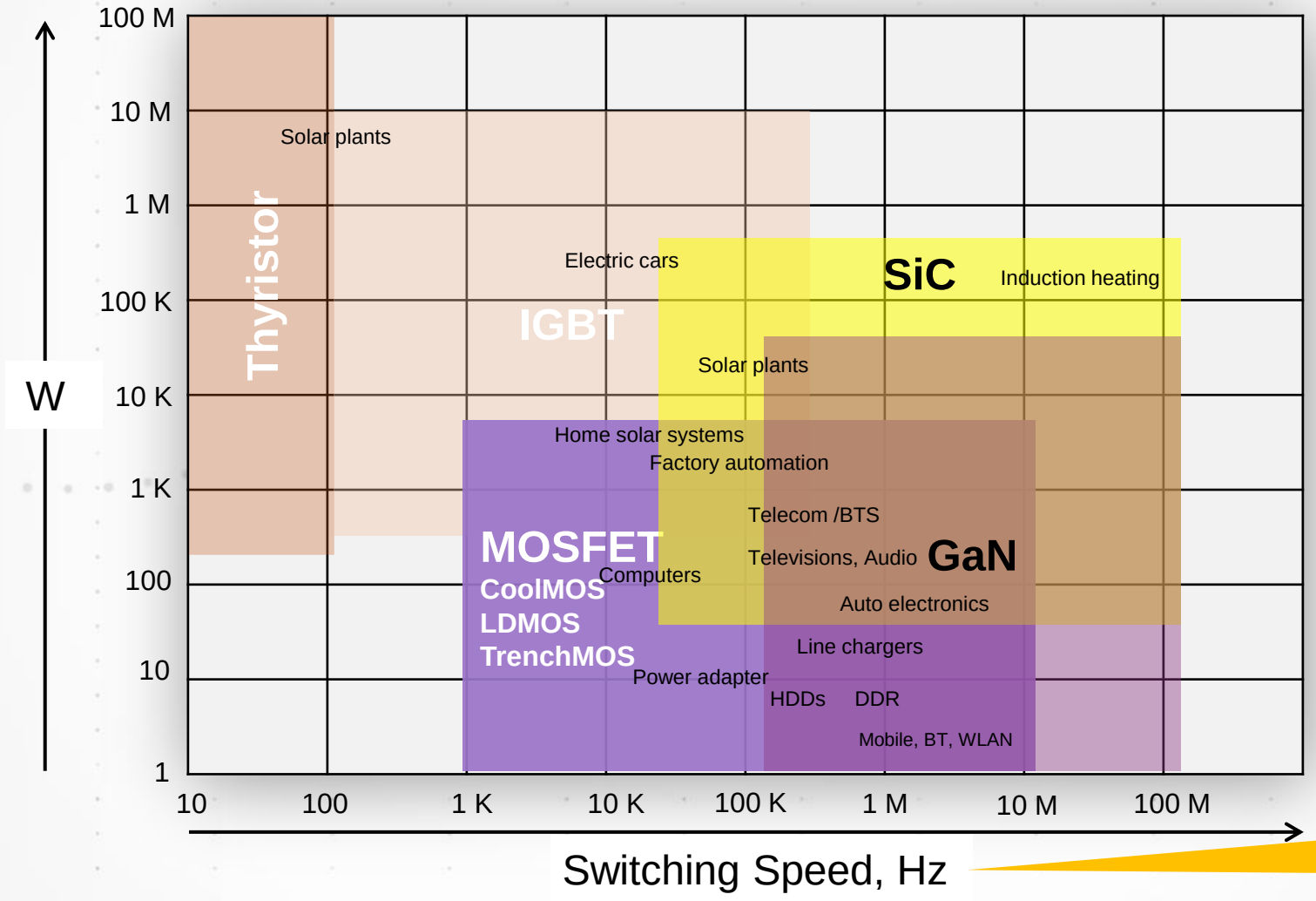
Small FOM = fast dv/dt switching



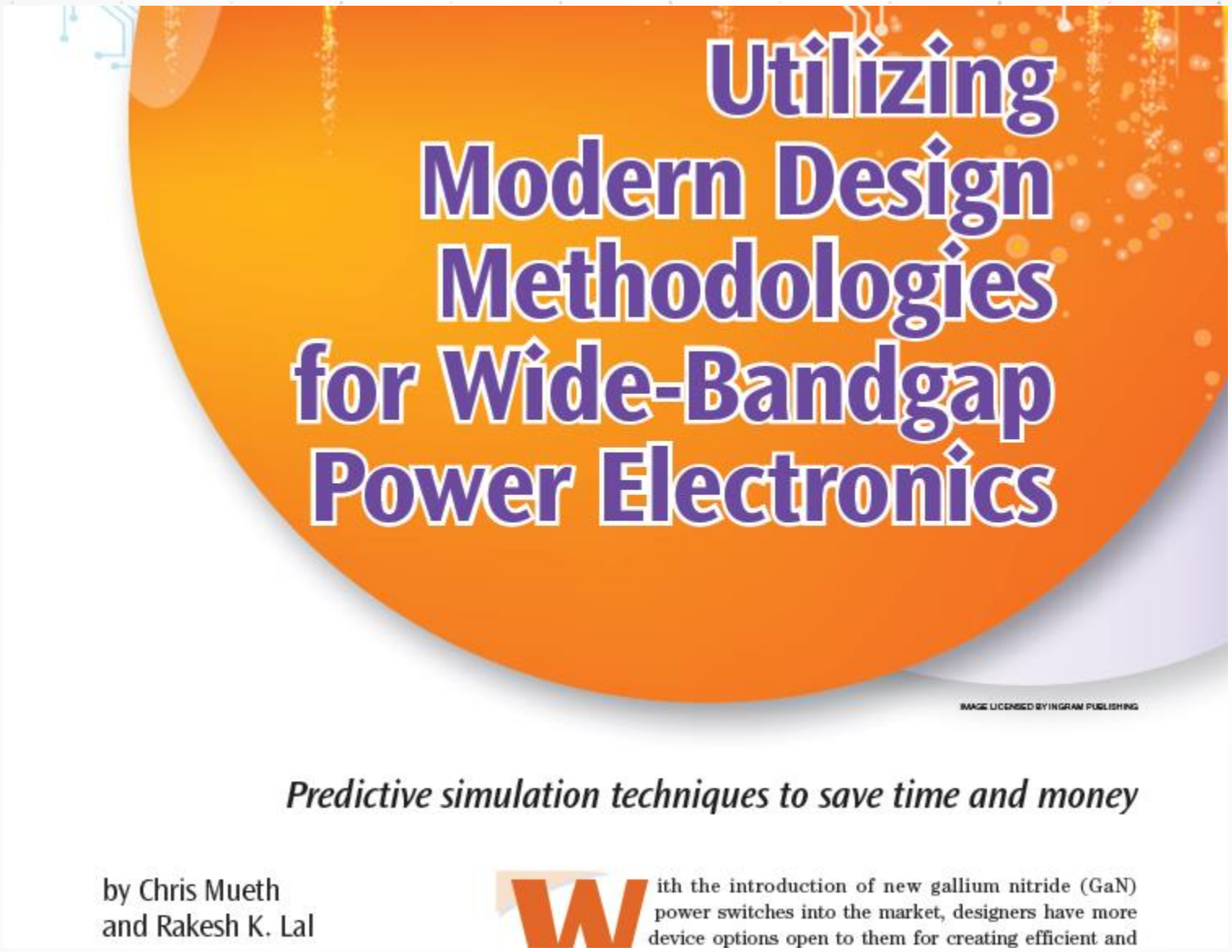
Sources:
Kalfass - Keysight workshop (2015)
Catrene (2013)

Enabling Semiconductor Technologies

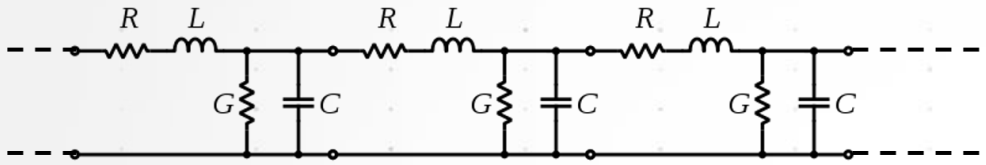
HIGH SPEED POWER CONVERTER APPLICATION AREA

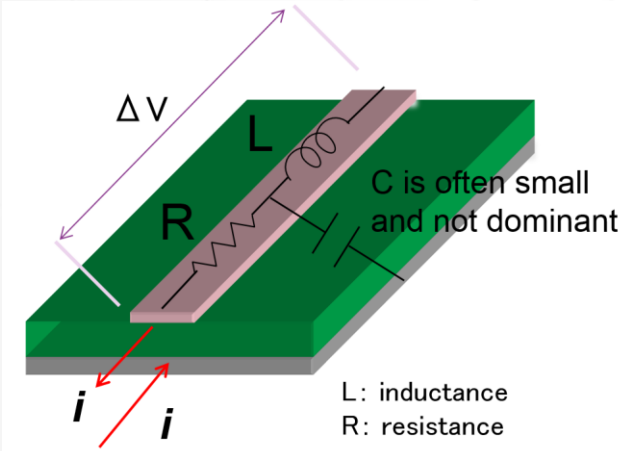


Rise/fall time and di/dt also increasing

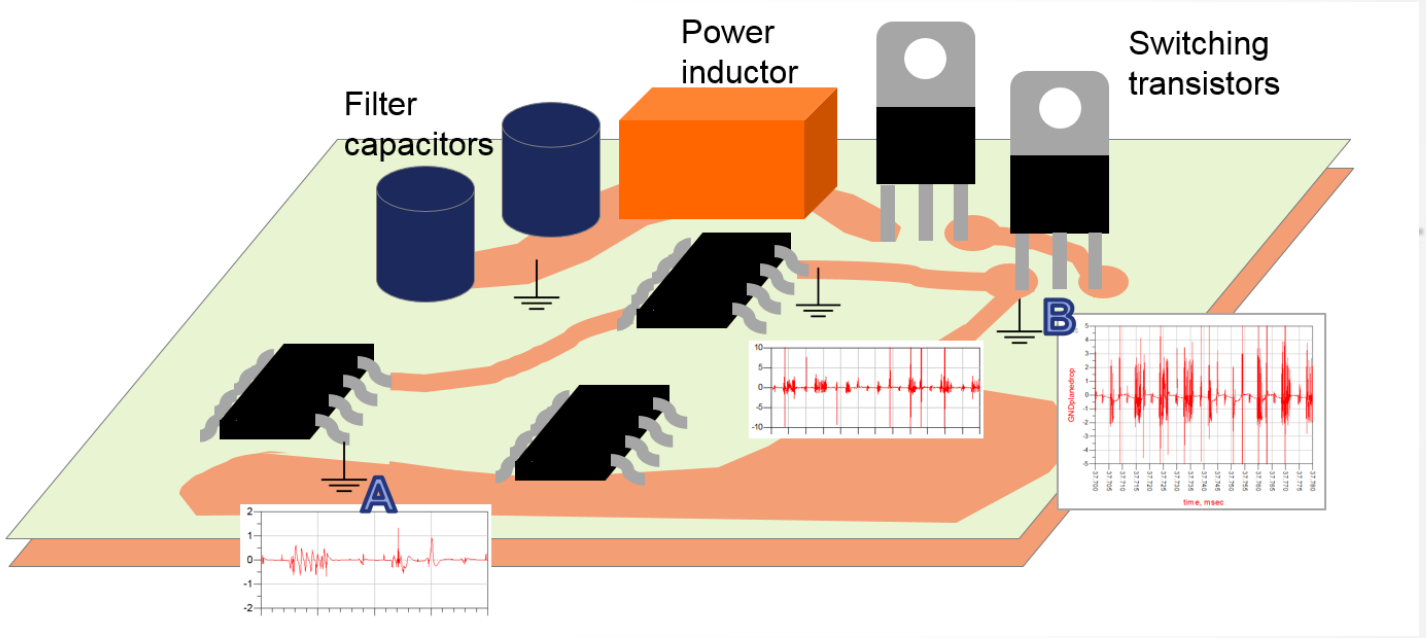


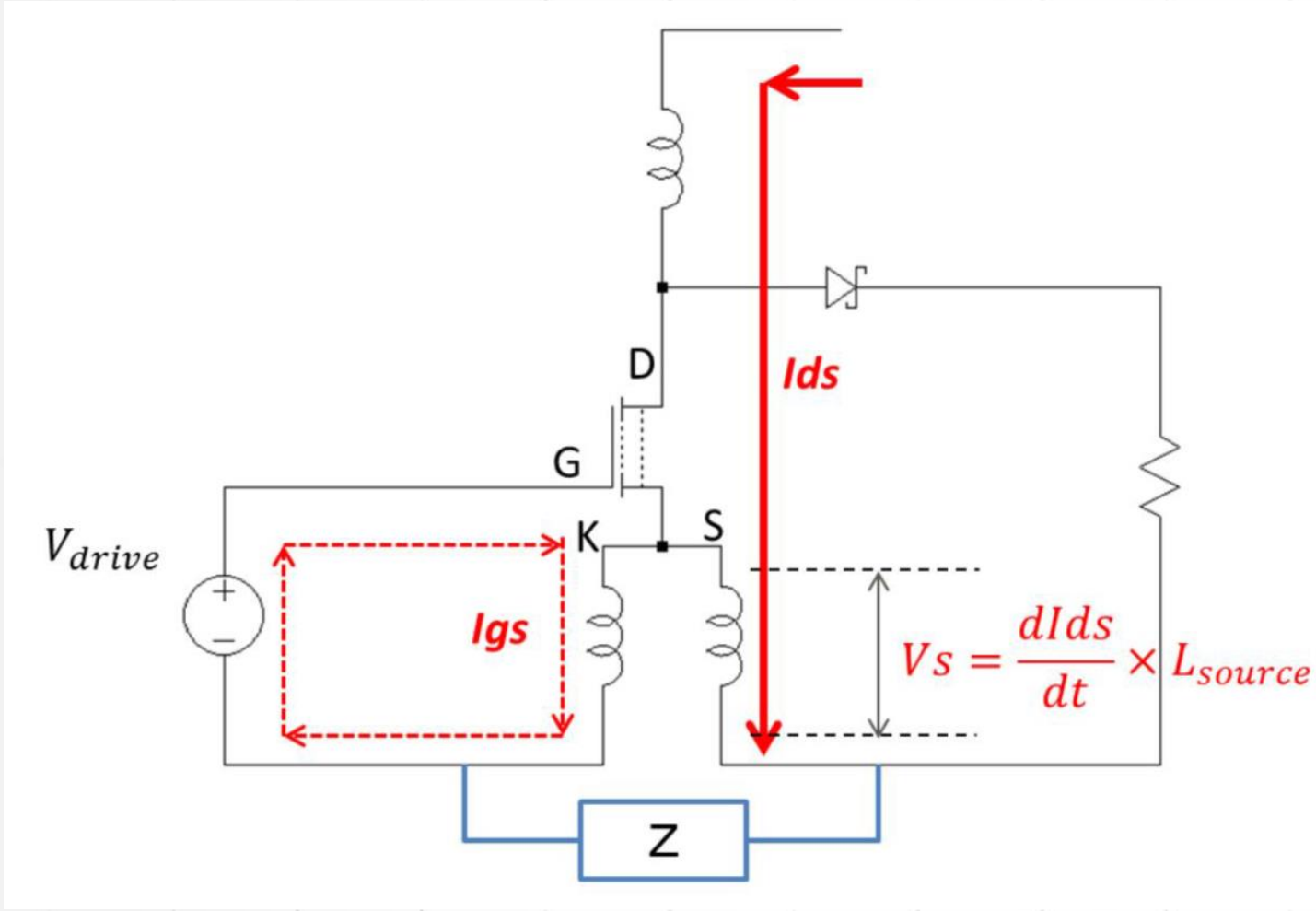
IEEE Power Electronics Magazine, June 2017 pp.46-55

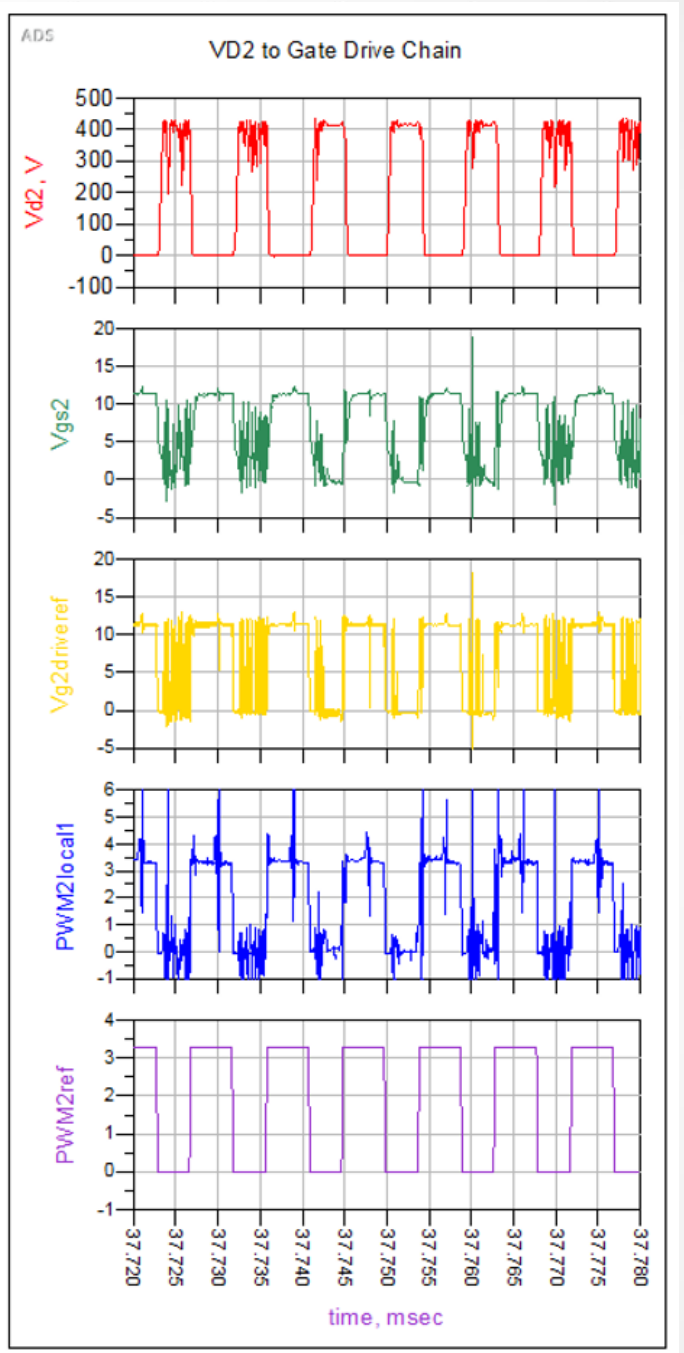




$$\Delta V = Ri + L\frac{di}{dt}$$





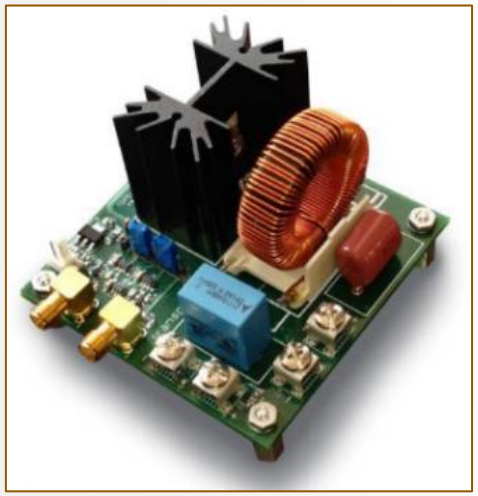


Identify the Limits of a Design

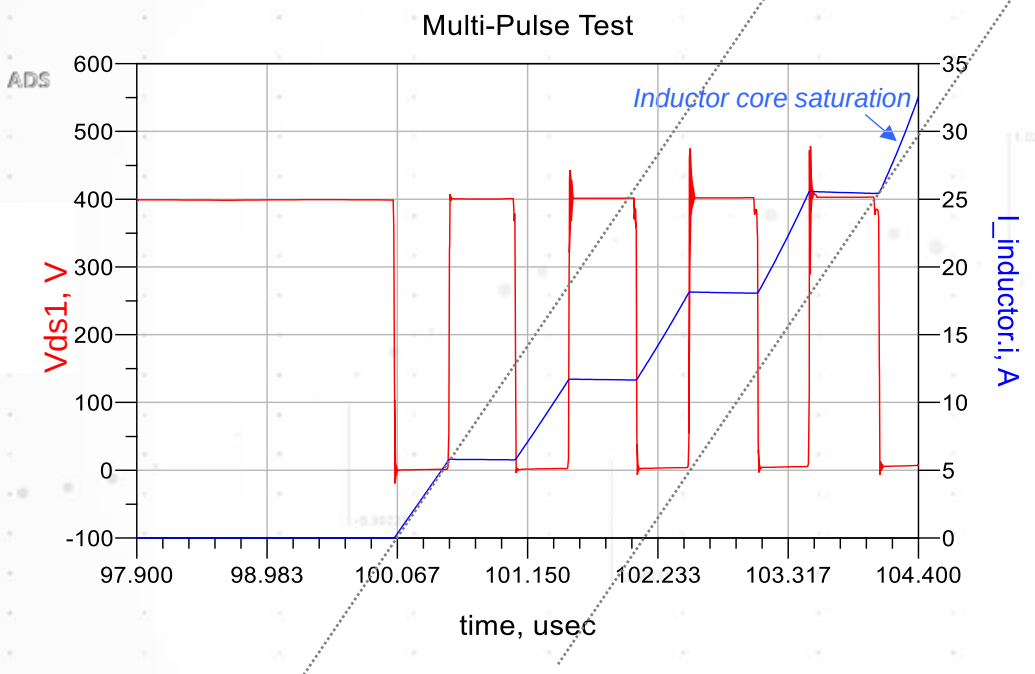
MULTI-PULSE TESTING

Transphorm

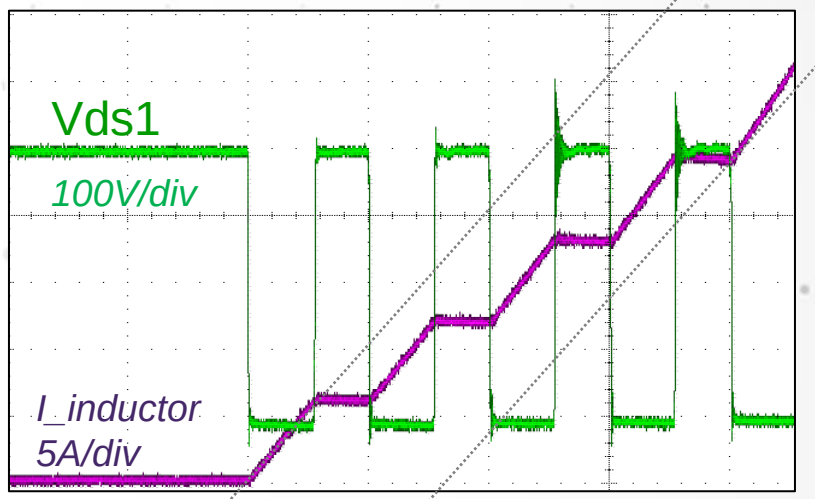
IEEE Power Electronics Magazine, June 2017 pp.46-55



ADS Simulated



Lab Measured



Designers using GaN devices often experience failures they blame on the devices. It is their layout which is at fault!

3 kW Multi-Phase PFC – Failure Analysis

ST Microelectronics

NOISE IMMUNITY IS COMPROMISED

Pre-layout Schematic Only

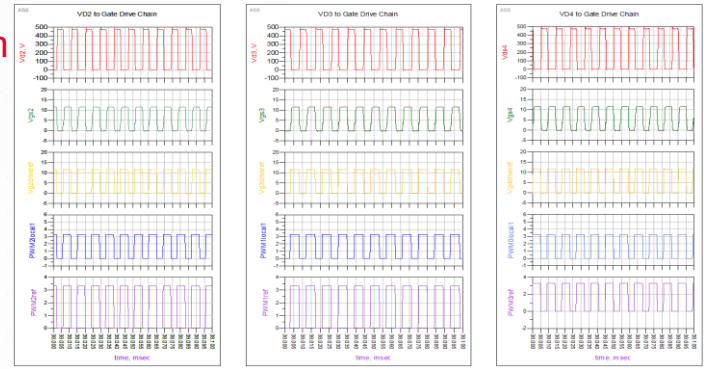
Power device drain

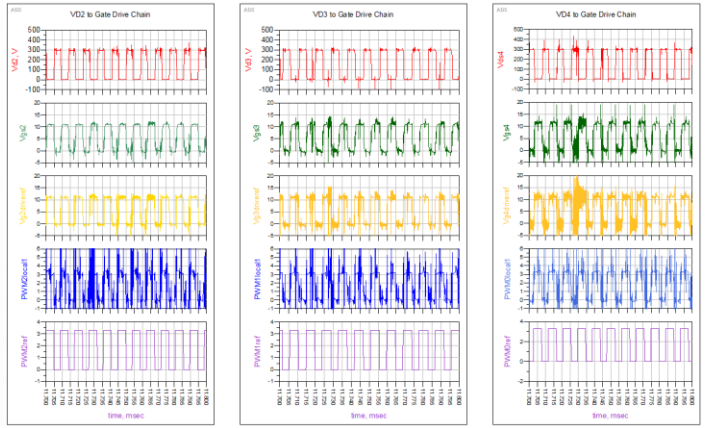
Power device gate

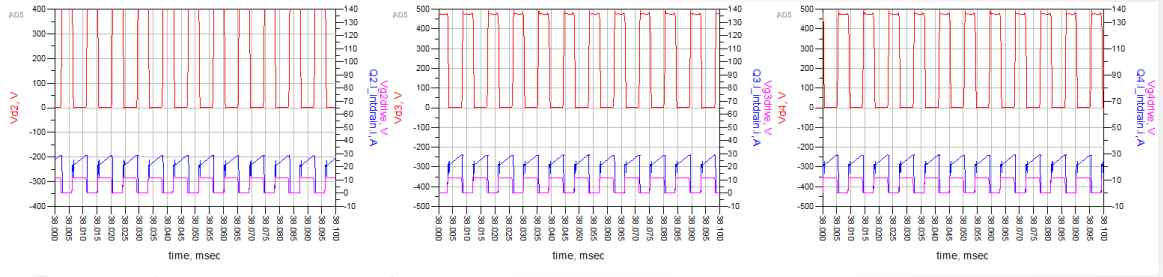
Gate driver output

Gate driver input

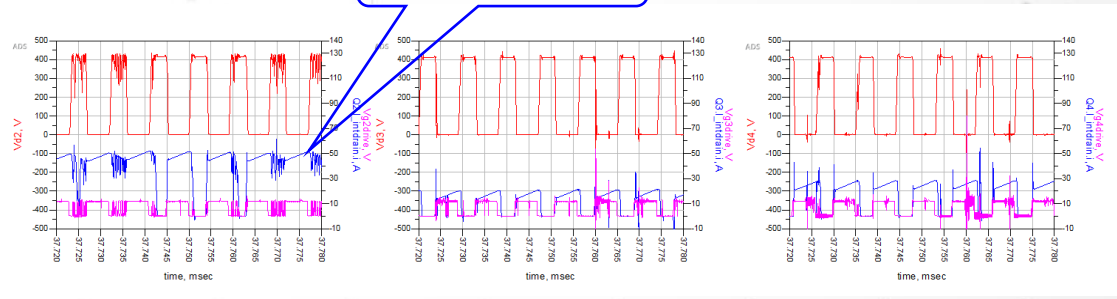
PWM output







Q2 current too high



Original layout EM Co-simulation

1st pass success of modified design

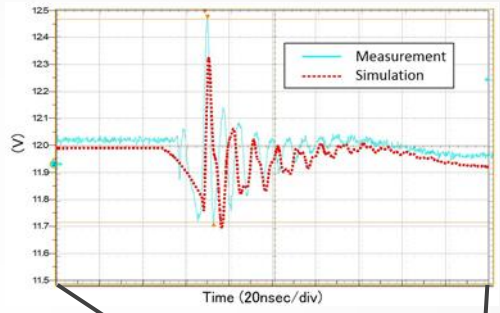
- 52W/cubic inch
- Pout = 3kW @ Vin = 230Vac
- Vout = 400V
- PF > 0.98 @ 20% load
- THD < 5% @ 20% load

Image courtesy of ST Microelectronics

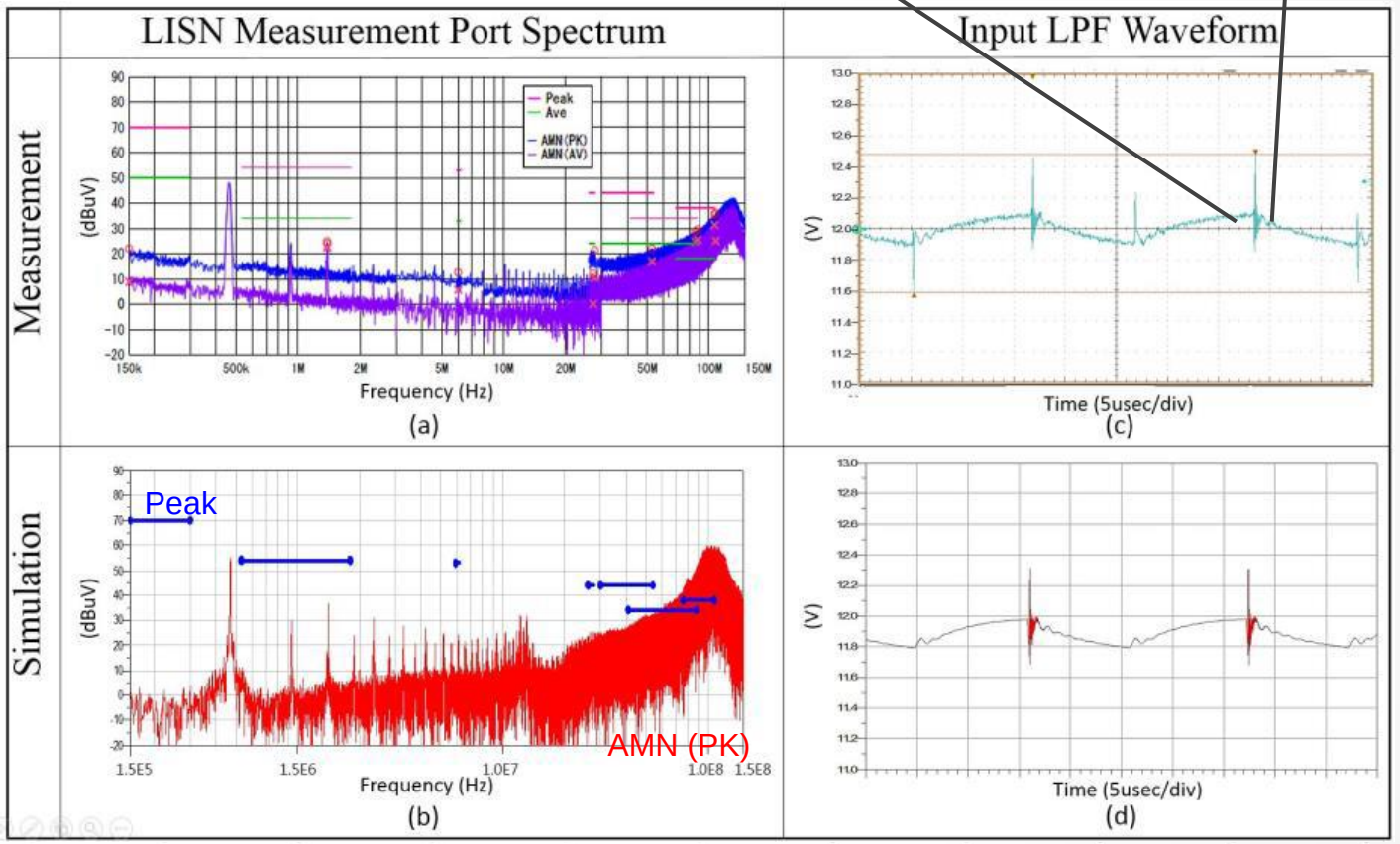
EMC Analysis

REASONABLE CORRELATION WITH MEASURED RESULT!

Rohm



EMC compliance testing is expensive and no insights are given on how to correct issues



International Conference on Electronics Packaging 2016: *Importance of Switched-Mode Power Supply IC Model for Conductive EMI Noise Simulation*
CISPR, part 25

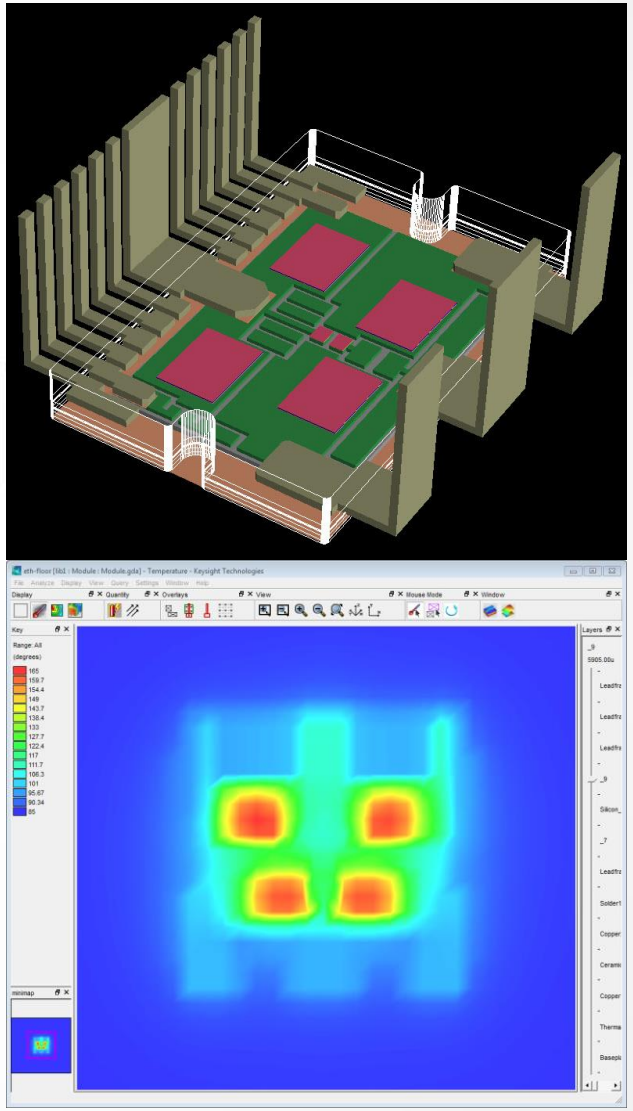
Thermal Floorplanning

On Semiconductor

SIC POWER MODULE ANALYSIS – ALL WITHIN ADS

Device	ICEPAK Point tool	ADS Electro-Thermal	Delta [K]
Q1	172.4	169.0	3.4
Q2	169.8	168.1	1.7
Q3	168.4	167.5	0.9
Q4	168.4	167.5	0.93

Temperatures are often difficult to measure in the lab, and thermal tools are difficult to use and too slow to be practical.



Simulation time ~25 seconds!

Conclusions

- Increasing power density trends are pushing up switching speed
- High switching speed introduces a whole new class of challenges
  - Parasitic effects destroy performance and are costly
- EM Co-simulation provides the best predictive analysis you can get
  - An integrated workflow provides more capability and streamlines the workflow
  - Quick Start Guide for ADS in Power Electronics
    https://literature.cdn.keysight.com/litweb/pdf/5992-2514EN.pdf