Digital Control for Power Electronics 2.0

Michael Harrison

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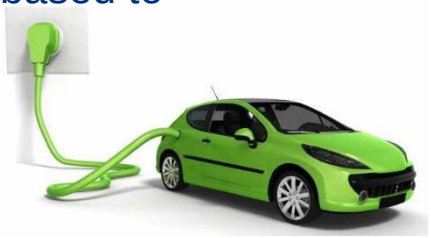
Driving Factors for Improved SMPS Control

- End market requirements for improved SMPS performance:
  - Power conversion efficiency
  - Wider control range
  - Faster load & input step response
  - Lower cost
  - Reduced size
  - Improved reliability
  - EMC – conducted/radiated emissions & surge robustness
- Growth of end market applications:
  - The transition from a carbon based to electron based economy
  - Renewable energy
  - Electric Vehicles

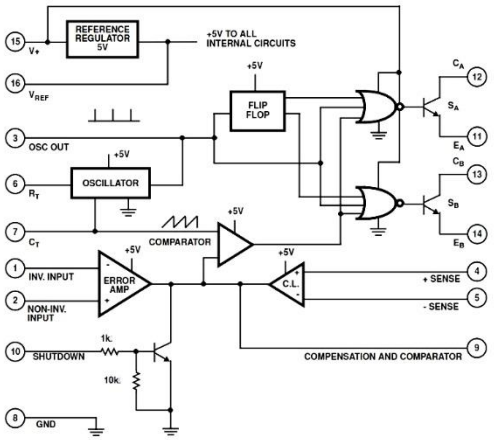


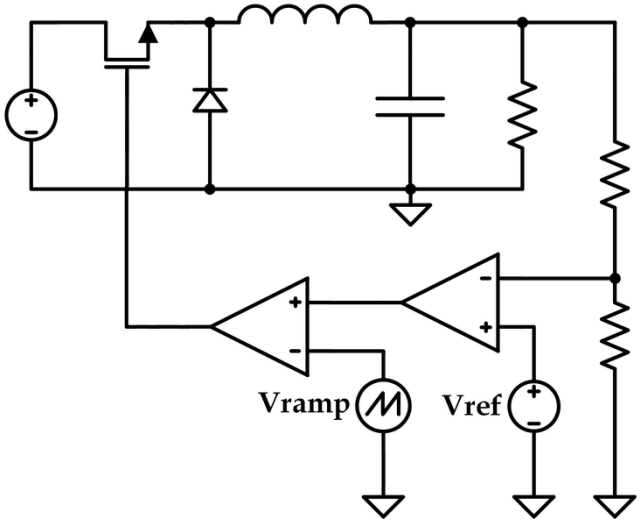
- Wide Band Gap semiconductor power switches:
  - SiC MOSFETs & GaN HEMT FETs
  - Enabling a more to higher switching frequencies

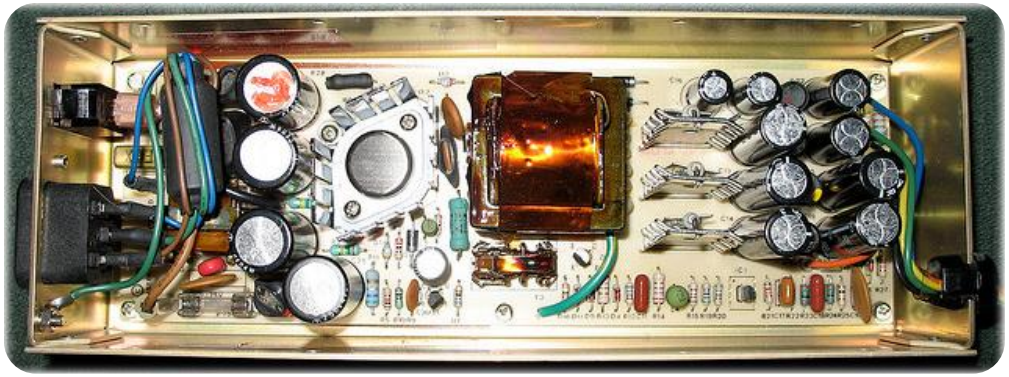
- Advanced power conversion topologies

In The Beginning…

- In 1976 Silicon General introduce the SG1524:
  - The first integrated circuit specifically designed for Switched Mode Power Supply (SMPS) control
  - Analog based control ASIC with 72 transistors (10um)
- In 1977 Apple popularize SMPS for powering the Apple II personal computer

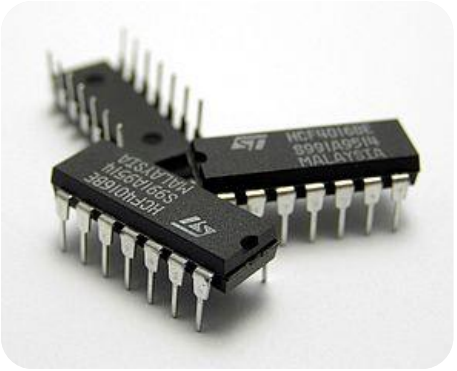




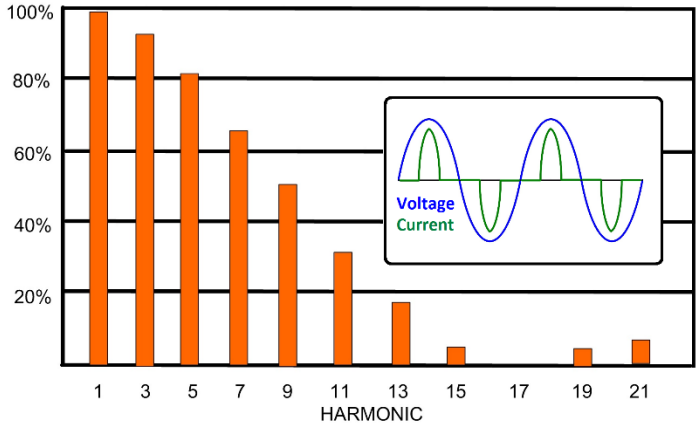


The Proliferation of Analog Control ASICs

- During the last three decades of the 20th century hundreds of different new analog control ASICs were developed



- The factors driving this proliferation:
  - Development of new control methods:
    - Voltage mode, peak current mode, average current mode, constant on-time control, constant off-time control, hysteretic control, multi-mode control, burst-mode control, etc.
  - Power supply circuit topologies:
    - Flyback, buck, boost, push-pull, half-bridge, full-bridge, phase shifted full-bridge, asymmetric half-bridge, quasi-resonant, resonant, ZVS, ZCS, LLC, PFC, interleaved, etc.
  - End market legislative changes:
    - Power Factor Correction – IEC 61000-3-2
    - Energy Efficiency – Energy Star 80-plus



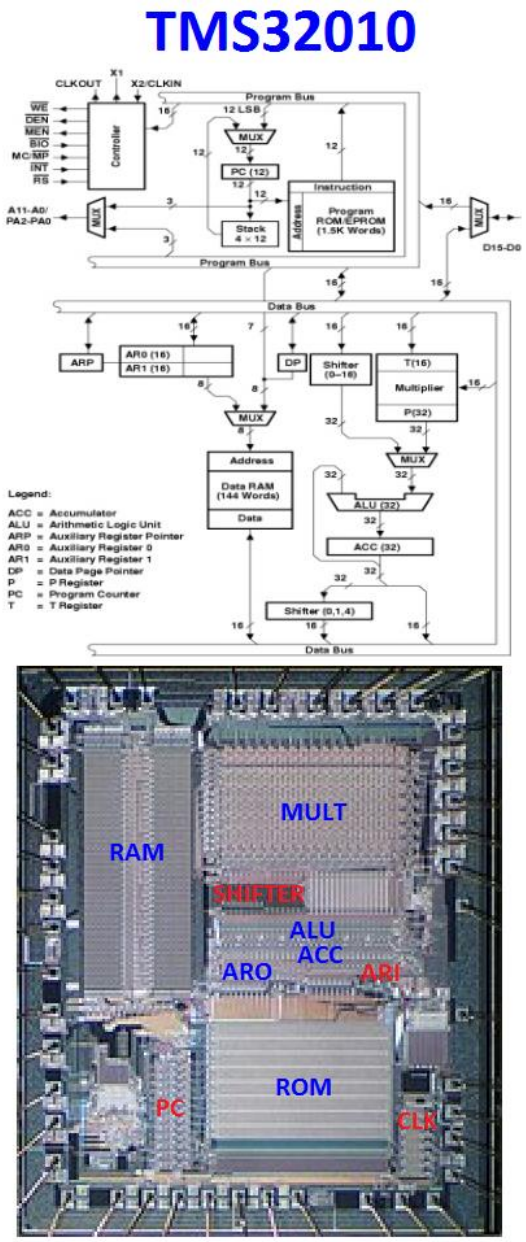
Limitations of Analog Control for SMPS

- Low accuracy and repeatability of control:
  - Inherent limit for control complexity resulting in the adoption of primitive control
  - Complex and expensive calibration requirements

- The inherently fixed design of analog control ASICs:
  - The pace of control technology advancement is limited by semiconductor companies ability to develop new control ASICs

The Rationale for Digital Control

- Superior control performance:
  - Accurate and repeatable control
  - Enables complex control functionality:
    - Control linearization
    - Multi-mode control
- Design reuse:
  - One controller can be used for multiple applications
  - Code reuse – libraries of standard control functions
- Communications functionality:
  - Manufacturing automation – calibration, self test, etc.
  - Monitoring and supervisory functions
  - Firmware upgrade capability
- In 1983 Texas Instruments Introduce the TMS320:
  - The first “single chip” digital microcontroller with Digital Signal Processing (DSP) functionality - $500 price!
  - Digital based control ASIC with 57,000 transistors (3um)
  - Ideal for power electronics control applications



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The Inflection Point for SMPS Control

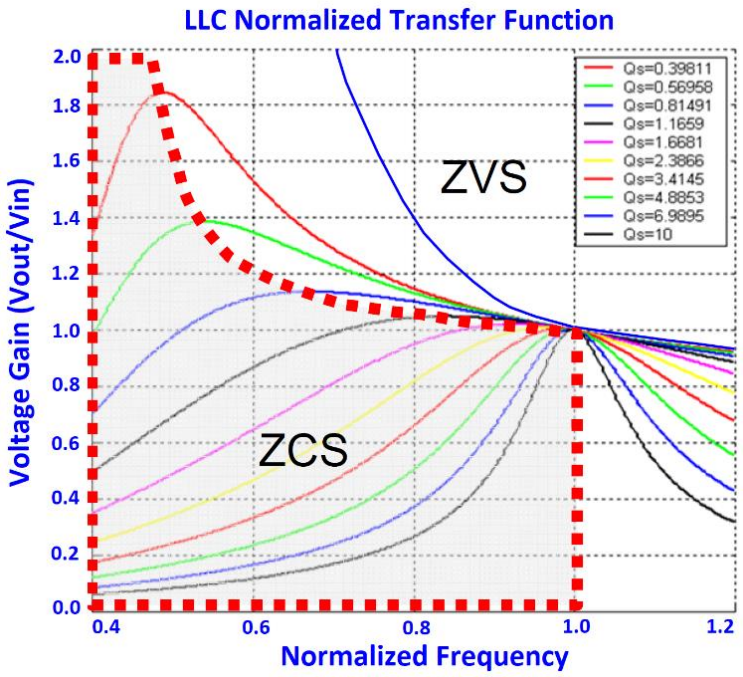
- The consequence of Moore's Law over the last 34 years from the introduction of the TMS320 in 1983 has enabled a factor of 130,000 more transistors to be integrated in an ASIC:
  - Enables even more control complexity
  - The main consequence however is enabling cost reduction – "die shrinks"
- The cost of digital control is approaching a packaging cost asymptote
- Signal-to-Noise requirements limit the minimum feature size that can be used for analog control ASICs:
  - The cost of analog control is not influenced by Moore's Law and does not reduce over time
  - End market legislative changes can drive increased control complexity over time
- The analog Vs digital controller cost parity point for SMPS applications occurred about a decade ago
- Some modern SMPS controllers that appear to be analog are in fact implemented in digital logic

Limitations of Conventional Digital Control

- Relative to the high switching frequencies used in SMPS applications the control speed possible with conventional digital control is very slow:
  - The PWM duty cycle value might typically be updated once every 10 switching cycles
  - The control latency that results from this slow update rate ultimately limits the maximum control loop bandwidth and hence load-step response
  - Operational conditions can change significantly over the period of 10 switching cycles – especially during load-step conditions
  - The update speed ‘bottle-neck’ with conventional digital controllers is inherent with microcontrollers that execute sequential logic (software code)
  - This inherent sequential logic ‘bottle-neck’ severely limits the control complexity that can be executed at the PWM update rate
  - The maximum ADC sample rate for typical microcontrollers is much higher than the inherent sequential logic ‘bottle-neck’
  - The improved control accuracy and repeatability that comes with digital control is no substitute for control speed

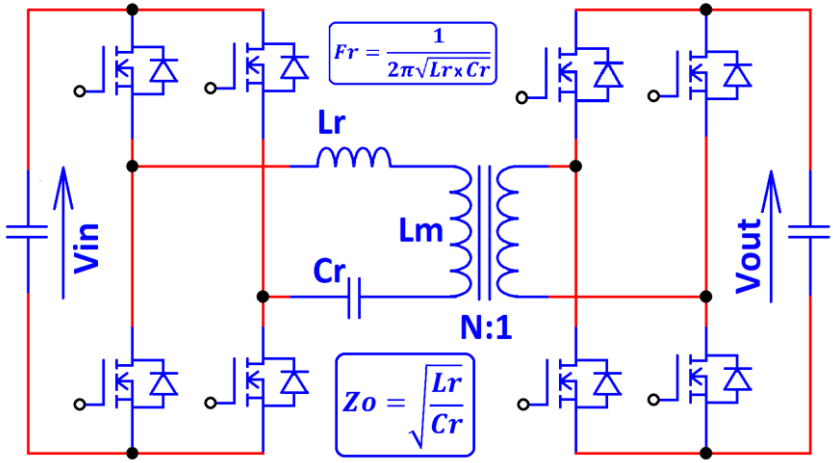
The LLC – A Practical Resonant Converter

- The utility of a 3 element resonant tank:
  - Enables simple variable frequency control
  - Output voltage/current regulation
  - Boost function – Vout/Vin>1 for F_n<1
  - No load regulation
  - Minimize switching frequency range



- Short circuit problem:
  - Need to avoid operation in ZCS region
  - A load step in boost mode operation can potentially drive into ZCS region

- Typical 1.8kW telco design solution:
  - Vin = 405 – 435V
  - Vout = 43 – 57.5V (54V nominal)
  - Cr = 72nF
  - Lr = 8uH
  - Lm = 26uH
  - Fr = 210kHz
  - Z_o = 10.5Ω
  - Lm/Lr = 3.25



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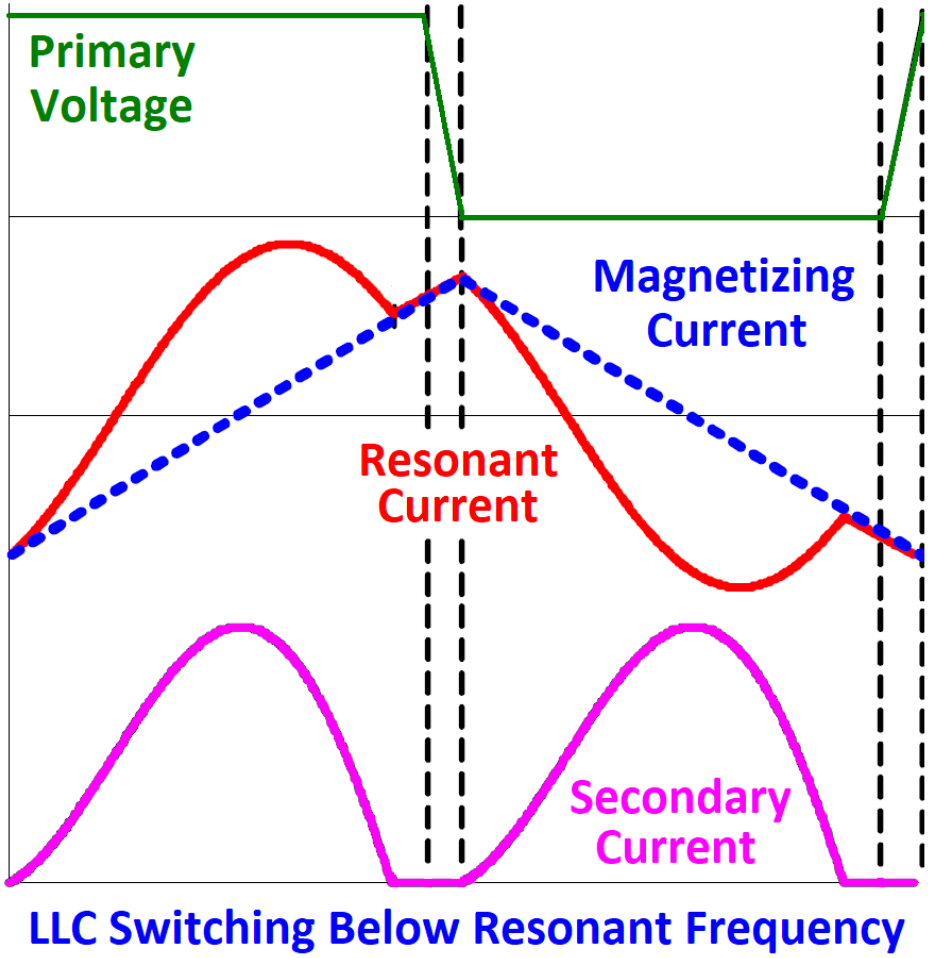
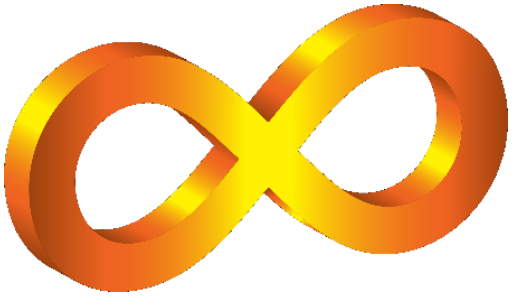
LLC Design Challenges

- The design cost for voltage/load regulation:
  - Low characteristic impedance (Z_o) of resonant tank – e.g. 11% of minimum load impedance
  - Ideally Z_o should equal load impedance for best conversion efficiency
  - Small inductor ratio (Lm/Lr) e.g. 3.25
  - Lm represents 30% of full load impedance at F_{min}
  - Magnetizing current is the dominant primary side load
  - This is the cost of simple control
- Synchronous rectifier control challenge:
  - Need to turn gate off early in boost mode
  - SR package inductance timing influence
  - Timing inaccuracy lowers efficiency



Beyond the Analog/Digital Inflection Point

- Moore's Law is continuing to enable more complexity in digital control:
  - Digital control cost is approaching a packaging cost asymptote
  - The incremental cost of increased control complexity is effectively zero
    - Apart from the ASIC engineering development costs
- The 'infinite computing complexity' thought experiment…
- "How could you improve a power supply if there was no limits to the control complexity that could be adopted?":
  - Approximate control techniques can be replaced by complex exact calculations
  - Consider primary, secondary, tertiary, and any higher order effects into control logic
  - Adopt topologies that are more complex to control:
    - e.g. Dual Active Bridge series resonant converter
- This thought experiment is useful if a practical solution exists before the reductio ad absurdum of infinite control complexity



Optimum Trajectory Control

- First proposed by Oruganti, Lee, & Yang in 1988:
  - Energy in a resonant LC tank follows a circular trajectory
  - Very complex and technically challenging control:
    - Need to monitor many high bandwidth signals
    - Need for low signal latency with accurate delay matching
    - Mathematical complexity – low latency ‘squaring function’
  - Primitive implementation based in analog control:
    - Single active (half) bridge LC series resonant topology
    - Trajectory control not used for ZVS commutation control
- What is technically possible today:
  - Ability to apply trajectory control to more complex resonant converter topologies – e.g. Dual Active Bridge
  - Full control of ZVS commutation for optimum efficiency
  - Real time hardware simulation:
    - Predictive control – delay compensation
    - Control optimization and self calibration

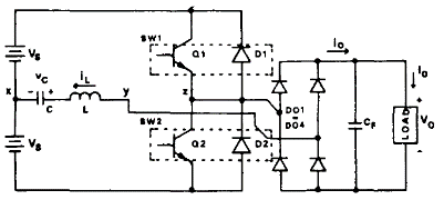


Fig. 1. Half-bridge series resonant converter.

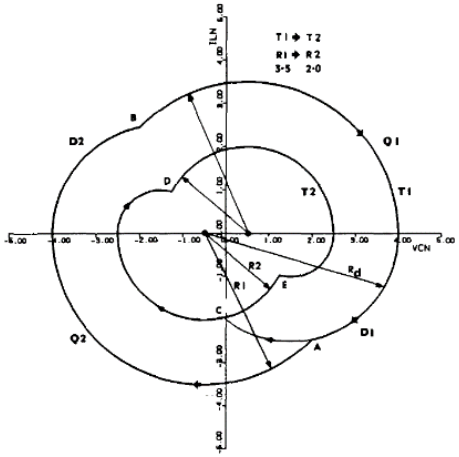
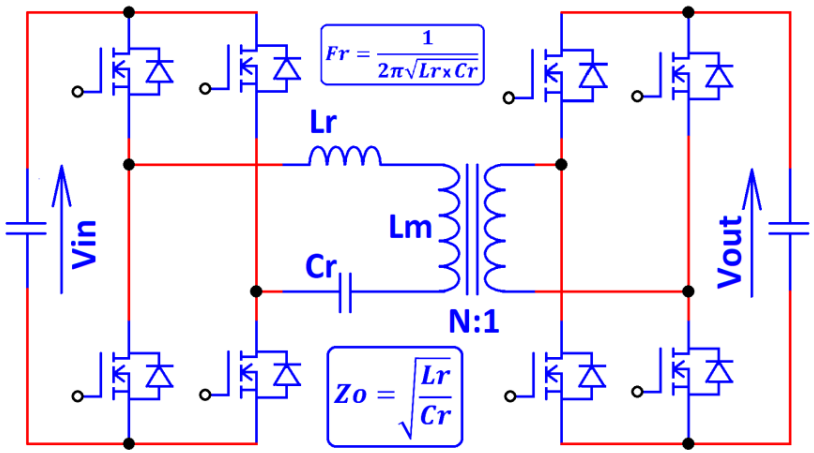


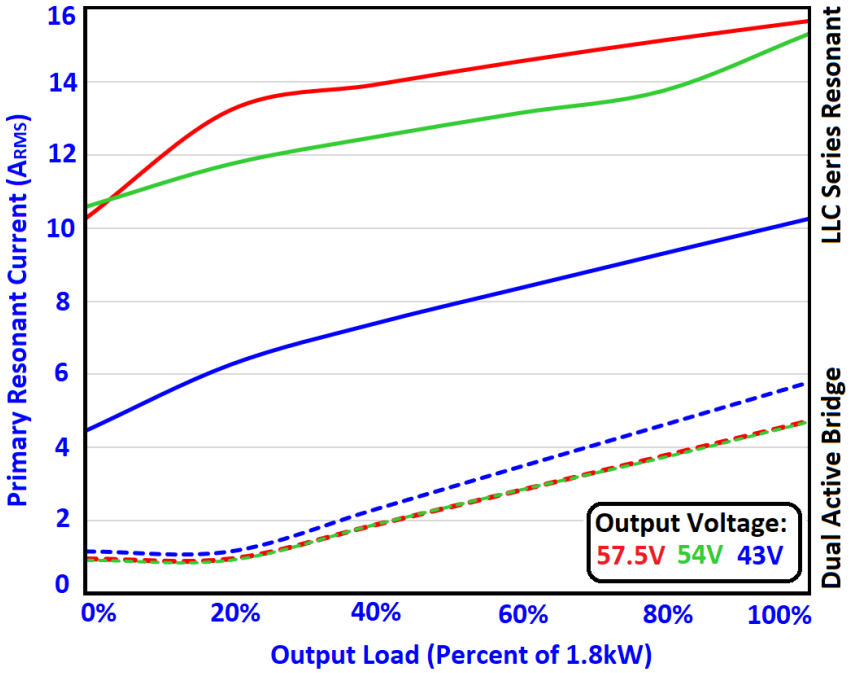
Fig. 6. Response of optimal trajectory control for step control change ($V_{ON} = 0.5$).

Dual Active Bridge Series-Resonant Converter

- Secondary side synchronous rectifier (SR) devices are controlled as an active bridge:
  - Conventional SR control = 'dumb diode emulation'
- Optimum Trajectory Control can minimize the need for circulating resonant currents:
  - Transformer core gap eliminated to maximize Lm
  - Primary to secondary bridge phase shift is utilized to maintain sufficient tank energy
  - Excellent efficiency over a extremely wide control range
- Symmetrical converter enables bi-directional power flow control
- Alternative 1.8kW telco design solution:
  - Vin = 405 – 435V
  - Vout = 43 – 57.5V (54V nominal)
  - Equivalent switching frequency range to LLC design
  - Cr = 10nF
  - Fr = 162kHz
  - Lr = 96uH
  - Z_o = 98Ω (= min. Z_{load})
  - Lm = 3mH
  - Lm/Lr = 31
  - Magnetizing current represents less than 0.1% of full load resonant current



Primary Resonant Current as a Function of Load



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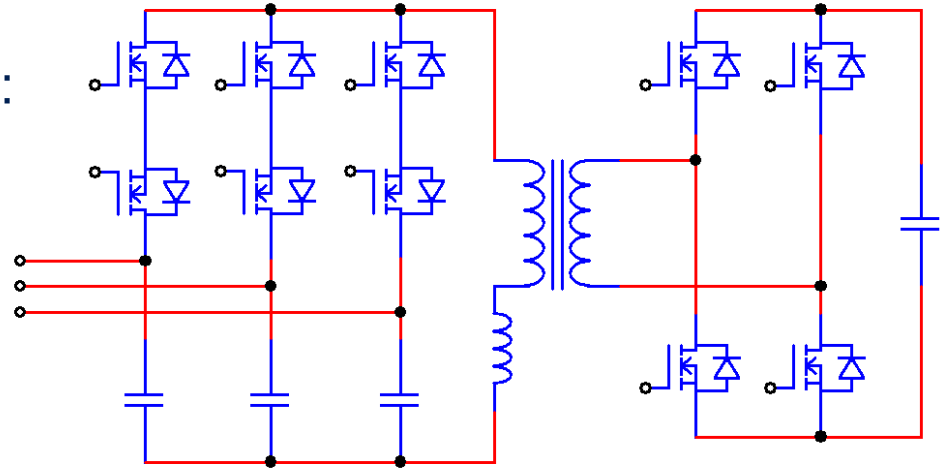
Digital Control 2.0 for SMPS Applications

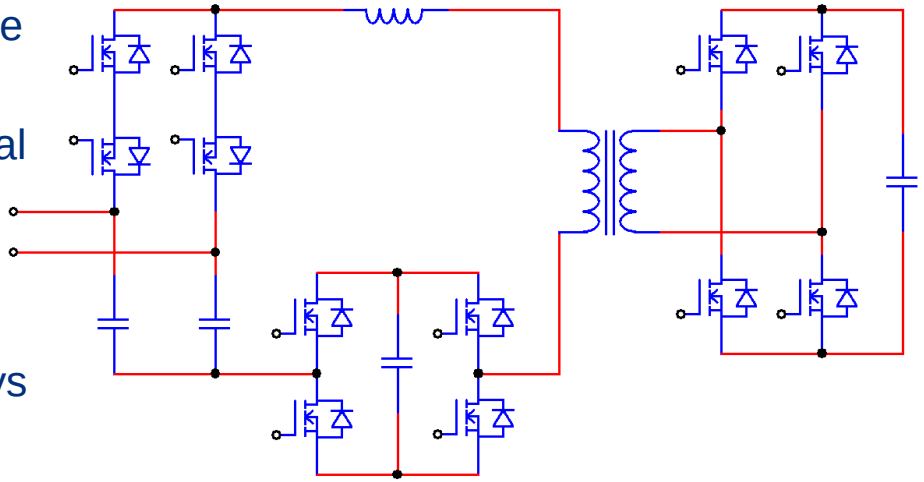
- Adopt parallel control architecture implemented in (digital) hardware:
  - A hardware accelerator using parallel hardware to perform a specific function considerable faster than sequential software:
    - e.g. Consider the video speed performance advantage of a GPU compared to a CPU
  - Effectively eliminate all control latency – extreme control bandwidth
  - Hardware accelerator should ideally have flexibility for a wide range of power conversion applications and different resonant topologies
- Implement real time full system circuit simulations:
  - Enabling sophisticated predictive control – delay/latency compensation
  - Signal synthesis:
    - Minimize the number of high bandwidth signal measurement
    - Create accurate input and output current measurements from the resonant current signal
    - Ensure all control input signals are accurately time aligned
  - Real time optimization:
    - Eliminate unnecessary ‘circulating’ currents
    - Eliminate body diode conduction from excessive ZVS current
    - Continuous self calibration
    - Highest conversion efficiency possible

Advanced Power Converter Topologies

- Cycloconverter based Topologies:
  - Resonant ZVS PFC
  - Single stage isolated PFC



- Triple Active Bridge series resonant:
  - Single stage isolated PFC with line cycle energy buffer
  - Functionally equivalent to a conventional dual stage ‘off-line’ SMPS
  - Single resonant tank serves all power conversion functions
  - Eliminate need for in-rush start-up relays



Questions?

Abstract

IEEE PELS Long Island Power Electronics Symposium

Thursday 9th November 2017 – 12:00pm to 8:00pm

Over the past decade the power electronics industry has experienced a fundamental shift from the use of analog control to digital based control. This change has been fueled by the impact of Moore's Law that has driven down the cost of implementing digital control and by the ever-increasing market demand for higher power conversion efficiency.

Digital based control enables the adoption of more sophisticated control strategies along with the control of more complex power conversion topologies such as 'Bridge-less' PFC, LLC series-resonant, and synchronous rectification, all of which support higher power conversion efficiency.

Power electronics engineers have embraced these changes and gained familiarity with both digital control and the application towards controlling more complex higher efficiency power converter topologies.

The power electronics industry is now approaching a point in time where the impact of Moore's Law is driving the cost of digital controllers towards a packaging cost asymptote and the incremental cost of adopting increased control complexity has effectively been driven to a zero-cost point.

This presentation explores the possible future for digital based control of power electronics by considering improvements in power conversion efficiency that can be afforded by adopting the next generation of increased complexity digital control architectures.

Format: – 45 minute presentation followed by 15 minutes of questions

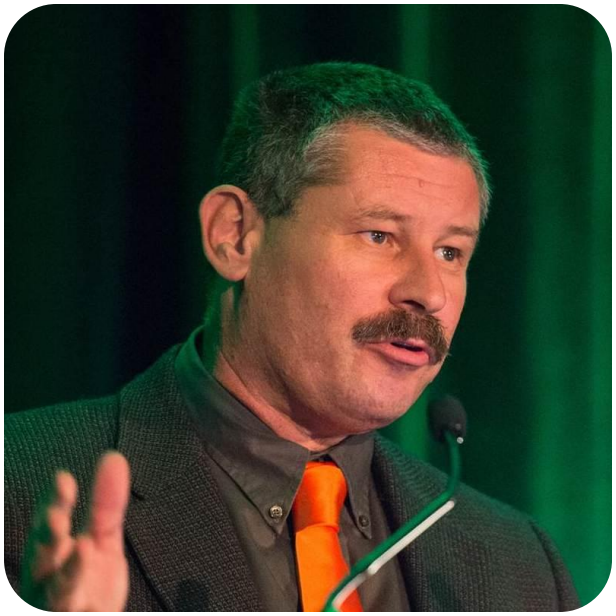
Biography – Michael Harrison

Michael Harrison received the NZCE degree from AUT University, New Zealand in 1988 and the BE degree from the University of Auckland, New Zealand in 1991. He is currently employed by ST Microelectronics in the capacity of Senior Applications Manager with a focus on Power Electronics Applications.

He holds over 30 international patents related to switched mode power conversion techniques. In previous employment, he has been involved in the research and development of Photo-Voltaic microinverters, telecommunications power conversion rectifiers, data center power systems, grid-tied inverters for distributed generation applications, and single-stage single-phase power-factor corrected converters.

Current areas of research interest include:

- Advanced resonant conversion digital control architecture design
- Investigation into ferroelectric behavior exhibited in advanced Super-Junction MOSFET structures
- High frequency power converter applications for bi-directional merged-drain GaN eHEMT JFET
- Application of SiC MOSFETs in high frequency series-resonant cycloconverter power converters



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