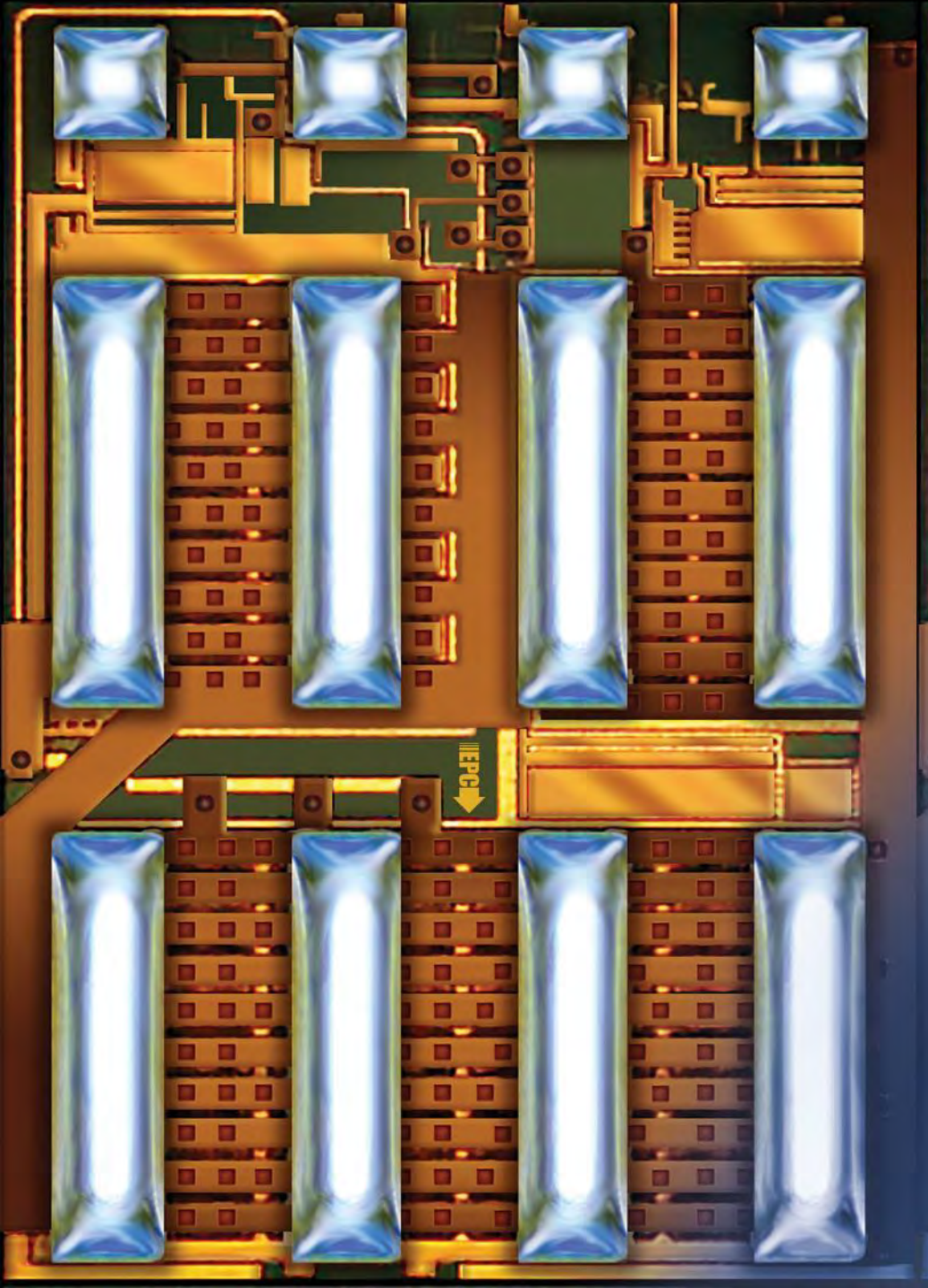


Do GaN FETs have Internal Diodes?

Brian Miller *Nov. 2023*
brian.miller@epc-co.com

EFFICIENT POWER CONVERSION

Agenda – Diodes in GaN Devices?

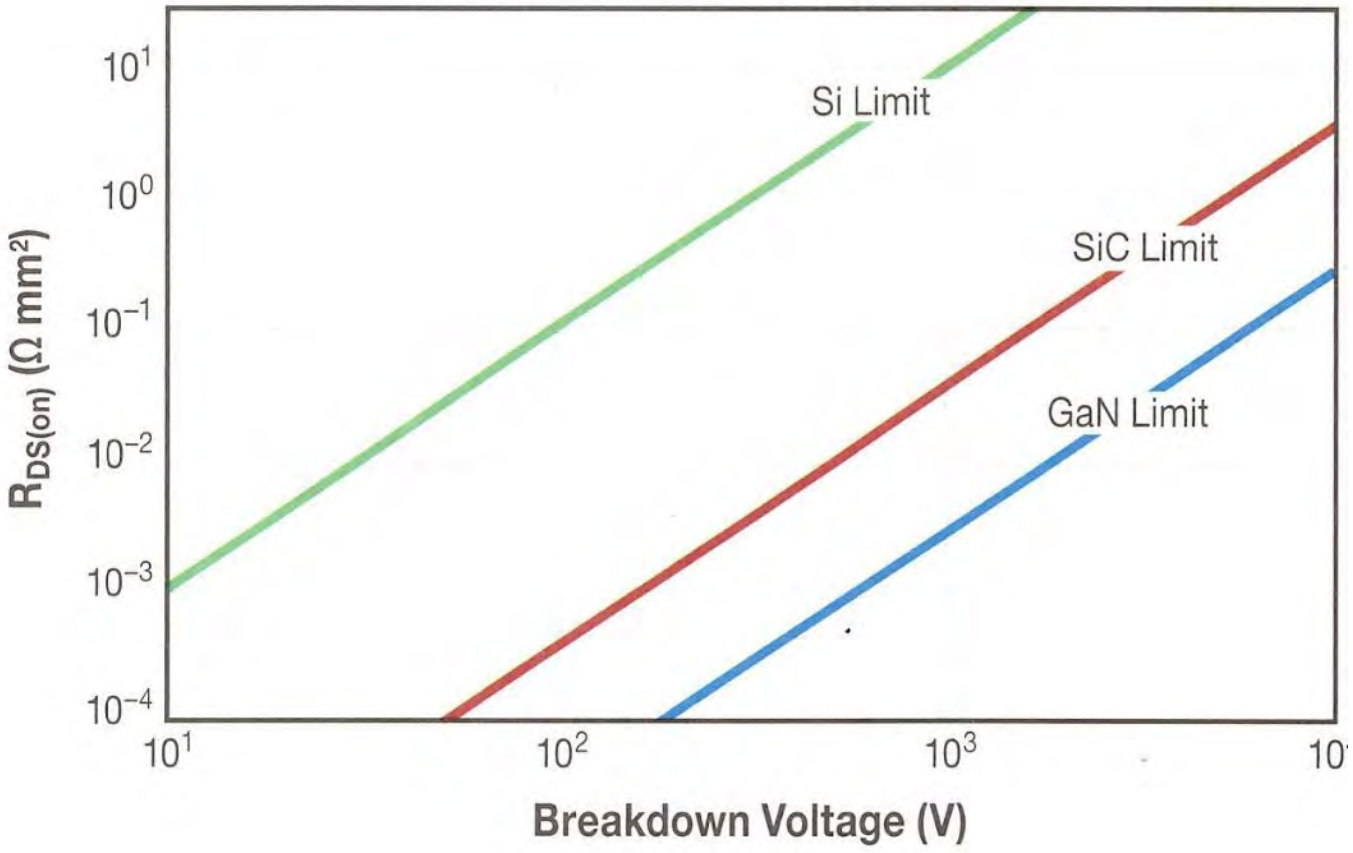
- Motivation: Why use GaN power devices?
- Do GaN FETs have a “diode”?
- GaN Reverse Conduction (“diode”) Advantages & Disadvantages
- Optimizing Design
- A Look Forward: GaN Advances

This talk is approved for CEU/PDH credit. Web link to apply for it:
www.ieee.li/forms/2871

Motivation for Wide Band Gap Devices

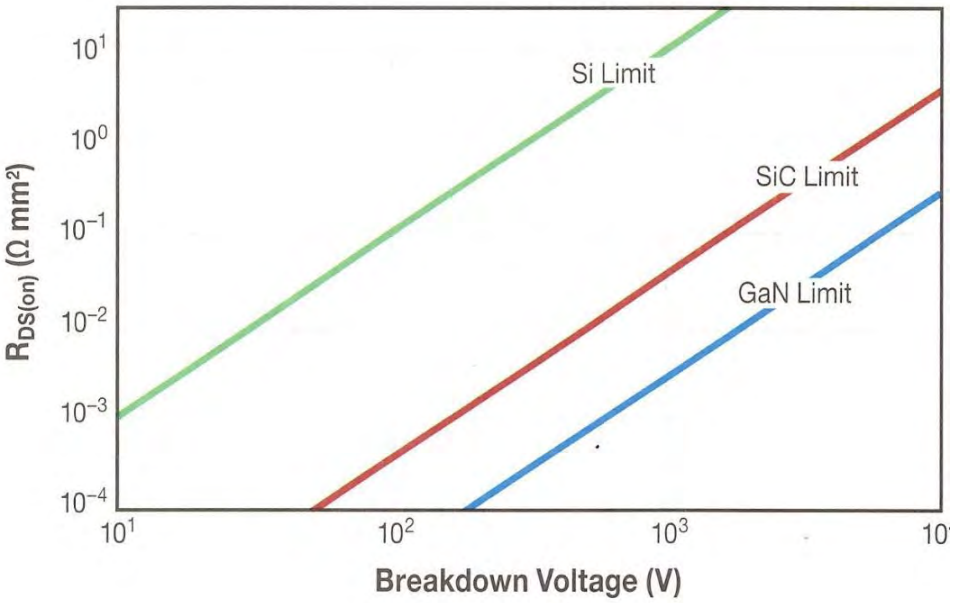
The potential of wide band gap

- SiC and GaN: theoretical much smaller size for a given Rds(on)
- Can this potential be realized?
  - Silicon MOSFETs **have** reached their potential. Real-world devices match the green line
  - What about GaN FETs? What advancement is seen?



Why use GaN FETs?

- From the previous graph:
  - Lower On Resistance
  - Smaller
- Faster – lower switching loss
- Lower System Cost – higher freq. → smaller L, C
- Reliability

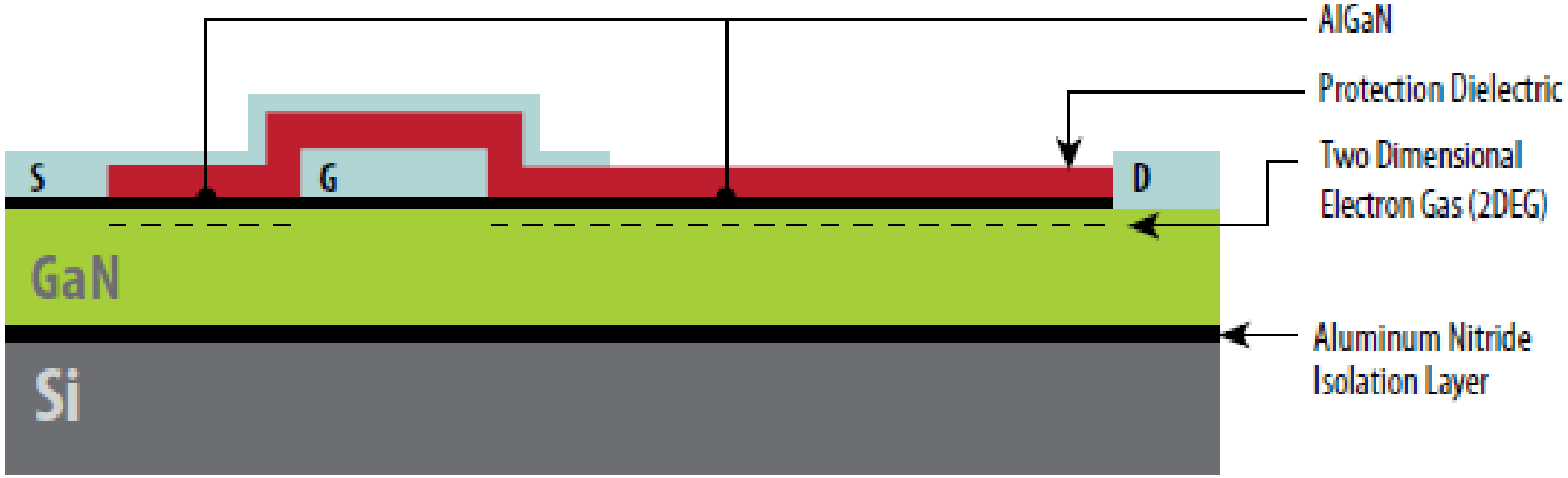


GaN FET Structure – Is there a Diode?

A Review – GaN Structure

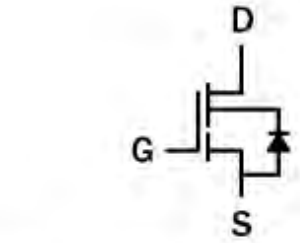
- Low voltage GaN are typically lateral devices
- MOSFETs have parasitic p-n diodes in their structure
- GaN FETs do not have this p-n parasitic diode element

- So… no diode in GaN?
- Not exactly…

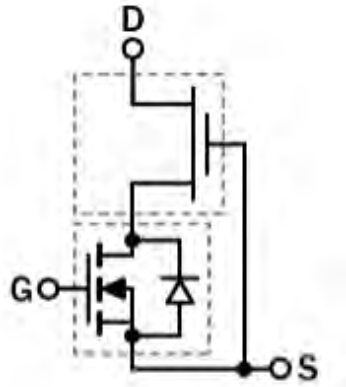


Various GaN FET Symbols

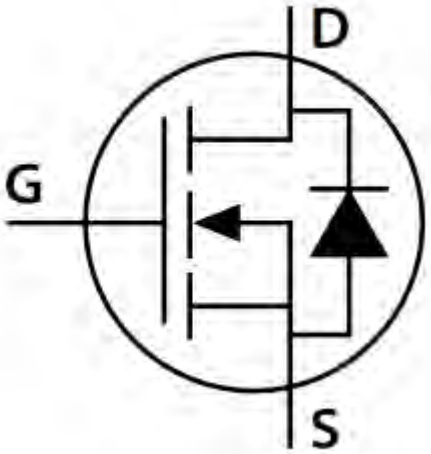
- Schematic symbol varies among GaN FET manufacturers
- EPC shows a diode
- GaN Systems doesn't show a diode
- Navitas Semi. doesn't show a diode
- Transphorm, Innoscience, TI, etc.

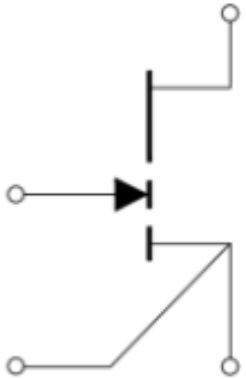


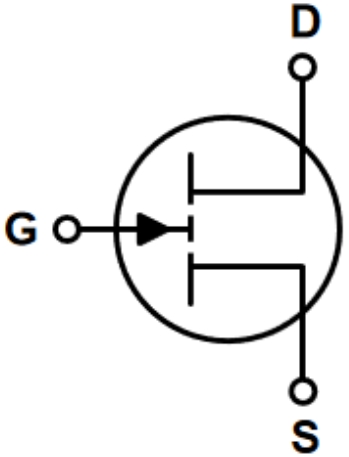
Cascode Schematic Symbol

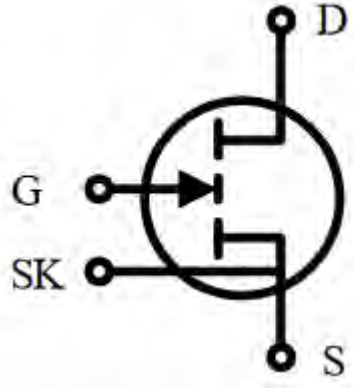


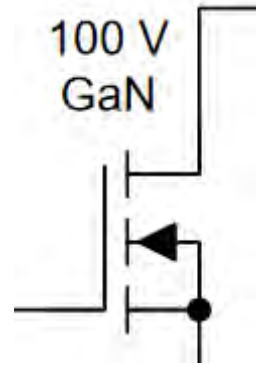
Cascode Device Structure





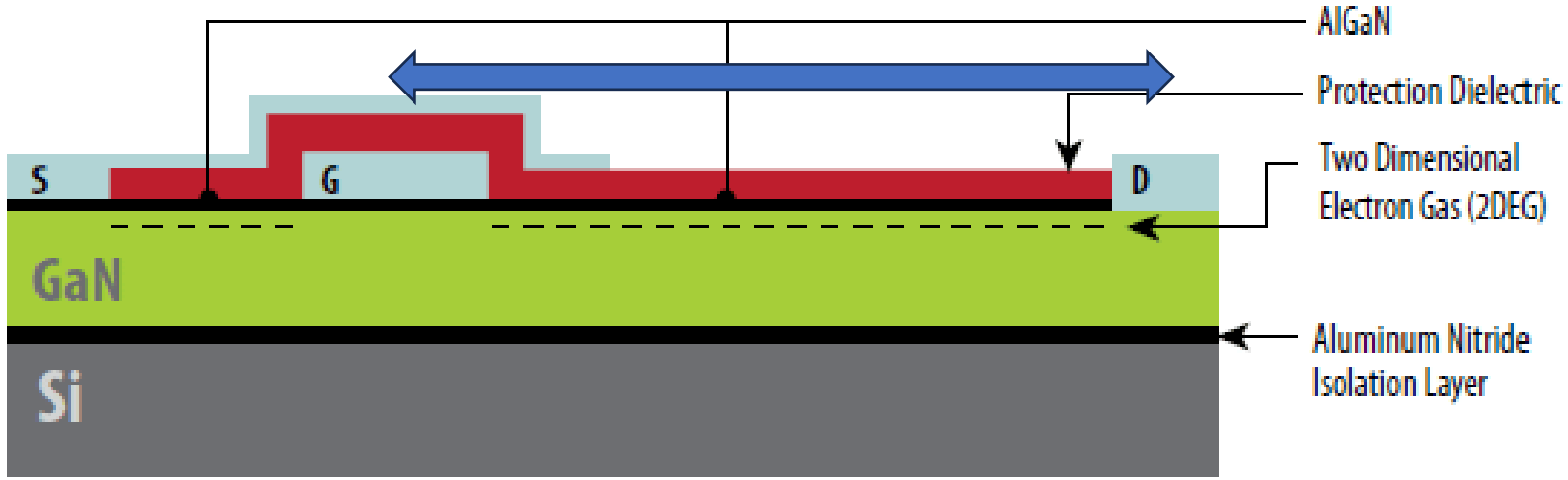






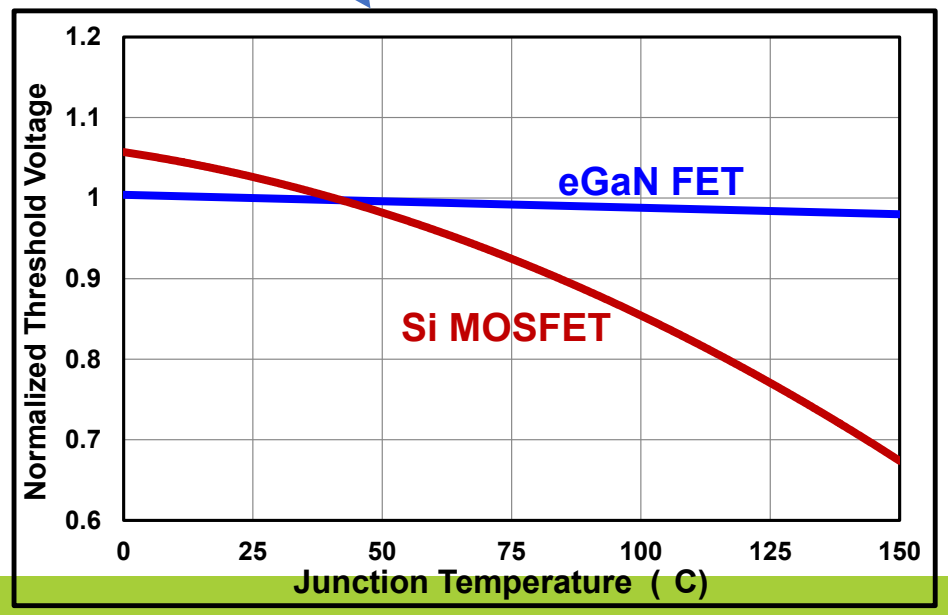
Another way to turn on GaN

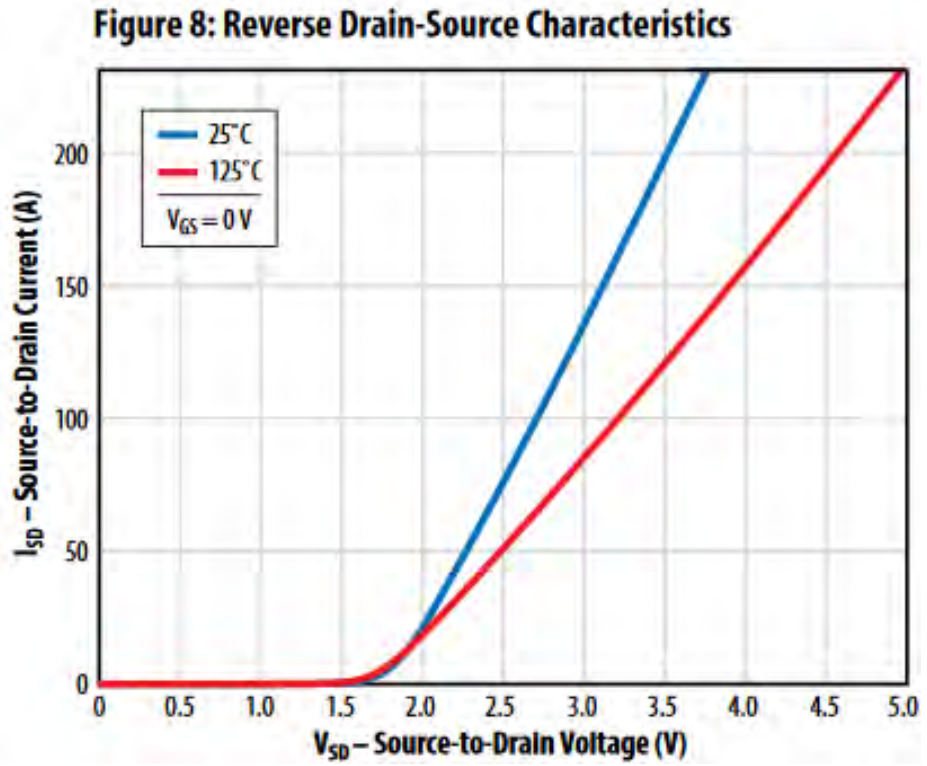
- The “regular” way of turning on: Voltage from Gate to Source
  - Vgs = 5-6 V
- Alternate way: voltage from Gate to Drain, Vgd
  - Still must respect Vgs limits (varies by GaN FET manufacturer)
  - Assume Vgs = 0V
  - Drain goes negative
- Diode behavior!



GaN Characteristics

- No Reverse Recovery (Qrr)
  - No parasitic p-n diode
- Reverse “diode” conduction
- Vth (gate threshold): very small temperature variation

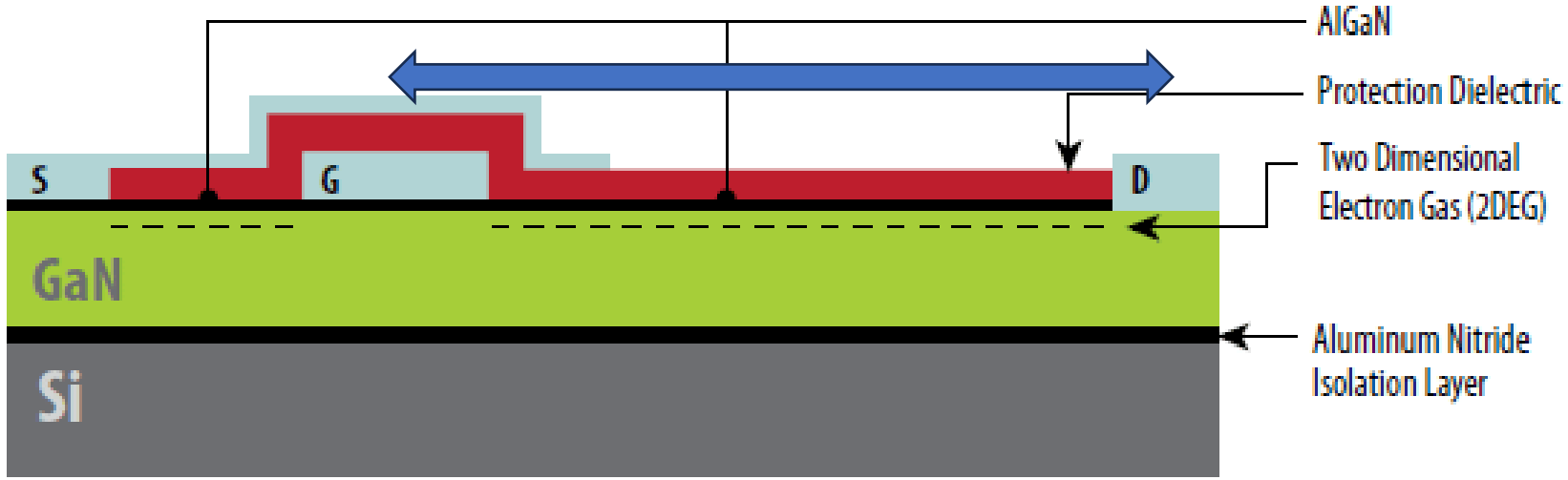




“diode” voltage vs. Vgs

- The GaN “diode” voltage is a function of:
  - Threshold voltage… varies within a range
  - Vgs

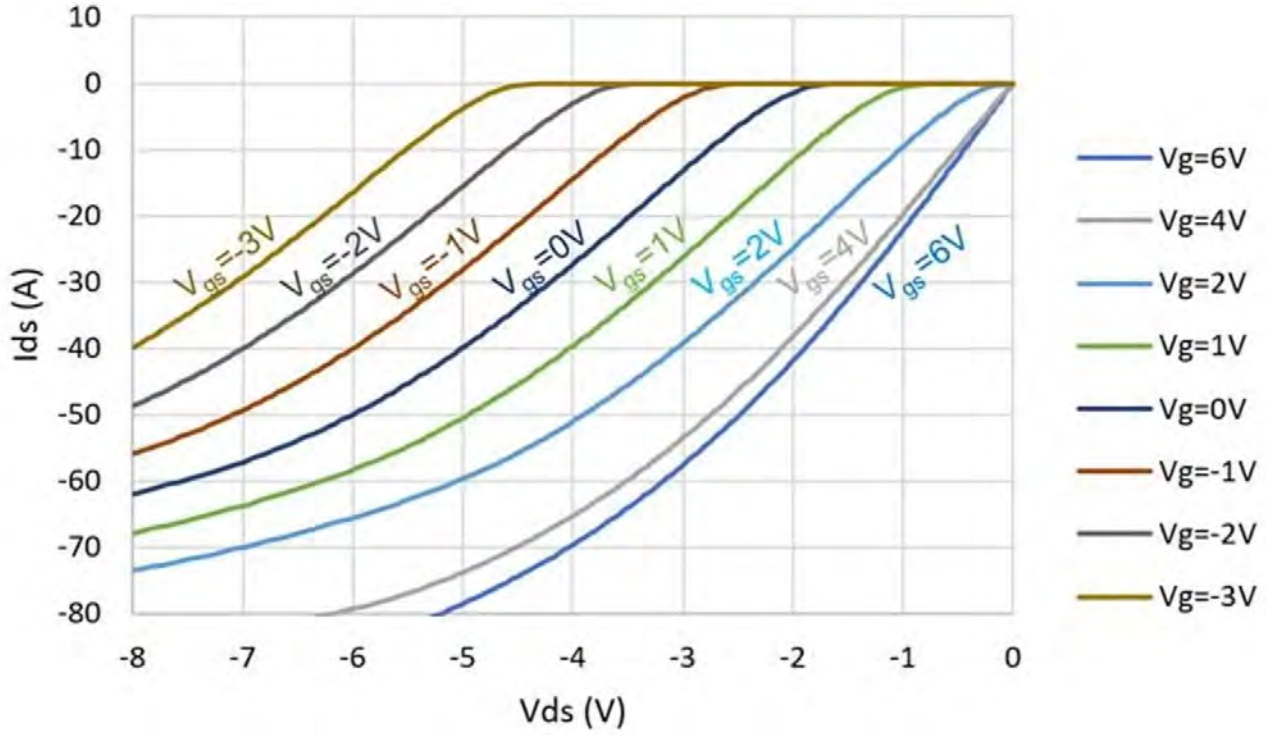
- Approximate, typical equation:
  - For EPC GaN FETs
  - Vsd = 2.5 V – Vgs



Graph

- Example graph:

- If Vgs is negative
  - Reverse conduction voltage drop increases with negative Vgs
  - So, a GaN FET can be used as bi-directional block
    - for 3.3 V power supply:
    - Vgs = -3 V: blocks 3.3 V
    - Vgs = 5 V: on
    - Not commonly done…



Graph from GaN Systems:
https://gansystems.com/wp-content/uploads/2018/02/gan-enhancement-mode-1500x861.jpg

GaN “Diode”: Advantages & Disadvantages

GaN Diode vs. MOSFET's diode

- GaN "diode" Advantages
  - Zero Reverse Recovery (no Qrr)
  - Very Fast
  - Current Rating high
    - Uses main channel

- GaN "diode" Disadvantages
  - High voltage drop
    - Thus, potential thermal concerns for long conduction times

GaN “Diode” vs. MOSFET’s diode

- Qrr (MOSFET) vs. GaN “diode’ drop: which is worse?
  - EPC did a paper
  - Built boards and tested

  - MOSFETs: **red** & **black**
  - GaN FET: **blue**

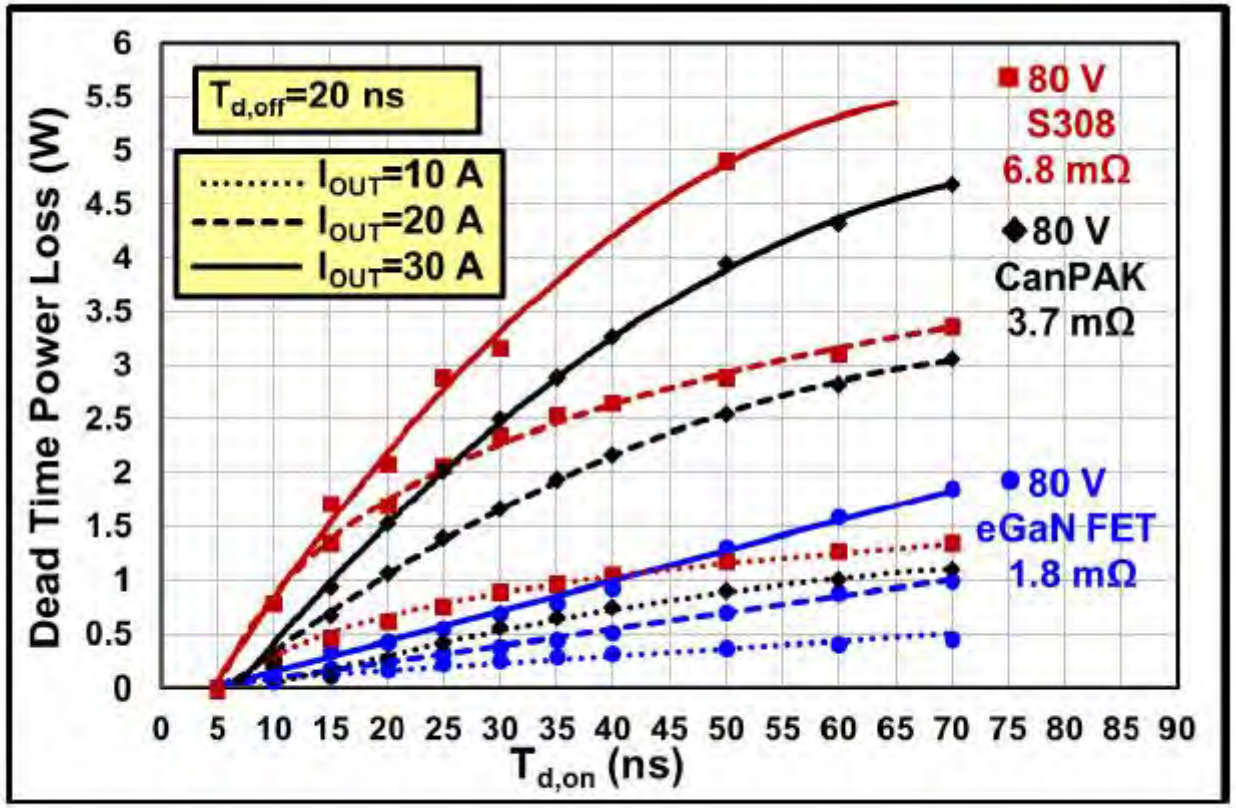


Fig. 11. Effect of $t_{d,on}$ on losses of test converters of Fig. 10.

Optimizing Design

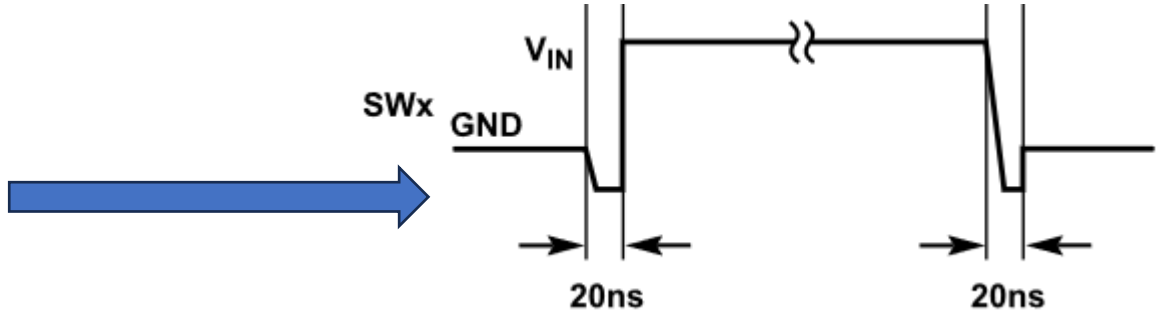
Optimizing a GaN Design for Diode

Can we overcome “diode” high voltage drop?

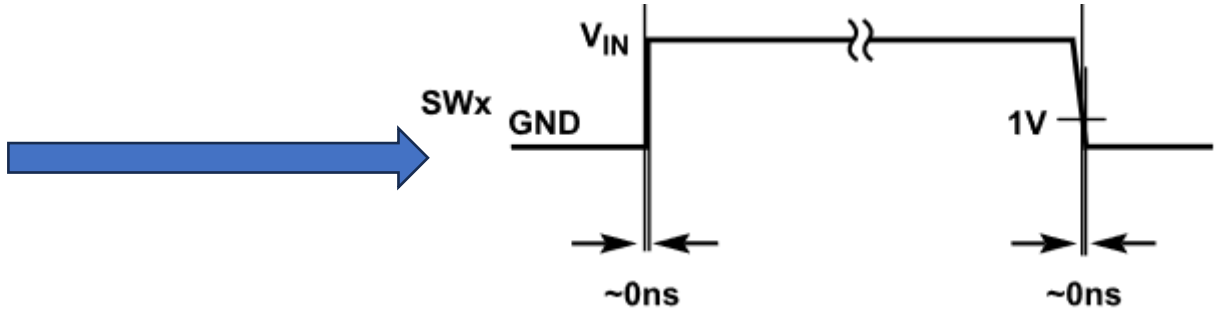
- Reduce “diode” voltage? How about a Vgs bias?
  - No, due to Vth variation. Risk of conduction
  - Maybe there is a way??
- Short dead time
  - Minimizes loss in diode
  - Loss proportional to dead time
  - Virtual zero dead time
- Parallel Diode?
  - Trade-off: capacitance of added Schottky
  - Benefit at low frequencies

Optimizing a GaN Design for Diode

- Short dead time
  - Minimizes loss in diode
    - Loss proportional to dead time
  - Examples: Renesas' ISL81806 (buck) & ISL81807 (boost) controllers
    - 15-20 ns dead time

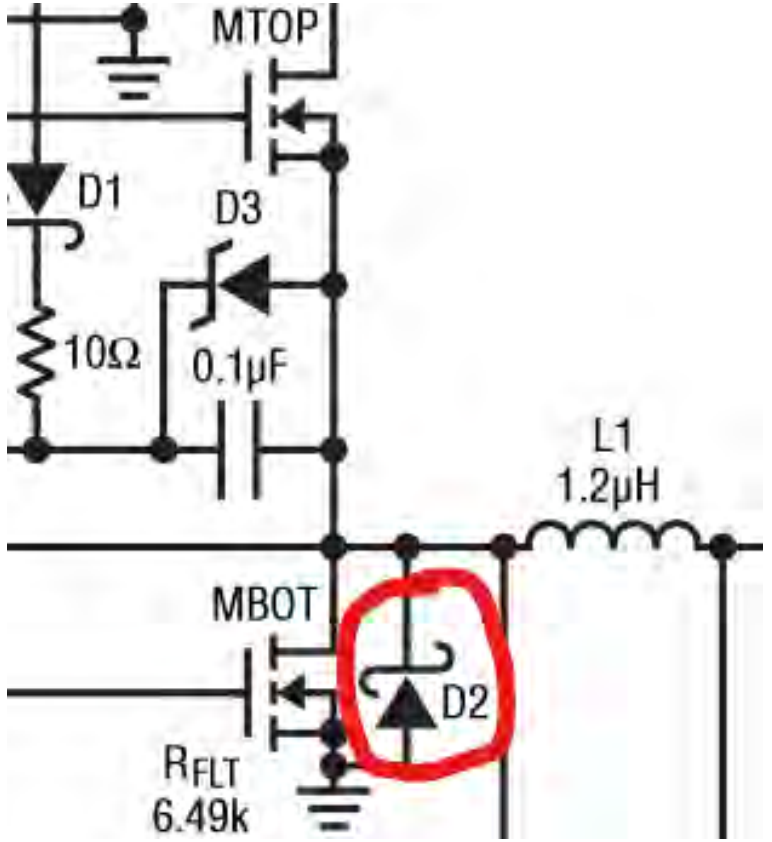


- Near-Zero Dead time
  - Example: Analog Devices' LTC7890 (buck)
    - Made-for-GaN
    - "smart near zero dead times"



Optimizing a GaN Design for Diode

- Parallel Diode?
  - Trade-off: capacitance of added Schottky
  - Still no reverse recovery
  - But: some controllers need this
- Example: LT8390A
  - 4-FET buck/boost
  - Works well with GaN FETs, IF switch node not too negative
  - Schottky D2 added



From Analog Devices' LTC7800 data sheet

A Look Forward

an update from last year…

A look at future GaN advancements

GaN future advancements coming:

- Generational Improvement
  - 2021: GaN FETs are 300x away from theoretical performance limit
  - 2023: Approaching a 2x improvement vs. 2021
  - This leaves 150x for future years
- GaN power ICs
  - Now: Power FETs + gate drivers
  - Future: other functions, higher voltage, etc.
  - Leading to wider adaption

  - Other Advances: NexGen, GaNPower, GaN Systems, etc.

A look at future GaN advancements

- Other advancements…
  - Made-for-GaN controllers and drivers
    - DC-DC, Motor drivers, synchronous rectification, etc.
  - New packaging
  - Automotive-approved GaN FETs and GaN ICs
    - To standard AEC-Q101 and –Q100
  - Radiation Hardened GaN FETs & GaN ICs

  - Analog LTC789x family
  - Rad-Hard
  - bi-directional blocking, thermal

GaN Compatible Gate Drivers

Single Drivers

- LMG1020 & -25[a] : ultra fast
- UCC27611 – with LDO
- LM5114
- 1EDB7275F* – isolated

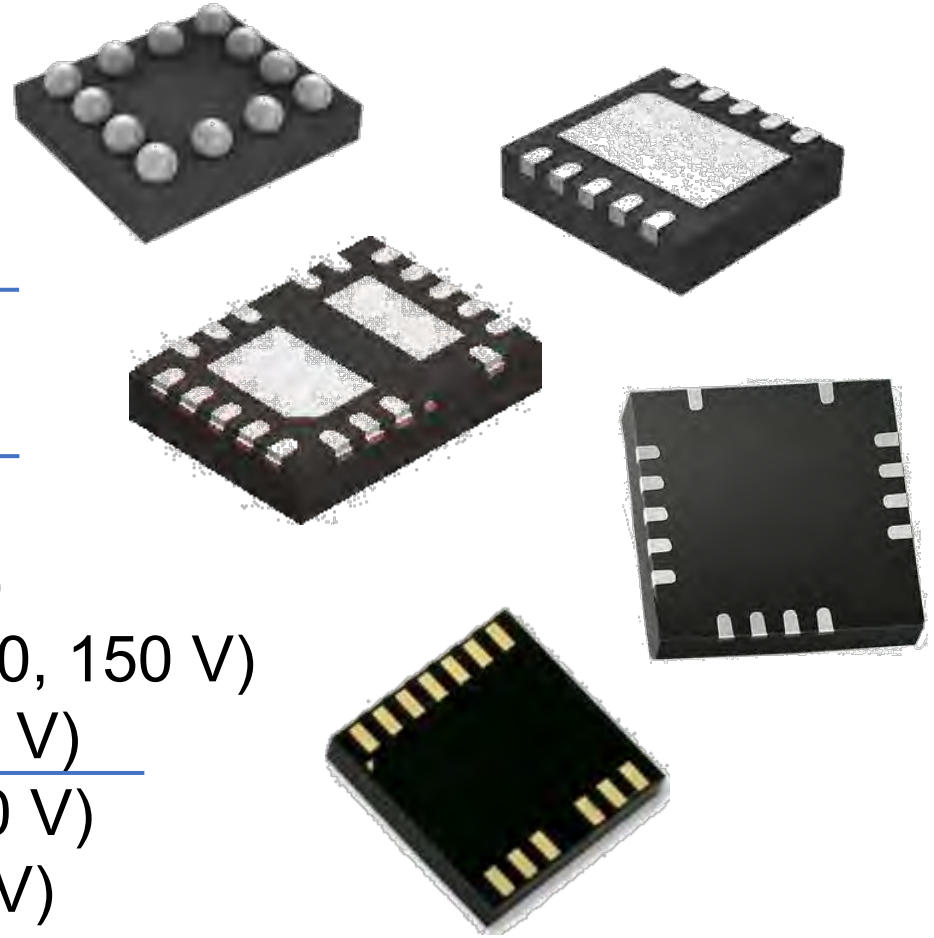
Half Bridge Drivers

- uP1966E‡ (80 V)
- LMG1205‡ (90 V)
- MP8699B ‡ (100 V)

- LM5113-Q1[a] (100 V)
- MPQ1918[a] (100 V)

- LMG1210 (200 V)
- 1EDN71x6U (200 V)
- NCP51820 & -10 (650, 150 V)
- STDRIVEG600 (600 V)

- Si827xGB1-IM*[a] (650 V)
- ADuM4221A* (>600 V)
- 2EDB7259Y* (>600 V)



*isolated ‡ Footprint compatible

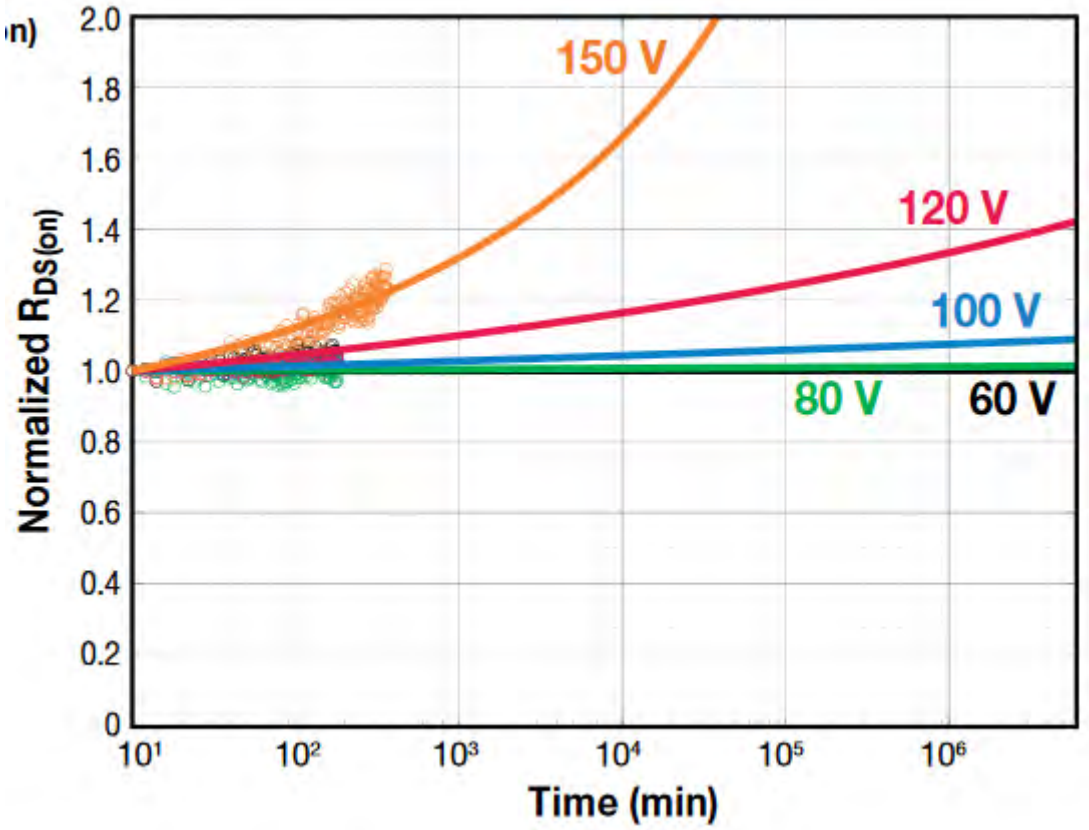
[a] automotive

Additional Gate drivers in development

A look at GaN advancements

Reliability Advances → data sheet specifications

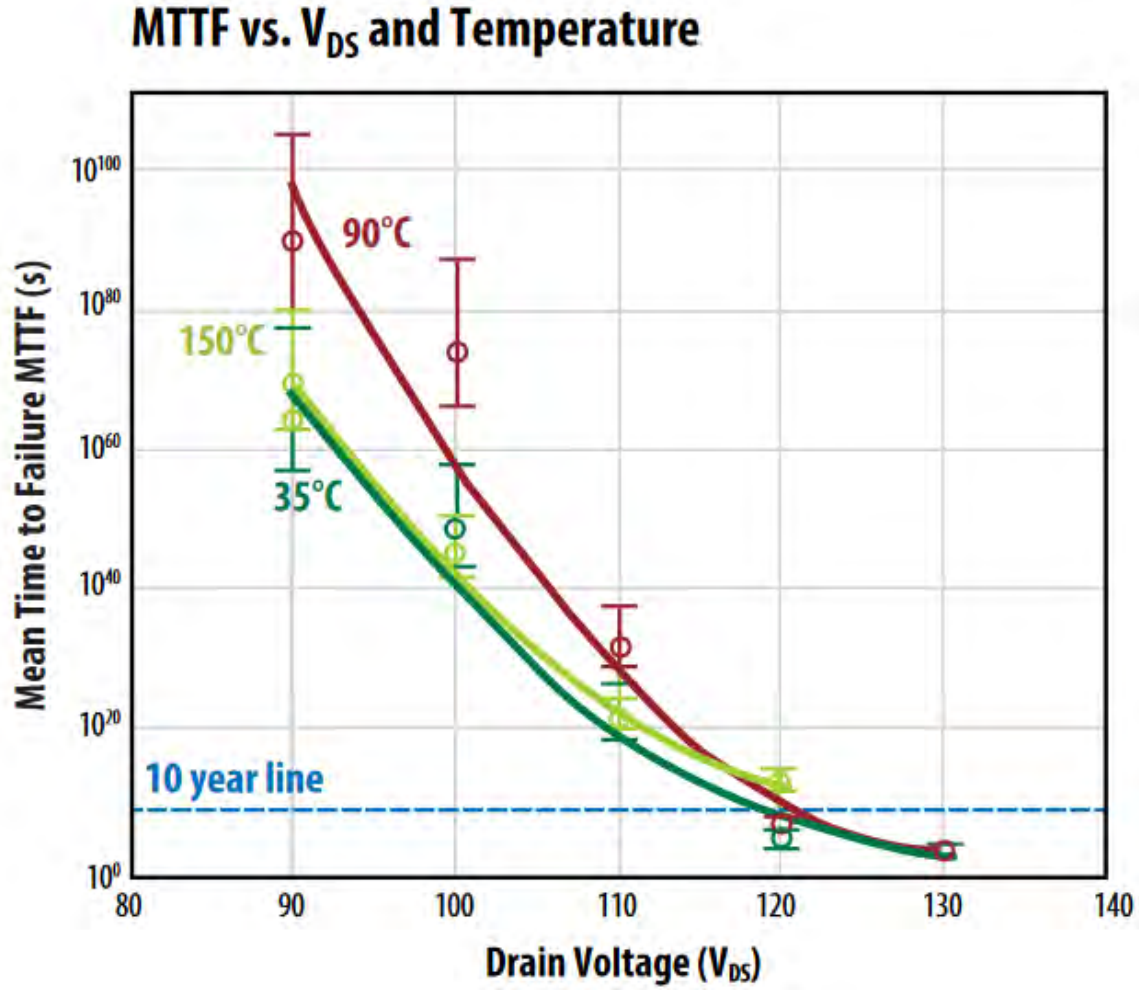
- GaN FETs: end of life often determined by Rds,on increase
- Main factor is Vds
- What about Vds transients?
- Study → increased transient rating



GaN Reliability: Temperature

Testing a 100 V GaN FET at various temperatures

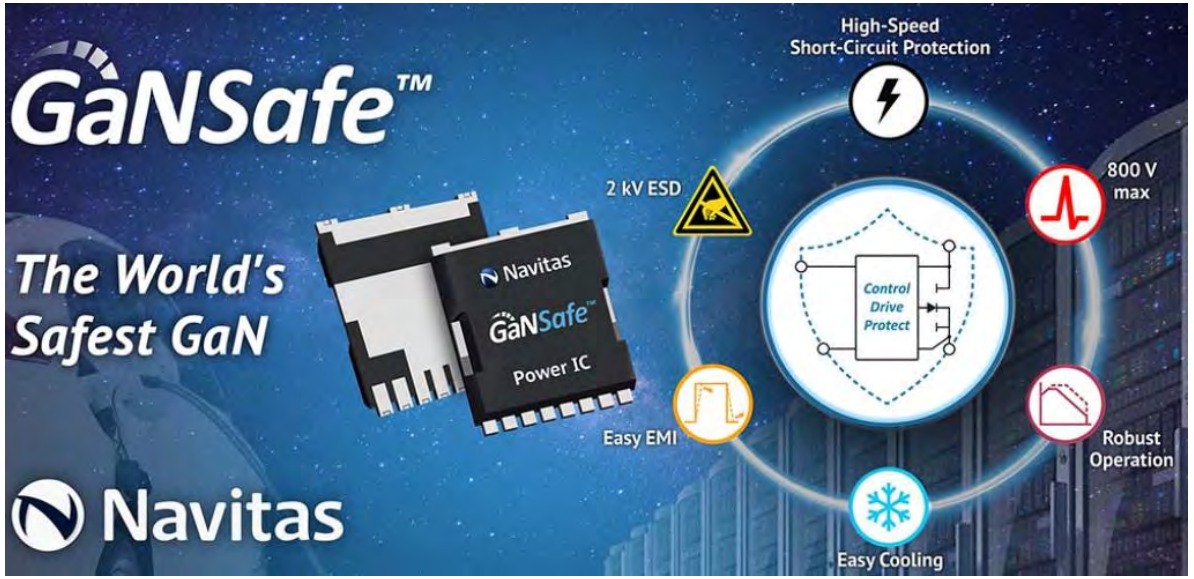
- Temperatures:
  - 35 C (dark green)
  - 90 C (red)
  - 150 C (light green)
- Note the reliability at 90 C > reliability at 35 C & 150 C.
  - For Vds < 100 V.



A look at GaN advancements

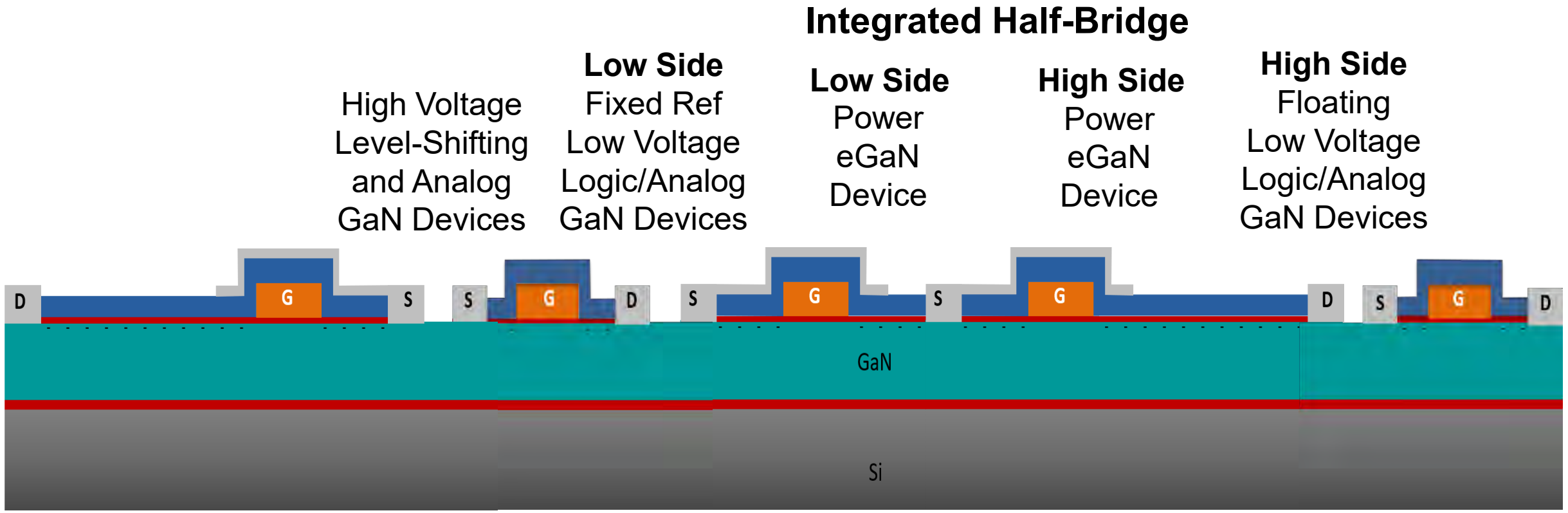
GaN future advancements coming:

- Navitas: protection features
- GaN Systems: next gen
- EPC: GaN ICs



GaN Integration

Lateral FETs allow various voltages and Rds,on FETs on one die:

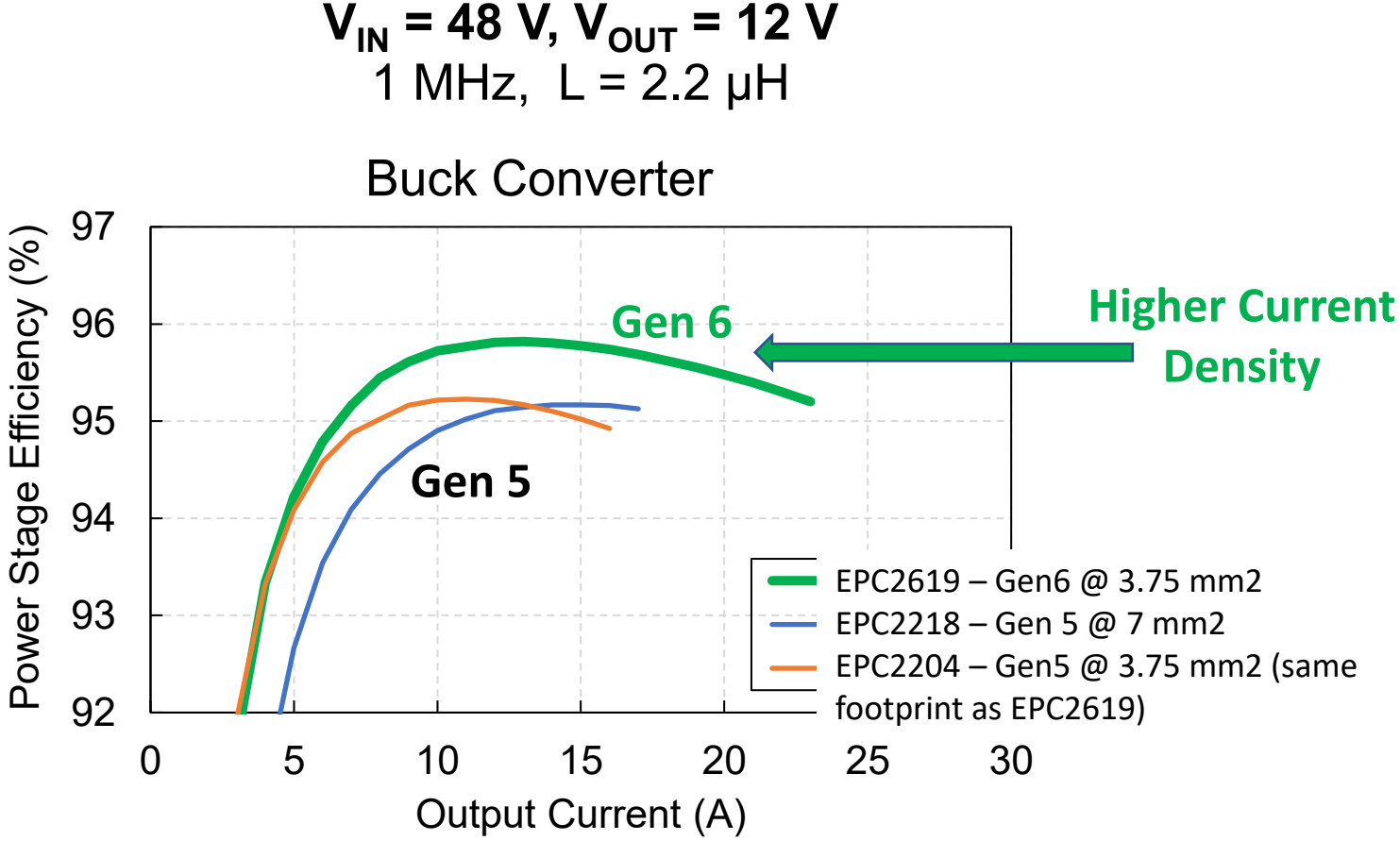


A look at GaN advancements

EPC's Gen 6 vs. Gen 5

- Same Size: orange & green
  - ~ same parasitics
  - Gen 6: 40% lower Rds,on
- Same Rds,on: blue & green
  - Lower parasitics
  - Green: smaller, lower cost

- Optimizes efficiency for a wider range



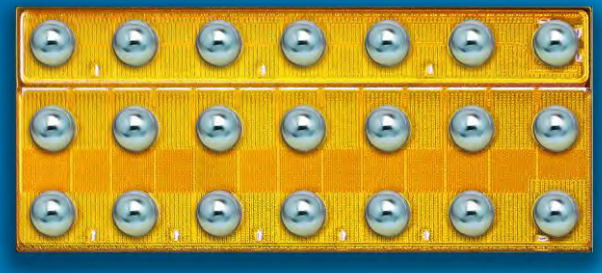
No heatsink, 1000-1500 LFM
Data shown for $T_{Case} \leq 110\ ^{o}C$

EFFICIENT POWER CONVERSION

Click on images to learn more

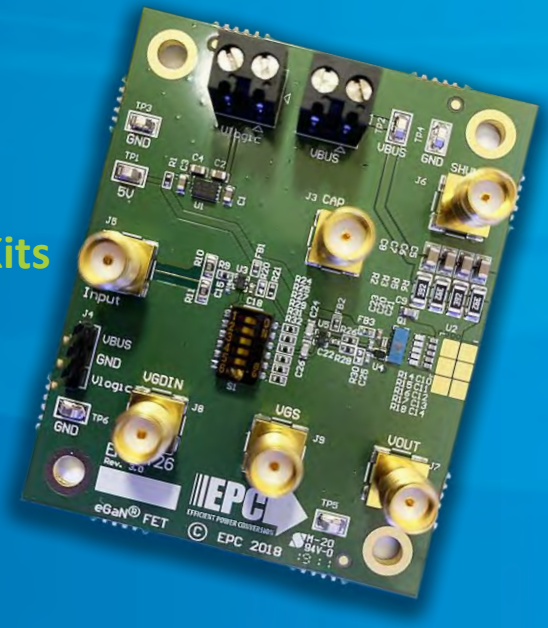
How To GaN Video Series

3rd Edition Textbook



eGaN® FETs and ICs

Evaluation Kits



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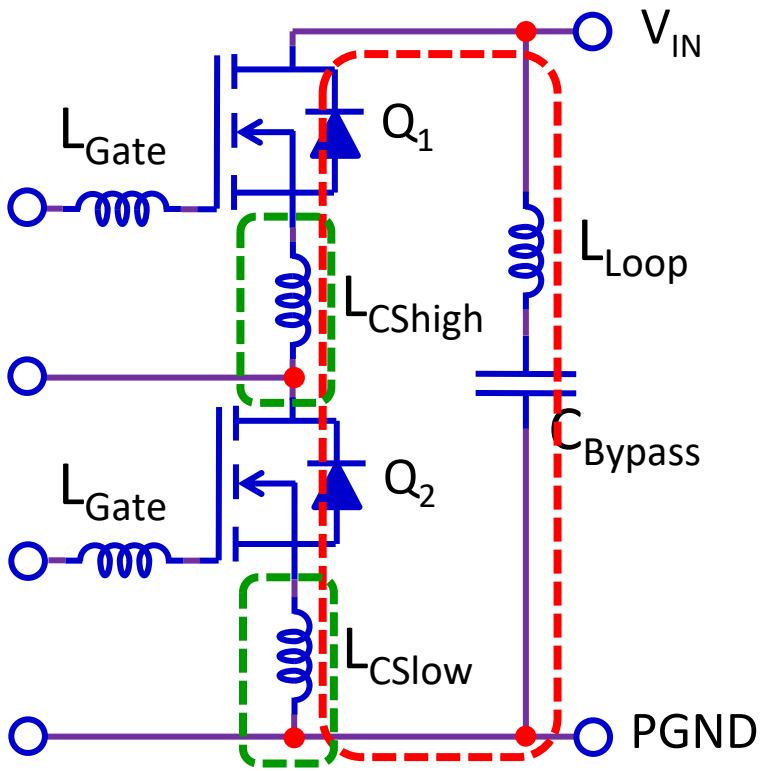
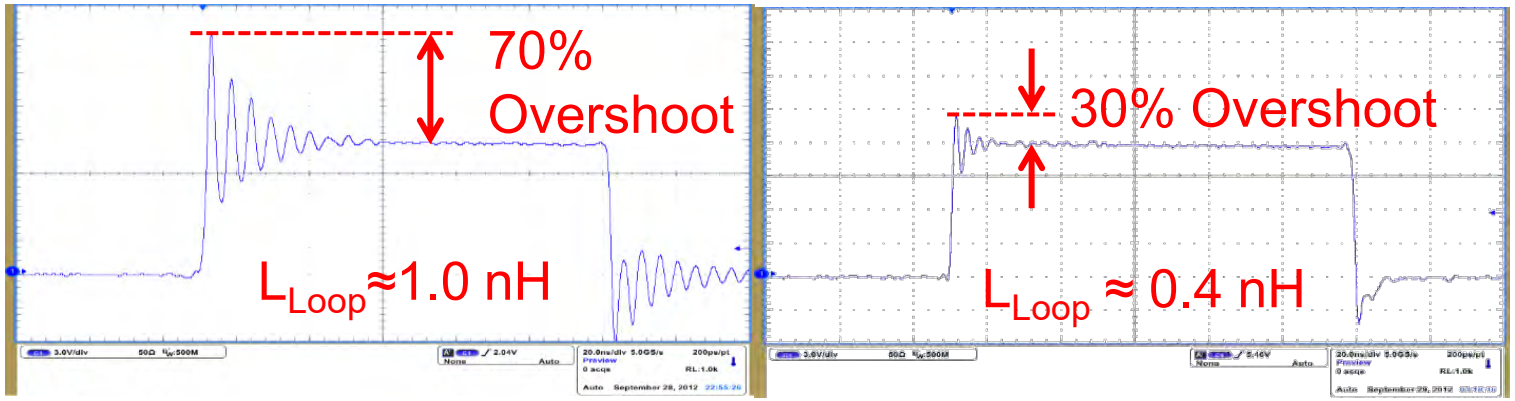
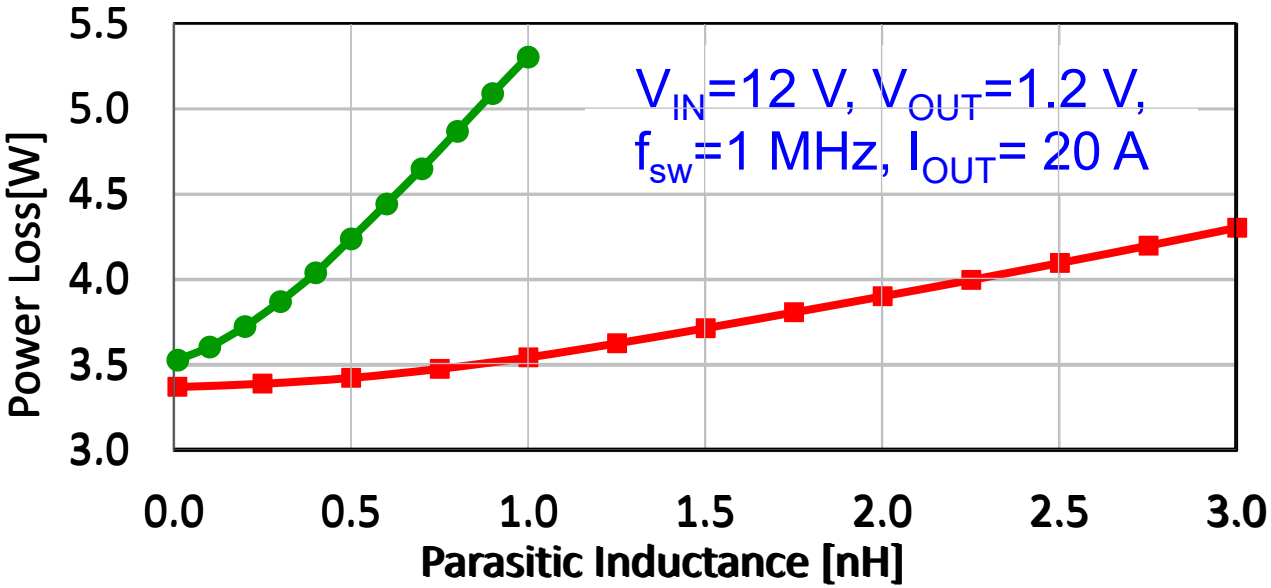
Layout Advances

- GaN FETs are faster than Silicon MOSFETs
- Good layout needed… or layout can limit performance!
  - GaN FETs' speed "forces" focus on layout
- Goal: minimizing inductances.
  - Let's review…

Impact of Power Loop Inductance







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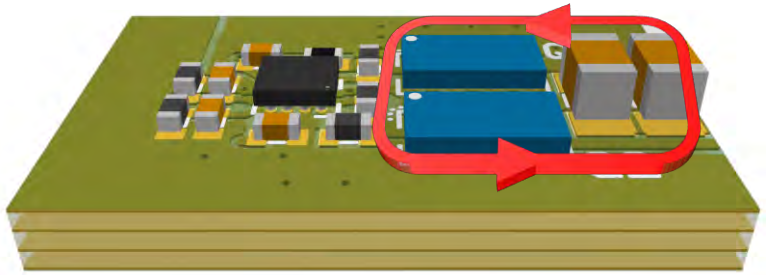
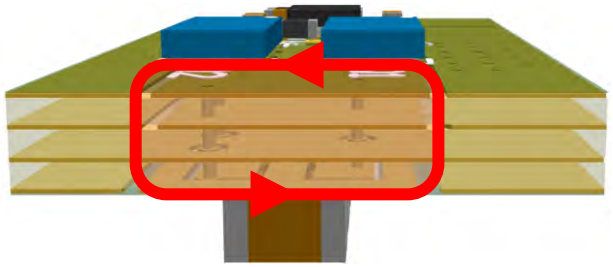
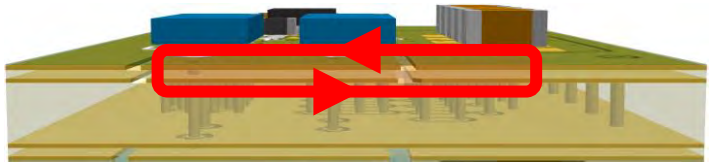
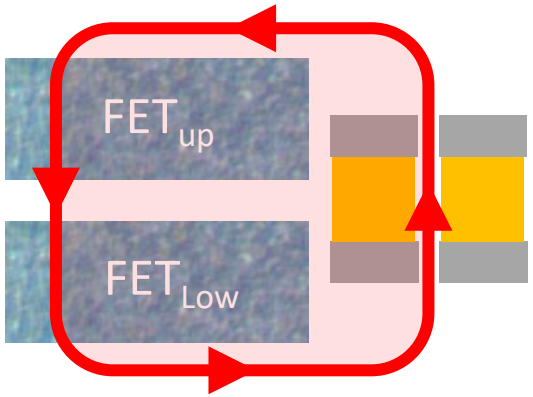
Layout Comparisons



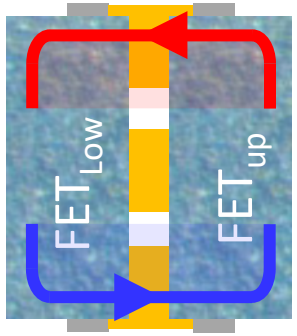






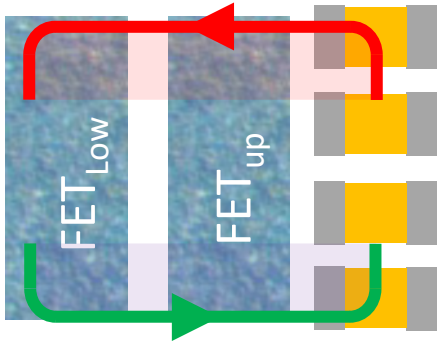
Top Layer

Lateral



Top Layer Bottom Layer

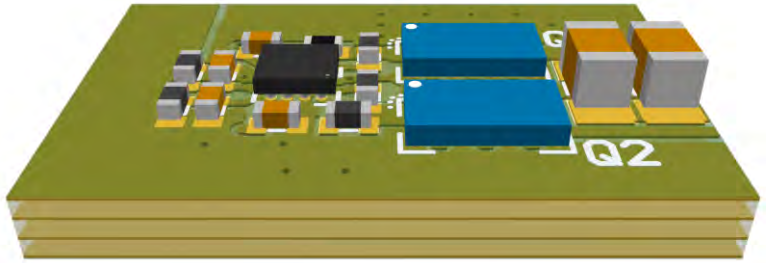
External Vertical



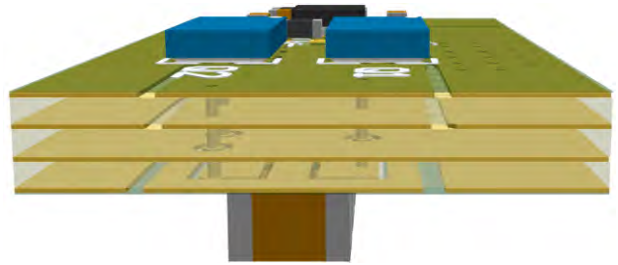
Top Layer Inner Layer 1

Internal Vertical

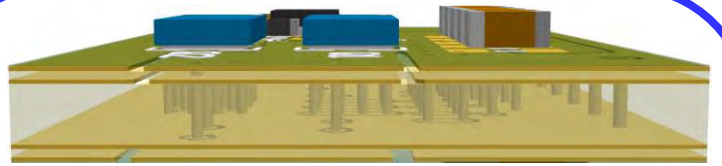
Layout Inductance Comparison



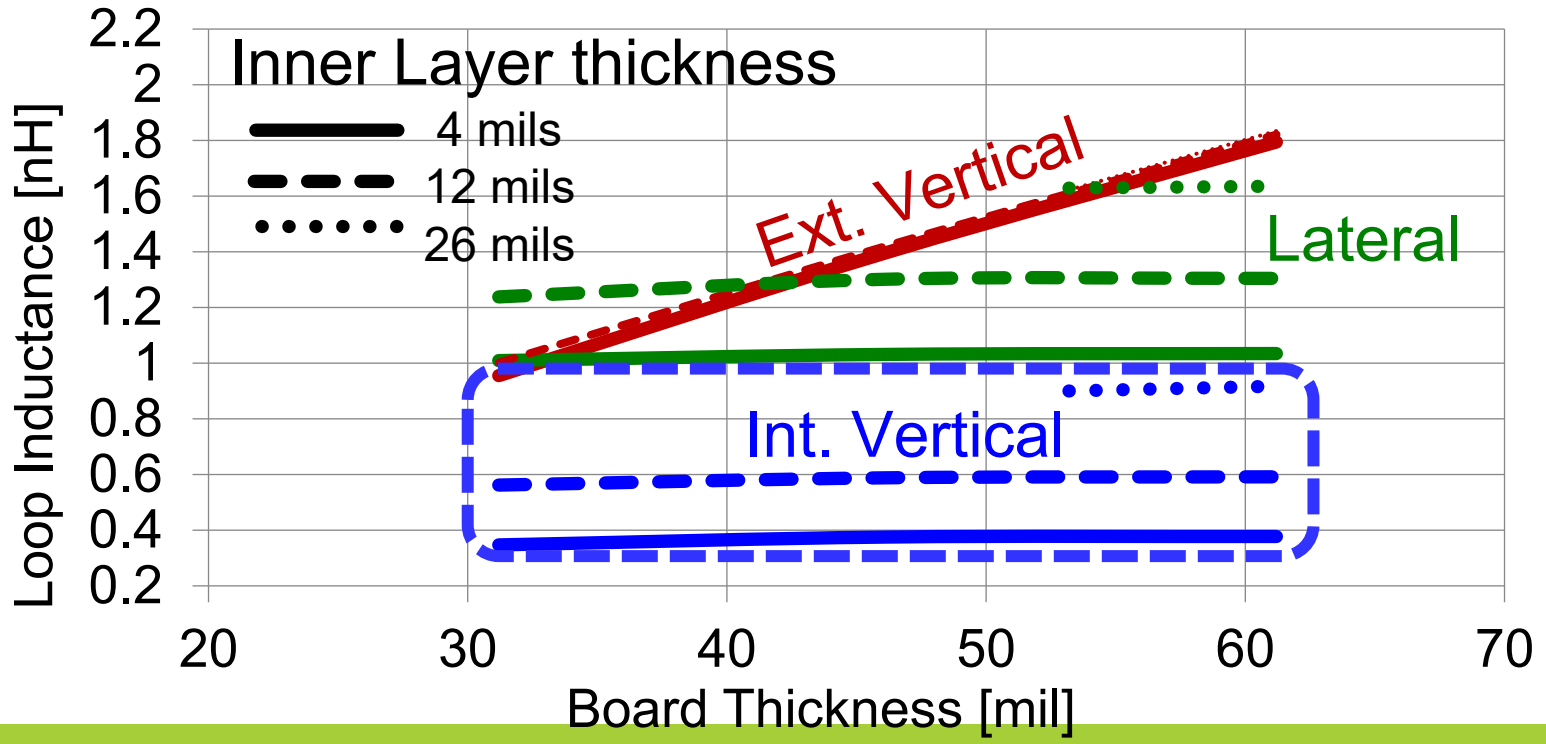
Lateral

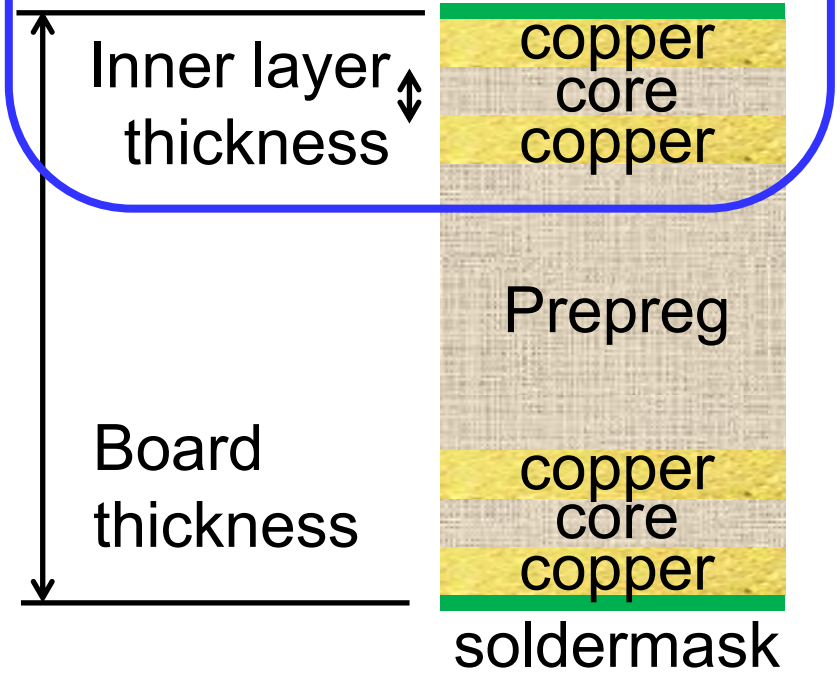


Ext. Vertical



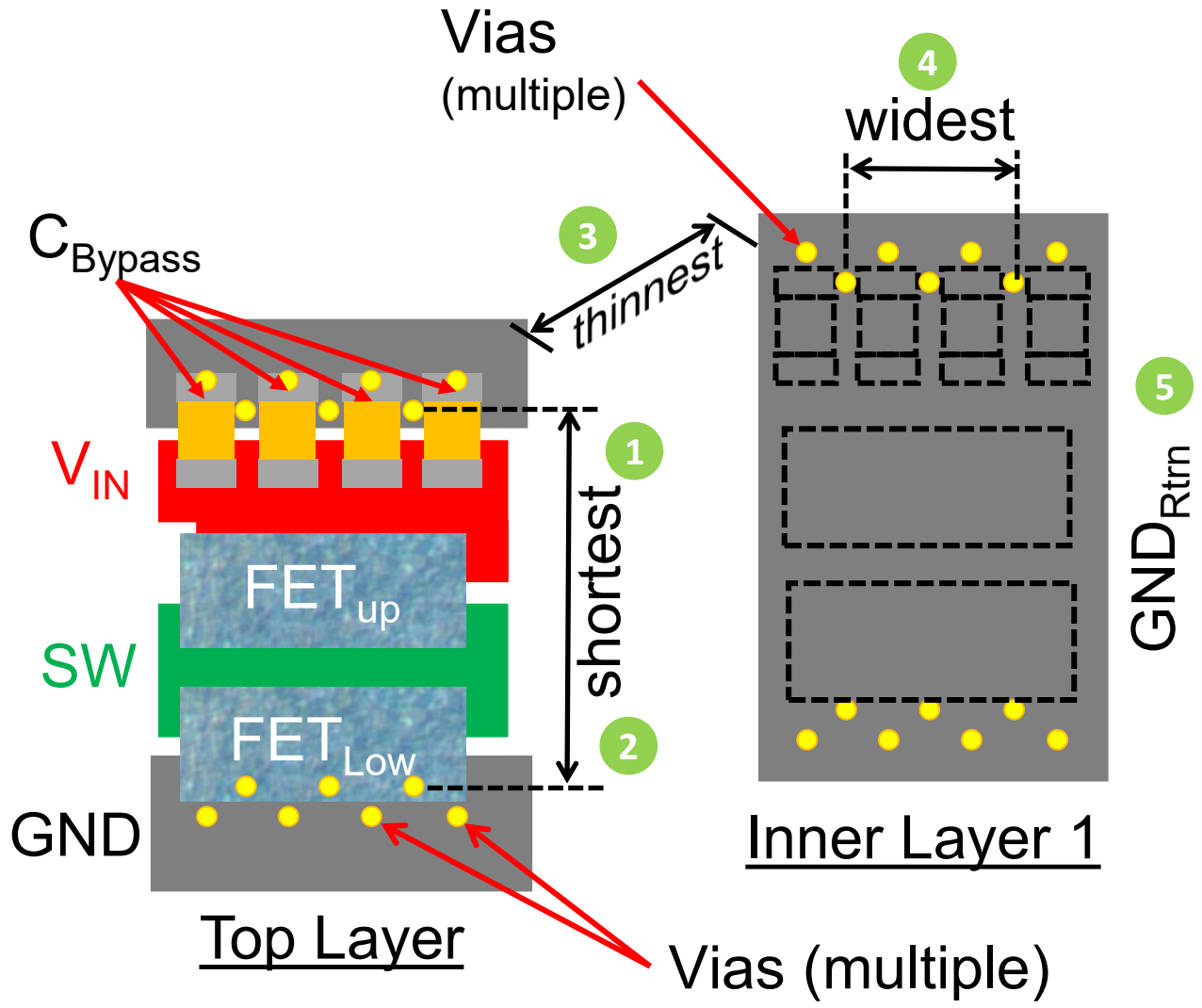
Int. Vertical
Best Choice





Getting to a Low Inductance Layout

1. Components: Vertically close
2. Vias: Close to the innermost electrical connection
3. Substrate: Thinnest permissible thickness between outer and first inner layer
4. Via Connections: Spread out at innermost connect
5. Ground Return: doesn't need to carry full current



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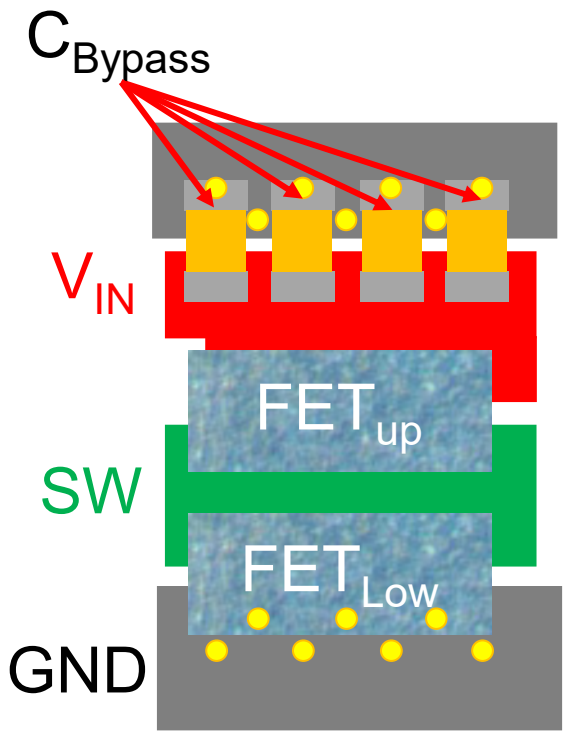
Getting to a Low Inductance Layout

Variations: vertically rotate caps & FETs

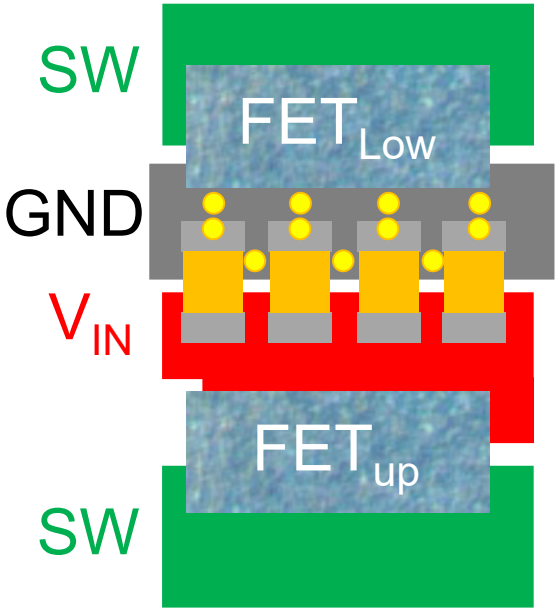
- Original: Caps → top FET → bottom FET
  - Ground on 2nd layer
- Variation 1: top FET → bottom FET → caps
  - Vin on 2nd layer
- Variation 2: bottom FET → caps → top FET
  - Switch node on 2nd layer.. Buried
  - FETs a bit separated, better for thermals

Original



Top Layer

Variation 2



Top Layer