EMI - ESD PROTECTION SEMINAR

Signal Integrity Discussion

Low Inductance Ceramic Capacitors
Low Inductance Feedthru Filters
High Capacitance Ceramics
Ta and Ta Alternatives
Double Barrier Later Capacitors
Signal Line Termination Options

Field Applications Engineering Team
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International EMC Regulations:

IEC
Military
China
Japan
FCC
SPECIFICATION ACTIVITY ACCELERATION

MILITARY

- MIL-STD-461E  Conducted and Radiated Emission and Susceptibility (+test methods)
- MIL STD 285  Shielding Effectiveness

To a lesser extent DO160 (Avionic specs) becoming ‘more powerful’ as a emergency defacto

IEC

- EN61000-4 Basic Immunity – all parts
  IEC requirements are being proposed as a harmonization step to the FCC
  IEC requirements are being used to design JNS and CNS (ASIA)

FCC

- FCC Part 15  Computing Devices, cordless phones, satellite receivers, TV interface units, ...
  receivers, Low power Transmitters, Spread Spectrum Transmitters
- FCC Part 22  Cellular Telephones
- FCC Part 24  Personal Communication Systems
- FCC Part 90  Private Land Radio Service (paging and Mobile radio Transmitters)
- FCC Part 95  Personal Radio Service
- ANSI/IEEE C95.1 & OET Bulletin 65  RF Exposure

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# IEC ESD IMMUNITY TEST

**IEC 61000-4-2**

<table>
<thead>
<tr>
<th>TEST LEVEL</th>
<th>AIR DISCHARGE</th>
<th>CONTACT DISCHARGE</th>
<th>PEAK CURRENT</th>
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<tr>
<td>1</td>
<td>2 kV</td>
<td>2 kV</td>
<td>7.5 amps</td>
</tr>
<tr>
<td>2</td>
<td>4 kV</td>
<td>4 kV</td>
<td>15 amps</td>
</tr>
<tr>
<td>3</td>
<td>8 kV</td>
<td>6 kV</td>
<td>22.5 amps</td>
</tr>
<tr>
<td>4</td>
<td>15 kV</td>
<td>8 kV</td>
<td>30 amps</td>
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</table>
Traditional non Varistor ESD & EMI Control Methods:

Lay Out
Integration Caps
Ferrites
Resistors
Zeners

Typical PCB Optimization Schemes
Discussion of Traditional Protection Methods

- Layout
- Integrated Spark Gaps
- Integration Capacitors
- Ferrites
- Resistors
- Zeners
- Broadband SMT EMI Filter

<table>
<thead>
<tr>
<th></th>
<th>Cost</th>
<th>Effectiveness</th>
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<tbody>
<tr>
<td></td>
<td>free</td>
<td>good</td>
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<tr>
<td></td>
<td>free</td>
<td>possible negative</td>
</tr>
<tr>
<td></td>
<td>low</td>
<td>possible negative</td>
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<tr>
<td></td>
<td>moderate</td>
<td>negative</td>
</tr>
<tr>
<td></td>
<td>about free</td>
<td>negative</td>
</tr>
<tr>
<td></td>
<td>intermediate</td>
<td>great</td>
</tr>
</tbody>
</table>
AVX SMT FeedThru Filters

T Configuration

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How well do FeedThru Filters work?

SINGLE BROAD RESPONSE – ELIMINATE POLES

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Discussion of Traditional Protection Methods

FERRITE RULE:

• Maximize the series inductance using traces when possible
• Place ferrite beads in no ground circuitry

• MANY TIMES CHEAPER FERRITES ARE INCONSISTANT
Discussion of Traditional Protection Methods

ZENER RULE:

• Place clamping devices as close to the ESD entry point as possible*
• Do not assume that the Zener is noiseless
• Do not eliminate the EMC capacitor
• Watch for peak current wear out
• Watch for repetitive strike wear out
• Turn on time may or may not be a problem

* EXCEPTION: Place a Zener as close to up reset as possible
Top 10 PCB Design Rules

1) Use a multilayer PCB with large Vcc and ground plane

- if a ground plane is not practical create a ground grid

- not practical - connect all ground runs to a common point

  A ground grid minimizes loop area decreases radiated emission and increase radiated immunity

  A ground grid minimizes the inductance of the circuit (lowers ground noise)

  Generates less radiated emissions due to lower ground inductance

  Increases decoupling efficiency (potentially lowers cap values needed)
Top 10 PCB Design Rules

2) Use proven decoupling methods

- route the IC power trace close to the ground
- use a high frequency decoupling capacitor at each IC
- use a high frequency decoupling capacitor at the regulator
- connect all decoupling capacitors in low inductance manner

Proper decoupling reduces radiated noise

Proper decoupling 'hurts' ESD survivability (on signal traces)
Top 10 PCB Design Rules

3) Keep I/O traces short:
- Route I/O traces close to ground plane
- Place any connectors on top of the ground plane
- Isolate I/O traces by guard ground traces at the periphery

Remember:
Traces are long or short depending on:

\[ L \leq \frac{Tr \times v}{2} \]

where: \( L = \) Track length in cm
\( Tr = \) digital signal fall time
\( v = \) signal propagation velocity

\[ v = \frac{c}{Er} \]

where: \( c = 30 \text{ cm/ns (speed of light)} \)
\( Er = \) PCB dielectric constant

If traces are long consider using terminating techniques
When to Terminate Lines

Terminate if: \( L \geq 8Tr \)

where: \( Tr = \text{rise time (ns)} \)
\( L = \text{trace length (cm)} \)

- \( Tr = 3 \text{ ns} \) \( 8 \times 3 = 24 \text{ cm} \)
- \( Tr = 0.7 \text{ ns} \) \( 8 \times 0.7 = 5.6 \text{ cm} \)
- \( Tr = 0.1 \text{ ns} \) \( 8 \times 0.1 = 0.8 \text{ cm} \)

TTL/CMOS = 3 ns
ECL = 0.7 ns
GaAs = 0.1 ns
Top 10 PCB Design Rules

4) use minimal cable length

• long traces need termination (which is costs space and $)
• place ground on outside (ribbon) cable pins (if possible)
Top 10 PCB Design Rules

5) Terminate high speed lines

- Place R/C on the I/O driver
- use series $R = Zo$ on each I/O
- place cap on each I/O
Top 10 PCB Design Rules

6) Use shielded cables with known ground points

- Shielding costs too much
- Use EMC gaskets
- Use low value wide tolerance caps as an EMC wall

\[
E = \frac{5.5 \sqrt{P \cdot A}}{D}
\]

RF Feedback from the Antenna is consistently a problem

Where: P = power in watts
A = antenna gain
D = distance from the Antenna
Top 10 PCB Design Rules

7) Maintain consistent low Z grounds from PCB to PCB
   • route differential traces next to one another
   • keep all decoupling capacitor traces minimized
Top 10 PCB Design Rules

8) Place ESD sensitive components on PCB interior

- series L always helps ESD suppression
- parallel integration caps don't work reliably
- Spark gaps can emit E fields - watch reset lines
  build an EM wall with caps
Top 10 PCB Design Rules

9) Choose the oldest possible semiconductor family available (within reason)

Wide line width semis have a much higher ESD damage voltage

Wide line width semis typically run slower (less EMISSIONS)
Top 10 PCB Design Rules

10) Use the slowest speed IC possible
Advanced EMI and Transient Control Methods:

MultiLayer Varistors
Equivalent Circuit Model
SPICE Software
FeedThru Varistors
Varistor Arrays
Discussion of **NEW** Protection Methods

**MultiLayer Varistor (MLV)**: Trade name **TransGuard**

Miniature size  0402 to 1210, x 2 or x 4 arrays, FeedThru and FeedThru Arrays
The ceramic material is doped Zinc Oxide where every grain is a Schottky Diode. The structure between the plates gives series/parallel diodes. The entire volume dissipates energy.
Discussion of **NEW** Protection Methods

MultiLayer Varistor (MLV) : Trade name **TransGuard**

May replace EMC cap and require no board changes

**Discrete MLV Model**

Where:
- \( R_V \) = Voltage Variable resistance (per VI curve)
- \( R_p \) \( \geq \) \( 10^{12} \) Ω
- \( C \) = defined by voltage rating and energy level
- \( R_{on} \) = turn on resistance
- \( L_p \) = parallel body inductance

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TransGuard Case Sizes

0402  0603  0805  1206  1210

AVX TransGuards (MLV)

SOT 23  SMB  SMC

Diodes

AVX CORPORATION
TransGuard vs Silicon TVS

Turn-on Time

TransGuard Turn-on Time ~ 400ps
Silicon TVS Turn-on Time ~ 1200ps

IEC 1000-4-2 (ESD)

Unprotected Energy

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## Turn On Time Comparison

<table>
<thead>
<tr>
<th>Device Type</th>
<th>Turn on Speed (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0402 TransGuard</td>
<td>417</td>
</tr>
<tr>
<td>0603 TransGuard</td>
<td>673</td>
</tr>
<tr>
<td>0805 TransGuard</td>
<td>756</td>
</tr>
<tr>
<td>1206 TransGuard</td>
<td>818</td>
</tr>
<tr>
<td>1210 TransGuard</td>
<td>798</td>
</tr>
<tr>
<td>SOT 23 Diode</td>
<td>1380</td>
</tr>
</tbody>
</table>
TransGuards have Simple Implementation

TransGuard Capacitance ranges from 2.2 pf to 4.7 nf

* Options exist for capacitance range to 0.5 pf in BGA packages
ASIC RESET & Vcc PROTECTION

5.6V 0.1-0.4J

1 µf 0.1 µf 0.01 µf

5.6V 0.1J

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FeedThru Filter Varistors
Signal Integrity:
Low Inductance Ceramic Capacitors
Low Inductance FeedThru Filters
High Capacitance Ceramics
Ta and Ta Alternatives
Double Barrier Capacitors
Signal Line Terminations
Future Direction - Integrated L, C, & R’s in thick or thin film technologies - Custom and Standard circuits
IDC

- Low inductance device
- 175pH
- One capacitor, eight terminations
- VIP pcb configuration
**LGA**

- Newest Low inductance device
- ~27pH
- 2 – 8 Terminals

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New Solid Electrolyte Capacitor Developed by AVX

- OxiCap™
  - 3.3 and 5V Rail Solution
  - Stable Parameters
  - Cost for Performance
  - Wide Availability of Materials
  - Non-Burn*

* 95% reduced ignition failure mode compare to conventional tantalum capacitors

Issued by Technical Marketing Group AVX Tantalum Division
Datasheets & Technical Assistance: techsale-niobium@avx.cz

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TACmicrochip

• A brief introduction to the technology
  – How does it differ from standard technology
• Improvements over the last 2 years
  – Round to square
  – Automation
• Reliability data
• Typical electrical data
• Range extension development plan
  – including 0402 (1005M) plans
• Available Ratings
TACmicrochip Manufacturing

- Manufactured in wafers Vs traditional parts are individual
  - Reduced handling
  - Ease of automation
  - Improved quality
- Gives scope for customisation
  - Array
  - Block
  - Special size & shape

3 x 2 Block  
2 x 2 Block  
3 unit Array

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TAC MICROchip

Downsizing: Packaging Technology

• Results in low ESR, low inductance, low leakage in miniature package
• 0805, 0603, 0402 sizes.

Molded Ta Chip

Ta MicroChip

Tantalum Anode
AVX SuperCap Line Up

- BestCap™
- PrizmaCap™
- Cylindrical
- Modules

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