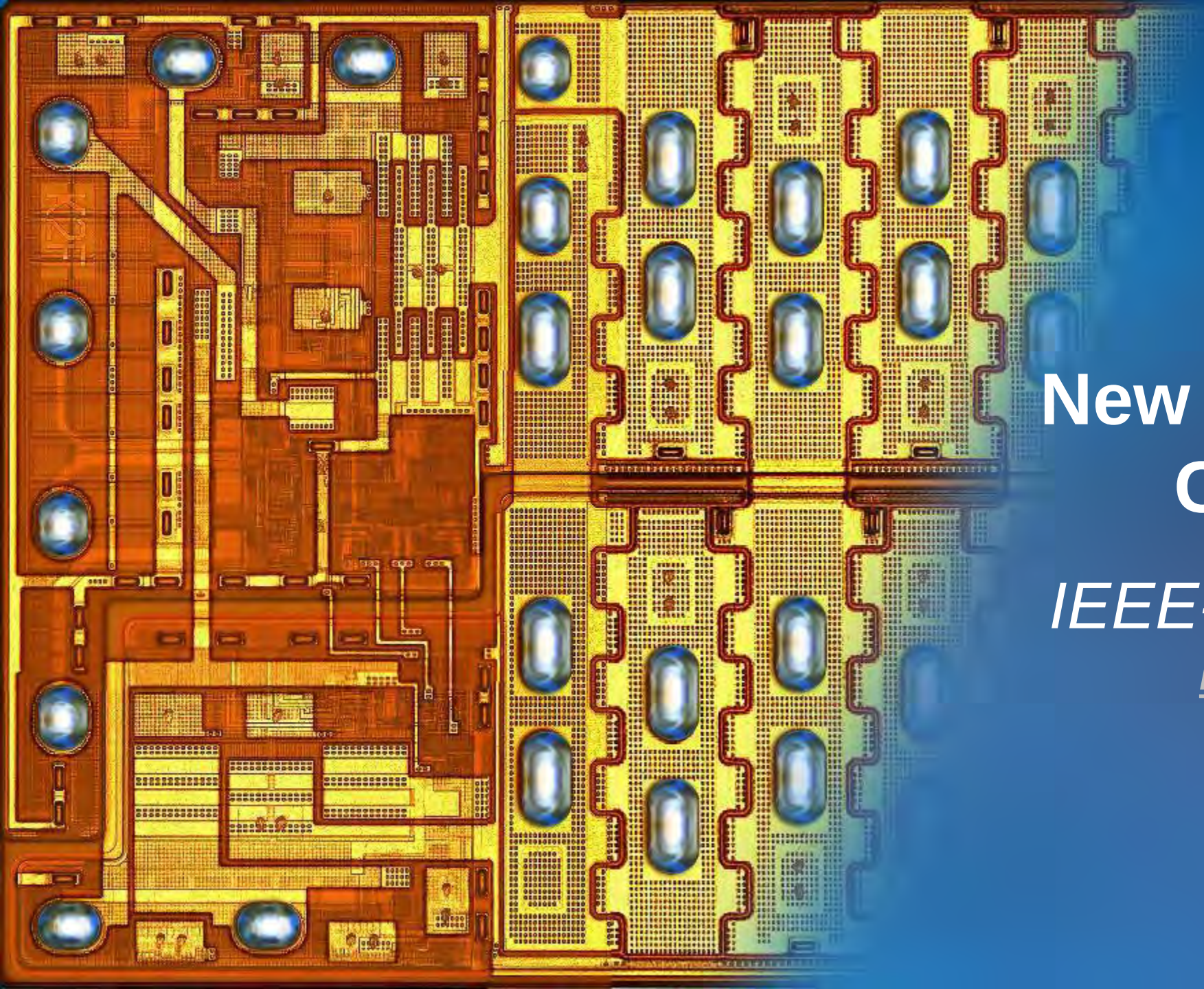


GaN FETs: New Packaging and Current Ratings

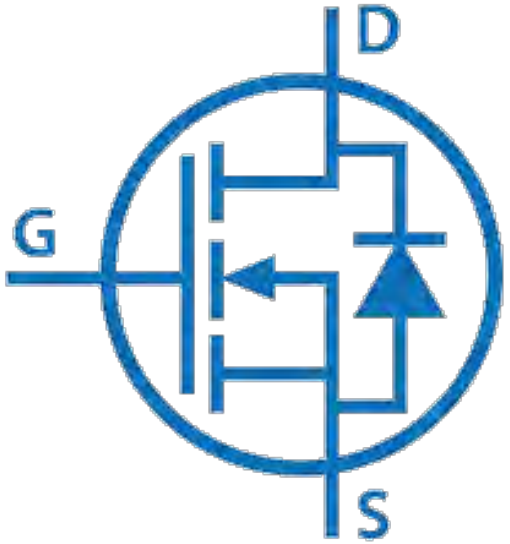
IEEE-Long Island 2026

brian.miller@epc-co.com

EFFICIENT POWER CONVERSION

Agenda: GaN Packages & Current Ratings

- Quick Review: GaN Power Devices
- Packages
  - FET Structure: Silicon vs. GaN FETs
  - MOSFET-optimized package
  - GaN-optimized package
  - System vs. device optimization
- Current Ratings
  - Developing *useful* current ratings
- Update
  - Technical advances in GaN FETs & ICs
- Summary



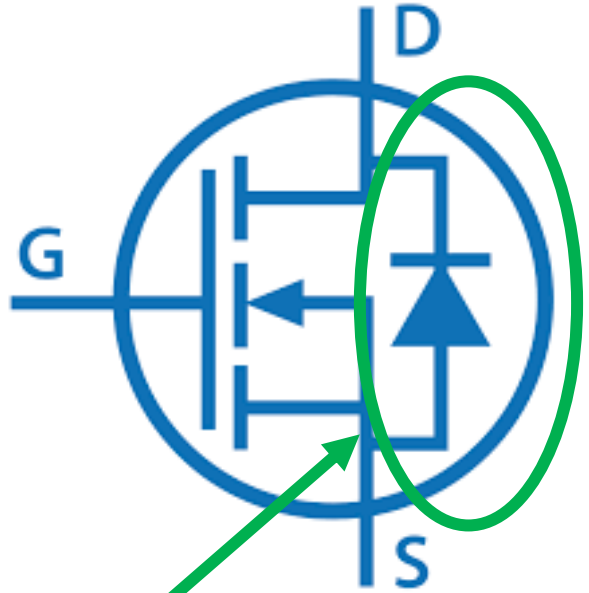
For PDH Credit:
www.ieee.li/forms/5458

review of
GaN Power Devices

Review

- Why GaN FETs?

- GaN FET characteristics:
  - Wide bandgap material GaN allows smaller FETs
  - Fast, efficient switching
    - Higher frequencies and/or higher efficiency
  - Thermally efficient: heat conducts very well
  - No parasitic PN diode
    - So, no reverse recovery
    - Diode *function*, but not a parasitic element

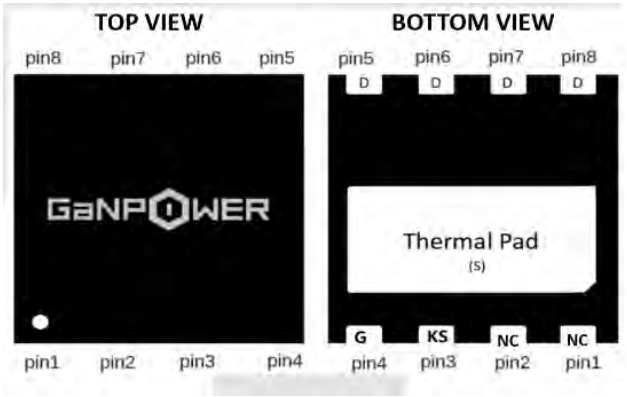


Review

- Many suppliers of GaN power FETs & ICs
- Voltage: 15 V to > 1.2 kV
  - 100 V as small as 0.9 x 0.9 mm
  - 650 V is very popular
  - 1200 V →
- Frequency: DC to GHz
  - RF GaN FETs were first:
    - depletion mode = normally ON
    - not popular for power FETs
  - Focus here: < 2 MHz power FETs
- Resistance:
  - 100 V: as low as 0.75 mΩ
  - 18 V: as low as 0.28 mΩ
- Gate Drive:
  - Typical: ON = 5V, OFF = 0V (← EPC devices)







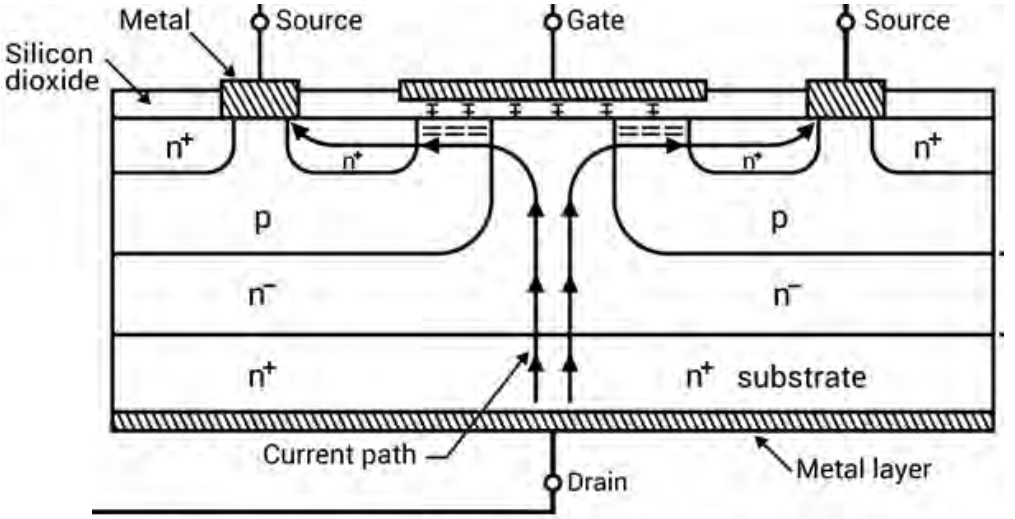




Packages

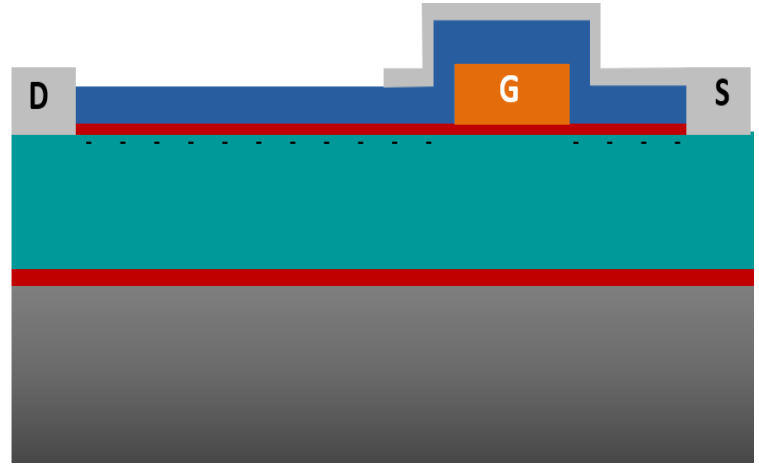
Structure of FETs

- Silicon MOSFETs – vertical conduction
  - Both sides of the FET die are terminals



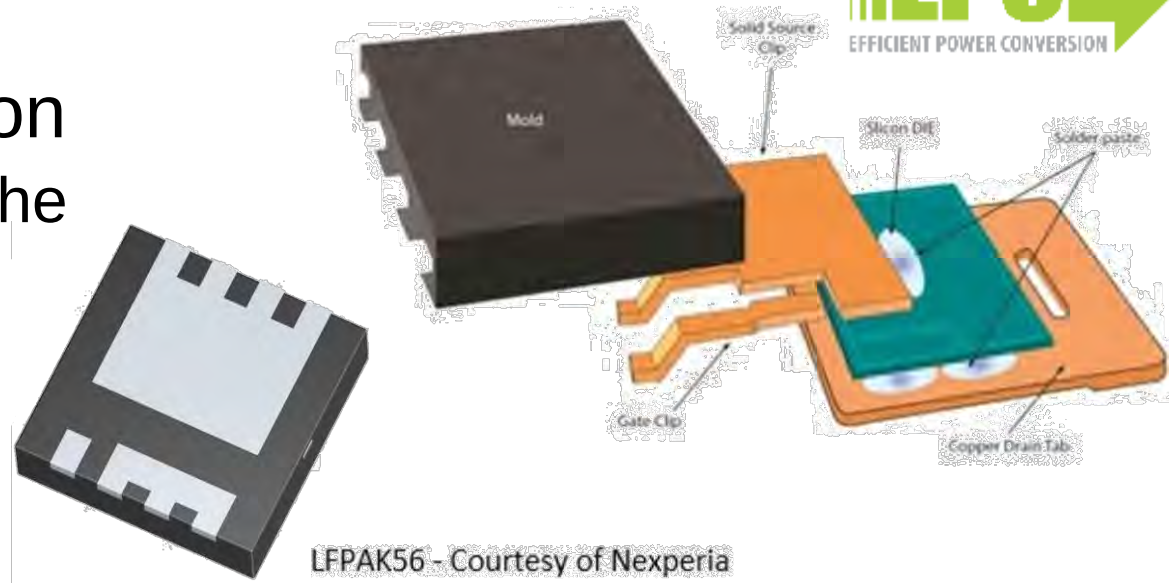
Basic structure of a n-channel DMOS power MOSFET

- GaN FETs (lower voltage) – lateral conduction
  - One side of the FET has all 3 connections



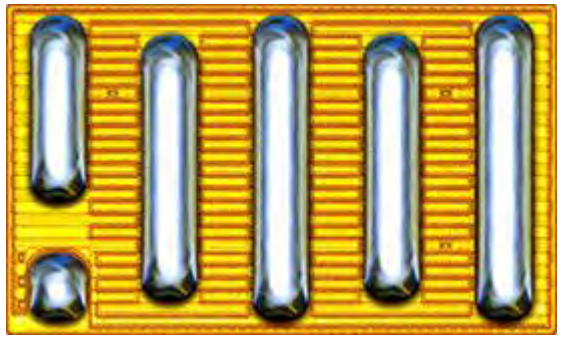
FETs in Packages

- Silicon MOSFETs – vertical conduction
  - Need to get top connection(s) down to the bottom (PCB)



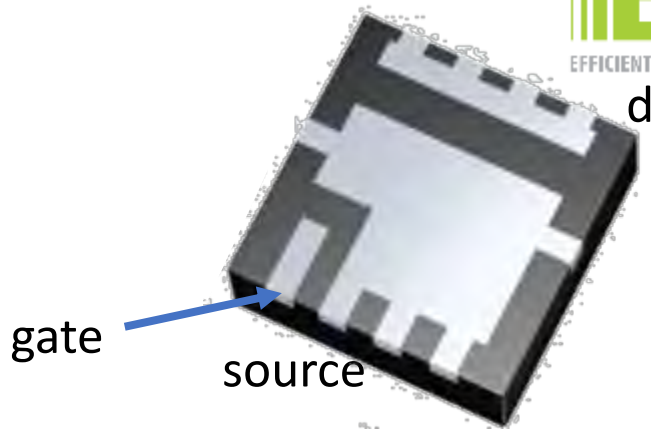
LFPAK56 - Courtesy of Nexperia

- GaN FETs (lower voltage) – lateral conduction
  - All connections already facing the board
  - So, don't need a package… but package has advantages

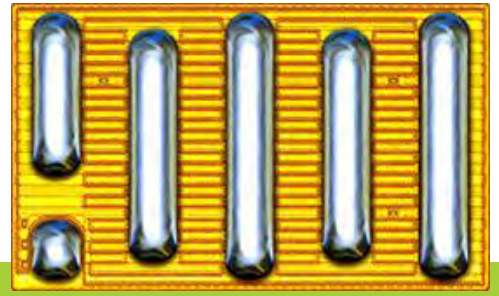


Package Footprints

- Silicon MOSFETs – electrical and thermal
  - One big pad connected to the bottom-facing terminal
  - Smaller pad for the lead-frame connected pins



- GaN FETs (lower voltage) – electrical and thermal
  - Both power pins are bottom-facing
  - No advantage for different-size pads (Source vs. Drain)
  - So, equal size is good





GaN Package Footprints

- Striped Pads
  - Many pins, alternating drain/source/drain/source…
  - Helps with inductance

- Disadvantages
  - Layout
  - Electrical
  - Thermal
  - Hand soldering

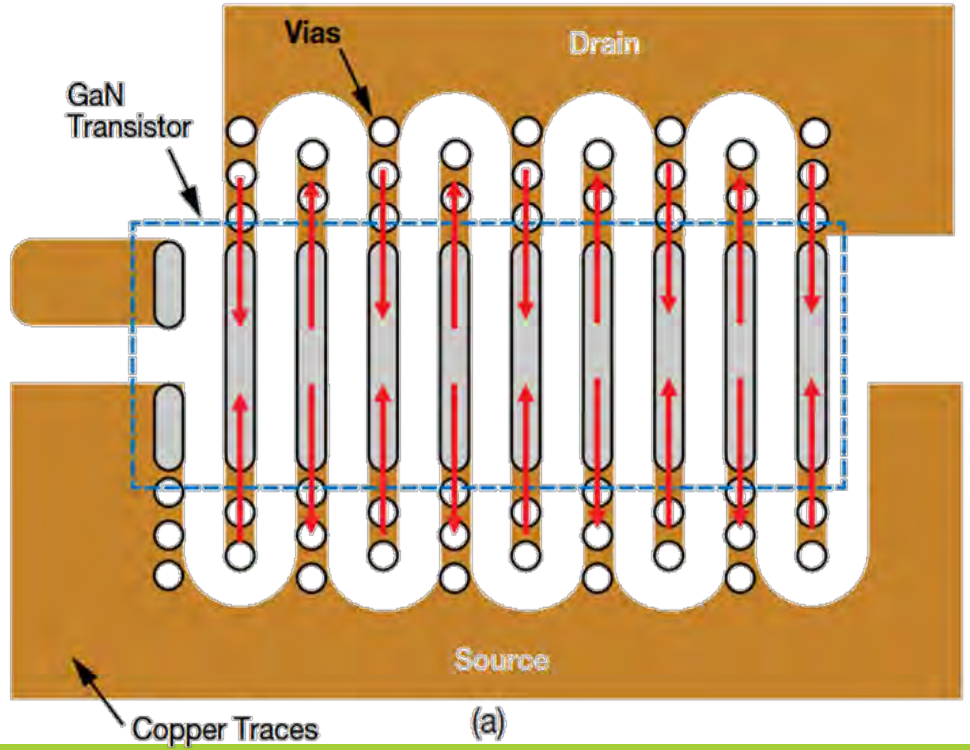
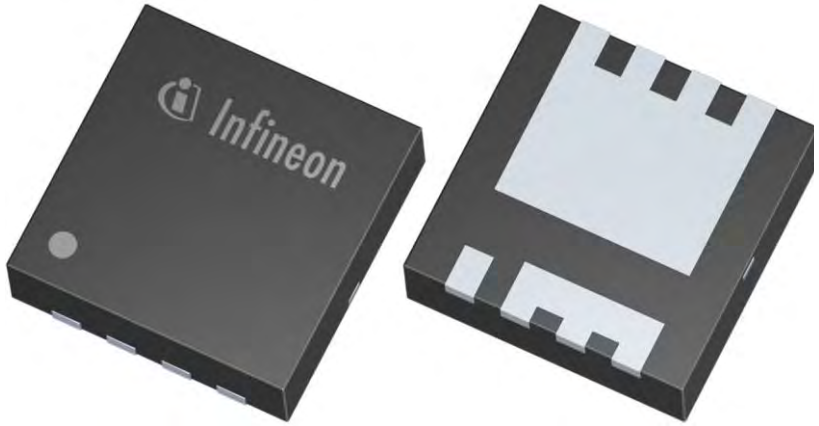


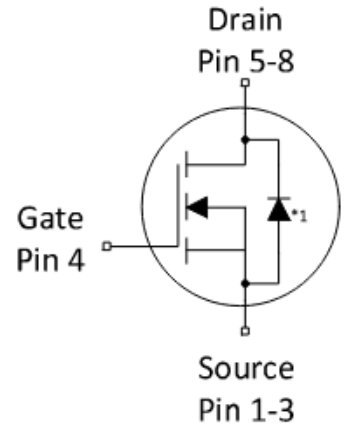


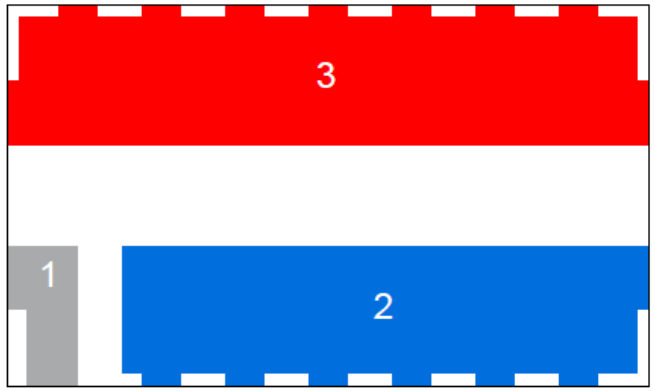
Diagram: [EPC app note]

What about MOSFET pin-out?

- You like it, right?
- Nice big pad,
  - good for current rating & thermal?
  - Standard 3.3 x 3.3 mm?
- ***Not optimum for GaN FETs!***
  - MOSFETs: *vertical* devices
  - GaN FETs: *lateral* devices
  - So, bad balance for GaN pins
  - Result: pins 1-3 high current density
- What to do?
  - Use almost equal-size power pads
  - A more ***GaN Optimized*** pinout

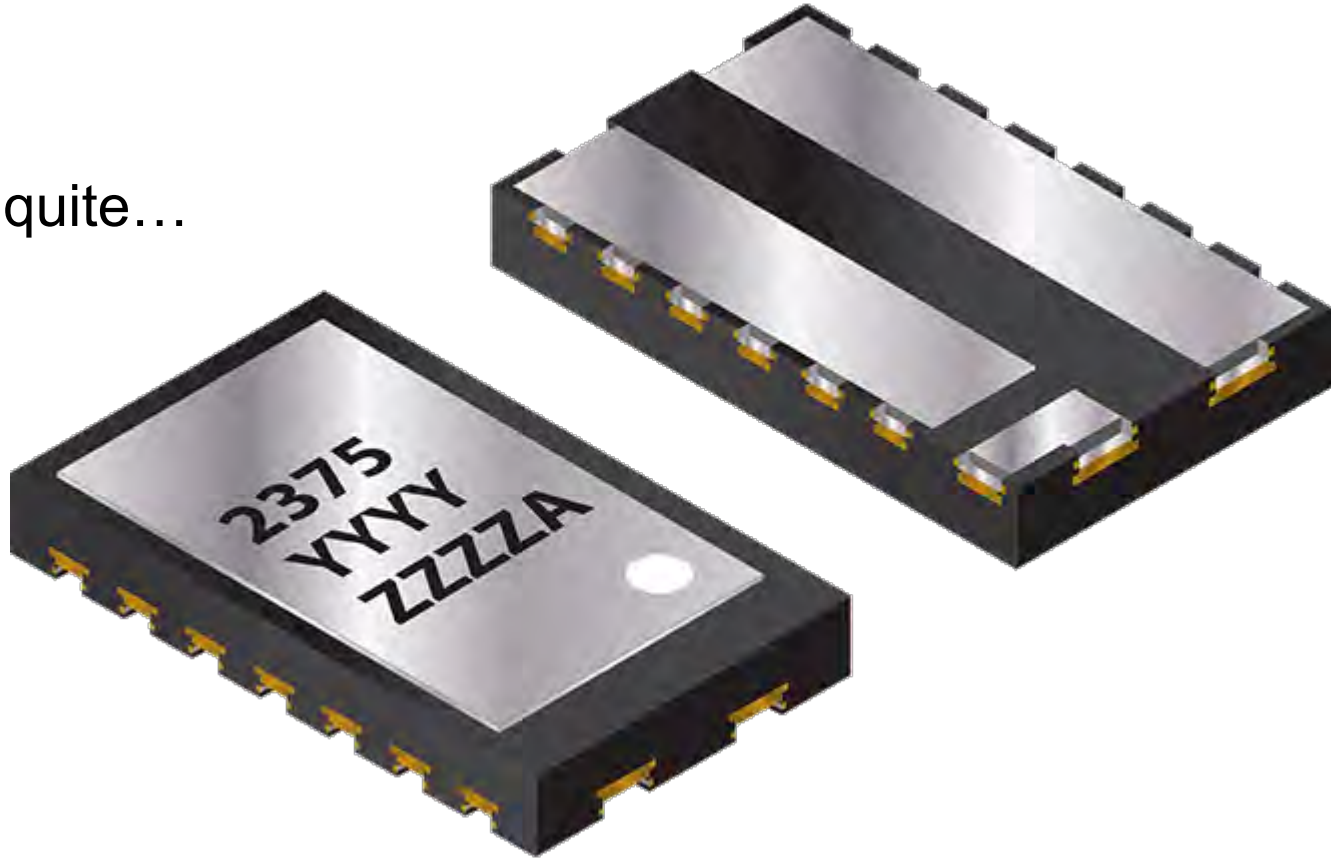






GaN-Optimized Package

- 3-Pin Packages
  - One Drain, one Source, one Gate
  - Like silicon MOSFET package? Not quite…
  - Equal-size Drain & Source
    - No reason not to

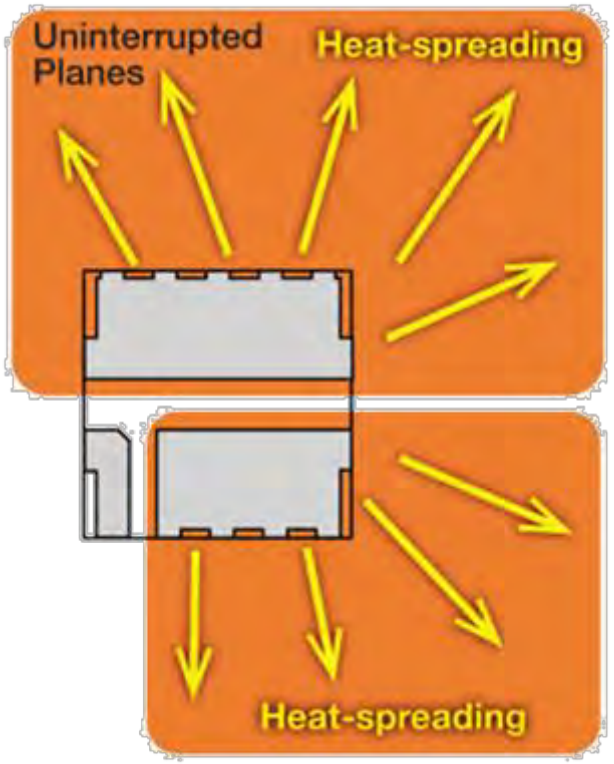


- Advantages
  - Layout
  - Electrical
  - Thermal
  - Hand soldering

  - Potential disadvantage: inductance at very high frequency

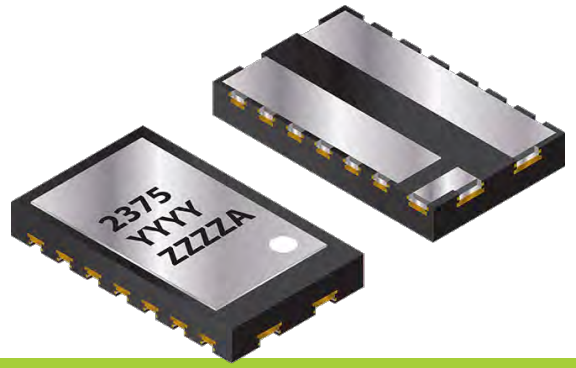
GaN-Optimized Package

- Thermal Differences
  - 3-Pin Package has the most uninterrupted copper planes

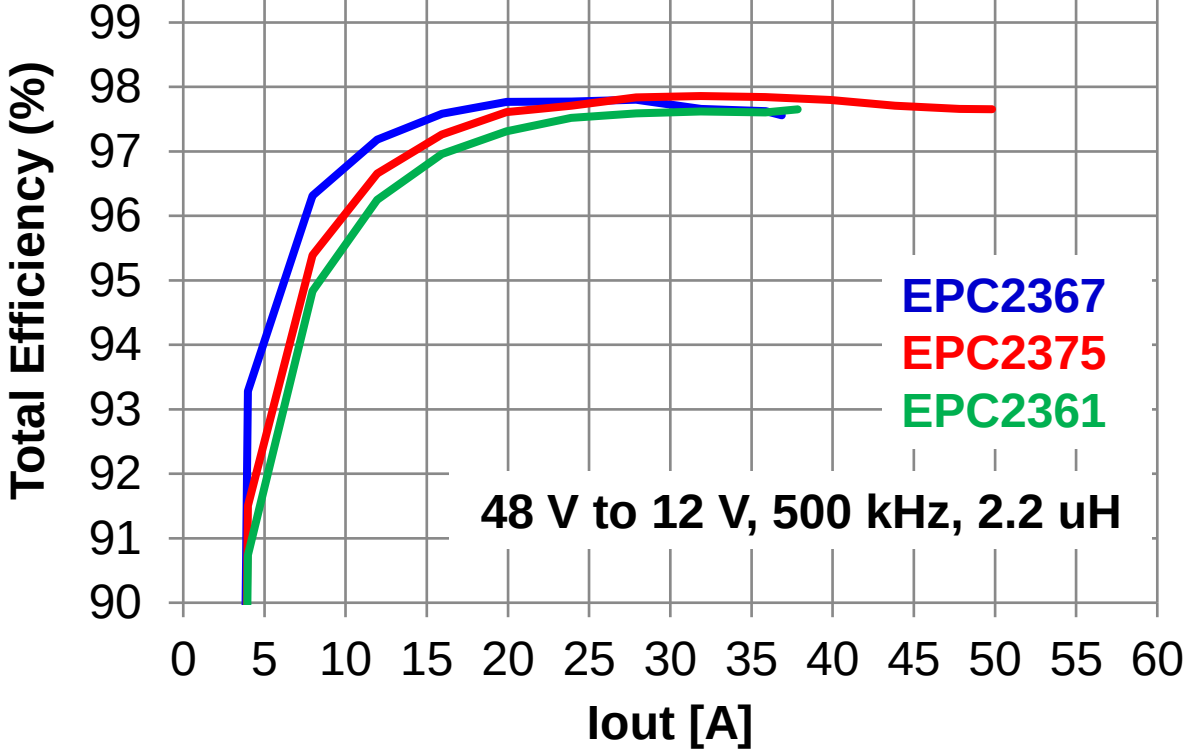


System Considerations

- FET with 3-Pin Packages
  - A bit higher Rds,on… oh no!
  - So… a bad idea?
- System
  - **Total R** = FET + PCB copper
  - **Thermal** into board
  - Test results – see **red** line
- Result: *System* Advantages



Rds,on: **0.9 mΩ** typical
Thermal: RθJC 0.2 °C/W
RθJB 1.5 °C/W



Rds,on: **0.75 mΩ** typical
Thermal: RθJC 0.2 °C/W
RθJB 1.5 °C/W



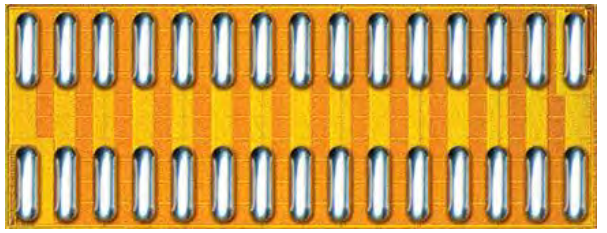
Current Ratings

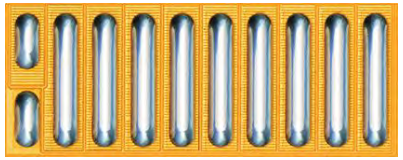
Are Continuous Current ratings practical?

Practical applications?

Examples @ max current

- EPC2022: 100 V, chip scale, 3.2 mΩ
  - Current rating (continuous): 90 A
  - Power: I2 R = 90^2 * 3.2 mΩ = **26 W (!) no!**
- EPC2015C: 40 V, chip scale, 4 mΩ
  - Current rating (continuous): 53 A
  - Power: I2 R = 53^2 * 4 mΩ = **11 W *maybe*…**



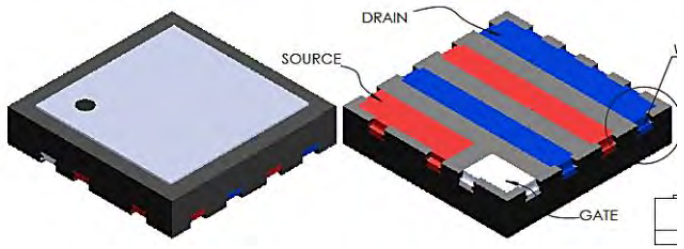


Worst:
100 V EPC2022
3.2 mΩ, 90 A
26 W

- Newer: EPC2366: 40 V, packaged, 0.84 mΩ
  - Current rating (continuous): 88 A
  - Power: I2 R = 88^2 * 0.84 mΩ = **6.5 W better**…



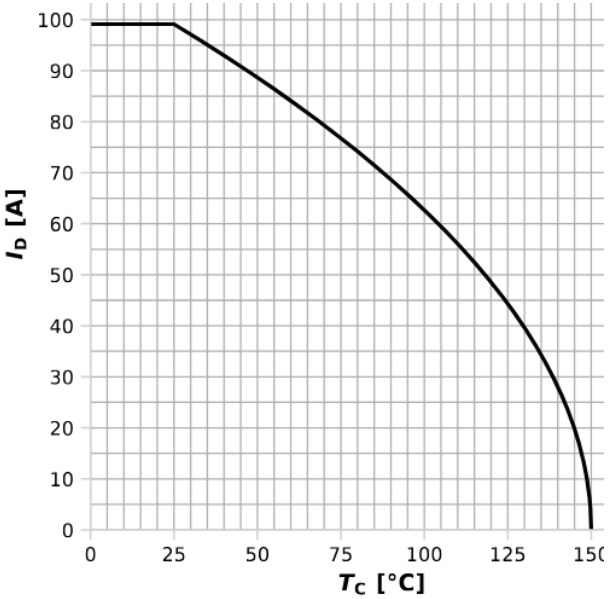
- New: EPC2370: 18 V, packaged, 0.28 mΩ
  - Current rating 101 A
  - Power: I2R = 101^2 * 0.28 mΩ = **2.85 W yes, practical!**



Continuous Current

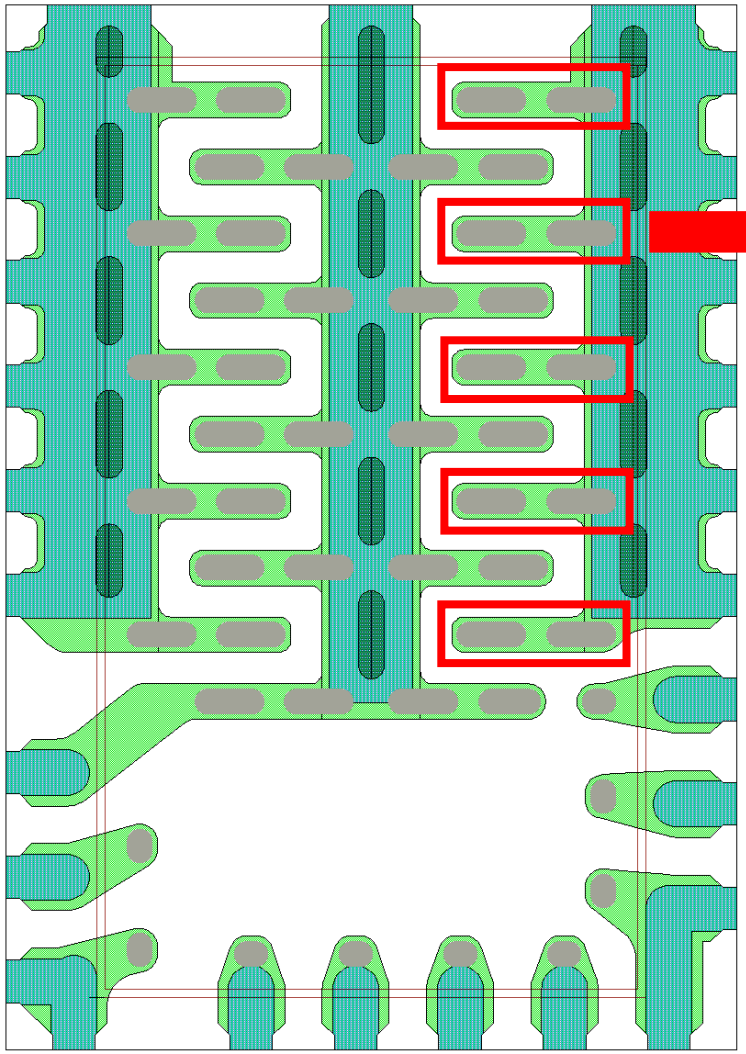
What is a useful current rating?

- **Rating at 25 °C junction?**
  - No, not a real max. operating point
- **Combining with thermal design into one rating?**
  - No… too many factors
  - Heat sink or not, air flow or not, environmental, etc.
- **Rating at 125 °C?**
  - Yes. Simple, one value
  - *If* this current rating is high enough to be OK for lower temps

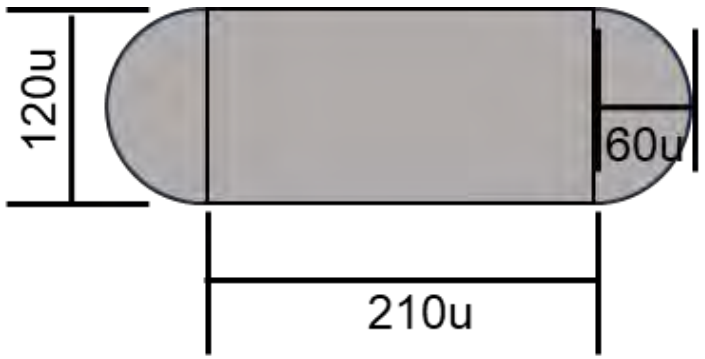


Continuous drain current	I_D	-	-	99	A	V_{GS}=5 V, T_C=25 °C	IGC019S06S1
I_D	Continuous (T_J < 125°C)			204	A		

How Is Continuous Current Rating Defined?



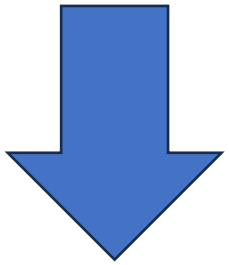
A=Area of A Cu Pillar Bump



- A total of 10 drain/source bumps
- The total Cu pillar bump cross-sectional area = 10A

How Is Continuous Current Rating Defined?

- Continuous Current Rating = **The total Cu pillar bump cross-sectional area** x ***current density, determined by electromigration***



- ***Old*** current limit = 10^4 A/cm^2 at 25°C

For more details…

- Documented in EPC's Reliability Report
- Link for Phase 17 Report
  - See page 19, section 4.3.4
  - Continuous Current Rating
- Structure of current path
- Why focus on copper pillars, etc.

> The primary cause of EM is the electron "wind" generated from the transfer of momentum between conducting electrons and metal ions in the crystal. When the momentum surpasses the diffusion threshold that is governed by an activation energy [30,31] metal atoms can move and create voids. The Black's model is widely accepted to predict lifetime under EM wear-out mechanism, as shown in Eq. 4-19 [29,30].

Old Datasheet for FET *EPC2361*

- ***Old*** current density = 10^4 A/cm^2 at 25 °C
- Total Cu pillar bump cross-sectional area = ~10^{-2} cm^2
- 10^4 A/cm^2 x ~10^{-2} cm^2 = ~100 A

Preliminary **EPC2361 – Enhancement Mode Power Transistor**

Maximum Ratings

	PARAMETER	VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150 °C)	120	
I_D	Continuous (T_A = 25°C)	101	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	519	

New Continuous Current Rating

- Through extensive electromigration testing, EPC results show that EPC's Cu pillar bumps are capable of ***1.3 x 10^4 A/cm^2 at 125°C with 0.1% failure rate in 10 years***
  - Reported in Phase 16 and Phase 17 Rel Report

- ***A 30% improvement than the old current density***
- ***And, at 125 °C***

Final Datasheet of EPC2361

- ***New*** current density = 1.3×10^4 A/cm^2 at 125°C
- Total Cu pillar bump cross-sectional area = ~10^{-2} cm^2
- 1.3×10^4 A/cm^2 x ~10^{-2} cm^2 = ~130 A

Final **EPC2361 – Enhancement Mode Power Transistor**

Maximum Ratings			
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
$V_{DS(tr)}$	Drain-to-Source Voltage (Repetitive Transient) (1)	120	
I_D	Continuous ($T_J \leq 125°C$)	131	A
	Pulsed (25°C, T_{PULSE} = 10 µs)	697	
	Pulsed (125°C, T_{PULSE} = 10 µs)	558	

Pulsed Current Rating Update

How is the Pulsed Current Rating Defined?

- I_{Pulse} = ***A Current Density*** X Gate Width (Wg)
  - Wg ≈ Die Size
  - Larger the die size or lower the $R_{DS(on)}$ → higher the pulsed current rating

- EPC2252: ***0.15 A/mm*** X Wg of 500 mm → I_{Pulse} = 75 A

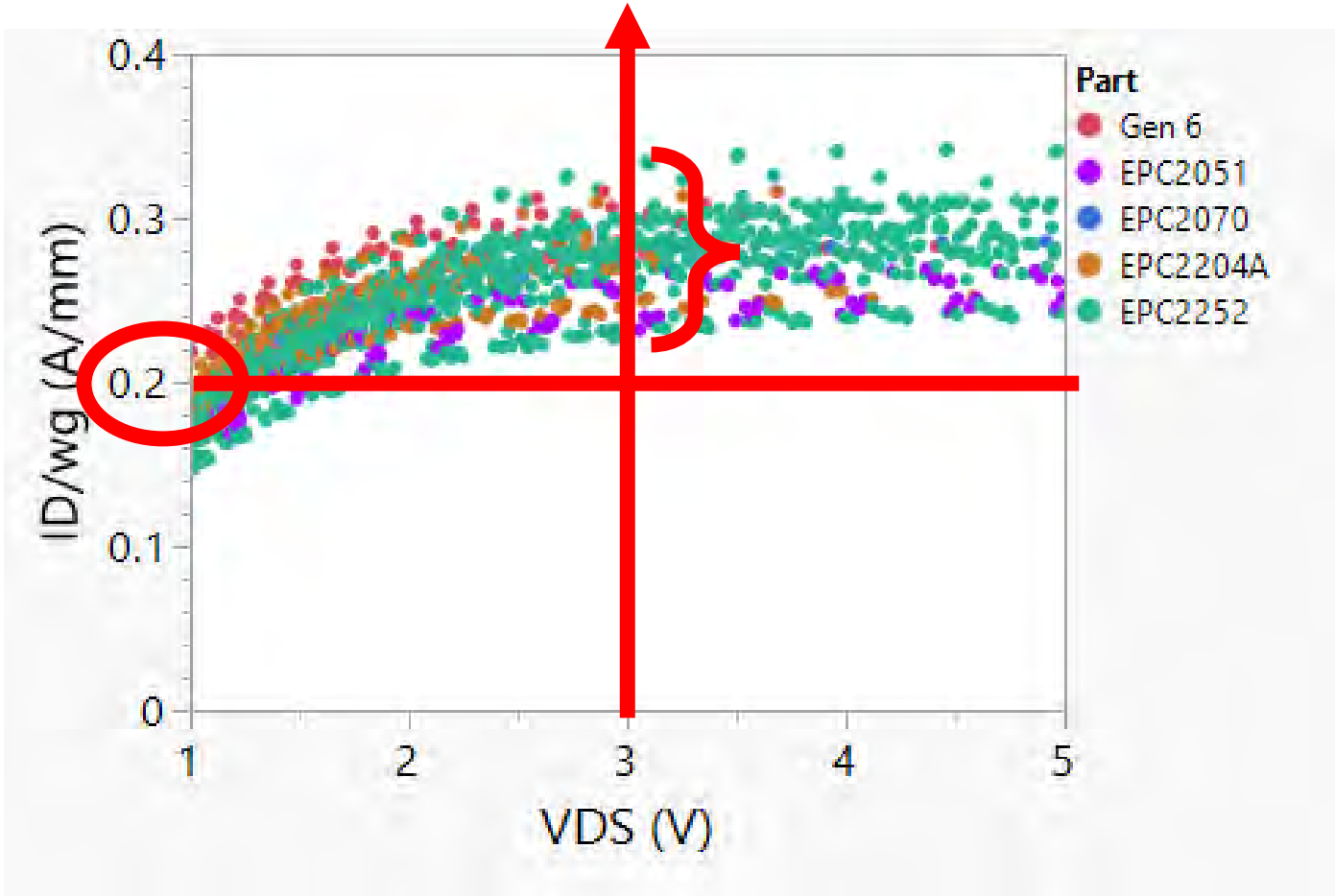
Maximum Ratings			
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	80	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	96	
I_D	Continuous (T_A = 25°C)	8.2	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	75	

Can We Improve 0.15 A/mm Current Density?

Yes, We Can!

- Tested Gen5 and Gen6, 5 different products, 10+ wafer lots at 25°C and V_{GS}=5V

- The new pulsed current density (***minimum***) is: ***0.2 A/mm***



For more details…

- Documented in EPC's Reliability Report
- Link for Phase 17 Report
  - See page 20, section 4.3.5
  - Pulse current rating
- Test results
- Deratings, etc.

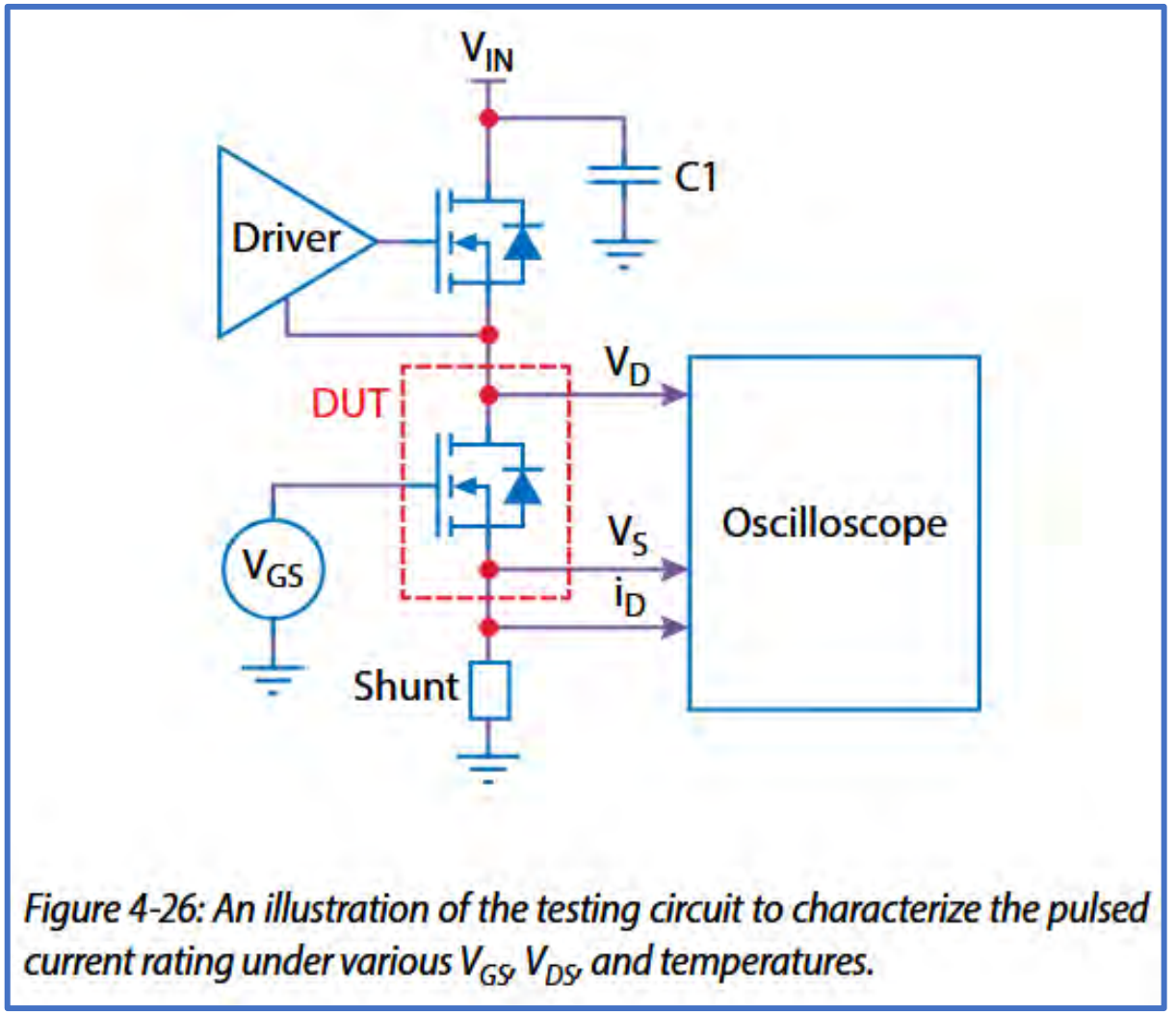


Figure 4-26: An illustration of the testing circuit to characterize the pulsed current rating under various V_{GS}, V_{DS}, and temperatures.

Improve the Pulsed Current Rating 33%

EPC2252 – Enhancement Mode Power Transistor

Before

Maximum Ratings			
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	80	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	96	
I_D	Continuous (T_A = 25°C)	8.2	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	75	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	

Now: 0.2 A/mmx500mm=100A

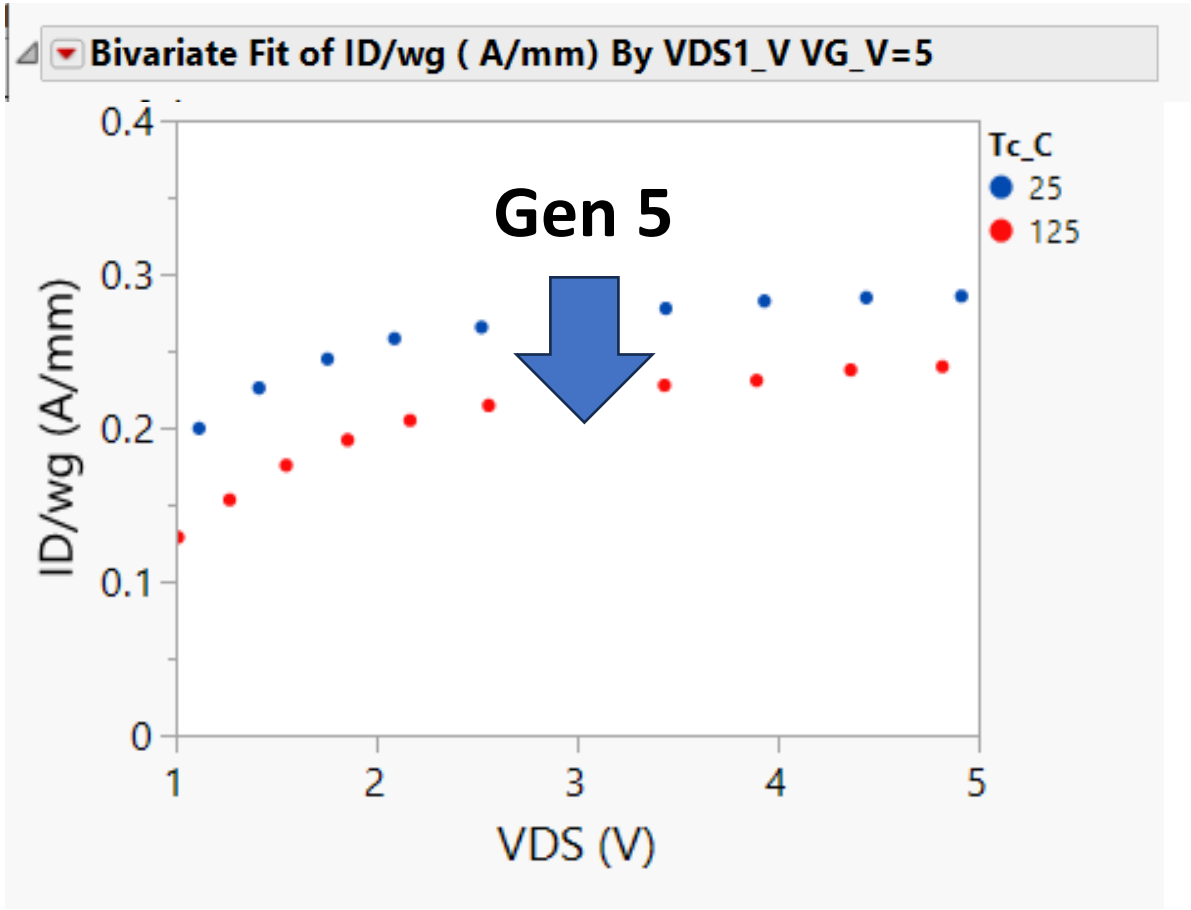
Maximum Ratings			
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	80	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	96	
I_D	Continuous (T_A = 25°C)	8.2	A
	Pulsed (25 °C, T_{PULSE} = 10 µs)	100	
	Pulsed (125 °C, T_{PULSE} = 10 µs)	80	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	

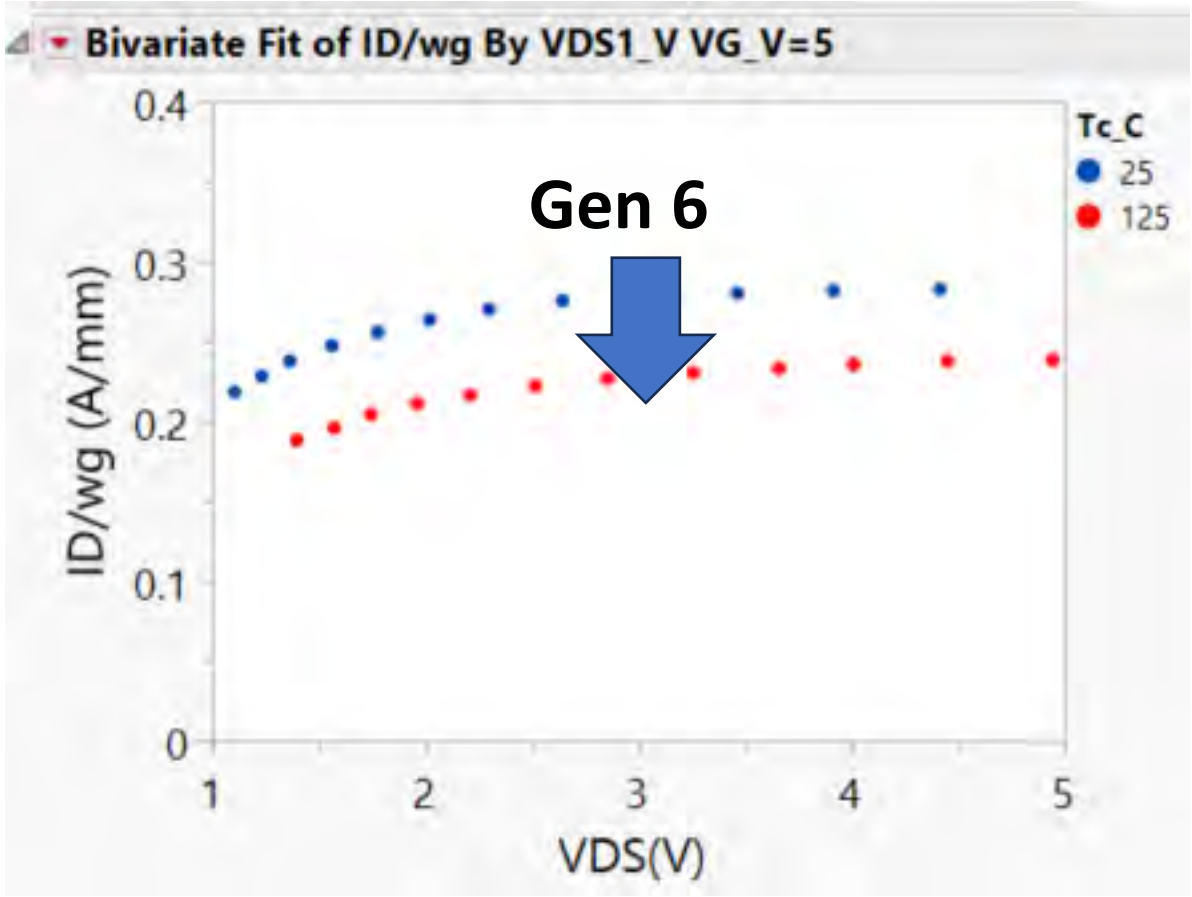
33% Improvement!

What about 125°C?

25°C vs. 125°C for Gen5 and Gen6 with V_{GS}=5V

20% decrease in pulsed current rating from 25°C to 125°C





EPC2252 – Enhancement Mode Power Transistor

Maximum Ratings			
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	80	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	96	
I_D	Continuous (T_A = 25°C)	8.2	A
	Pulsed (25 °C, T_{PULSE} = 10 µs)	100	
	Pulsed (125 °C, T_{PULSE} = 10 µs)	80	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	

20% lower

> 75 A

Summary of Current Ratings

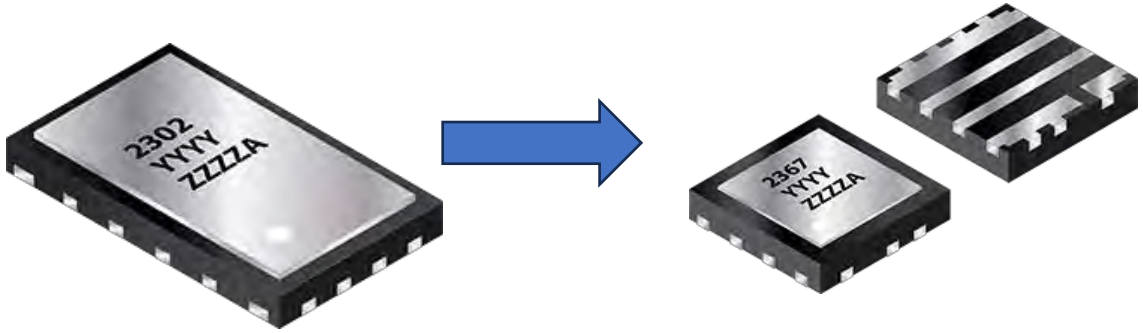
- **Continuous Current Rating**
  - Determined by current density of internal copper pillars
  - New ratings: given for 125 °C junction
  - Thermal system design is important, but a separate issue

- **Pulse Current Rating**
  - Related to: die area & current density
  - This rating used often used for laser pulsing

GaN Advances

Generational Advances

- EPC: Gen 5 → Gen 6
  - For 100 V, FETs comparison →
  - Conduction loss: reduced
  - Switching loss: reduced
  - Dead-time loss: about the same
  - Size & Cost: reduced



1.8 mΩ max
Qgs 8.9 nC; Qoss 85 nC
3 x 5 mm

1.5 mΩ max
Qgs 5.3 nC; Qoss 54 nC
3.3 x 3.3 mm

- Nice Advances from other GaN suppliers
  - **Navitas Semi.**: 650 V, ~ 175 mΩ, 8 A
    - ***Size Reduction***: from 48 sq. mm to 30 sq. mm
  - **Infineon, others**: similar size reduction

- GaN monolithic power ICs

Summary

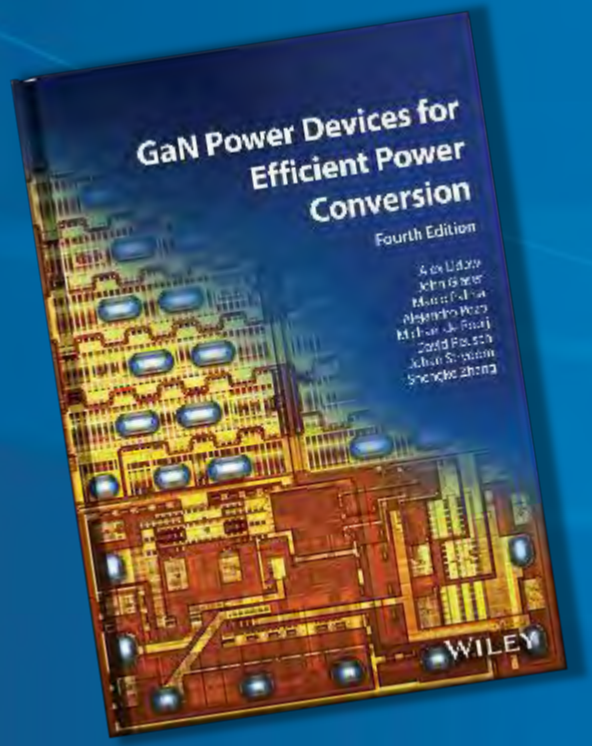
- GaN FETs have advantages for power electronics
- **Packages** can be optimized for GaN FETs
  - Current flow direction is lateral (vs. vertical for silicon)
  - Optimization based on lateral produces a different footprint
  - System optimization factors
- **Current Rating** for GaN FETs
  - Goal: easy-to-use, realistic rating system
  - Continuous current rating: limited by Metal Migration
- Advances for GaN power devices

EFFICIENT POWER CONVERSION

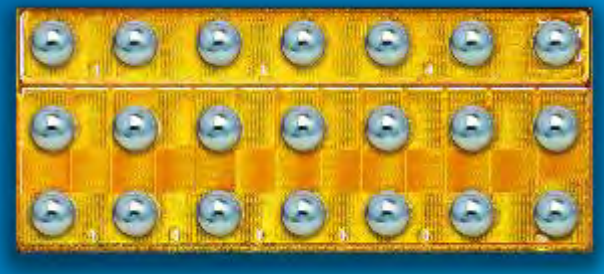
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How To GaN Video Series

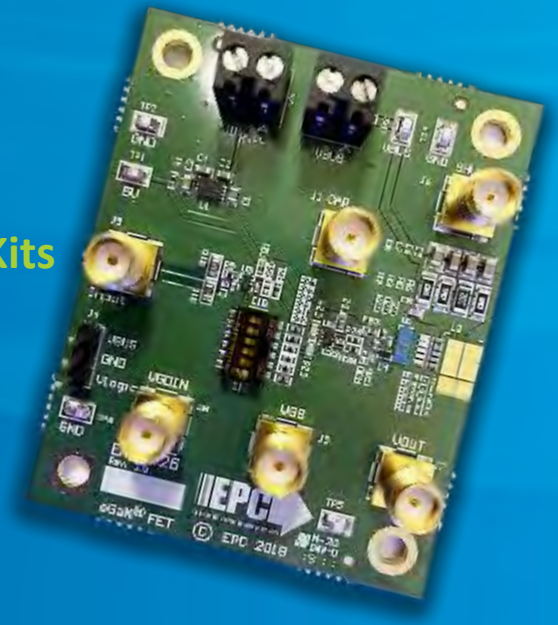


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