GaN Power Amplifier Design

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GaN Power Amplifier Design

- This lecture introduces attendees to the GaN transistor, its properties, various structures, including the latest GaN power amplifier (PA) design techniques.
- The properties of GaN will be presented showing the advantage of these devices over GaAs and Si. GaN HEMT transistors will be shown delineating the various geometries, semiconductor processes and structures with associated performance.
- Guidelines for reliable operation will be presented considering device junction temperature including thermal management techniques.
- The nonlinear models of GaN HEMT devices necessary for the CAD of PAs will be presented.
- Design considerations for both constant amplitude envelope signals as well as the non-constant amplitude envelope signals will be presented.
- Step-by-step design procedures will be shown for various GaN PA examples including different classes of operation as well as the popular Doherty PA.
EDWARD C. NIEHENKE, Ph.D., PE, Consultant, Baltimore, Maryland, USA.

- Niehenke has pioneered the development of state-of-the-art RF, microwave, and millimeter wave components at Westinghouse/Northrop Grumman for 34 years. Circuits include low noise amplifiers, low noise oscillators, mixers, power amplifiers, phase shifters, attenuators, limiters, frequency multipliers, low-phase noise millimeter wave fiber optical links, and miniature integrated assemblies and subsystems. He previously worked in cryogenic electronics research at Martin-Marietta. He now consults and lectures on linear/nonlinear and wireless transmit/receive circuits and systems. Since 1983 he lectured to over 3000 professionals throughout the world for Besser Associates and the Continuing Education of Europe. He holds nine patents, one George Westinghouse Innovation Award, and has authored numerous papers on RF, microwave, and millimeter wave circuits.

- Niehenke is active in IEEE MTT-S activities serving on three technical committees and is their Ombudsman. He was technical program chair of the 1998 IMS, chair 1986 IMS, 1986/87 IEEE Distinguished Microwave Lecturer, and served as a member of ADCOM for 9 years. Niehenke taught electricity and magnetism for 3 years at Johns Hopkins University. He was a recipient of the IEEE Centennial and Millennium Medals, is a fellow of the IEEE, and is a registered professional engineer in the State of Maryland.

What is Important for a Power Amplifier

- High Power
- High Efficiency
- High Reliability
- Good Frequency Range
- Non Complex Matching with wide bandwidth
- Linear for Varying Amplitude Modulation
- Low Cost
Let's Examine a Transistor

- To see what parameters are important
  - For Output Power
  - For Efficiency

Power and Efficiency Class A

- Transistor Voltage Swing = \( V_{\text{max}} - V_{\text{min}} \)
- Transistor Current Swing = \( I_{\text{max}} - I_{\text{min}} \)
- Adjust load resistance \( R_L \) for full ac swing
- \( V_{\text{max}} - V_{\text{min}} = R_L (I_{\text{max}} - I_{\text{min}}) \)
- \( R_L = \frac{V_{\text{max}} - V_{\text{min}}}{I_{\text{max}} - I_{\text{min}}} \)
- \( V_{\text{DC}} = \frac{V_{\text{max}} + V_{\text{min}}}{2} \) \( \Rightarrow \) \( I_{\text{DC}} = \frac{I_{\text{max}} + I_{\text{min}}}{2} \)
- \( P_{\text{DC}} = \frac{(V_{\text{max}} + V_{\text{min}})(I_{\text{max}} + I_{\text{min}})}{4} \)

\( \eta = \frac{P_{\text{EFF}}}{P_{\text{DC}}} = 0.5 \frac{(V_{\text{max}} - V_{\text{min}})(I_{\text{max}} - I_{\text{min}})}{(V_{\text{max}} + V_{\text{min}})(I_{\text{max}} + I_{\text{min}})} \)
### GaN HEMT Basic Transistor Circuitry

- **Gate to Source**
- **DC Bias Voltage**
- **Gate Biasing**
- **RF Source**
- **Temperature Increase Monitor Probe**
- **Drain to Source**
- **DC Blocking Cap**
- **GaN HEMT**
- **Tcase = 25°C**
- **Rth = 3.8°C/W**
- **Drain Biasing**
- **Output Port Load Resistance**

### Material Properties Comparison

#### RF Power = (Vmax – Vmin)Imax/8

<table>
<thead>
<tr>
<th>Material</th>
<th>Band Gap Energy (eV)</th>
<th>Critical Breakdown Field (MV/cm)</th>
<th>Thermal Conductance (W/cm²K)</th>
<th>Mobility (cm²/V·s)</th>
<th>Saturated Velocity (10⁷ cm/s)</th>
<th>Relative Dielectric Constant εr</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>1.1</td>
<td>0.3</td>
<td>1.5</td>
<td>1300</td>
<td>1</td>
<td>11.9</td>
</tr>
<tr>
<td>GaAs</td>
<td>1.4</td>
<td>0.4</td>
<td>0.5</td>
<td>6000</td>
<td>1.3</td>
<td>12.9</td>
</tr>
<tr>
<td>4H SiC</td>
<td>3.2</td>
<td>3.3</td>
<td>3.7</td>
<td>610</td>
<td>2</td>
<td>9.7</td>
</tr>
<tr>
<td>6H SiC</td>
<td>3.0</td>
<td>3.0</td>
<td>4.9</td>
<td>310</td>
<td>2.0</td>
<td>9.7</td>
</tr>
<tr>
<td>GaN</td>
<td>3.4</td>
<td>3.0</td>
<td>1.5</td>
<td>1500</td>
<td>2.7</td>
<td>9.0</td>
</tr>
</tbody>
</table>

- High Temperature Operation
- High Power (High Vmax)
- High Power (High Imax)

GaN mobility enhanced with HEMT structure for higher gain and frequency operation

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Differences Between 4H and 6H SiC Substrates

- 4H and 6H SiC are different crystalline structures of the material with different properties.
- 6H SiC is conductive and used for LED’s (one contact).
- 4H Semi-insulating, better crystalline matched to GaN, and easier to make.

GaAs Low Noise Operation

- The mobility of GaN is so much lower than GaAs. For Ultra Low Noise GaAs PHEMTs are used over GaN.
- The mobility shown is for GaN but GaN HEMT’s have higher mobility. The noise figure is very good for these devices not as low as the GaAs PHEMTs.
- For example the Crey 0.4 mm device:
  - Where the GaN HEMT will shine is to have reasonable NF with high power capability so a receiver protector could be eliminated also they would have a high IP3.
Silicon LDMOS Versus GaN HEMT Transistor

- The bandgap energy of silicon is only 1.1eV but Si LDMOS are used for high power applications.
- Silicon as used in LDMOS can be run at 150°C for high reliability, not 180 to 225°C for GaN (Higher bandgap).
- LDMOS has good breakdown voltages and also can use a large device to get the current for power. However, it is typically limited to use around 3 GHz. The GaN HEMT is a much higher frequency device.
- Cost is the issue and GaN price is now coming down.
High Efficiency ($\eta$)

- $\eta = k \frac{(V_{\text{max}} - V_{\text{min}})}{(V_{\text{max}} + V_{\text{min}})}$
  - $k = 50\%$ Class a, $78.5\%$ Class b and higher for class c, d, e, f, and f
- We will discuss later in the lecture all the details of the various classes of operation
- With high voltage operation (high $V_{\text{max}}$), and reasonable low $V_{\text{min}}$ (knee voltage) the ratio of $(V_{\text{max}} - V_{\text{min}})/(V_{\text{max}} + V_{\text{min}})$ will close to unity as opposed to low voltage operation where the ration takes a big hit on efficiency

Operation with high standing waves

- With a highly mismatched load, the transistor will see a higher voltage depending on the phase of the mismatch, so for the worse case the breakdown voltage must be larger than normal for this condition.
GaN Transistor Meets Objectives

- High Power
  - High breakdown voltage
  - High peak current, (Saturated velocity)
  - High current capability
- Good efficiency
  - Low knee voltage (V_{min})
  - High V_{max} --- High breakdown voltage
  - Can cutoff current at high voltage – low I_{min}
  - Low semiconductor and circuit losses
- High Reliability
  - High temperature operation (High band gap material)
  - High reliability process
  - Low thermal resistance

Let's Look at a GaN Device to See How it Performs Compared to the Calculated Performance

- 1.9 GHz
- 28V DC operation
- GaN HEMT Device on 100 \mu m of 4H SiC
- 0.25 Gate Length
- 1.8 mm Wide
- Nonlinear Model Developed by Dr. Walter Curtice
- Load the file cfet9.dll into AWR model directory
- Open up the file hb_cfet_1p8mmClassA.emp for class A operation and hb_cfet_1p8mmClassB.emp for class B operation
Note that the IV has a Negative Slope 

In the Saturated Region

- This is due to self heating of the transistor. As the transistor heats up the current decreases

Self heating turned off  With self heating
1.8 mm GaN HEMT Class A

- $V_{\text{max}} = 58.29$, $V_{\text{min}} = 0$
- $V_{\text{min}} = 3.2$ V, $I_{\text{max}} = 1.12$ A
- $RL = (V_{\text{max}} - V_{\text{min}})/I_{\text{max}} = 49.2 \Omega$
- $P = (58.29 - 3.2)/(1.12)/8 = 7.72$ W or 38.9 dBm
- $P_{\text{dc}} = 28 \times 0.62A = 17.36$ W
- $\eta = 7.72/17.36 = 45\%$
- $\eta = 0.5 \times (58.28-2)/(58.28+3.2)$
- $\eta = 45\%$
- $PAE = (P_{\text{out}} - P_{\text{in}})/P_{\text{dc}}$
- $PAE = \eta (1 - 1/G)$
- $G = \text{Gain}$
- For high gain $PAE = \eta$

Load Line Selection

- Examine the load line and adjust $P_{\text{in}}$, $V_{\text{gs}}$ and $R_{\text{Load}}$ until you get simultaneously a good voltage and current swing.
- There are many answers so you should also look at the data of $P_{\text{out}}$, $PAE$, $Gain$ and $Gain\ Compression$ and choose the best.
- When choosing possibilities, always compare possibilities with the same gain compression amount.
- I chose a condition is where the gain is compressed about 1 dB in comparing the various possibilities.
- You can also do an optimization procedure.
1.8 mm GaN HEMT Class A
Calculated parameters similar to Harmonic Balance results

- $P = 38.9 \text{ dBm}$
- $\eta = \text{PAE} = 45\%$

1.8 mm GaN HEMT Class A
Gain and Phase VS Pin

- Note low Gain and Phase variation versus Pin ideal for low ACPR and EVM for digitally amplitude variant modulated signals
Thermal Considerations

- $T_j = T_{hs} + P_{diss} \times \theta$
- $T_j = \text{Junction temperature}$
- $T_{hs} = \text{heat sink temperature}$
- $\theta = \text{Thermal resistance}$
- $P_{diss} = P_{dc\ in} + P_{rf\ in} - P_{rf\ out}$
- Class a has high temperature when not obtaining output power because dc power and inputs power are the heat inputs.
- With higher input powers, significant power is extracted, reducing the dissipated power and junction temperature rise

Thermal Port Voltage

- The thermal port voltage is calibrated to read the junction temperature rise over heat sink temperature. The heat sink temperature is an input to the model.
- You just put a voltage monitor on it and read the voltage value and change volts to $0^\circ C$. 
1.8 mm GaN HEMT Class A Thermal Considerations

- Models of transistors include a thermal port to check thermal rise as part of nonlinear program and also vary RF modeling parameters as a function of heating
- Note high thermal rise for class a for low input powers
- Let's work in class b and examine properties

Operation under Pulsed Conditions

- Some transistor models have the capability to consider pulsed conditions.
- In the model below, the current source represents the instantaneous power in the transistor.
- The RC represents the thermal time constant of the device.
- The voltage out is the temperature rise above the heat sink.
- So you can run pulsed conditions with specific duty cycles to determine the temperature
Thermal resistance vs time

- Crey device

Effect of Conduction Angle on An’s

An Coefficients Normalized to Imax = 1A  Constant Gm
Normalized Efficiency ($\eta_{\text{NORM}}$), Normalized Power ($P_{\text{NORM}}$), and Normalized Load Conductance ($G_{\text{NORM}}$) Versus Amplifier Conduction Angle - Constant Transconductance - Resistive (R) and Tuned (T) Load

Relative Output Power ($P/P_{\text{norm}}$), and Efficiency ($\eta$) vs Input Power ($p^2$) and Conduction Angle (CA)

- Class A and B linear, Class AB nonlinear
- $\eta$ improved for class AB especially at low drive level ($p$)
Class B Operation - Tuned Load, 78.5% \( \eta \)

Transistor Current (I):

\[ I = I_{\text{min}} + |I_{\text{max}} - I_{\text{min}}| \sum \frac{A}{2\pi} \cos(n \omega t) \]

Class B, \( A_0 = 1 / \pi \), \( A_1 = 0.5 \)

Transistor Voltage Swing:

\[ V_{\text{DC}} - V_{\min} \]

Transistor Current Swing:

\[ I_{\text{max}} - I_{\text{min}} \]

Output Load Current:

\[ 2A_1(I_{\text{max}} - I_{\text{min}}) \]

Adjust load resistance \( R_L \) for full ac swing:

\[ R_L = \frac{V_{\text{max}} - V_{\min}}{2A_1(I_{\text{max}} - I_{\text{min}})} \]

Transistor Voltage:

\[ V_{\text{DC}} = \frac{V_{\text{max}} + V_{\min}}{2} \]

\[ I_{\text{DC}} = \frac{I_{\text{max}} + A_0(I_{\text{max}} - I_{\text{min}})}{2\pi} \]

\[ P_{\text{DC}} = \frac{4(V_{\text{max}} + V_{\min})}{I_{\text{min}} = 0} \]

\[ \eta = \frac{P_{\text{out}}}{P_{\text{DC}}} = \frac{\pi(V_{\text{max}} - V_{\min})}{I_{\min} = 0} \]

1.8 mm GaN HEMT Class B

- Second harmonic short added to circuit for good class b efficiency
- Power same for class a and b
- Efficiency better, \( \eta = \frac{78.5(56.26 - 3.2)}{(56.26+3.2)} = 70\% \)
1.8 mm GaN HEMT Class B

- Gain and phase varying VS Pin for class B
- May need redesign for better linearity

Gain Compression with GaN Devices

- Some GaN HEMTs devices show a soft compression, so in my example I took the performance where I got the Pout
- If the product is used for a constant envelop, then work the PA where the PAE is maximum
- If the PA is used for varying envelop device, then design the semiconductor process and matching techniques for low AM/AM and AM/PM characteristics, and you have a winner
AM to PM of Power Amplifiers

- AM/PM is caused by a nonlinear parameter or temperature parameter changing with input power.
- For example, the transistor has nonlinear capacitors (varactors) which vary depending on the input power to the device.
- Also as the temperature changes (input power), this can cause a phase shift.

Thermal Considerations

- For Class b, current low at low output power.
1.8 mm GaN HEMT Class B Thermal Considerations

- Models of transistors include a thermal port to check thermal rise as part of nonlinear program and also vary RF modeling parameters as a function of heating.
- Temperature rise only 42°C now not 160°C rise.

GaN Transistor Meets Objectives

- High Power
  - High breakdown voltage
  - High peak current, (Saturated velocity)
  - High current capability
- Good efficiency
  - Low knee voltage (Vmin)
  - High Vmax --- High breakdown voltage
  - Can cutoff current at high voltage – low Imin
  - Low semiconductor and circuit losses
- High Reliability
  - High temperature operation
  - High reliability process
  - Low thermal resistance
- Thermal management critical because of the very high power density in a small area and heat must be removed with low thermal resistance.
Class A, B, AB, C, D, E, F, and F^-1 Operation

Constant transconductance, tuned load

\[ \theta \] is angle from origin where current is at \( I_{\text{min}} \)

Conduction angle is \( 2\theta \)

<table>
<thead>
<tr>
<th>Class</th>
<th>Conduction Angle Efficiency</th>
<th>Gain</th>
<th>Linearity</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>360°</td>
<td>50%</td>
<td>High</td>
</tr>
<tr>
<td>AB</td>
<td>180° - 360°</td>
<td>50%  - 78.5%</td>
<td>-3 -6 dB Harmonics</td>
</tr>
<tr>
<td>B</td>
<td>180°</td>
<td>78.5%</td>
<td>-6 dB Harmonics</td>
</tr>
<tr>
<td>C, D, E, F, F^-1</td>
<td>180°</td>
<td>&gt;78.5%</td>
<td>Low Harmonics</td>
</tr>
</tbody>
</table>

Class D, E, F, and F^-1

Class D

Class E

Class F

Class F^-1

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Class D1 (Push-Pull)

- Odd mode balance places virtual short circuit in symmetry plane providing low Z at second harmonic
- Series L-C provides open at harmonics especially important for 3rd and 5th harmonic
- This enhances Vce to look like square wave with value when Icd = 0 and Vce = 0 with current value
- Result: very high efficiency

Power Amplifier Operating Class Summary

<table>
<thead>
<tr>
<th>Operating Class</th>
<th>A</th>
<th>AB</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
<th>D1</th>
<th>F Inverse</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conduction Angle</td>
<td>°</td>
<td>Degrees</td>
<td>360</td>
<td>180 to 360</td>
<td>180</td>
<td>&lt;180</td>
<td>180</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain Reduction To Class A</td>
<td>dB</td>
<td></td>
<td>3</td>
<td>6</td>
<td>8</td>
<td>8</td>
<td>6</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>Ideal Efficiency</td>
<td>η</td>
<td>%</td>
<td>50</td>
<td>65</td>
<td>78</td>
<td>85</td>
<td>100</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>Efficiency Reduction</td>
<td>k</td>
<td>1-Vo/Vcc</td>
<td>1-2Vo/Vcc</td>
<td>See Notes</td>
<td>1-Vo/Vcc</td>
<td>1-Vo/Vcc</td>
<td>1-Vo/Vcc</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Efficiency at Reduced Power</td>
<td>Poor</td>
<td>Good</td>
<td>Very</td>
<td>Good</td>
<td>Poor</td>
<td>Poor</td>
<td>Class D, D1, E, and F need to be driven hard to obtain square wave pulse required for high η</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Frequency</td>
<td>fo</td>
<td>GHz</td>
<td>&lt;100</td>
<td>&lt;20 MHz</td>
<td>Watts</td>
<td>P</td>
<td>&lt;100</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Harmonic Suppression</td>
<td>info</td>
<td></td>
<td>Short 20</td>
<td>Short All n&lt;0</td>
<td>Series LC circuit resonant at fo</td>
<td>Short even n</td>
<td>Open odd n</td>
<td>Open even n</td>
<td>Short odd n</td>
</tr>
<tr>
<td>Peak Transistor Voltage</td>
<td>Vmax</td>
<td>Volts</td>
<td>2Vcc-Vo</td>
<td>Vcc-Vo</td>
<td>3.5Vcc-2.5Vo</td>
<td>2Vcc-Vo</td>
<td>Vn+Vcc</td>
<td>Volts</td>
<td></td>
</tr>
<tr>
<td>Pout/Pin Gain Linearity</td>
<td>Good</td>
<td>Fair</td>
<td>Good</td>
<td>Poor</td>
<td>Poor</td>
<td>(Good with system solution)</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Supply Voltage</td>
<td>Vcc</td>
<td>Volts</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Knee Voltage</td>
<td>Vo</td>
<td>Volts</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

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Conclusions

- We have seen that the GaN HEMT meets theoretical performance limits
- Let's now examine substrates for the GaN HEMT
- Transistor Configurations
  - With and without field plate
- Packaging for high density transistors
- Cree Devices, on 4H-SiC
  - Pout, PAE, Reliability, Thermal Improvements
- Nitronex Devices on high resistivity Silicon

Packaging of High Power Density Transistors

- Package flange material needs to have high thermal conductivity but also have a coefficient of expansion that is close to SiC
- Unfortunately there a limited number of choices to get both right simultaneously!
Properties of Relevant Materials

<table>
<thead>
<tr>
<th>Material</th>
<th>Structure</th>
<th>Thermal Conductivity W/mK</th>
<th>Coefficient of Thermal Expansion ppm/K</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cu</td>
<td>Pure</td>
<td>393</td>
<td>17</td>
</tr>
<tr>
<td>Diamond</td>
<td></td>
<td>1500</td>
<td>1.4</td>
</tr>
<tr>
<td>Silicon</td>
<td></td>
<td>136</td>
<td>4.1</td>
</tr>
<tr>
<td>SiC</td>
<td>4H-Si</td>
<td>430</td>
<td>4</td>
</tr>
<tr>
<td>AlSiC</td>
<td>63%SiC</td>
<td>~175</td>
<td>7.9</td>
</tr>
<tr>
<td>W90Cu</td>
<td>90% W</td>
<td>185</td>
<td>6.5</td>
</tr>
<tr>
<td>W75Cu</td>
<td>75% W</td>
<td>225</td>
<td>9</td>
</tr>
<tr>
<td>Mo75Cu</td>
<td>75% Mo</td>
<td>185</td>
<td>9.1</td>
</tr>
<tr>
<td>Mo50Cu</td>
<td>50% Mo</td>
<td>250</td>
<td>11.5</td>
</tr>
<tr>
<td>CuMoCu</td>
<td>1:4:1</td>
<td>220</td>
<td>6</td>
</tr>
<tr>
<td>CuMoCu</td>
<td>1:1:1</td>
<td>310</td>
<td>8.8</td>
</tr>
<tr>
<td>Cu/Mo70Cu/Cu</td>
<td>1:4:1 laminate</td>
<td>340</td>
<td>8</td>
</tr>
</tbody>
</table>

"GaN-on-SiC MEMT Transistors and MMICs Enter the Mainstream."
Ray Pengelly, Cree RF and Microwave Products
Presented to IEEE AP/MTT Chapter, November 3, 2011

Field plate is connected to source. This reduces the gate to drain capacitance due to field plate insertion.
Double Recess Process to Increase Breakdown Voltage

- Many GaN HEMTs employ a double recess process to increase the breakdown voltage similar to GaAs HEMTs.
- Also many GaN HEMTs employ a field plate similar to many LDMOS transistors.
Thermal Improvements

At the transistor level
- New power transistor layouts to reduce channel temperature at constant power density
  - Parallel gate layout
  - Different layout provides 20% reduction in operating temperature

At the package level
- New flange materials with higher thermal conductivity and CTE match to SiC
- Present CuW is ~200 W/mK
- Super-CMC is 350 W/mK

- Aluminum diamond is 600 W/mK
- \( T_0 \) decreases by 10%
- \( T_0 \) decreases by turnover 12%

Cree GaN devices are the most reliable in the industry

"GaN-on-SiC MEMT Transistors and MMICs Enter the Mainstream,"
Ray Pengelly, Cree RF and Microwave Products
Presented to IEEE AP/MTT Chapter, November 3, 2011
The AlGaN/GaN HEMT structure results higher current and mobility compared to a FET structure.

The field plate improves the breakdown voltage.

Metal organic chemical vapor deposition (MOCVD) is the preferred method of producing GaN-based thin films on Si or SiC for RF applications.

GaN-based devices and structures have been mass-produced using MOCVD for lighting applications and the same supporting high volume epitaxial manufacturing infrastructure can be leveraged for RF applications.
GaN HEMT Devices Nitronex

- Can operate at 180°C with MTBF of 10^6

Nitronex GaN on Si HEMT Device

NPTB00004 Datasheet

Gallium Nitride 28V, 5W RF Power Transistor

Built using the SIGANTM NRF1 process - A proprietary GaN-on-Silicon technology

FEATURES
- Optimized for CW, pulsed, WiMAX, Wi-CDMA, LTE, and other applications from DC to 5GHz
- 100% RF Tested at 2500MHz
- 5W P1dB CW Power
- 15.5dB Power Gain
- Low-cost surface mount SOIC package
- High reliability gold metallization process
- Lead-free and RoHS compliant
- Subject to EAR99 Export Control

RF Specifications (CW): VDS = 28V, ID = 50mA, Frequency = 2500MHz, TC = 25°C, Measured in Nitronex Test Fixture

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Typ</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1dB</td>
<td>Average Output Power at 3dB Compression</td>
<td>5.1</td>
<td>W</td>
</tr>
<tr>
<td>P1dB</td>
<td>Average Output Power at 1dB Compression</td>
<td>2.9</td>
<td>W</td>
</tr>
<tr>
<td>η</td>
<td>Drain Efficiency at 3dB Compression</td>
<td>56</td>
<td>%</td>
</tr>
</tbody>
</table>
GaN HEMT Structures Higher Frequencies

BAE Non Field Plate 0.2 μm Gate MMIC Process

- $f_t = 50$ GHz, $f_{max} = 220$ GHz, 5W/mm, 46% PAE at 30 GHz

"High Efficiency Ka/Q Band PHEMT Power Amplifier MMICs" Dr. James J. Komiak, BAE Systems, IMS2011 Workshop
HRL’s Baseline T Gate Structure

Characteristics of HRL’s Baseline T-Gate Process

- State of the art GaN device technology
  - Double Heterojunction Structure (DHFET)
    - Improves electron confinement
    - Alleviates short channel effects
  - T-gate device
    - $L_g \approx 0.15 \, \mu m$, S/D spacing $\approx 1.7 \, \mu m$
    - Drain voltage range: 1V to 14V (Breakdown $\approx 40V$)
  - Low Ohmic contact resistance and access resistance
    - Low $\text{Ron} < 1.6 \, \text{ohm-mm}$
  - High $f_t$ and $f_{\text{max}}$, low $\text{Fmin}$
    - $f_t$ of 90 GHz
    - $f_{\text{max}}$ of $\approx 190 \, \text{GHz}$ (at $V_{\text{ds}}=10V$)
    - $\text{Fmin}$ of $< 1.6 \, \text{dB}$ at 26 GHz (at $V_{\text{ds}}=5V$)

“GaN T-Gate and Field Plate Technology for Applications Below 45 GHz” Harris Moyer, HRL Laboratories, IMS2011 Workshop, “Introduction to GaN MMIC Design”
HRL’s Baseline T Gate Structure

GaN HFET with Lateral-scaling, BV> 100V

- 25% reduction in $R_{on}$
- > 20% increase in $I_{max}$
- Keep Breakdown voltage high
- $g_m$ and $f_t$ improved by ~20%
- $f_t = 55 – 60$ GHz
- Gain (35GHz) = 12.5 dB

“GaN T-Gate and Field Plate Technology for Applications Below 45 GHz” Harris Moyer, HRL, IMS2011 Workshop, “Introduction to GaN MMIC Design”

E-Band Test Fixture with HRL MMIC

Power & PAE Measurements at 74 GHz

- GaN MMIC
- 3-Stages
- 600um Output Gate
- $P_{out} = \sim 1W$
- Gain = 20 dB

Presentation: IMS2011 Workshop WMA, Q/V-Band Linear Power Amplifiers using Envelope Tracking and Digital Pre-distortion James Schellenberg, QuinStar Technology, Inc., Contributors: Bumjin Kim, Jonmei Yan*, Donald Kimball** University of California, San Diego, CA, USA 92093
Millimeter Wave Results

This Work
Dual-Gate GaN MMICs for Mm-Wave Operation
IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS, VOL. 21, NO. 2, FEBRUARY 2011, pp. 95-97


New Epitaxial Material for GaN

- Less Strain using In_{0.17}Al_{0.83}N on GaN compared to existing AlGaN on GaN
- Higher Reliability, Higher Power, Less short channel effects meaning can use shorter gate lengths for higher frequency operation

Predicted $N_s$

$E_g$ (eV) vs. Lattice constant (Å)

© 2014 Niehenke Consulting Inc.
\( \text{IN}_{0.17}\text{Al}_{0.83}\text{N on GaN} \)

- InAlN/GaN heterojunction structures offer several potential advantages over AlGaN/GaN. These include:
  1. Improved lattice matched structure with much reduced lattice stress.
  2. Higher reliability and robustness due to the improved lattice match.
  3. Higher output current and current density and thus higher output power where the breakdown condition is preserved.
  4. Potentially higher chemical and thermal stability due to the higher temperature the structure can withstand.
  5. Potentially improved control of surface instabilities.
  6. Thinner barrier and shorter gate structures which will lead to higher power performance at higher frequencies into the millimeter range.

Addressed in IMS2013 Workshop WMA: Advancements in InAlN/GaN Device and Microwave/MMW Circuit Technology.

---

**Design a 30 W (P1dB) PA using the Crey CGH35030F GaN HEMT at 1.9 GHz**

Cree's CGH35030F is a gallium nitride (GaN) high electron mobility transistor (HEMT) designed specifically for high efficiency, high gain and wide bandwidth capabilities, which makes the CGH35030F ideal for 3.3-3.5GHz WiMAX and BIS amplifier applications. The transistor is supplied in a ceramic/metal range package.

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>High</th>
<th>Min.</th>
<th>Typ.</th>
<th>Min.</th>
<th>Units</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate Threshold Voltage</td>
<td>1.2</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>V</td>
<td>HBM</td>
</tr>
<tr>
<td>Source-Drain Voltage</td>
<td>38</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>mA</td>
<td>HBM, TM</td>
</tr>
<tr>
<td>Source-Drain Current</td>
<td>5.0</td>
<td>1.0</td>
<td>1.0</td>
<td>1.0</td>
<td>mA</td>
<td>HBM, TM</td>
</tr>
<tr>
<td>Source-Source Breakdown Voltage</td>
<td>107</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>V</td>
<td>HBM, TM</td>
</tr>
</tbody>
</table>

Operate at 28 Vds and design for Class a and Class b.
Stability

- For stable operation, $k > 1$
- Amplifier unstable

For stable operation, no circles in Smith chart.
Stabilization

Add Series Resistance

Add Shunt Resistance

Stabilization

Add Series or Shunt Resistance
AWR Schematic Class A
Stability achieved by placing a series resistor and a parallel resistor on the input

Resource = 6.5 Ω
Rin = 5Ω
Pin = 29.5 dBm
Cin = 0 pF
Rload = 15 Ω

Unconditionally Stable (K>1)
Unconditionally Stable

Load Line
Vgs = -1.17 V, RL = 15 Ω. Pin = 34.2 dBm
AWR Current Voltage Class A

Pout @ P1dB = 31.6 W
PAE = 50.37%
Low AM/AM and AM/PM

Output Match

- Output needs to see 15 Ω

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Input Match

- 0.13 +j0.02 to 1

Match Input and Output with Low Pass Matching Circuits
Gate Current and Reliability

- High gate current leads to metal migration which can open circuit the gate. With GaAs devices, the rule of thumb is not to exceed 1 ma per mm of gate periphery.
- So under normal operation the gate current is low, but when driven with higher power than normal, gate current is experienced.
- One way to reduce gate current with higher powers is to place a resistor in the DC portion of the gate bias circuitry.
- Many times the manufacturer will suggest a gate resistor for their device.
- The metal migration process does not happen immediately, and it takes time to develop.
- Always monitor the gate current for your PA design.
- As a precaution, do not overdrive the PA, an place a resistor in the gate dc portion of the DC bias circuit.

Example

- $R_{gate} = 0$ Ohms
Example

- **Rgate = 50 Ohms**

![Graph showing the relationship between output power (Pout), gain (Gain), and power added efficiency (PAE) for various input power levels, with the curve for Rgate=50 Ohms highlighted.](image)

- **Rgate = 100 Ohms**

![Graph showing the relationship between output power (Pout), gain (Gain), and power added efficiency (PAE) for various input power levels, with the curve for Rgate=100 Ohms highlighted.](image)
**Example**

- **Rgate = 1K**

**Conclusion**

- For this transistor, the Pout at P1dB does not change for gate resistors 1 to 1000 Ohms.
- The gate current starts at 4 dB above the P1dB point. So do not operate the transistor here.
- Operating the transistor there does not make sense, because this is past the peak PAE point.
- Adding 1K helps tremendously should one by accident overdrive the PA 4 dB or more above the P1dB point.
At P1dB, Second Harmonic down 17.3 dB and third down 23.2 dB
Second Harmonics follow 2dB/dB
Third Harmonic follows 3dB/dB

Input Matched
Note Zin changes with input power a cause of AM/PM
Pdc = 49.2 W for low RF Input Power

\[ P_{dc} = 49.2 \text{ W with low RF input} \]

\[ T = 25 + 171 = 196 \degree \text{C for low RF input power} \]
Investigate Working at Class B

- Better PAE
- Similar power
- Lower temperature for low input powers
- Better PAE at lower power compared to Class a
- However Class B has a gain and phase variation versus input power so design will sacrifice on Pout with digitally modulated signals with varying input amplitude envelop as experienced with modern digitally modulated signals like WCDMA, LTE, and WIMAX.

Use Tuner for Optimization

Optimum values for
Good Pout@P1dB
PAE and Low
AM/AM and AM/PM

Mag1=0.612
Ang1=157.4
Mag2=1
Ang2=141.8
Mag3=0
Ang3=-90
Translate the Impedances into a Circuit

Model

Circuit Representation

Second Harmonic Short

Matching at Second Harmonic

- First we will design the second harmonic circuit close to the transistor
- It want to see a $\Gamma = 1\angle 141.8^\circ$

$Mag_2 = 1$
$Ang_2 = 141.8$

50 $\Omega$ Line 19.1$^\circ$ Long

Short
Matching at Second Harmonic

- First we will design the second harmonic circuit close to the transistor.
- It wants to see a \( \Gamma = 1@141.8^\circ \).
- Add a 50 ohm line 19.1 ohm long and terminate it with a short and you have the circuit as seen by the transistor.
- This is 9.55 ohm long at the fundamental.
Matching at Fundamental

- Now work at fundamental with the second harmonic circuit installed

\[
\begin{align*}
\text{Mag1} &= 0.612 \\
\text{Ang1} &= 157.4 \\
\end{align*}
\]

Transistor

\[
\Gamma = 0.612@157.4^0
\]

50 Ω 9.55° line

23 Ω 90° line

Results \( P_{out} = 20 \, \text{W @P1dB}, \, \text{PAE} = 72\%, \, 11.9 \, \text{dB SS Gain} \)
Match 5.5 Ohm Input

Results $P_{out} = 20\, W\, @P_{1dB}$, $PAE = 72\%$, 11.9 dB SS Gain
Low temp rise 35°C, DC current rises with $P_{in}$
Results $P_{out} = 20\, W$ @$P_{1\text{dB}}$, $PAE = 72\%$, 11.9 dB SS Gain
Low temp rise 35°C, DC current rises with $P_{in}$
Unconditionally stable, Input Matched, however AM/AM & AM/PM variation
Results: Pout = 20 W @P1dB, PAE = 72%, 11.9 dB SS Gain
Low temp rise 35°C, DC current rises with Pin
Unconditionally stable, Input Matched, Low AM/AM & AM/PM,
Low Harmonics

Summarization of AM/AM and AM/PM for Class A and B

- **Class A**
  - Pout = 20 W @P1dB
  - PAE = 51%
  - 14 dB SS Gain

- **Class B**
  - Pout = 20 W @P1dB
  - PAE = 72%
  - 11.9 dB SS Gain
Summarization of AM/AM and AM/PM for Class A and B
- Class A: Phase flat then phase increases rapidly with increasing power past around P1dB
- Class B: phase not flat with increasing power because dc average current constantly changing with increasing power. Phase increases slightly with increasing power then decreases slightly around P1dB.

Modeling GaN HEMT, GaN Nuances
- Trapping effects and associated current-knee collapse: Increases knee voltage at which electron velocity occurs
- Bias dependencies:
  - Source resistance and drain to source resistance important
- Sub threshold valid modeling important for designers for Class B, C, D, E, and F high efficiency operating modes since not all models can fit behavior in this region. Curtice FET (CFET) model is well behaved in this region
- Models should be checked for gate voltages at or below threshold, if this is important
- Electrothermal modeling important for high voltage-current products
- Measurements must use pulsed IV characteristics

Modeling GaN HEMT

- As GaN technology has developed, first in research laboratories and more recently in multiple commercial device manufacturers, the demand for improved nonlinear models has grown alongside the device process improvements.
- The need for improved models for GaN is twofold:
  - First, GaN devices have unique nuances in behavior to be addressed
  - Second, there is a desire for improved accuracy to take full advantage of the performance wins to be gained by GaN HEMT performance in the areas of high efficiency and high-power operation.

Pulsed IV measurements are required

Comparison of pulsed I–V (solid lines without symbols) and static I–V for a GaN HEMT. Pulse conditions were 0.2 ms pulse width and 1-ms separation with quiescent bias set at Vdsq 5 0, Vgsq 5 0. Vgs is varied from 25 to 21 V in 1 V steps.

Modeling GaN HEMT
Pulsed IV Measurements Important for accurate modeling

Pulsed S-parameter and static S-parameter comparison for a 10 W GaN HEMT. Pulse conditions: 5 ms pulse width, 0.1% duty cycle (IF BW 5 1/pulse width 5 ,200 kHz).


Cree CGH3503F_r6 Device
IV Curves with and Without Self Heating

Self Heating Turned Off in Model    Self Heating Turned ON

Electrothermal model feature essential for accurate design
Measurements for Modeling GaN HEMT
Main considerations for non-linear (NL) Empirical transistor models

- Overall measurement accuracy
  - Correct calibration
  - Repeatability
  - De-embedding model
  - Pulsed IV

- Suitability of model
  - equation set (model template) limitations/intent
  - physically meaningful parameters?

- Model testing/validations
  - Conventional - general
  - Advanced – application specific

IMS2011 WMJ Workshop: Modeling Considerations for GaN HEMT and Higher Level IC Devices, Dr. Larry Dunleavy, Dr. Jiang Liu, Modelithics, Inc.

Modeling GaN HEMT
Nonlinear transistor modeling process

Modeling GaN HEMT
Comparison of example FET models used for GaAs, silicon, and GaN FET/HEMT devices.

<table>
<thead>
<tr>
<th>FET Models</th>
<th>Approx. Number of Parameters</th>
<th>Electrothermal Model</th>
<th>Geometry Scalability Built-In</th>
<th>Original Device Context</th>
</tr>
</thead>
<tbody>
<tr>
<td>Curtice3 [12]</td>
<td>59</td>
<td>No</td>
<td>No</td>
<td>GaAs MESFET</td>
</tr>
<tr>
<td>Motorola</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Electrothermal (MET) [25]</td>
<td>62</td>
<td>Yes</td>
<td>Yes</td>
<td>LD MOSFET</td>
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<tr>
<td>CMC (Curtice/Modelithics/Cree) [26]</td>
<td>55</td>
<td>Yes</td>
<td>Yes</td>
<td>LD MOSFET</td>
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<tr>
<td>BSIMSO3 [24]</td>
<td>191</td>
<td>Yes</td>
<td>Yes</td>
<td>SOI MOSFET</td>
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<tr>
<td>CFET [5]</td>
<td>48</td>
<td>Yes</td>
<td>Yes</td>
<td>HEMT</td>
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<tr>
<td>EHEMT [13]</td>
<td>71</td>
<td>No</td>
<td>Yes</td>
<td>HEMT</td>
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<tr>
<td>Angelov [14]</td>
<td>80</td>
<td>Yes</td>
<td>No</td>
<td>HEMT/ MESFET</td>
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<tr>
<td>Angelov GaN [11]</td>
<td>90</td>
<td>Yes</td>
<td>No</td>
<td>HEMT</td>
</tr>
<tr>
<td>Aurega [4]</td>
<td>100</td>
<td>Yes</td>
<td>Yes</td>
<td>HEMT</td>
</tr>
<tr>
<td>Cree (Modified Fager - Statz)</td>
<td>18+</td>
<td>Yes</td>
<td>Yes</td>
<td>HEMT</td>
</tr>
</tbody>
</table>


Electrothermal Models


Modeling GaN HEMT
Topology for the Angelov GaN HEMT model

The electrothermal model elements $R_{therm}$ and $C_{therm}$ enable estimation of channel temperature rise due to power dissipation and vary model parameters to account for temperature rise.

Millimeter Wave MMIC Foundries

<table>
<thead>
<tr>
<th>Foundry</th>
<th>Device Technology</th>
<th>Wafer Dia. (in.)</th>
<th>Power Figure of Merit</th>
<th>Max Frequency</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>HRL</td>
<td>0.15 μm GaN HEMT, on 50 μm SiC</td>
<td>3</td>
<td>0.84W Pout, 14.7% PAE, 1.4W/mm</td>
<td>88 GHz</td>
<td>Owned by Boeing and GM</td>
</tr>
<tr>
<td>Northrop Grumman</td>
<td>0.2 μm GaN HEMT on 100 μm SiC</td>
<td>3</td>
<td>1.13W Pout, 23.3% PAE, 3.96W/mm @38V</td>
<td>55 GHz</td>
<td>Captive Foundry</td>
</tr>
<tr>
<td>Raytheon</td>
<td>GaN HEMT 8C</td>
<td>4</td>
<td></td>
<td>W-band, 17V</td>
<td>Captive Foundry</td>
</tr>
<tr>
<td>TriQuint</td>
<td>0.25μm GaN HEMT on 100 μm SiC</td>
<td>3</td>
<td>5.7W/mm</td>
<td>18 GHz</td>
<td>Independent Foundry</td>
</tr>
<tr>
<td></td>
<td>0.15μm GaN HEMT</td>
<td>-</td>
<td>2.5W/mm</td>
<td>35 GHz</td>
<td>R&amp;D results</td>
</tr>
</tbody>
</table>

BAE 0.2mm Non field Plate HEMT, ft = 50 GHz, fmax = 220 GHz, 5W/mm, 46% PAE at 30 GHz

10W WIMAX PA Design

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10W WIMAX PA Design

- Transistor:
  - Eudyna 10W GaN HEMT amplifier, EGN010MK
  - Vds = 50V
  - Ids = 100 ma (no RF power) deep class b

- Frequency range: 3.4 to 3.8 GHz
- Design objectives: (at P1.5 dB)
  - Power > 41 dBm
  - PAE > 70%
  - η > 80%
  - G > 8.5 dB
  - Stable 0.1 to 10 GHz
  - Input return loss > 15 dB

PA Design Steps

- Step 1:
  - Examine IV Curves and note knee voltage (one point on load line) and no current point at Vgs = 95 V
  - Note input dc voltage for no gate current
  - Determine Vgs for 100 ma of current
  - AWR circuit GaN HEMT WIMAX PA Step1

- Step 2:
  - Examine Load Pull data and determine optimum load for max power at Pin = 30 dBm
  - Determine circuit using transmission line. Hint try a length of line of length theta and impedance Zmatch
  - Examine Pout vs Pin and Pout vs freq at Pin = 30 dBm
  - Optimize circuit for operation over full frequency
  - AWR circuit GaN HEMT WIMAX PA Step2
PA Design Steps

- **Step 3:**
  - Match input at Pin = 30 dBm over frequency. Need to use a 10 degree 50 Ω length of line on input in order to solder input transistor lead
  - Suggestion: try a shunt cap and series which will also serve as an input blocking cap
  - Examine circuit stability (k, MU2, input stability plane)
  - AWR circuit GaN HEMT WIMAX PA Step3

- **Step 4:**
  - Now examine stability (k factor and MU2 as well as input stability plane) and completely stabilize circuit with minimal degradation of gain and rematch input circuit. This is the hardest step
  - AWR circuit GaN HEMT WIMAX PA Step5
  - Suggestion: See schematic next page
  - Try to keep Rsh equal to or greater than 200 Ω so that gain is not severely reduced
  - AWR circuit GaN HEMT WIMAX PA Step4

---

**Suggested Circuit Schematic for Stability**

![Circuit Diagram](image)
Results: Step 1

Load Line

50 V
101.2 mA

Gate Current

Gate Current
Results: Step 2

- Optimize circuit for $P_{out} > 43$ dBm, $PAE > 80\%$ with $Pin = 30$ dBm and $f = 3.5$ GHz

<table>
<thead>
<tr>
<th>Frequency (GHz)</th>
<th>$DB(Re/Recom)$</th>
<th>$DR/Gain$</th>
<th>$PAE(PORT_{-1})$</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.5</td>
<td>42.101</td>
<td>12.101</td>
<td>83.812</td>
</tr>
</tbody>
</table>
Results: Step 2

- Review parameters versus Pin

![Graph showing output matched PA swept parameters with various data points at different power levels.](image)

Results: Step 2

- Optimize over frequency: 3.4 to 3.8 GHz

![Graph showing output matched frequency sweep across 3.4 to 3.8 GHz with various data points demonstrating the optimization.](image)
Results: Step 3 Input Match

- Unmatched
- Matched

Results: Step 3 Unstabilized Stability
Results: Step 3 Unstabilized Stability

Results: Step 4 Stabilized Stability
Results: Step 4 Stabilized Stability

Results: Step 4 : Input Match
Results: Step 4: Power Sweep

Matched PA Swept Parameters

Results: Step 4: Frequency Sweep Pin = 33 dBm
Doherty Amplifier Design

- Main Amp Class AB, Aux amp Class C
- At -6dB for high power, aux amp turned off
- Each amp changes load that each sees resulting in better efficiency and linear power
Design Doherty PA Using 10W WIMAX PA

AWR Balanced PA for Comparison

PORT_PS1
P=1
Z=50 Ohm
PSMin=6 dBm
PSMax=38 dBm
PSStep=3 dB

SUBCKT
ID=S1
NET="Main PA"

QHYB
ID=U1
R=50 Ohm
COUPL=3 dB
LOSS=0 dB

RES
ID=R1
R=50 Ohm

TUN
ID=T1
25-50 Ohm
EL=90 Deg
F0=3.5 GHz

PORT
P=2
Z=50 Ohm

TUN
ID=T2
25-50 Ohm
EL=90 Deg
F0=3.5 GHz

QHYB
ID=U2
R=50 Ohm
COUPL=3 dB
LOSS=0 dB

RES
ID=R2
R=50 Ohm

SUBCKT
ID=S2
NET="Aux PA"

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Design Doherty PA Using 10W WIMAX PA

- \( \phi \) length set to 43° for high output Reflection Coefficient (\( \Gamma \)) Aux PA when turned off

Performance the same for both circuits with equal gate biases for each PA
Design Doherty PA Using 10W WIMAX PA

- Examine DC Current of Aux PA and adjust so that at 6 dB down the Transistor DC current is zero so the aux PA should be turned off.

![Graph showing AUX PA DC Current with 6 dB marker.](image)
Design Doherty PA Using 10W WIMAX PA

- Performance enhanced with similar PA output with significant enhancement of PAE
- Suspect there is a problem with nonlinear model operating in deep class C
- The exercise does show technique and better performance but not that of theoretical performance (Same PAE at 6 dB backoff)

Conclusions

- GaN HEMT for power amplifiers
  - High breakdown voltages with Vds dc operation at 28 to 50 V depending on manufacturer
  - How power in a small footprint requiring care to get the heat out
  - High reliability operation MTBF $10^6$ to $10^8$
  - More easily matched due to high voltage operation and small equivalent capacitances and high bandwidth operation
  - Design techniques shown for class a and class b operation
  - Design techniques shown for digitally modulated signals as well as Dougherty PA operation