GaN Transistors for Efficient Power Conversion (and RF)

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Agenda

• How GaN works and the state-of-the-art
  — Reliability
  — Radiation Tolerance
• Design Basics
• Design Examples
• GaN Integration
• Thermal Characteristics
• What is in the future?
Power Switch Wish List

- Lower On-Resistance
- Faster
  - Less Capacitance
  - Less Inductance
- Smaller
- Lower Cost

Material Comparison

<table>
<thead>
<tr>
<th>Parameter</th>
<th>GaN</th>
<th>Silicon</th>
<th>SiC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Band Gap $E_g$ (eV)</td>
<td>3.2</td>
<td>1.12</td>
<td>3.4</td>
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<td>Breakdown Field $E_{BV}$ (MV/cm)</td>
<td>3.3</td>
<td>0.3</td>
<td>3.5</td>
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<tr>
<td>Electron Mobility $\mu_n$ (cm$^2$/V·s)</td>
<td>2000</td>
<td>1500</td>
<td>650</td>
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</table>
State of the Art: Fundamentally Material Superiority

- GaN has a 10x advantage in critical electric field.
  - For a given breakdown voltage, GaN terminals can be one tenth the distance apart compared with Silicon.
- GaN has a 50x advantage in resistivity.
  - For a given geometry, GaN resistance will be one 50th of that of Silicon.
- GaN has a 500x theoretical material advantage over Silicon.

GaN (R/500)

Product Matrix

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Configuration</th>
<th>V_{DS} Max</th>
<th>V_{GS} Max</th>
<th>R_{DS(on)} @5VGS (mΩ)</th>
<th>Q\text{G typ} (nC)</th>
<th>Q\text{GS typ} (nC)</th>
<th>Q\text{GD typ} (nC)</th>
<th>Q\text{OSS typ} (nC)</th>
<th>I_D (A) Pulsed</th>
<th>LGA Package (mm)</th>
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<tr>
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<td>Dual Asymmetric</td>
<td>30</td>
<td>6</td>
<td>6</td>
<td>3.5</td>
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EPC - The Leader in GaN Technology | February, 2014 | www.epc-co.com
**eGaN FET Structure**

- Silicon Substrate
  - Low cost starting material
  - Standard CMOS (0.35 µm) wafer processing
  - Isolation Layer allows integration
  - Enhancement mode for power conversion applications

- Simple Structure for low mask count
- Very low capacitance for a given Voltage and $R_{DS(on)}$ compared with MOSFET technology
- Zero $Q_{RR}$

**Package Wish List**

- Low parasitic resistance
- Low parasitic inductance
- Low thermal resistance
- Small size
- Low cost
- Isolated from environment
**Wafer Level Packaging**

- Low inductance give fast current commutation and low noise
- Minimal footprint on PCB
- Thermally efficient, dual sided cooling
- MSL 1 rated and RoHS 6/6

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**Size Comparison – 200 V**

- eGaN FET
  - 5.76 mm²
  - 25 mΩ maximum
- D-PAK
  - 65.3 mm²

[Drawn To Scale]
Predicting Reliability

Drain-Source Reliability

MTTF vs. $V_{DS}$ and Temperature

FIT Rate vs. $V_{DS}$ and Temperature
Gate Reliability

MTTF vs. $V_{GS}$

FIT Rate vs. $V_{GS}$

Radiation Capability
> 1 MRad Gamma Radiation Stability

Negative voltage gate drive is not needed

> 1E15 Neutron Stability

eGaN technology is tolerant to Neutron Radiation
Single Event Stability

Negative voltage gate drive is not needed

Au at ~85.4 LET
Hard Switching Buck Converter
Low Voltage Buck Converter

VIN=12 V VOUT=1.2 V

EPC2015 + EPC2023
EPC2015 + EPC2015
30 V MOSFET Module

\[ f_{sw}=0.5 \text{ MHz} \]
\[ f_{sw}=1 \text{ MHz} \]

Higher Voltage Buck Converter

VIN=48 V VOUT=12 V

EPC2001 + EPC2001
EPC2001 + EPC2021
80V MOSFET

\[ f_{sw}=300 \text{ kHz} \]
\[ f_{sw}=500 \text{ kHz} \]
EPC9107 Demonstration Board

Switching Node Voltage

\[ V_{\text{IN}} = 28 \text{ V}, \quad I_{\text{OUT}} = 15 \text{ A} \]

Vin=12-28 V  VOUT=3.3 V
IOUT=15 A  fsw=1 MHz
2 x EPC2015

~3V overshoot @ 15 A\text{OUT}  \quad V_{\text{IN}} = 28 \text{ V}

~1.1ns rise time @ 15 A

5 V/ div

20ns

eGaN Eighth-brick Target Specifications

- Eighth-brick integrated bus converter
  - Fully regulated
  - Isolated
  - 500 W output at 12V
  - 52 V nominal input (4:1 transformer)
  - > 96% efficient
  - DOSA-compliant footprint
  - Off the shelf parts

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Board Images

TOP and Bottom views

Thermal Images @ 400W
Waveforms @ 500W

Preliminary Efficiency and Power Loss
Resonant Bus Converter

High Frequency DC/DC Transformer


ZVS Switching Comparison

TZVS = 42 ns  eGaN FET VDS
TZVS = 87 ns  MOSFET VGS
TZVS = 42 ns  MOSFET VDS
TZVS = 87 ns  eGaN FET VGS

fsw = 1.2 MHz, Vin = 48 V, and Vout ≈ 12 V
Duty Cycle Comparison

\[ f_{sw} = 1.2 \text{ MHz}, \ V_{IN} = 48 \text{ V}, \text{ and } V_{OUT} \approx 12 \text{ V} \]

Efficiency Comparison

\[ f_{sw} = 1.2 \text{ MHz}, \ V_{IN} = 48 \text{ V}, \text{ and } V_{OUT} \approx 12 \text{ V} \]
• Envelope Tracking can **double** base station efficiency.
• n-Stat forecasts that there will be 160.3 million active small cells, and the retail value of small cell shipments will reach $14B by 2015.

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**Envelope Tracking Supply**

- ET power supply topologies vary
  - Open loop boost – full BW required
  - Closed loop linear-assisted Buck*

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*B. Yousefzadeh, et. Al. Efficiency optimization in linear-assisted switching power converters for envelope tracking in RF power amplifiers, ISCAS 2005*
Envelope Tracking

![Graph showing the relationship between gate-to-source voltage (Vgs) and gate charge (Qg) for EPC8004 and EPC2014 eGaN FETs.](image)

- **EPC8004 eGaN FET**
- **EPC2014 eGaN FET**

Envelope Tracking

![Graph showing efficiency and power loss for EPC8005 under 42 V in to 20 V out, 10 MHz conditions.](image)

- **42 V in to 20 V out, 10 MHz**
- **Efficiency**
- **Power Loss (W)**
- **Output power (W)**

- Efficiency:
  - 95%
  - 93%
  - 91%
  - 89%
  - 87%
  - 85%
  - 83%
  - 81%
  - 79%
  - 77%
  - 75%
  - 73%
  - 71%

- Power Loss (W):
  - 6
  - 5
  - 4
  - 3
  - 2
  - 1
  - 0

- Output power (W):
  - 40
  - 30
  - 20
  - 10
  - 0

EPC - The Leader in GaN Technology | February, 2014 | www.epc-co.com
Envelope Tracking

![Graph showing efficiency and power loss for 42 V in to 20 V out, 10 MHz, with and without improved driver.]

Wireless Power

The global wireless charging market is estimated to grow to $10B by 2018, a CAGR of 42.6%.
Class-E Schematic

Output power decreases with increasing load impedance above design point

ZVS Class-D Schematic

Output power increases with increasing load impedance
### Topology Comparison

**Peak Performance**

![Graph showing efficiency and output power for different models of EPC GaN technology. The graph compares EPC8009 ZVS-CD, EPC2012 SE-CE, EPC2014 VM-CD, and EPC2016 CM-CD. The DC load is 23.6 Ω.]

- **Output Power [W]**
- **Efficiency [%]**
- **DC in to DC out, including Gate power**

- EPC8009 ZVS-CD
- EPC2012 SE-CE
- EPC2014 VM-CD
- EPC2016 CM-CD

### Topology Comparison

**Load Variation**

![Graph showing efficiency and output power variation with DC load resistance for different models of EPC GaN technology. The graph compares efficiency and output power across different models.]

- **DC Load Resistance [Ω]**
- **Efficiency [%]**
- **Output [W]**

- η EPC8009 ZVS-CD
- η EPC2012 SE-CE
- η EPC2016 CM-CD

**Fixed Supply voltage**
Topology Comparison
Load Regulation

Class-D Audio
Why eGaN FETs in Class-D Audio

- Low $R_{DS(on)}$ & Low $C_{OSS}$
  - High Efficiency
  - High Damping Factor = Low open loop output Impedance = **Low T-IMD**

- Fast Switching & No Reverse Recovery ($Q_{rr}$)
  - High output linearity, Low Cross-over Distortion = **Low THD**

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eGaN FET Class-D Audio Amplifier

- Bridge-Tied-Load (BTL)
- EPC2016 with LM5113

EPC FET Power Stage:
250 W into 4 Ω at 440 kHz without a heatsink
### Other Key Applications

- LiDAR
- High Resolution MRI Imaging
- Network and Server Power Supplies
- AC Adapters
- Class-D Audio
- Energy Efficient Lighting
- Robotics

### Design Basics
Low $V_{GS(on)}$ Overhead

$V_{GS(Max)} = 6 \, \text{V}$

eGaN FET Drive Requirements

To avoid overshoot:

$$R_G \geq \sqrt{\frac{4(L_G + L_S)}{C_{GS}}}$$

- Minimize gate loop inductance
- Separate source and sink transistors allowing for separate drive paths
- Wandering gate drive return has been issue
Minimizing Overshoot

V_{GS} eGaN FET

2 V/ div 80 ns/ div

Minimizing Overshoot

V_{GS} eGaN FET

1 V/ div 20 ns/ div
eGaN FET Driver IC

- Bootstrap clamp limits (HS) supply
- Separate inputs allow accurate, dead-time management
- Optimized drive impedance
- Synchronous bootstrap rectifier eliminates this need

Reference: Texas Instruments, "Gate Drivers for Enhancement Mode GaN Power FETs 100 V Half-Bridge and Low-Side Drivers Enable Greater Efficiency, Power Density, and Simplicity," SNVB001

Layout
### LGA has very low inductance

<table>
<thead>
<tr>
<th>Control</th>
<th>LS</th>
<th>L_LOOP</th>
<th>L</th>
<th>Gate Return</th>
<th>Source Return</th>
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<tbody>
<tr>
<td>Driver</td>
<td>Rectifier</td>
<td>C_out</td>
<td></td>
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</tbody>
</table>

- Source Inductance common to the gate drive and control loops, $L_S$, slows current commutation by reducing effective gate drive during $di/dt$.
- High Frequency Loop Inductance causes increased losses, high peak voltage and increased ringing.
- LGA Package has low common source inductance and enables low high frequency loop inductance.

### Half Bridge Layout Options

- **Horizontal**
- **Vertical**
- **Optimal**
**Layout Impact on Efficiency**

**Measured Efficiency**

- **EPC Optimal Layout**

V\textsubscript{IN}=12 V, V\textsubscript{OUT}=1.2 V, f\textsubscript{sw}=1 MHz, L=300 nH

**Layout Impact on Peak Voltage**

- **L\textsubscript{Loop} ≈ 1.0 nH**
  - 70% Overshoot

- **L\textsubscript{Loop} ≈ 0.4 nH**
  - 30% Overshoot

Switching Node Voltage

V\textsubscript{IN}=12 V V\textsubscript{OUT}=1.2 V I\textsubscript{OUT}=20 A
f\textsubscript{sw}=1 MHz L=150 nH
eGaN FET vs. MOSFET

Si MOSFET

eGaN FET

V_{\text{in}}=12 \text{ V} \quad V_{\text{out}}=1.2 \text{ V} \quad I_{\text{out}}=20 \text{ A} \quad f_{\text{sw}}=1 \text{ MHz} \quad L=300 \text{ nH} \quad \text{eGaN FET}

Optimal Layout Implementation

C_{\text{IN}} \quad U_2 \quad Q_1 \quad Q_2

www.epc-co.com
• Fine pitched LGA requires careful footprint and solder mask design.
  – Please see detail in:

Paralleling High-Speed eGaN FETs
Parallel Power Devices

- eGaN FETs have a positive temperature coefficient over most of the operating range
  - Current distributes over die area in hot swap and solid state circuit breaker applications
  - Parallel devices share in both constant current and on state regions
Parallel Layout Performance

**Efficiency (%)**

- **Conventional Single Power Loop Design**
- **Proposed Four Distributed Power Loops Design**

**Output Current (A)**

- 2
- 6
- 10
- 14
- 18
- 22
- 26
- 30
- 34
- 38
- 42

**Vin=48 V Vout=12 V fsw=300 kHz L=3.3 µH GaN FET T/SR: 4x100 V EPC2001**
**4 Layer 2 oz PCB**

Parallel Layout Implementation

**Vin=48 V Vout=12 V Iout=30 A fsw=300 kHz L=3.3 µH GaN FET T/SR: 100 V EPC2001**

**T1, T2, T3, T4**

**SR1, SR2, SR3, SR4**

**FLIR Images**

- Tref=20 Tatm=20 Dst=0.1 FOV 37 θ=2.0
- 9/19/13 3:51:20 PM -40 - 120 e=0.96 °C

- Tref=20 Tatm=20 Dst=0.1 FOV 37
- 9/19/13 8:11:54 PM -40 - 120 e=0.96 °C
Parallel Layout Performance

![Graph showing Performance Comparison]

V_{IN}=48 \text{ V} \quad V_{OUT}=12 \text{ V} \quad f_{sw}=300 \text{ kHz} \quad L=3.3 \mu\text{H} \quad \text{GaN FET T/SR: 100 V EPC2001}

Fan Speed 200 LFM 4 Layer 2 oz PCB

Parallel Buck in IBC Applications

![Graph showing Efficiency Comparison]

V_{IN}=48 \text{ V} \quad V_{OUT}=12 \text{ V} \quad \text{Fully Regulated IBC}
Monolithic eGaN Half Bridge

GaN Integration - Smaller

Description and Diagrams are not visible in the image.
GaN Integration - Faster

EPC2100 driven by an LM5113 driver IC from Texas Instruments

GaN Integration
More Efficient at High Frequency

EPC2100 driven by an LM5113 driver IC from Texas Instruments
Thermal Management

Performance Comparison

V_{IN}=12 \, \text{V}, \, V_{OUT}=1.2 \, \text{V}, \, f_{sw}=1 \, \text{MHz}, \, L=300 \, \text{nH}
Thermal Comparison

GaN is 38% Smaller 13% Cooler

\[ V_{IN}=12 \, \text{V}, \quad V_{OUT}=1.2 \, \text{V}, \quad I_{OUT}=20 \, \text{A}, \quad f_{sw}=1 \, \text{MHz}, \quad L=300 \, \text{nH} \]

Thermal Comparison

\[ V_{IN}=12 \, \text{V}, \quad V_{OUT}=1.2 \, \text{V}, \quad I_{OUT}=20 \, \text{A}, \quad f_{sw}=1 \, \text{MHz}, \quad L=300 \, \text{nH} \]
Design Basics Summary

eGaN FETs raise the bar for power conversion performance

- Lower resistance per die area
- Better FOM’s give faster voltage commutation
- Better Packaging gives faster current commutation
- Improved PCB Layout Techniques
  - Superior In-Circuit Performance
  - Can parallel devices for higher current
- Avoid gate overshoot

A Look Into the Future:
Moore’s Law is Alive and Well for GaN FETs
On-Resistance Comparison

- Generation 2 (2011): 2.3x
- Generation 4 (2014): 2.6x

 Drain-to-Source Voltage (V)

V_{GS}=5 \text{ V}

Hard Switching FOM

- Generation 2 (2011): 1.4x
- Generation 4 (2014): 2.4x

 FOM=\frac{(Q_{GD}+Q_{GS2})}{R_{DS(on)} (pC \cdot \Omega)}

 Drain-to-Source Voltage (V)

V_{DS}=0.5 \cdot V_{DSS}, I_{DS}=20 \text{ A}
Hard Switching FOM

FOM_{HS} = (Q_{GD} + Q_{GS2}) \cdot R_{DS(on)} (pC \cdot \Omega)

Drain-to-Source Voltage (V)

EPC Gen 4
EPC Gen 2
Vendor A
Vendor B
Vendor C
Vendor D
Vendor E

V_{DS} = 0.5 \cdot V_{DSS}, I_{DS} = 20 A

Soft Switching FOM

FOM_{SS} = (Q_{G} + Q_{OSS}) \cdot R_{DS(on)} (pC \cdot \Omega)

Drain-to-Source Voltage (V)

EPC Gen 4
EPC Gen 2
Vendor A
Vendor B

V_{DS} = 0.5 \cdot V_{DSS}
Looking forward...

Higher Power RF FETs and ICs
Broadband to 6 GHz
Need Customer Input

Higher scale Integrated Circuits
Q4/2015
Need Customer Input

High Voltage
450 V
Available

Fill In Matrix
Need Customer Input

Gen 3 & 4 FETs and ICs
2014
40 V - 300 V
3 GHz

Generation 5
40% Improvement
Q4/2015

Summary

• eGaN FETs continue to improve rapidly – even faster than Moore’s Law!
• GaN transistors enable exciting new applications such as LiDAR, RF Envelope Tracking and Wireless Power Transmission
• GaN transistors have the potential to replace silicon power MOSFETs and LDMOS in power conversion applications with a low-cost and higher efficiency solution
• eGaN FETs are straightforward to use, but you can’t just drop them into a MOSFET socket. Some R&D is needed – start today!

eGaN is a registered trademark of Efficient Power Conversion Corporation
The end of the road for silicon.....

is the beginning of the eGaN FET journey!