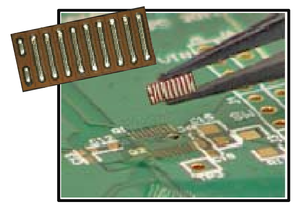
GaN Transistors for Efficient Power Conversion (and RF)



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Agenda

- How GaN works and the state-of-the-art
  - Reliability
  - Radiation Tolerance
- Design Basics
- Design Examples
- GaN Integration
- Thermal Characteristics
- What is in the future?

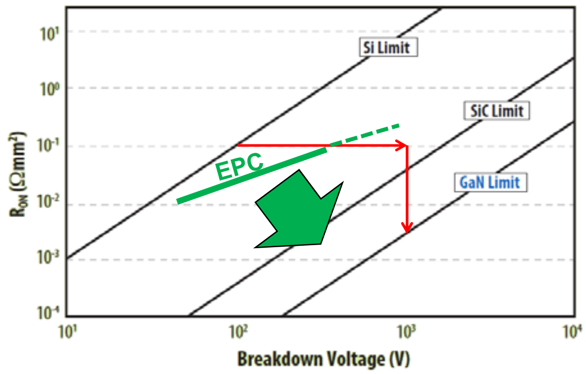
Power Switch Wish List

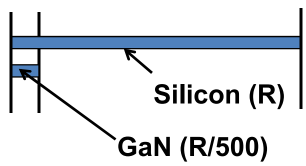
- Lower On-Resistance
- Faster
  - Less Capacitance
  - Less Inductance
- Smaller
- Lower Cost

Material Comparison

Parameter		GaN	Silicon	SiC
Band Gap E_g	eV	3.2	1.12	3.4
Breakdown Field E_{BV}	MV/cm	3.3	0.3	3.5
Electron Mobility μ_n	$cm^2/V \cdot s$	2000	1500	650

State of the Art:
Fundamental Material Superiority



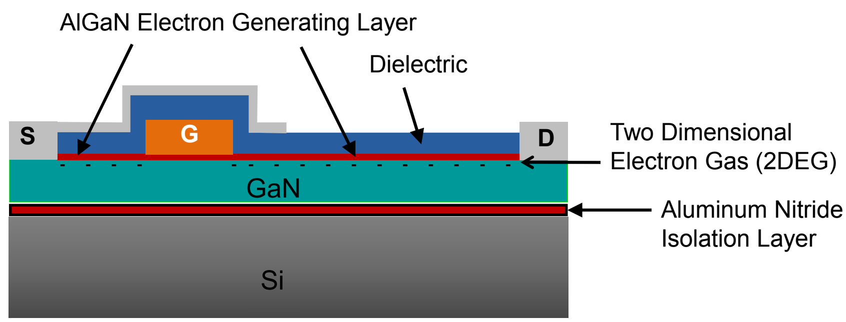


- GaN has a 10x advantage in critical electric field.
  - For a given breakdown voltage, GaN terminals can be one tenth the distance apart compared with Silicon
- GaN has a 50x advantage in resistivity
  - For a given geometry, GaN resistance will be one 50th of that of Silicon
- GaN has a 500x theoretical material advantage over Silicon

Product Matrix

Part Number	Configuration	V_{DS}	Max V_{GS}	Max $R_{DS(ON)}$ (mΩ) @5V_{GS}	Q_G typ (nC)	Q_{GS} typ (nC)	Q_{GD} typ (nC)	Q_{OSS} typ (nC)	Q_{RR} (nC)	I_D (A)	Pulsed I_D (A)	LGA Package (mm)	Half-Bridge Development Board
EPC2100	Dual Asymmetric	30	6	8 2	3.5 15	1.4 4.6	0.57 2.6	5.5 28	0	9.5 38	100 400	6.1 x 2.3	EPC9036
EPC2023	Single	30	6	1.3	20	5.8	1.9	28	0	60	590	6.1 x 2.3	EPC9031
EPC2024	Single	40	6	1.5	19	6.4	2.0	32	0	60	550	6.1 x 2.3	EPC9032
EPC2015	Single	40	6	4	10.5	3.0	2.2	18.5	0	33	150	4.1 x 1.6	EPC9001
EPC2014C	Single	40	6	16	2.0	0.70	0.30	4	0	10	60	1.7 x 1.1	N/A
EPC8004	Single	40	6	110	0.370	0.120	0.047	0.63	0	2.7	7.5	2.1 x 0.85	EPC9024
EPC8007	Single	40	6	160	0.302	0.097	0.025	0.406	0	2.7	6	2.1 x 0.85	EPC9027
EPC8008	Single	40	6	325	0.177	0.067	0.012	0.211	0	2.7	2.9	2.1 x 0.85	EPC9028
EPC2020	Single	60	6	2	16	5.0	2.0	42	0	60	470	6.1 x 2.3	EPC9033
EPC2101	Dual Asymmetric	60	6	11.5 2.7	2.7 12	1 3.7	0.50 2.5	9 45	0	9.5 38	80 350	6.1 x 2.3	EPC9037
EPC2102	Dual Symmetric	60	6	4.4	6.8	2.3	1.4	25	0	23	215	6.1 x 2.3	EPC9038
EPC8009	Single	65	6	130	0.370	0.120	0.055	0.94	0	2.7	7.5	2.1 x 0.85	EPC9029
EPC8005	Single	65	6	275	0.218	0.077	0.018	0.414	0	2.7	3.8	2.1 x 0.85	EPC9025
EPC8002	Single	65	6	530	0.141	0.059	0.009	0.244	0	2*	2	2.1 x 0.85	EPC9022
EPC2021	Single	80	6	2.5	15	3.8	2.1	56	0	60	420	6.1 x 2.3	EPC9034
EPC2105	Dual Asymmetric	80	6	14.5 3.5	2.5 10	1 3.2	0.50 2	11 55	0	9.5 38	75 320	6.1 x 2.3	EPC9041
EPC2103	Dual Symmetric	80	6	5.5	6.5	2.0	1.3	1.5	0	23	195	6.1 x 2.3	EPC9039
EPC2022	Single	100	6	3.2	13	3.7	2.0	62	0	60	360	6.1 x 2.3	EPC9035
EPC2001C	Single	100	6	7	7.5	2.4	1.2	31	0	36	150	4.1 x 1.6	N/A
EPC2016	Single	100	6	16	3.8	0.99	0.7	20	0	11	50	2.1 x 1.6	EPC9010
EPC2007	Single	100	6	30	2.1	0.52	0.61	10.2	0	6	25	1.7 x 1.1	EPC9006
EPC8010	Single	100	6	160	0.360	0.130	0.060	2.2	0	2.7	7.5	2.1 x 0.85	EPC9030
EPC8003	Single	100	6	300	0.315	0.110	0.034	1.1	0	2.7	5	2.1 x 0.85	EPC9023
EPC2018	Single	150	6	25	5.0	1.3	1.7	40	0	12	60	3.6 x 1.6	N/A
EPC2010C	Single	200	6	25	3.7	1.3	0.7	40	0	22	90	3.6 x 1.6	EPC9003C
EPC2019	Single	200	6	50	1.8	0.60	0.35	18	0	8.5	42	2.7 x 0.95	EPC9014
EPC2012C	Single	200	6	100	1.0	0.30	0.20	10	0	5	22	1.7 x 0.9	EPC9004C
EPC2025	Single	300	6	150	1.9	0.61	0.30	20	0	4	20	1.95 x 1.95	EPC9042
EPC2027	Single	450	6	400	1.7	0.60	0.25	19	0	4	12	1.95 x 1.95	EPC9044

eGaN FET Structure

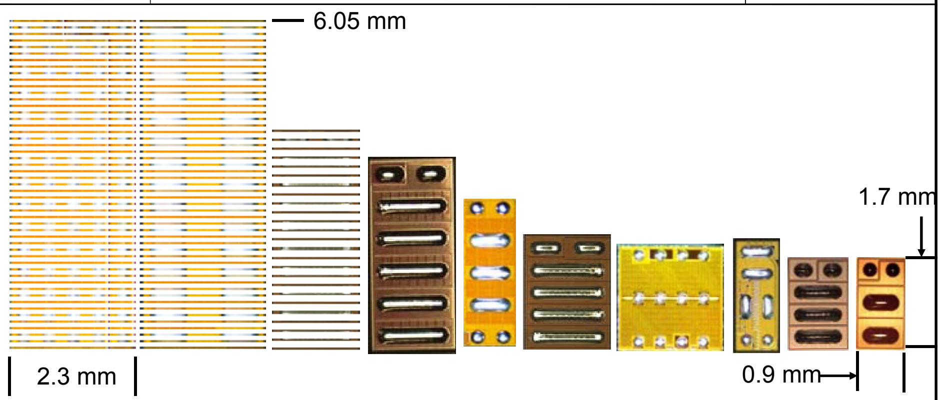


- Silicon Substrate
  - Low cost starting material
  - Standard CMOS (0.35 µm) wafer processing
- Isolation Layer allows integration
- Enhancement mode for power conversion applications
- Simple Structure for low mask count
- Very low capacitance for a given Voltage and $R_{DS(on)}$ compared with MOSFET technology
- Zero Q_{RR}

Package Wish List

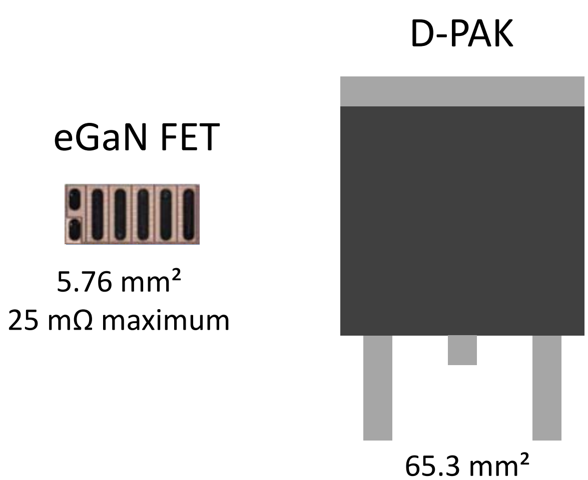
- Low parasitic resistance
- Low parasitic inductance
- Low thermal resistance
- Small size
- Low cost
- Isolated from environment

Wafer Level Packaging



- Low inductance give fast current commutation and low noise
- Minimal footprint on PCB
- Thermally efficient, dual sided cooling
- MSL 1 rated and RoHS 6/6

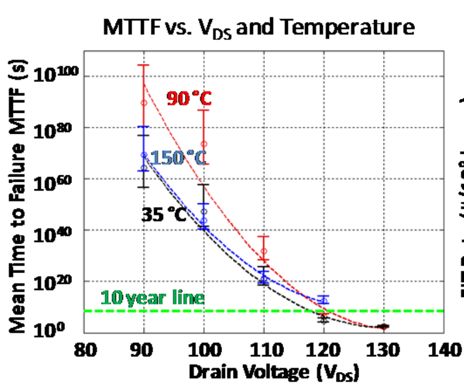
Size Comparison – 200 V

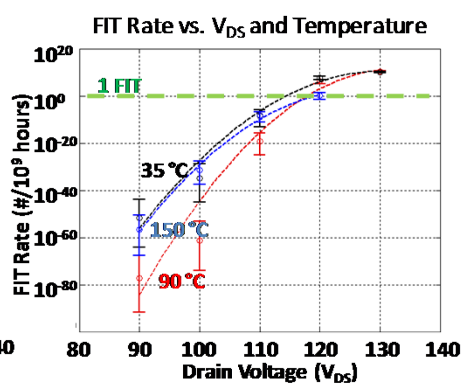


Drawn To Scale

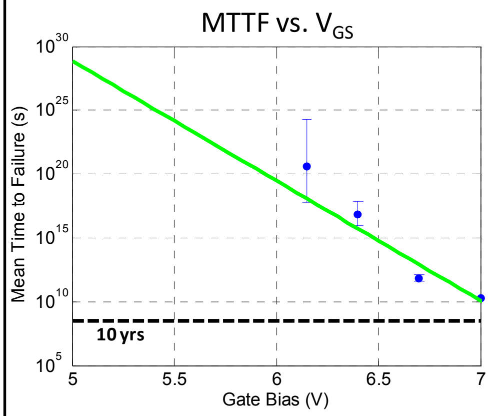
Predicting Reliability

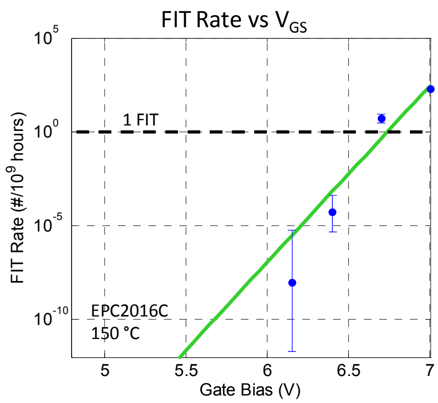
Drain-Source Reliability





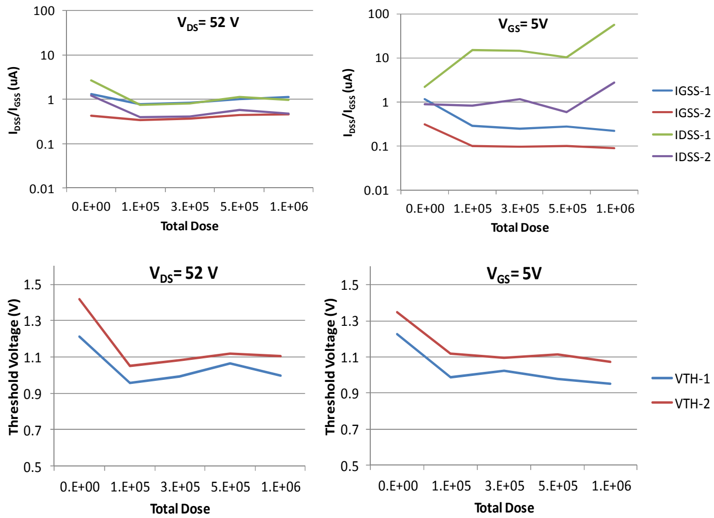
Gate Reliability





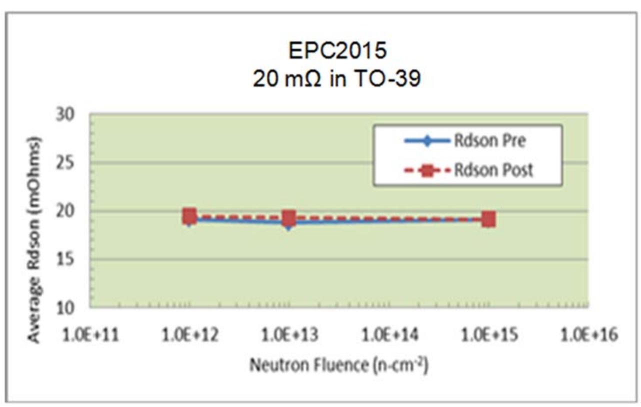
Radiation Capability

> 1 MRad Gamma Radiation Stability



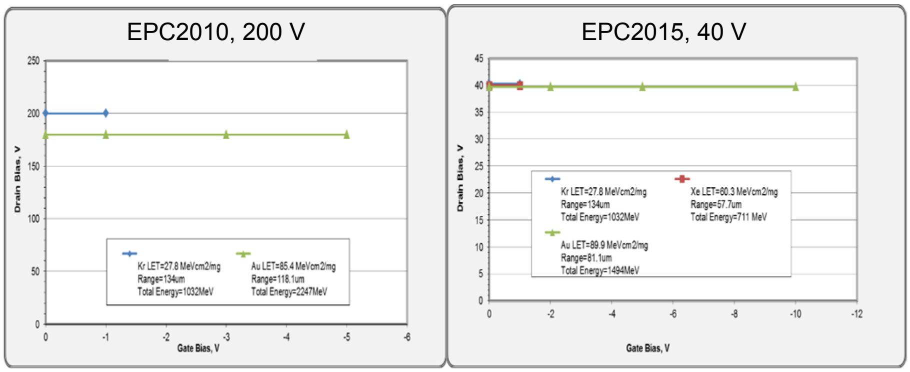
Negative voltage gate drive is not needed

> 1E15 Neutron Stability



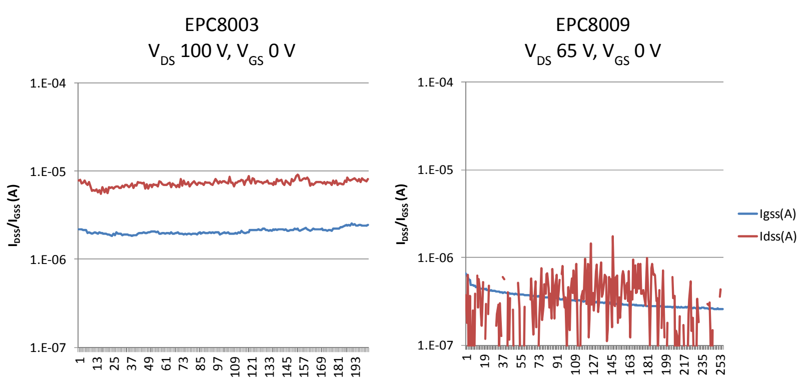
eGaN technology is tolerant to Neutron Radiation

Single Event Stability



Negative voltage gate drive is not needed

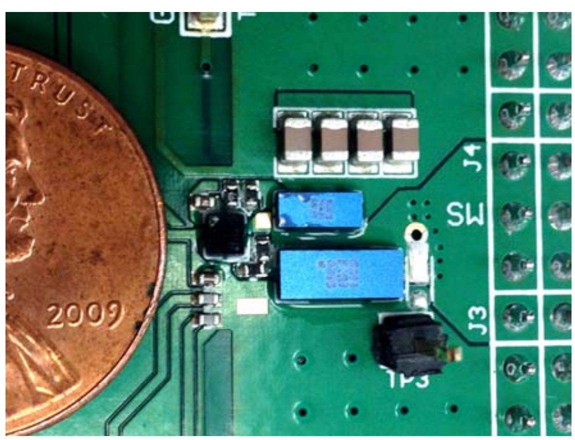
Single Event Stability



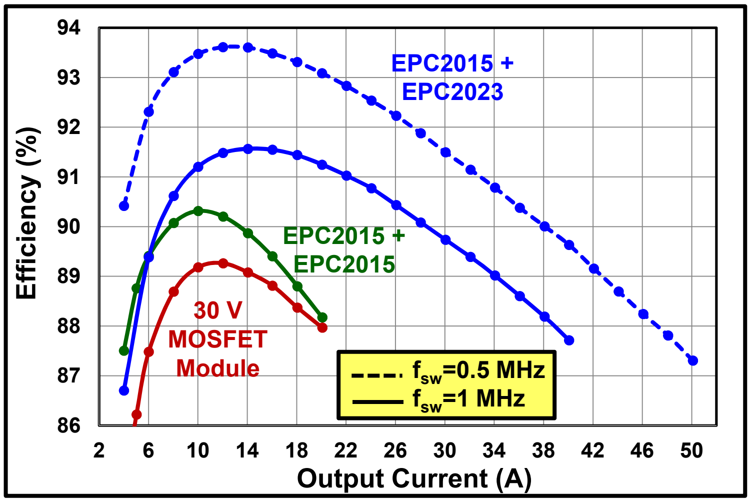
Au at ~85.4 LET

Where is GaN going…

Hard Switching Buck Converter

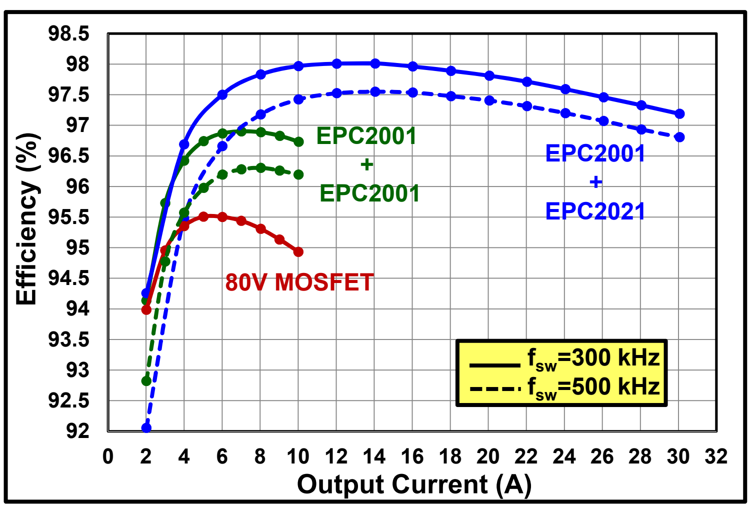


Low Voltage Buck Converter



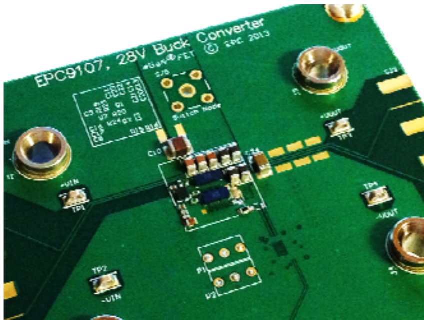
V_{IN}=12 V V_{OUT}=1.2 V

Higher Voltage Buck Converter

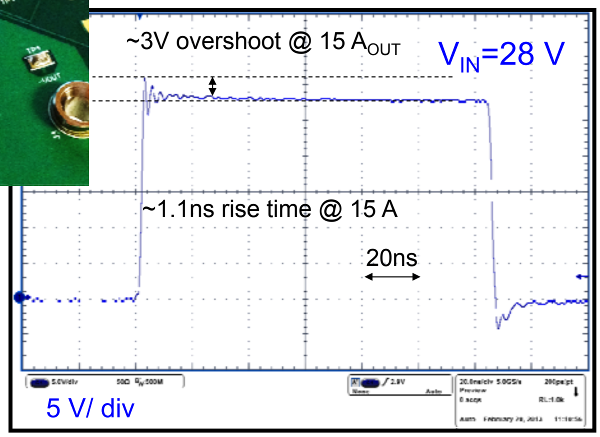


V_{IN}=48 V V_{OUT}=12 V

EPC9107 Demonstration Board



V_{IN}=12-28 V V_{OUT}=3.3 V
I_{OUT}=15 A f_{sw}=1 MHz
2 x EPC2015

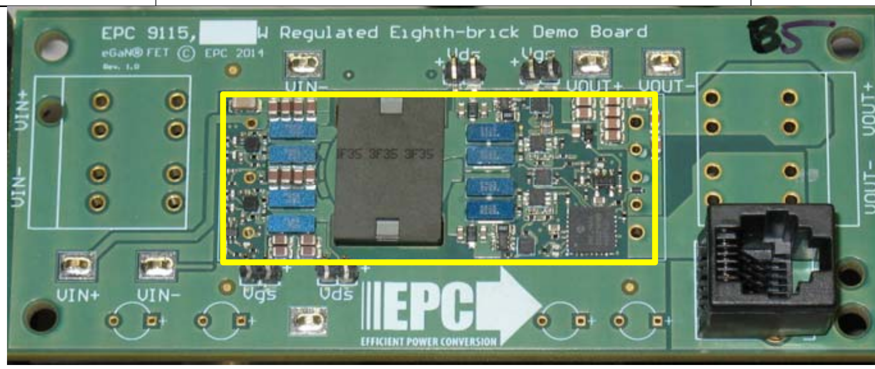


Switching Node Voltage
V_{IN}=28 V, I_{OUT}=15 A

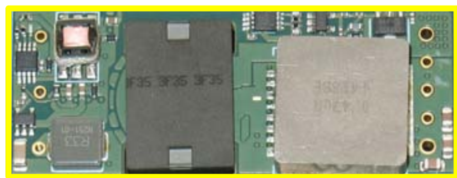
eGaN Eighth-brick Target Specifications

- Eighth-brick integrated bus converter
  - Fully regulated
  - Isolated
  - 500 W output at 12V
  - 52 V nominal input (4:1 transformer)
  - > 96% efficient
  - DOSA-compliant footprint
  - Off the shelf parts

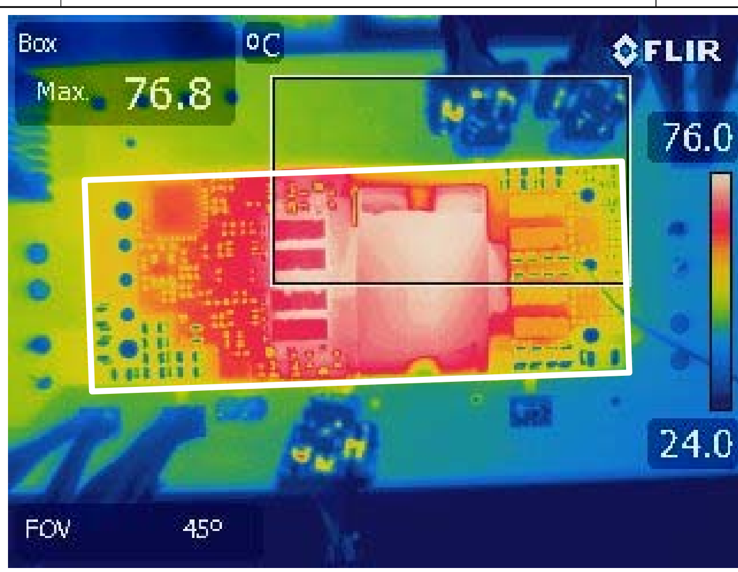
Board Images



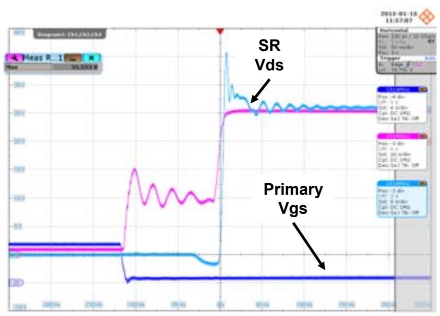
TOP and Bottom vies

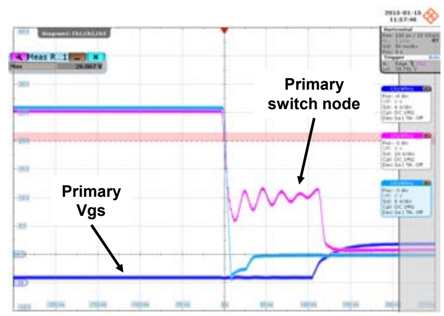


Thermal Images @ 400W

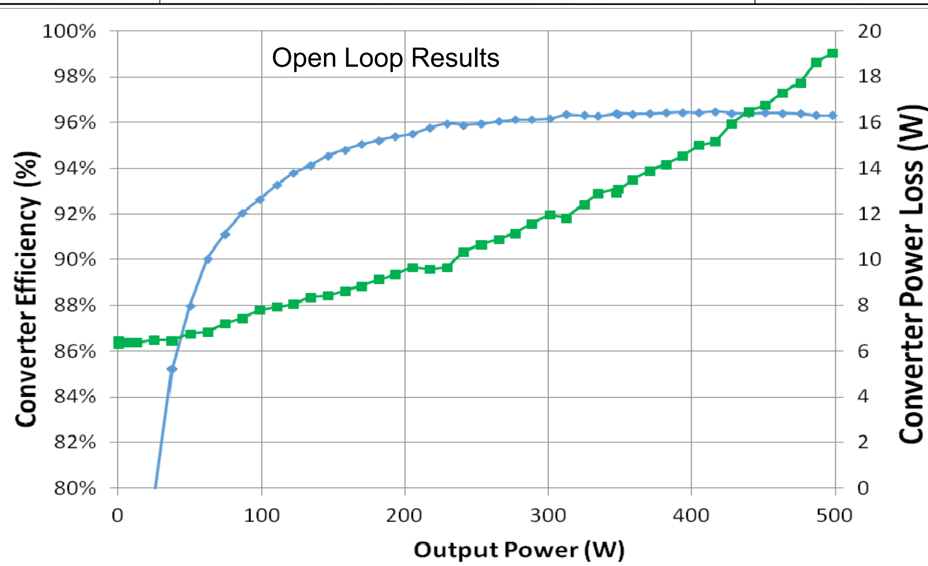


Waveforms @ 500W



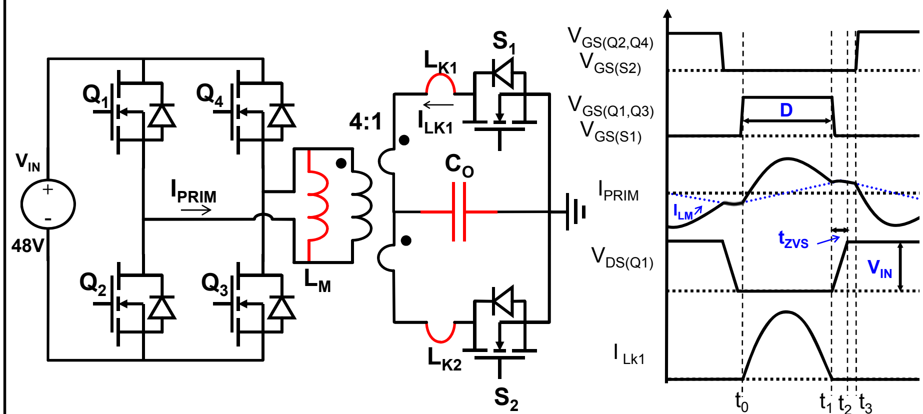


Preliminary Efficiency and Power Loss



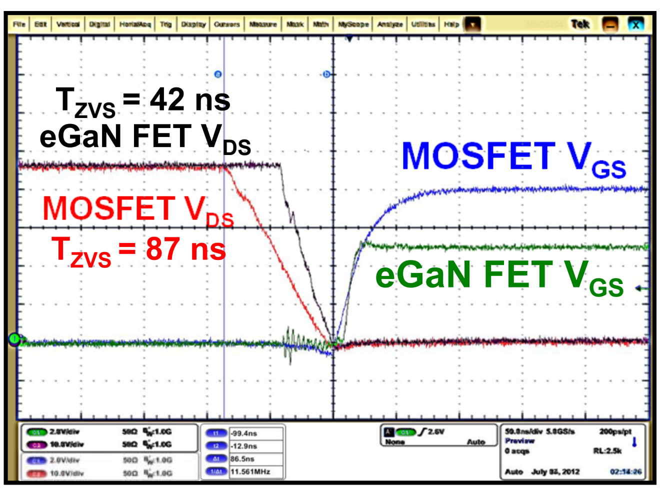
Resonant Bus Converter

High Frequency DC/DC Transformer



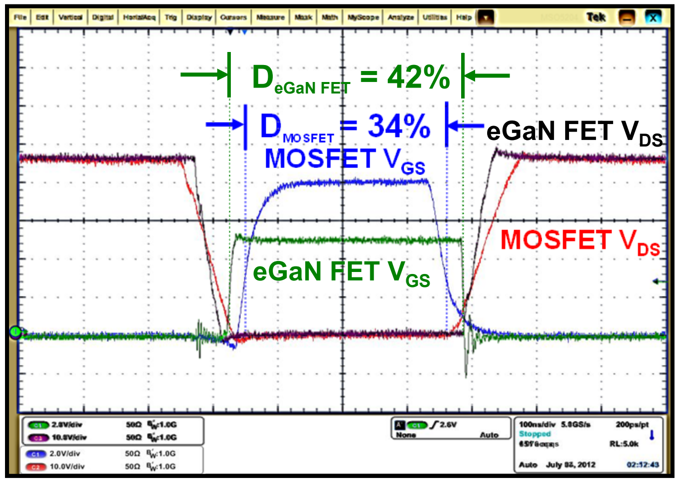
Ref: Y. Ren, M. Xu, J. Sun, and F. C. Lee, "A family of high power density unregulated bus converters," IEEE Trans. Power Electron., vol. 20, no. 5, pp. 1045–1054, Sep. 2005.

ZVS Switching Comparison



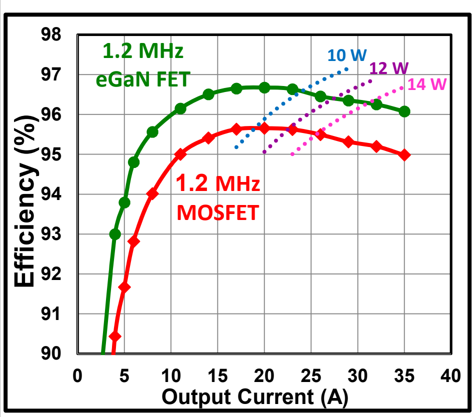
f_{sw} = 1.2 MHz, V_{IN} = 48 V, and V_{OUT} ≈ 12 V

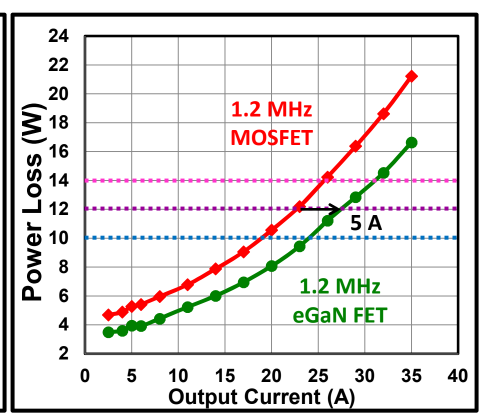
Duty Cycle Comparison



f_{sw} = 1.2 MHz, V_{IN} = 48 V, and $V_{OUT} \approx$ 12 V

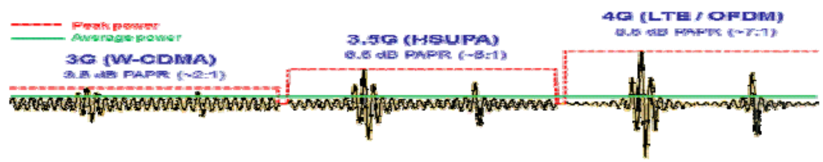
Efficiency Comparison





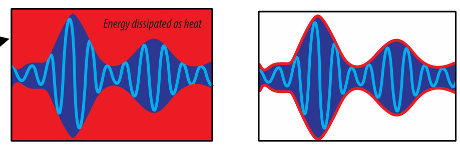
f_{sw} = 1.2 MHz, V_{IN} = 48 V, and $V_{OUT} \approx$ 12 V

Envelope Tracking



W/O ET | With ET

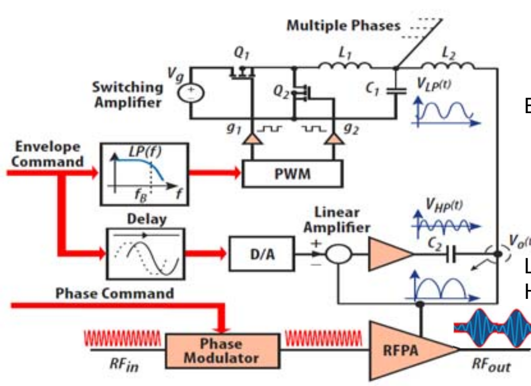
Red represents wasted energy dissipated as heat



- **Envelope Tracking can *double* base station efficiency.**
- **n-Stat forecasts that there will be 160.3 million active small cells, and the retail value of small cell shipments will reach $14B by 2015.**

Envelope Tracking Supply

- ET power supply topologies vary
  - Open loop boost – full BW required
  - Closed loop linear-assisted Buck*

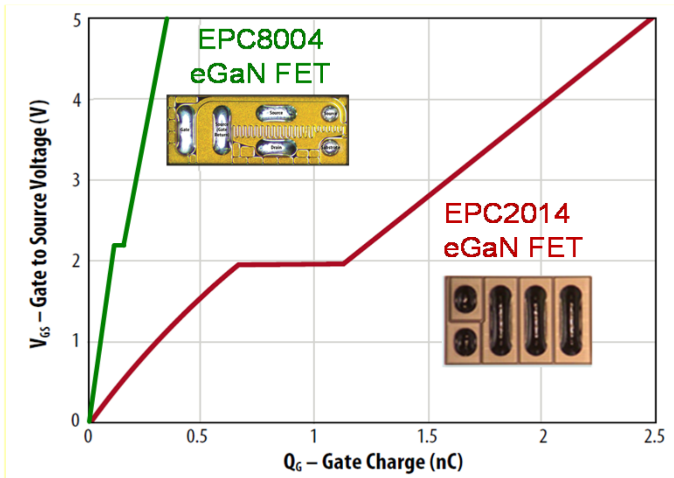


Buck ~ 10% Bandwidth
~ 90% Power

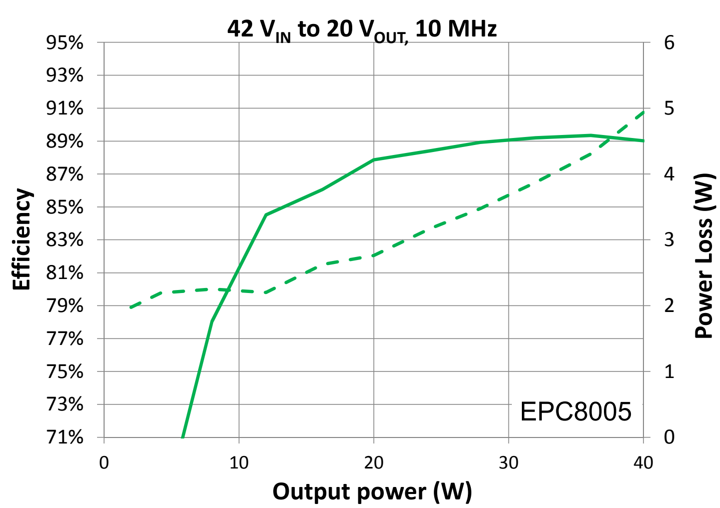
Linear AMP ~ 10% Power
Highest 90% of Bandwidth

*V. Yousefzadeh, et. Al, Efficiency optimization in linear-assisted switching power converters for envelope tracking in RF power amplifiers, ISCAS 2005

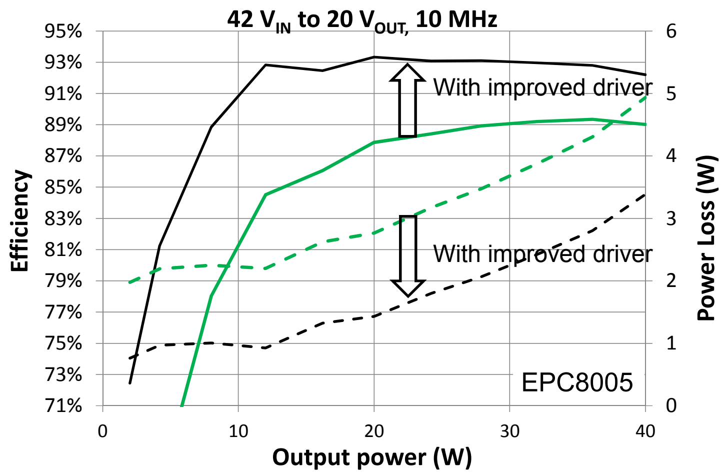
Envelope Tracking



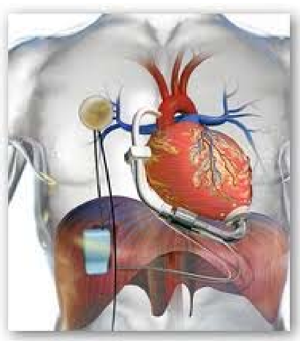
Envelope Tracking



Envelope Tracking



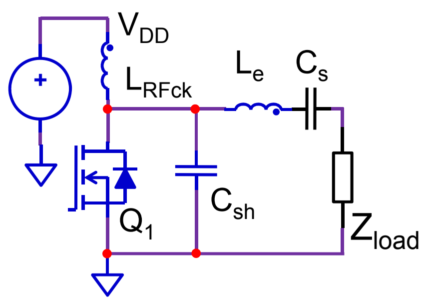
Wireless Power

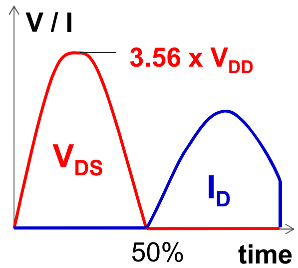


The global wireless charging market is estimated to grow to $10B by 2018, a CAGR of 42.6%.

Class-E Schematic

Output power decreases with increasing load impedance above design point

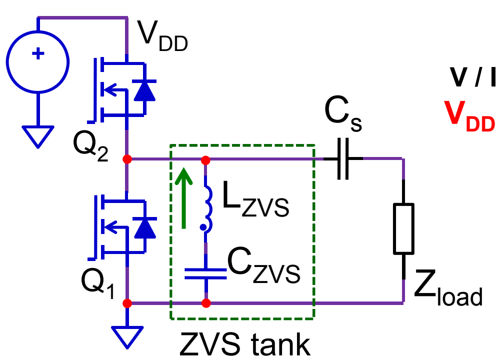


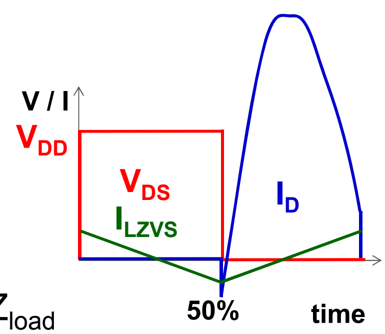


Ideal Waveforms

ZVS Class-D Schematic

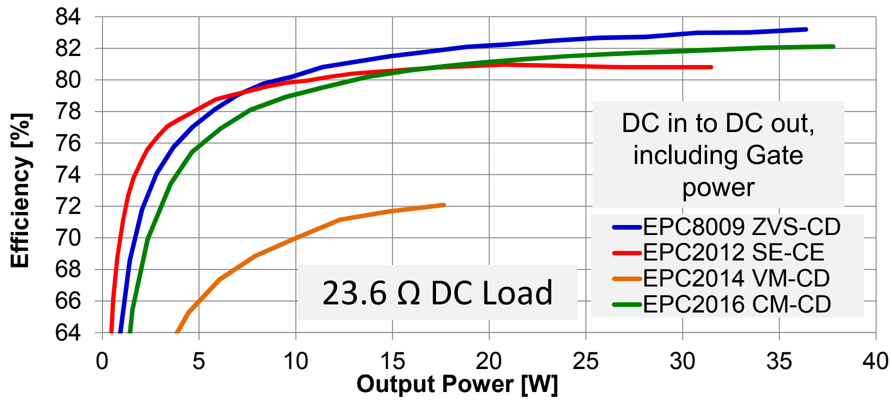
Output power increases with increasing load impedance



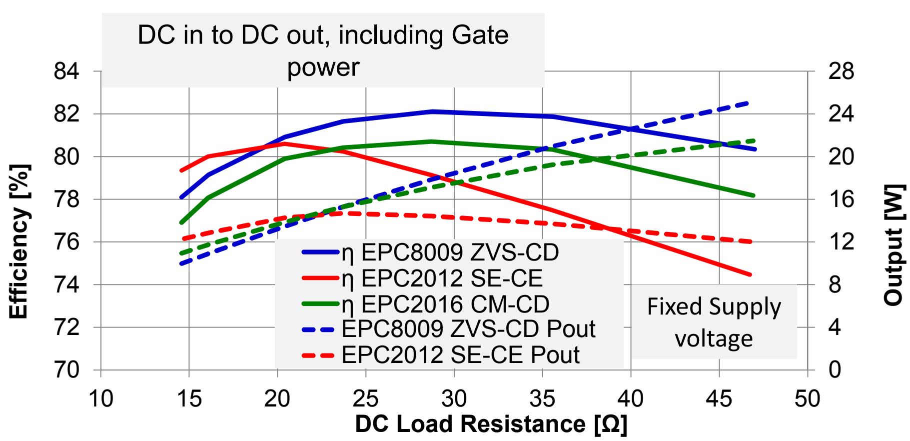


Ideal Waveforms

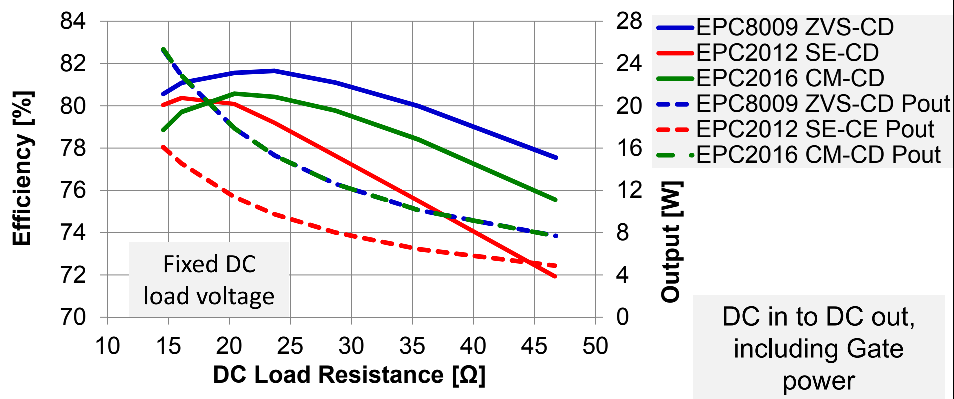
Topology Comparison
Peak Performance



Topology Comparison
Load Variation



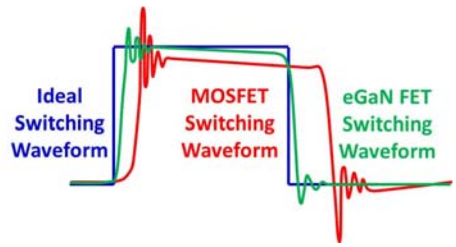
Topology Comparison
Load Regulation

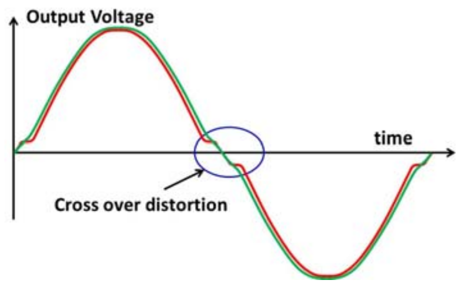


Class-D Audio

Why eGaN FETs in Class-D Audio

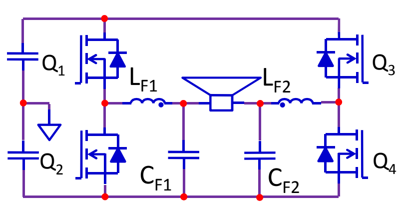
- Low $R_{DS(on)}$ & Low C_{OSS}
  - + High Efficiency
  - + High Damping Factor = Low open loop output Impedance = **Low T-IMD**
- Fast Switching & No Reverse Recovery (Q_{rr})
  - + High output linearity, Low Cross-over Distortion
    = **Low THD**

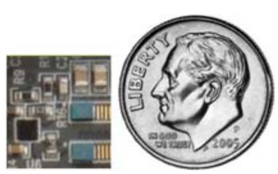




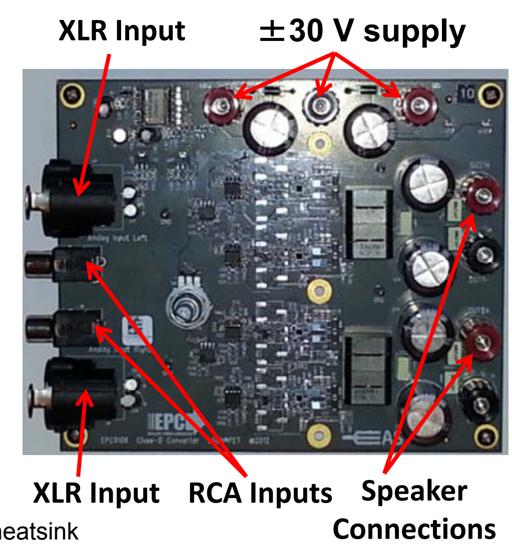
eGaN FET Class-D Audio Amplifier

- Bridge-Tied-Load (BTL)
- EPC2016 with LM5113





eGaN FET Power Stage:
250 W into 4 Ω at 440 kHz without a heatsink

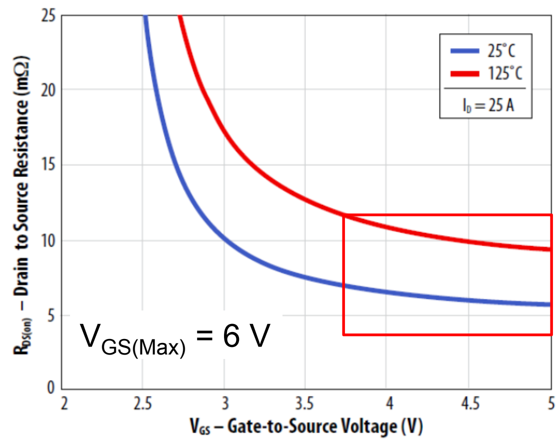


Other Key Applications

- LiDAR
- High Resolution MRI Imaging
- Network and Server Power Supplies
- AC Adapters
- Class-D Audio
- Energy Efficient Lighting
- Robotics

Design Basics

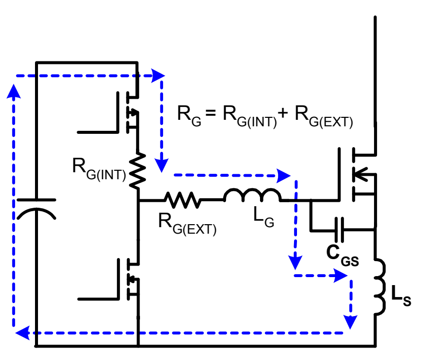
Low $V_{GS(on)}$ Overhead



eGaN FET Drive Requirements

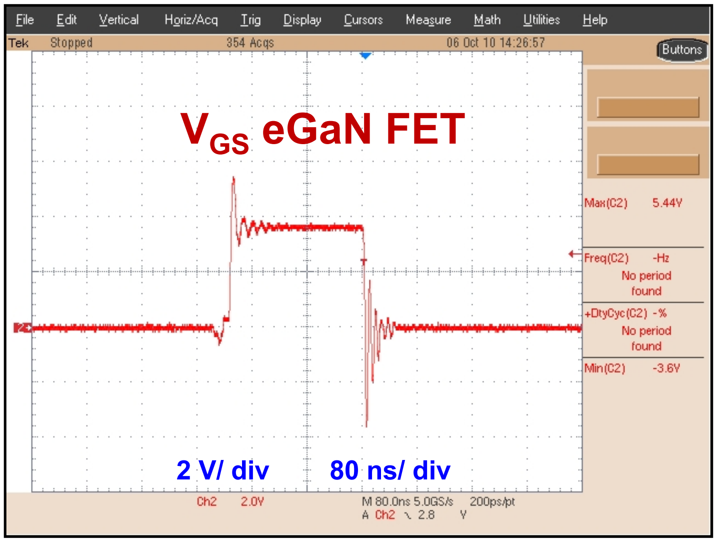
To avoid overshoot:

$$R_G \geq \sqrt{\frac{4(L_G + L_S)}{C_{GS}}}$$

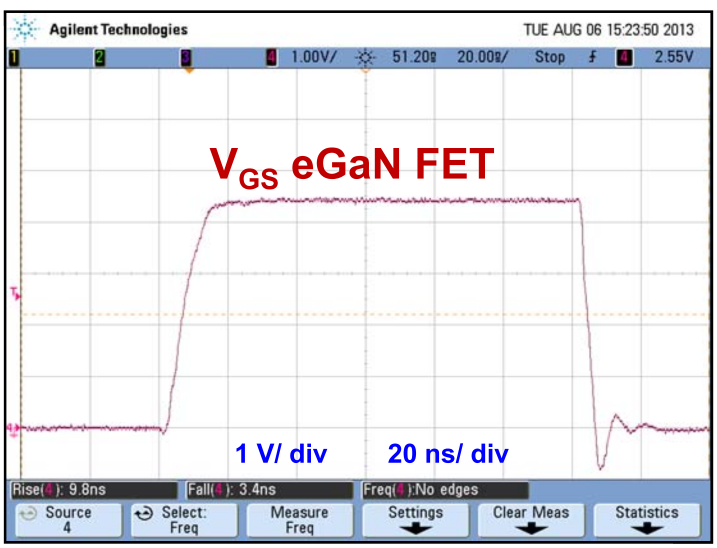


- Minimize gate loop inductance
- Separate source and sink transistors allowing for separate drive paths
- Wandering gate drive return has been issue

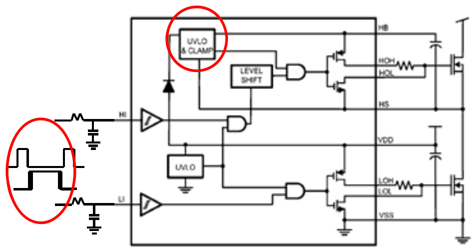
Minimizing Overshoot

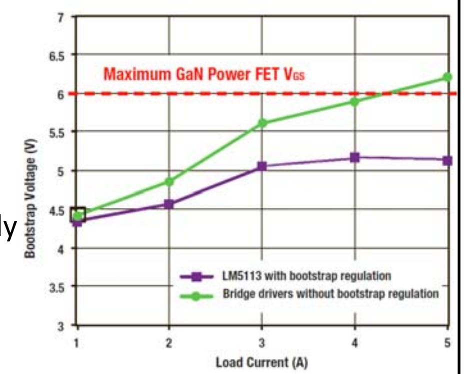


Minimizing Overshoot



eGaN FET Driver IC



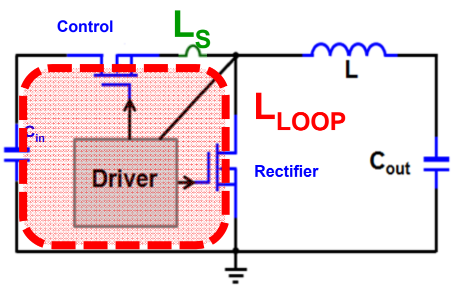


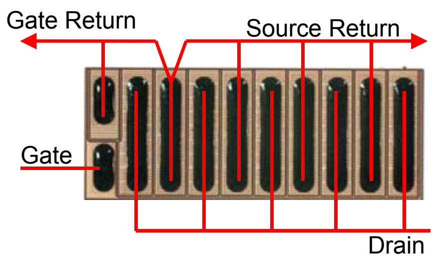
- Bootstrap clamp limits (HS) supply
- Separate inputs allow accurate, dead-time management
- Optimized drive impedance
- Synchronous bootstrap rectifier eliminates this need

Reference: Texas Instruments, "Gate Drivers for Enhancement Mode GaN Power FETs 100 V Half-Bridge and Low-Side Drivers Enable Greater Efficiency, Power Density, and Simplicity," SNVB001

Layout

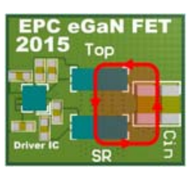
LGA has very low inductance



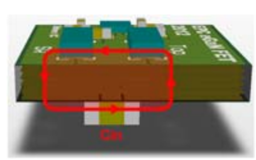


- Source Inductance common to the gate drive and control loops, L_S, slows current commutation by reducing effective gate drive during di/dt
- High Frequency Loop Inductance causes increased losses, high peak voltage and increased ringing
- LGA Package has low common source inductance and enables low high frequency loop inductance

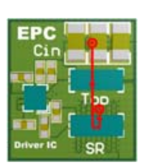
Half Bridge Layout Options

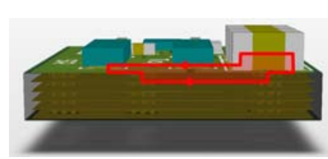


Horizontal



Vertical

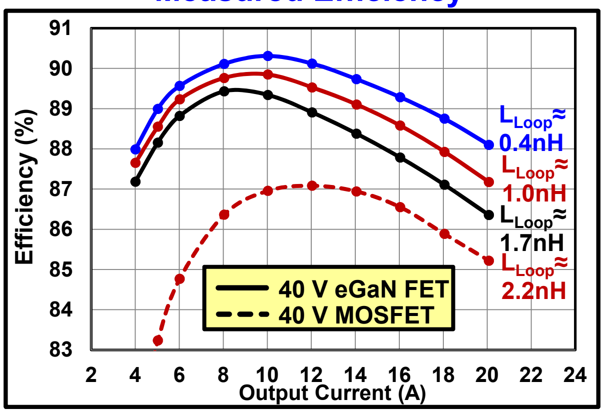




Optimal

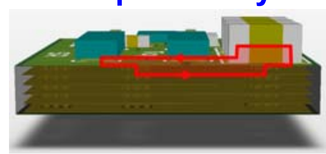
Layout Impact on Efficiency

Measured Efficiency



V_{IN}=12 V, V_{OUT}=1.2 V, f_{sw}=1 MHz, L=300 nH

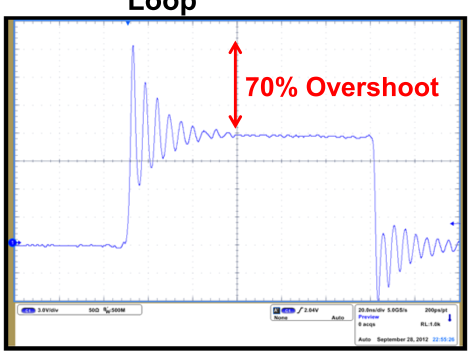
EPC Optimal Layout



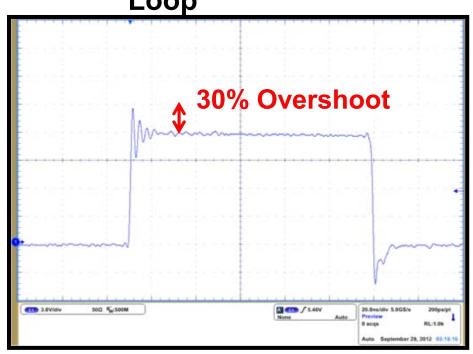
Ref: D. Reusch, J. Strydom, "Understanding the Effect of PCB Layout on Circuit Performance in a High Frequency Gallium Nitride Based Point of Load Converter," APEC 2013

Layout Impact on Peak Voltage

L_{Loop}≈1.0 nH



L_{Loop} ≈ 0.4 nH

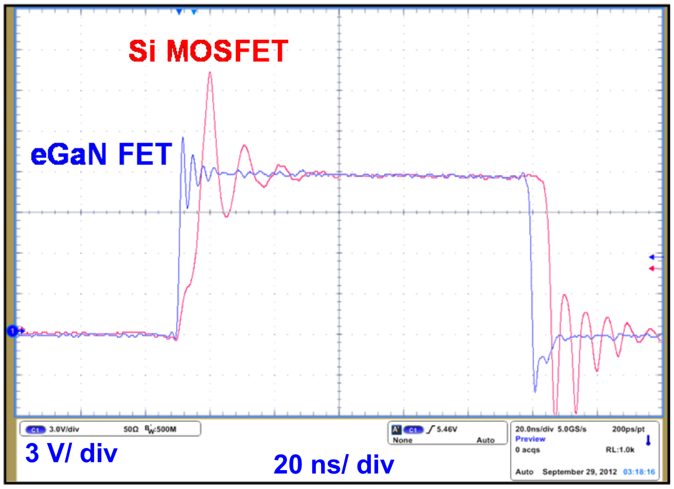


Switching Node Voltage

V_{IN}=12 V V_{OUT}=1.2 V I_{OUT}=20 A

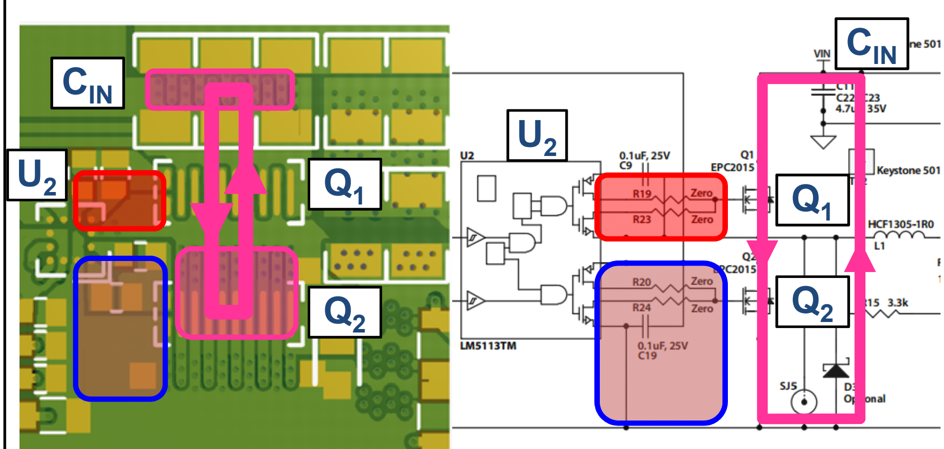
f_{sw}=1 MHz L=150 nH

eGaN FET vs. MOSFET

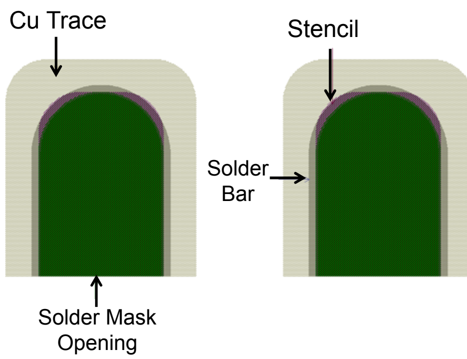


V_{IN}=12 V V_{OUT}=1.2 V I_{OUT}=20 A f_{sw}=1 MHz L=300 nH eGaN FET

Optimal Layout Implementation



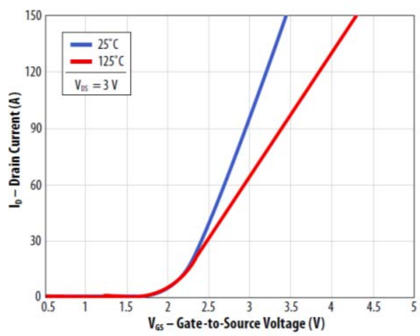
Footprint

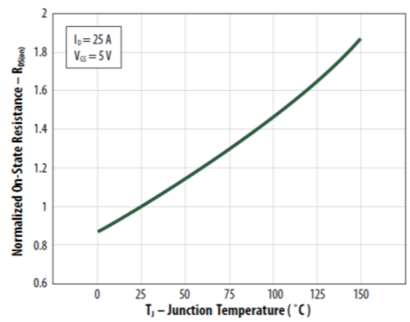


- Fine pitched LGA requires careful footprint and solder mask design.
  - Please see detail in:
  - http://epc-co.com/epc/documents/product-training/Appnote_GaNassembly.pdf

Paralleling High-Speed eGaN FETs

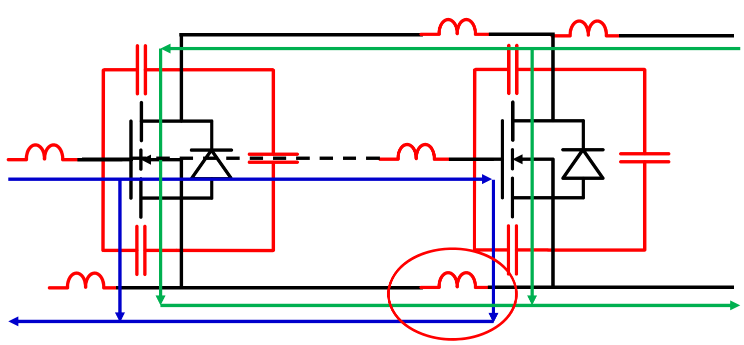
Parallel Power Devices



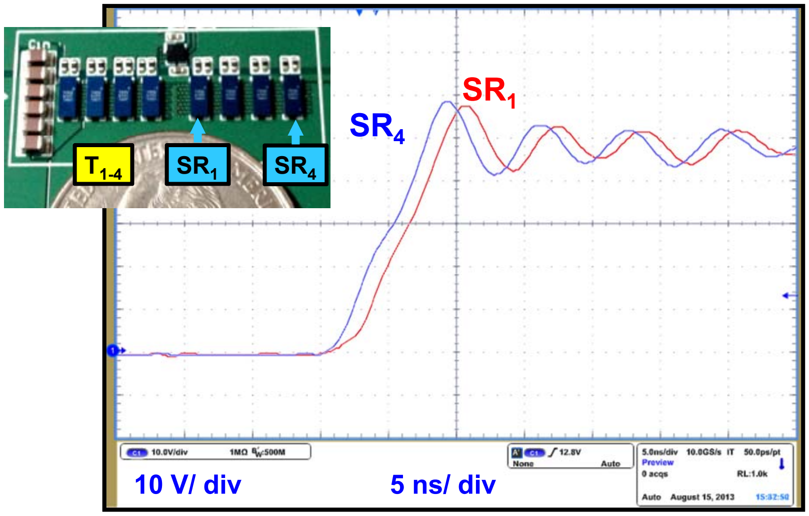


- eGaN FETs have a positive temperature coefficient over most of the operating range
  - Current distributes over die area in hot swap and solid state circuit breaker applications
  - Parallel devices share in both constant current and on state regions

Parallel Power Devices

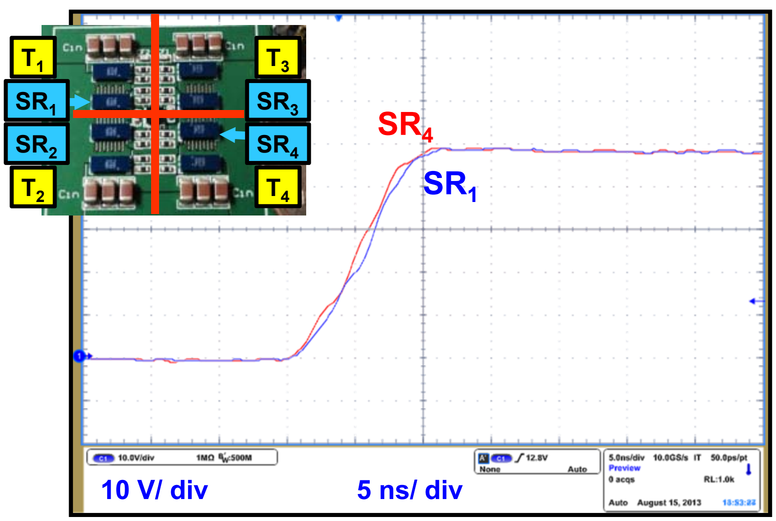


Single Loop Optimal Layout



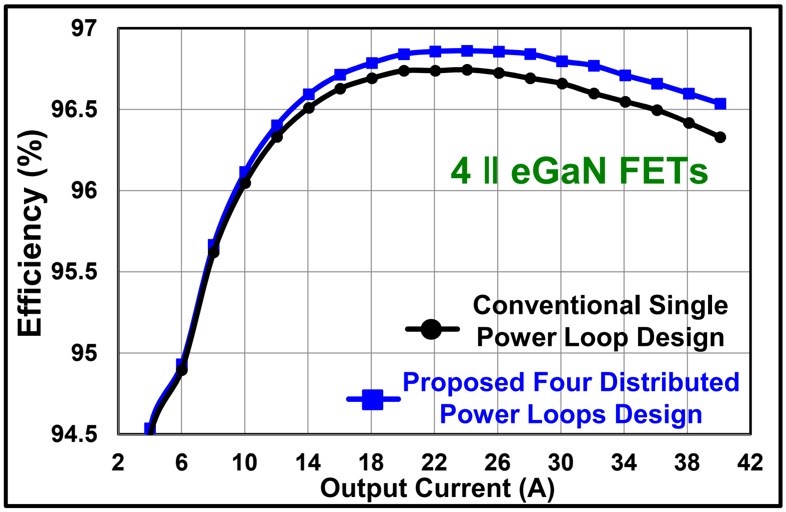
V_{IN}=48 V V_{OUT}=12 V I_{OUT}=30 A f_{sw}=300 kHz L=3.3 μH GaN FET T/SR: 100 V EPC2001

Parallel Loop Optimal Layout



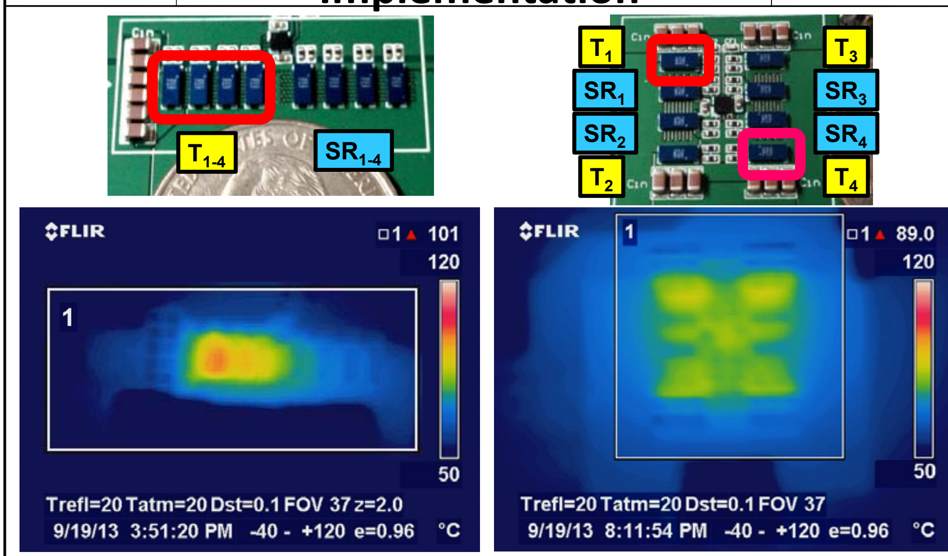
V_{IN}=48 V V_{OUT}=12 V I_{OUT}=30 A f_{sw}=300 kHz L=3.3 μH GaN FET T/SR: 100 V EPC2001

Parallel Layout Performance



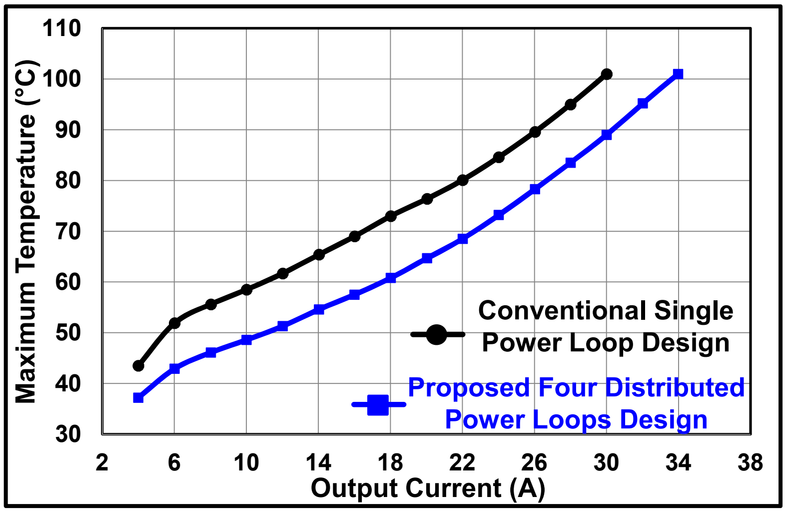
V_{IN}=48 V V_{OUT}=12 V f_{sw}=300 kHz L=3.3 µH GaN FET T/SR: 4x100 V EPC2001
4 Layer 2 oz PCB

Parallel Layout Implementation



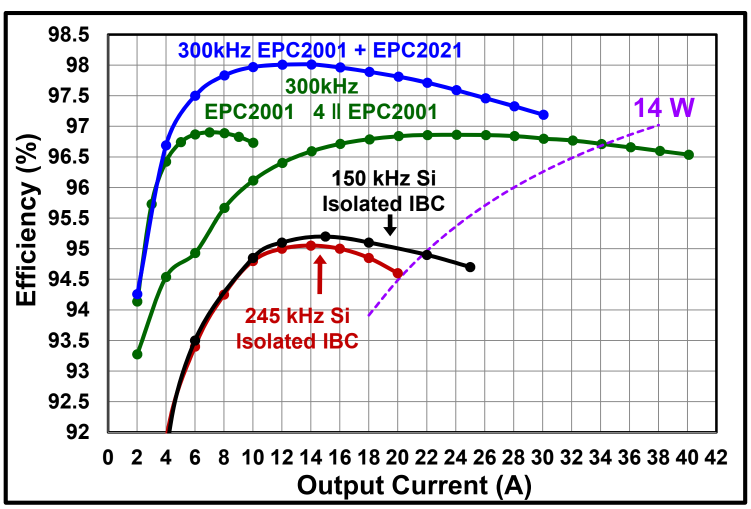
V_{IN}=48 V V_{OUT}=12 V I_{OUT}=30 A f_{sw}=300 kHz L=3.3 µH GaN FET T/SR: 100 V EPC2001

Parallel Layout Performance



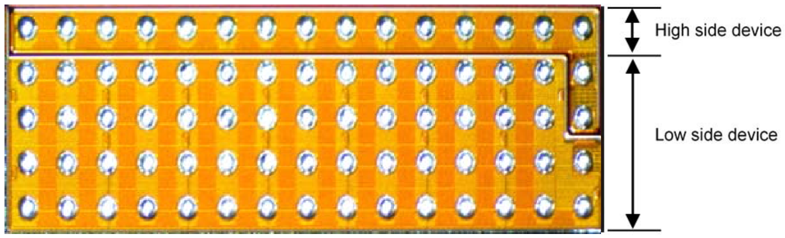
V_{IN}=48 V V_{OUT}=12 V f_{sw}=300 kHz L=3.3 µH GaN FET T/SR: 100 V EPC2001
Fan Speed 200 LFM 4 Layer 2 oz PCB

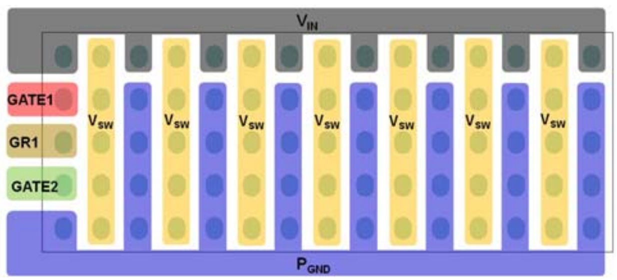
Parallel Buck in IBC Applications



V_{IN}=48 V V_{OUT}=12 V Fully Regulated IBC

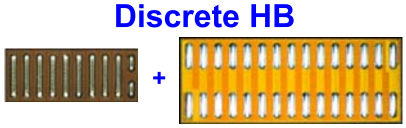
Monolithic eGaN Half Bridge





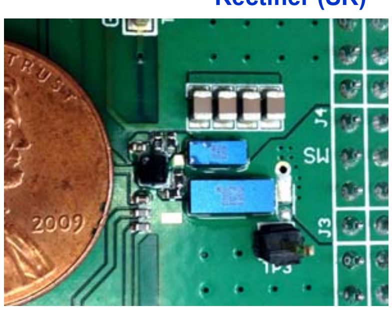
GaN Integration - Smaller

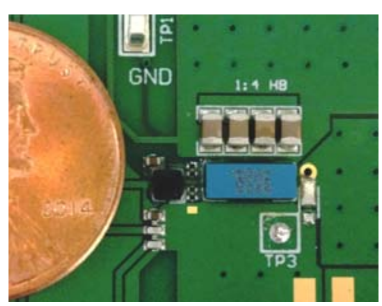
Generation 2/4
Discrete HB



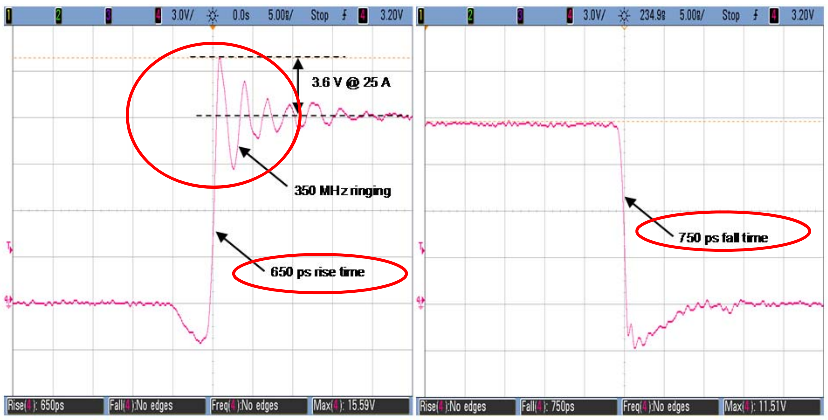
Top Switch (T) Synchronous Rectifier (SR)

Generation 4
Monolithic 4:1 HB





GaN Integration - Faster



EPC2100 driven by an LM5113 driver IC from Texas Instruments

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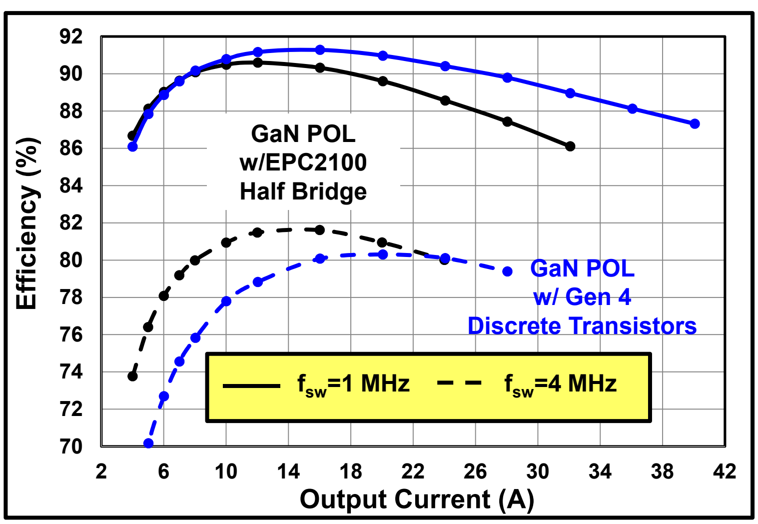
GaN Integration
More Efficient at High Frequency



V_{IN}=12 V V_{OUT}=1.2 V L=100 nH

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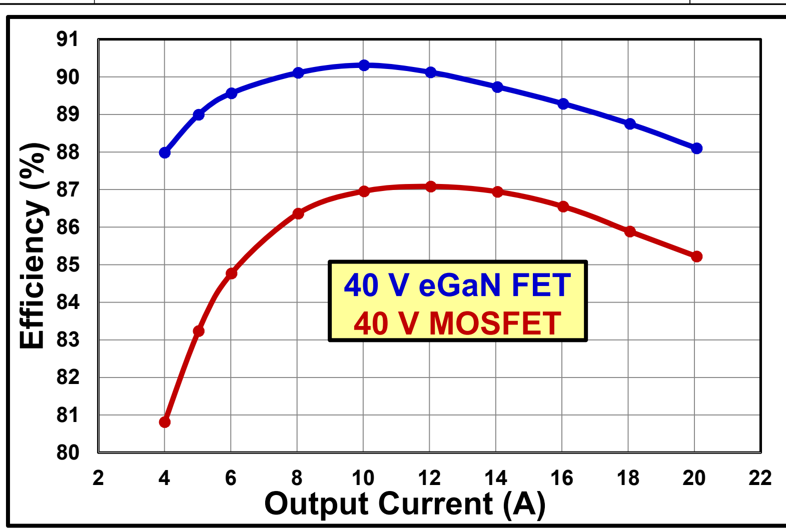
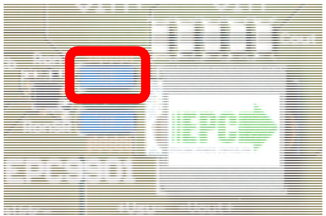
Thermal Management

Performance Comparison

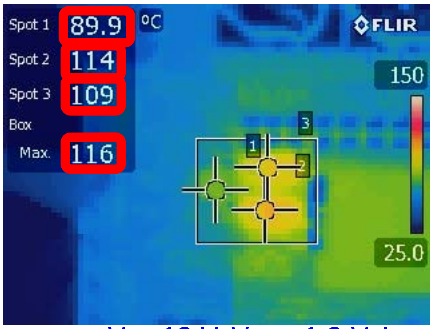


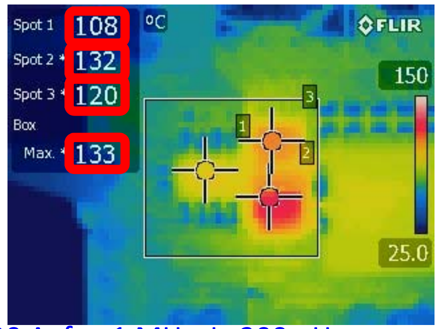
V_{IN}=12 V, V_{OUT}=1.2 V, f_{sw}=1 MHz, L=300 nH

Thermal Comparison



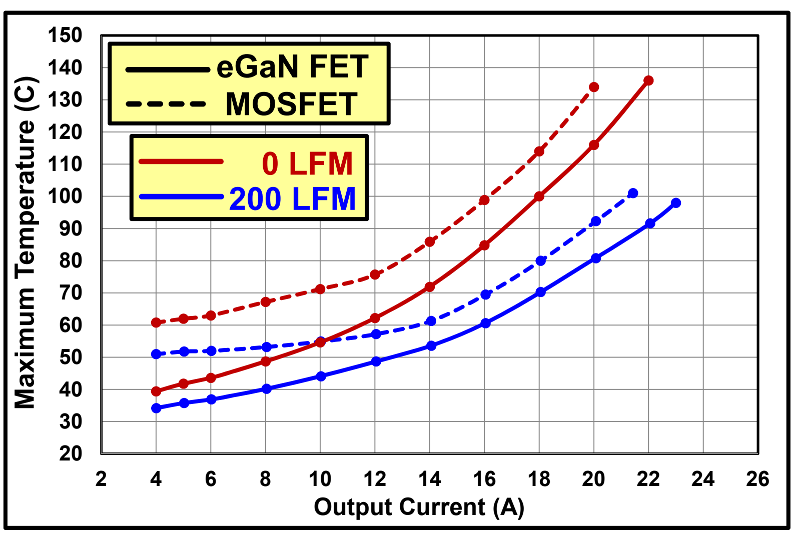
GaN is
38% Smaller
13% Cooler





V_{IN}=12 V, V_{OUT}=1.2 V, I_{OUT}=20 A, f_{sw}=1 MHz, L=300 nH

Thermal Comparison



V_{IN}=12 V, V_{OUT}=1.2 V, f_{sw}=1 MHz, L=300 nH

Design Basics Summary

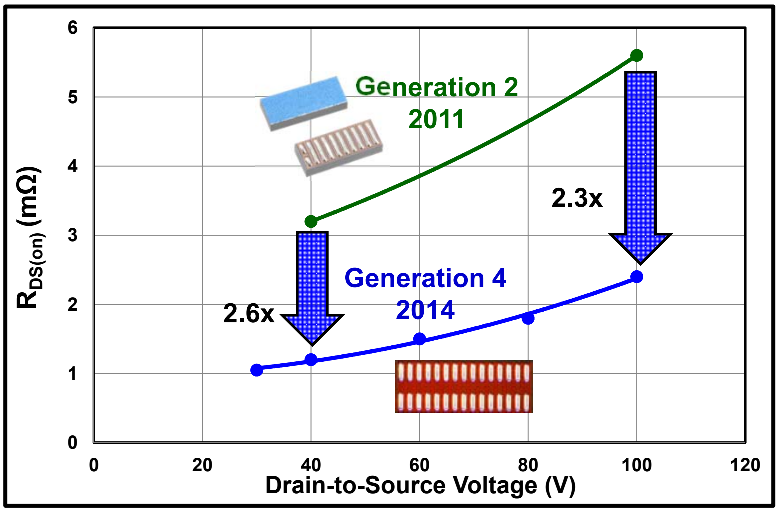
eGaN FETs raise the bar for power conversion performance

- **Lower resistance per die area**
- **Better FOM's give faster voltage commutation**
- **Better Packaging gives faster current commutation**
- **Improved PCB Layout Techniques**
  - **Superior In-Circuit Performance**
  - **Can parallel devices for higher current**
- **Avoid gate overshoot**

A Look Into the Future:

Moore's Law is Alive and Well for GaN FETs

On-Resistance Comparison



V_{GS}=5 V

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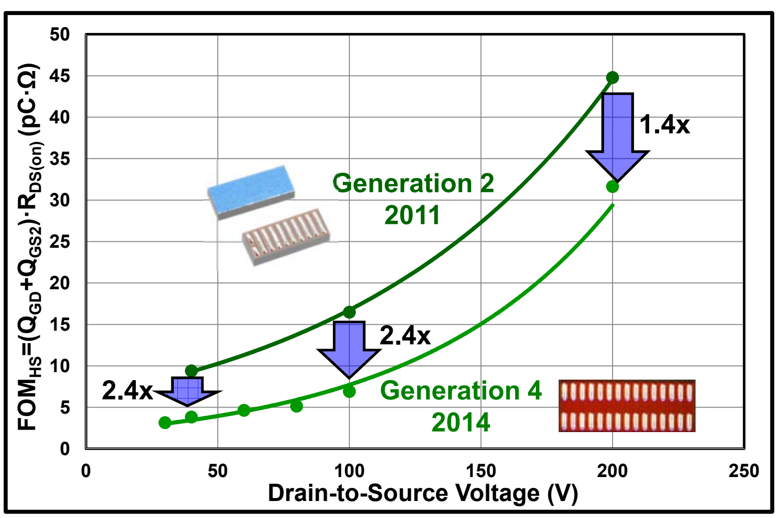
Hard Switching FOM



V_{DS}=0.5·V_{DSS}, I_{DS}=20 A

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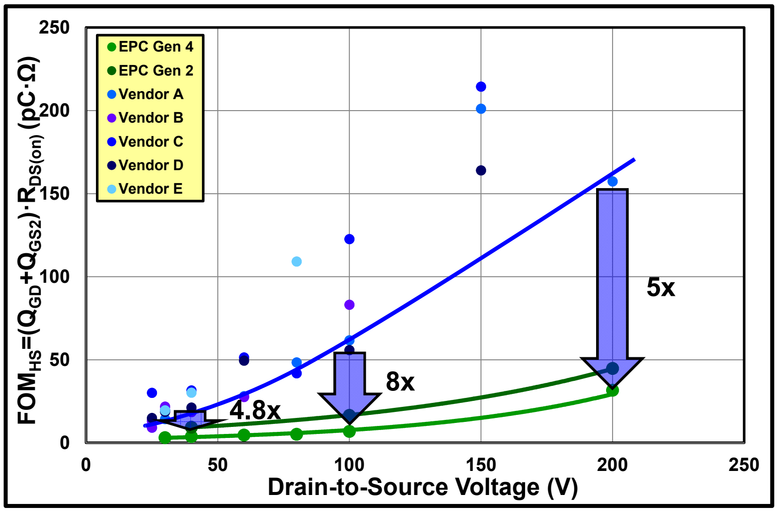
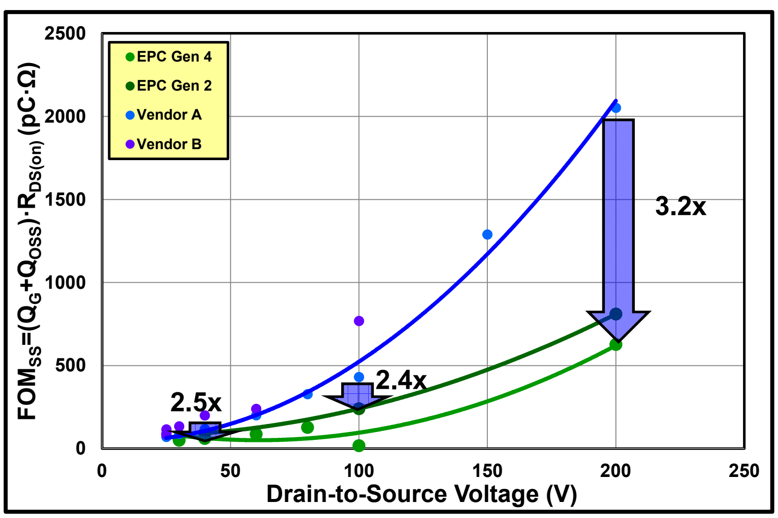
Hard Switching FOM



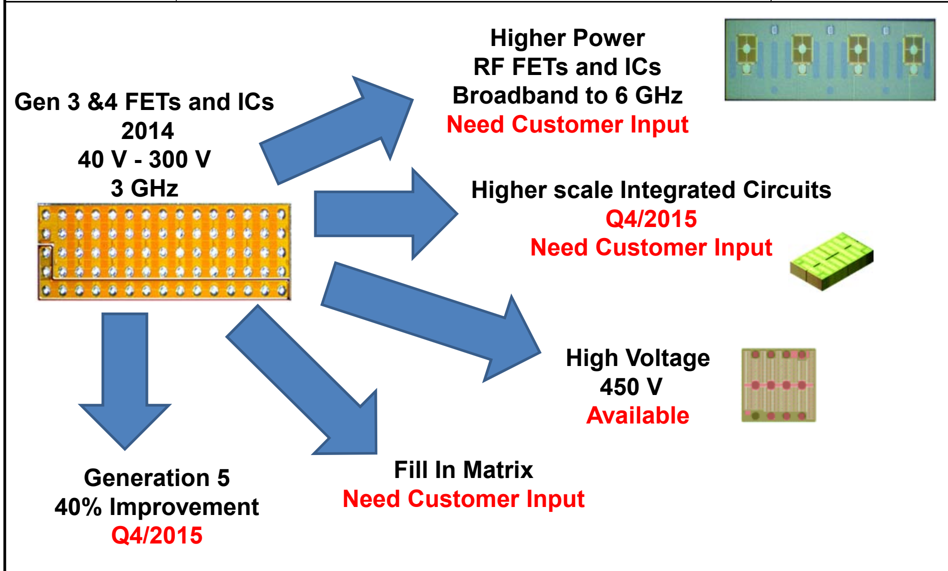
$V_{DS}=0.5 \cdot V_{DSS}$, $I_{DS}=20$ A

Soft Switching FOM



$V_{DS}=0.5 \cdot V_{DSS}$

Looking forward…



Summary

- eGaN FETs continue to improve rapidly – even faster than Moore's Law!
- GaN transistors ***enable exciting new applications*** such as LiDAR, RF Envelope Tracking and Wireless Power Transmission
- GaN transistors have the ***potential to replace silicon power MOSFETs and LDMOS*** in power conversion applications with a low-cost and higher efficiency solution
- eGaN FETs are straightforward to use, but you can't just drop them into a MOSFET socket. ***Some R&D is needed – start today!***

EPC
EFFICIENT POWER CONVERSION

The end of the road for silicon…..

is the beginning of the eGaN FET journey!