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High-Step-Ratio Dual-Active-Bridge Converters for Aerospace and AI Data-Center Power Systems

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Presentation Outline

1. Motivation and Application Drivers

- Aircraft electrification and AI data-center power architectures
- Need for compact, isolated, high-step-ratio DC-DC conversion

2. High-Step-Ratio DAB Development

- Topology selection and design requirements
- LV GaN stage, HV SiC stage, and planar transformer development

3. Parasitic Coupling and Switching Challenges

- Near-field power-to-gate coupling on the LV side
- HV dv/dt propagation through transformer parasitics

4. Mitigation Strategies

- SSAB layout for reduced magnetic coupling
- Transformer redesign for reduced interwinding capacitance

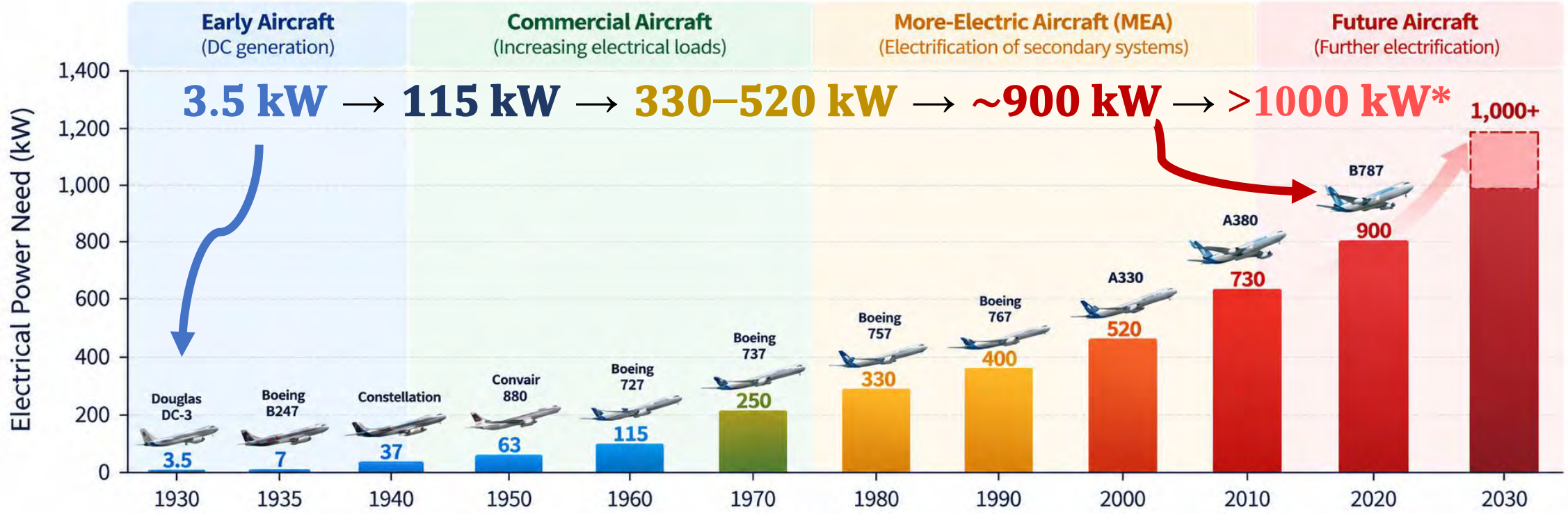
5. Experimental Validation and Outlook

- Maxwell/Q3D, VNA S21, and hardware measurements
- Continuous DAB operation, key findings, and future directions

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Motivation: Growing Electrical Power Demand

- **Progressive electrification of onboard systems has increased aircraft electrical power requirements by more than two orders of magnitude.**



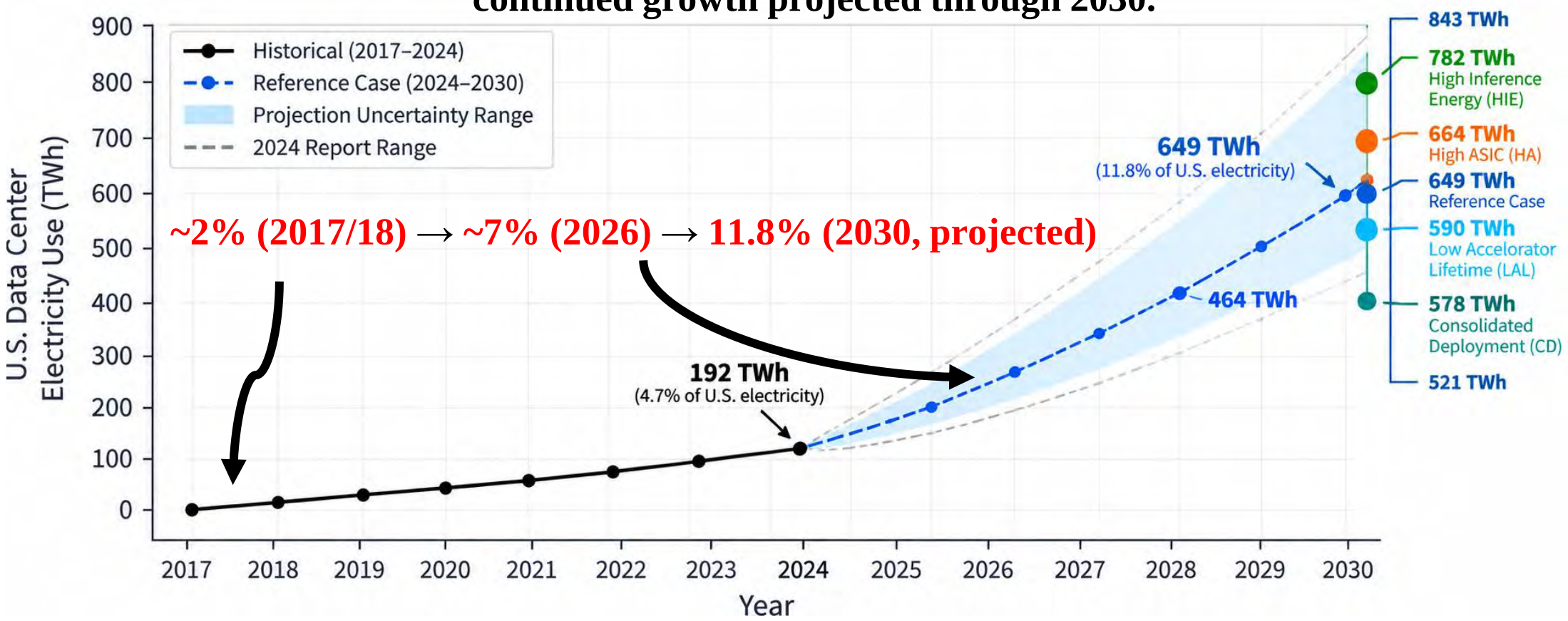
- From **a few kilowatts to near-megawatt levels,** aircraft electrification has fundamentally reshaped onboard power demand since 1930.
- > 250 times growth in electrical power demand

[1] V. Madonna, P. Giangrande, and M. Galea, "Electrical Power Generation in Aircraft: Review, Challenges, and Opportunities," IEEE Trans. Transp. Electrific., vol. 4, no. 3, pp. 646–659, Sep. 2018.
[2] M. Tariq et al., "Aircraft batteries: current trend towards more electric aircraft," IET Electr. Syst. Transp., vol. 7, no. 2, pp. 93–103, Jun. 2017.

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Motivation: Growing Electrical Power Demand

- **AI-driven computing demand is rapidly increasing U.S. data-center electricity use, with strong continued growth projected through 2030.**

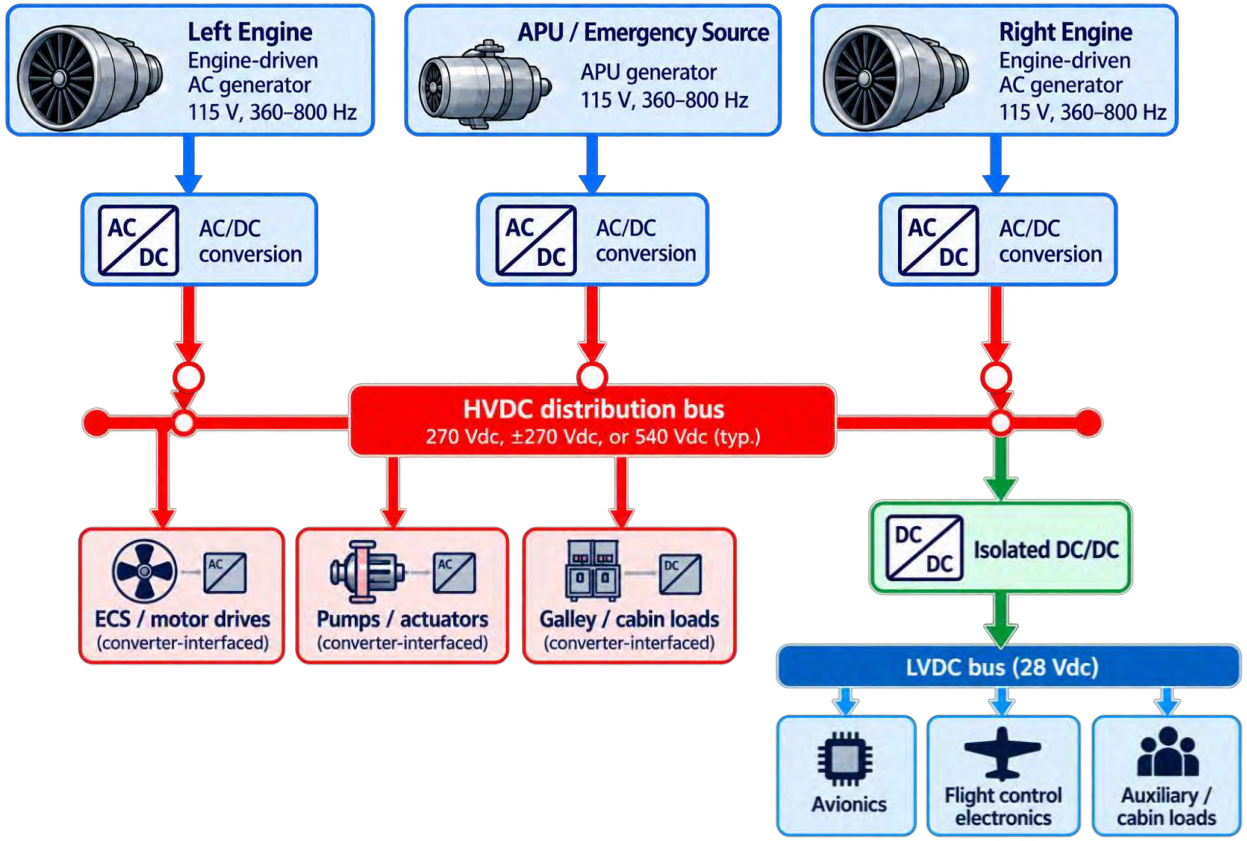


- ✓ **Data centers are projected to grow from roughly 2% (in 2017) of U.S. electricity use to nearly 12% by 2030.**

[1] S. J. Smith, A. Hubbard, A. Newkirk, M. Ganeshalingam, B. Holecek, D. A. Sartor, M. Mills, and A. Shehabi, United States Data Center Energy Usage Report: 2025 Update, Lawrence Berkeley National Laboratory, Berkeley, CA, USA, LBNL-2001758, Jun. 2026.

Motivation: Aircraft Power Architecture

- More Electric Aircrafts (MEA) rely on **HVDC distribution to interconnect multiple power sources, high-power loads**, and **lower-voltage onboard systems.**



- Representative Aircraft HVDC Architecture

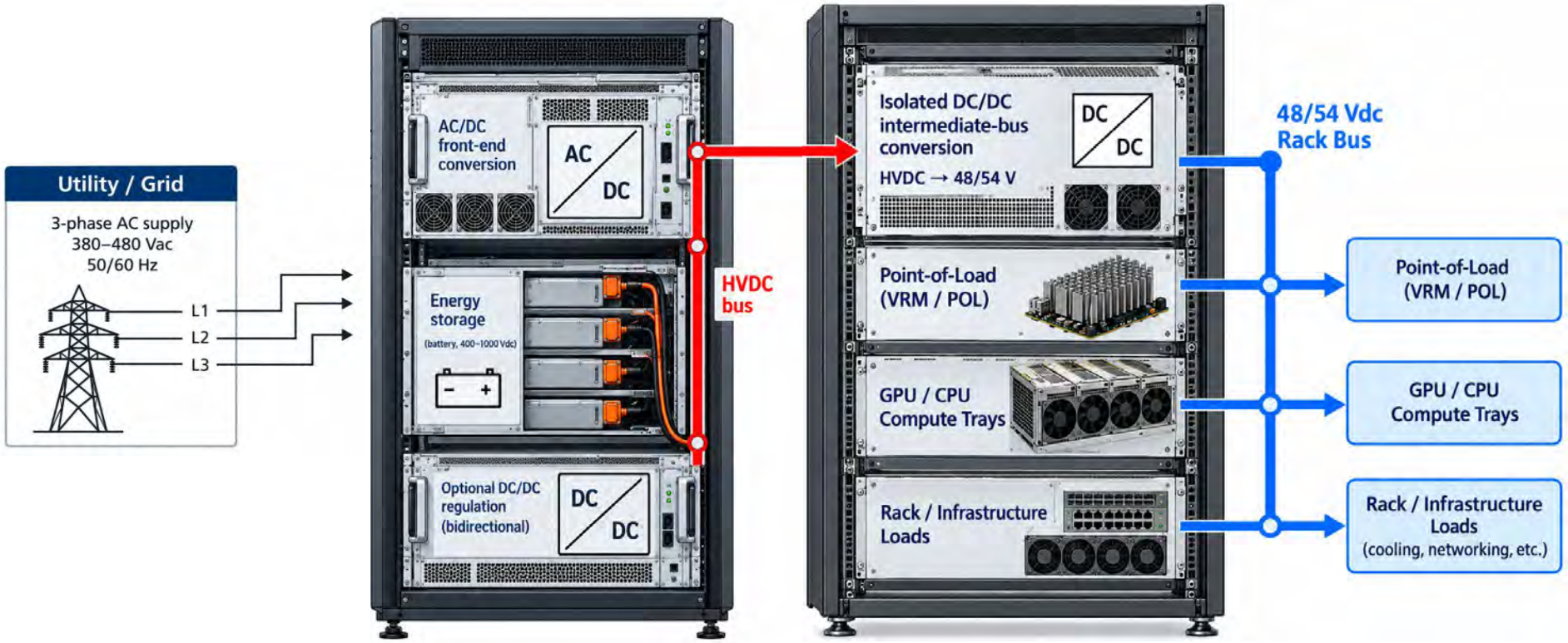
Primary Sources
Engine Generators / APU
↓
Power Conversion
AC/DC Converters
↓
Primary Distribution
HVDC Bus
↓
Two branches

- **Branch 1:**
  HVDC Bus → High-Power Loads
- **Branch 2:**
  HVDC Bus → Isolated DC/DC → **28 V LVDC Bus → Avionics / Electronics**

[1] G. Buticchi, S. Bozhko, M. Liserre, P. Wheeler, and K. Al-Haddad, "On-Board Microgrids for the More Electric Aircraft—Technology Review," IEEE Trans. Ind. Electron., vol. 66, no. 7, pp. 5588–5599, Jul. 2019.
[2] V. F. Barbosa, O. F. A. Eleodoro, D. B. Rodrigues, G. B. Lima, and L. C. G. Freitas, "Three-Phase Hybrid Rectifier for HVDC Distribution System in More Electric Aircrafts," IEEE Trans. Power Electron., vol. 39, no. 1, pp. 1422–1432, Jan. 2024.

Motivation: Aircraft Power Architecture

- **Modern AI data-center power architectures convert utility AC to a high-voltage DC distribution bus, followed by localized conversion near the compute racks.**



Primary Sources
Utility Grid / Battery Backup / Energy Storage
↓
Power Conversion
AC/DC Front-End (PFC)
↓
Primary Distribution
HVDC Bus
↓
Two branches
Branch 1:
HVDC Bus → Rack / Infrastructure Loads
(cooling, networking, storage, etc.)
Branch 2:
HVDC Bus → Isolated DC/DC → **48/54 V Rack Bus → VRM / POL → GPU / CPU Compute Loads**

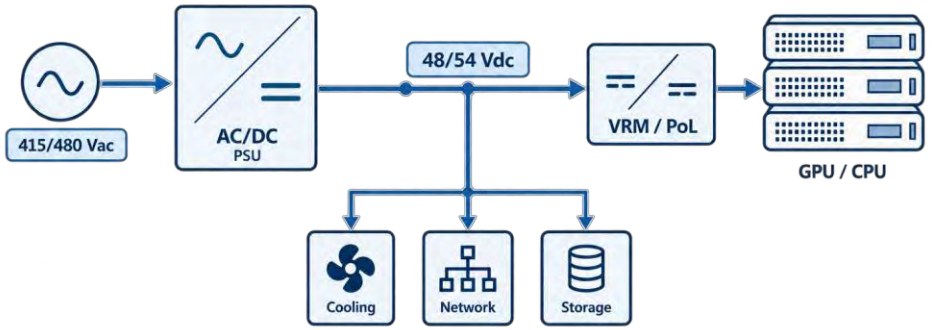
- **Representative AI Data Center Rack Power Architecture**

[1] J. Geng et al., "Vertically Stacked Dual-Bus DC–DC Converter for Data Center High-Current Power Delivery," IEEE TPEL, vol. 40, no. 5, pp. 7002–7014, May 2025.
[2] S. Elangovan et al., "State-of-the-Art Power Electronics in AI Data Centers," IEEE OJPEL, vol. 7, pp. 2434–2463, 2026.
[3] P. R. Prakash and Q. Li, "High-Density, High-Efficiency GaN-Based 800 V/50 V LLC Converter for Future Datacenters," IEEE APEC, pp. 2790–2797, 2026.

Motivation: Evolution of AI Power Distribution Voltage

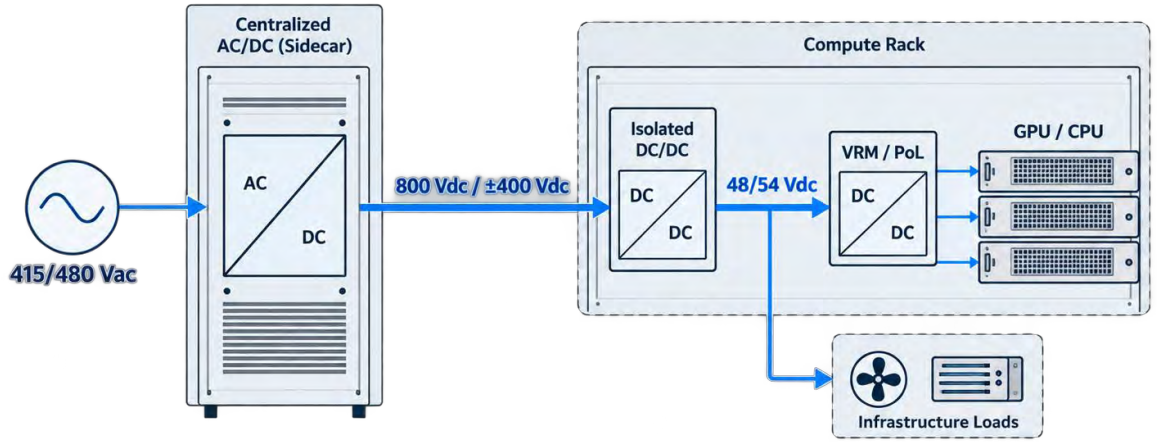
- **Increasing AI rack power is driving data-center power architectures from conventional AC rack distribution toward higher-voltage DC distribution.**

More-Electric Aircraft (MEA)



- 415/480 Vac rack input
- AC/DC PSU → 48/54 Vdc rack bus

Emerging AI HVDC Architecture



- 800 Vdc / ±400 Vdc HVDC distribution
- Isolated DC/DC → 48/54 Vdc → GPU/CPU loads

Rack-Level AC Distribution **Power-Delivery Trend** **800-V-Class HVDC**

- **AI data-center power delivery is shifting toward 800-V-class HVDC distribution as rack power moves into the hundreds-of-kilowatts and toward megawatt-class levels.**

[1] J. Geng et al., "Vertically Stacked Dual-Bus DC–DC Converter for Data Center High-Current Power Delivery," IEEE TPEL, vol. 40, no. 5, pp. 7002–7014, May 2025.
[2] S. Elangovan et al., "State-of-the-Art Power Electronics in AI Data Centers," IEEE OJPEL, vol. 7, pp. 2434–2463, 2026.
[3] P. R. Prakash and Q. Li, "High-Density, High-Efficiency GaN-Based 800 V/50 V LLC Converter for Future Datacenters," IEEE APEC, pp. 2790–2797, 2026.

Motivation: Evolution of Aircraft Distribution Voltage

- **Increasing onboard electrical power demand is driving aircraft power architectures from conventional AC distribution toward higher-voltage DC systems.**

Traditional Aircraft



- 115 Vac, 400 Hz
- Conventional AC distribution

More-Electric Aircraft (MEA)



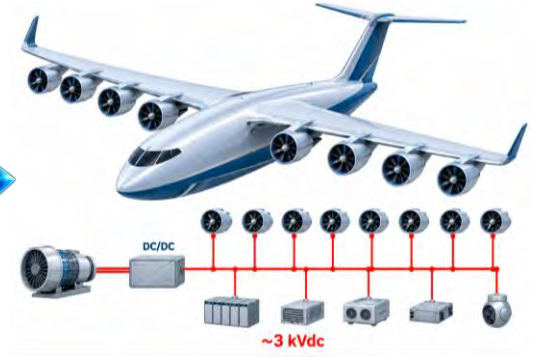
- 270 Vdc / ±270 Vdc / 540 Vdc
- Hybrid AC/DC distribution

Emerging All-Electric Aircraft



- ~800 Vdc High-voltage DC architecture under investigation

Future MW-Class Aircraft



- ~3 kVdc Kilovolt-class DC architecture under investigation

Conventional Distribution — **Power Demand** — **Higher Voltage Distribution**

- **Research trend moves toward higher-voltage HVDC distribution, and around 800 volts DC is emerging as an important currently investigated architecture level.**

[1] G. Buticchi, S. Bozhko, M. Liserre, P. Wheeler, and K. Al-Haddad, "On-Board Microgrids for the More Electric Aircraft—Technology Review," IEEE Trans. Ind. Electron., vol. 66, no. 7, pp. 5588–5599, Jul. 2019.

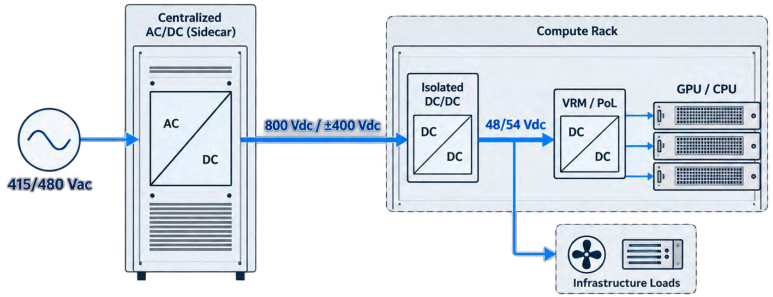
[2] V. F. Barbosa, O. F. A. Eleodoro, D. B. Rodrigues, G. B. Lima, and L. C. G. Freitas, "Three-Phase Hybrid Rectifier for HVDC Distribution System in More Electric Aircrafts," IEEE Trans. Power Electron., vol. 39, no. 1, pp. 1422–1432, Jan. 2024.

Motivation: Evolution of Aircraft Distribution Voltage

➢ **Emerging All-Electric Aircraft**



➢ **Emerging AI HVDC Architecture**



➢ **Both emerging aircraft and AI data-center architectures distribute power at ~800 V, but their load-side buses remain much lower voltage.**

Aircraft: 800 V → 28 V (**~28.6:1**)

AI data center: 800 V → 48/54 V (**~14.8:1–16.7:1**)

✓ **Thus, despite serving different end applications, both domains converge on the same converter-level.**

⬇

? **Challenge: An isolated, bidirectional high-step-ratio DC/DC interface between an ~800-V bus and a low-voltage bus.**

[1] G. Buticchi, S. Bozhko, M. Liserre, P. Wheeler, and K. Al-Haddad, "On-Board Microgrids for the More Electric Aircraft—Technology Review," IEEE Trans. Ind. Electron., vol. 66, no. 7, pp. 5588–5599, Jul. 2019.

[2] P. R. Prakash and Q. Li, "High-Density, High-Efficiency GaN-Based 800 V/50 V LLC Converter for Future Datacenters," IEEE APEC, pp. 2790–2797, 2026.

Selection of High-Step-Ratio Bidirectional DC/DC Topology

➢ **The required topology must combine high step ratio, galvanic isolation, bidirectional power flow, soft switching, control, and high-power density.**

Tab I. Comparison of candidate isolated bidirectional DC/DC topologies

Selection Criterion	DAB	CLLC / LCLC	Current-Fed DAB	Modular / ISOP
Isolation + Bidirectionality	✓✓✓	✓✓✓	✓✓✓	✓✓✓
High Step-Ratio Capability	✓✓✓	✓✓✓	✓✓✓	✓✓✓
Soft-Switching Capability	✓✓	✓✓✓	✓✓✓	✓✓
Control Simplicity	✓✓✓	✓	✓✓	✓
Hardware Simplicity	✓✓✓	✓	✓✓	✓
High-Power / WBG Scalability	✓✓✓	✓✓	✓✓	✓✓✓

➢ **Legend:** ✓✓✓ Excellent ✓✓ Good ✓ Moderate

✓ **DAB SELECTED**

- ➢ **High step-ratio capability**
- ➢ **Bidirectional power flow**
- ➢ **Galvanic isolation**
- ➢ **Simple phase-shift control**
- ➢ **High-frequency WBG operation**
- ➢ **High-power scalability**

? **Challenge: Realizing high step ratio DAB while maintaining high efficiency and controlled switching behavior.**

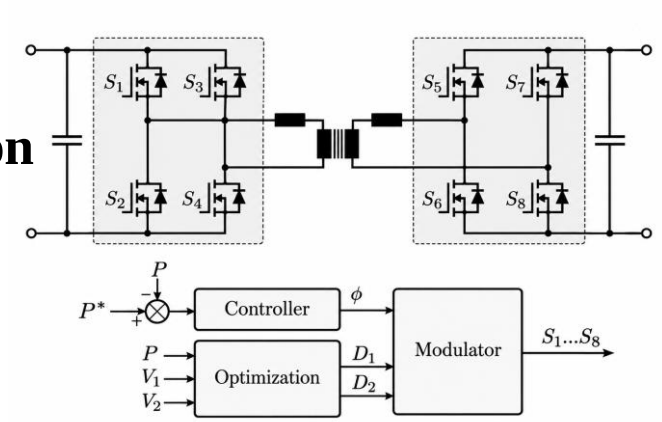
[1] R. W. De Doncker et al., "A Three-Phase Soft-Switched High-Power-Density DC/DC Converter," IEEE Trans. Ind. Appl., vol. 27, no. 1, 1991.
[2] C. Nagesha and N. Lakshminarasamma, "High-Gain Bidirectional LCLC Resonant Converter," IEEE Trans. Power Electron., vol. 38, no. 2, 2023.
[3] Z. Guo et al., "Magnetic Integration of Current-Fed Dual Active Bridge DC–DC Converters," IEEE Trans. Power Electron., vol. 40, no. 8, 2025.
[4] A. Pozo Arribas et al., "ISOP LLC Converter With Integrated Magnetics for Server Power Supplies," IEEE APEC, 2026.

High-Step-Ratio DAB: What Has Been Explored

Extensively Explored in Literature:

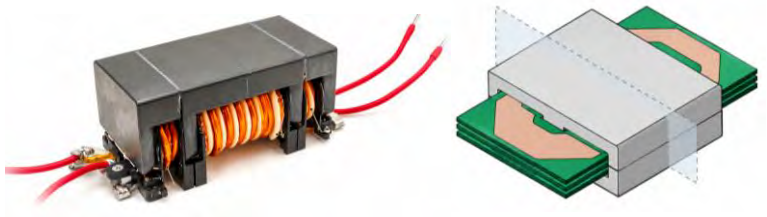
✓ Modulation & Control

- SPS / EPS / DPS / TPS
- Power-transfer regulation
- ZVS range extension
- RMS / peak-current optimization



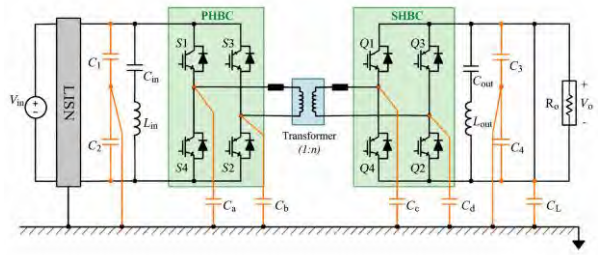
✓ Magnetics

- Leakage-inductance design
- Integrated magnetics



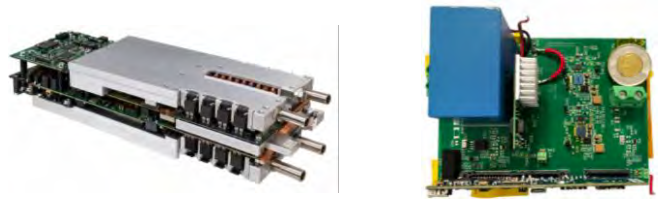
✓ EMI / Parasitics

- CM / DM propagation
- Conducted-EMI modeling



✓ WBG Power Stages

- GaN / SiC switching
- Low-inductance power-loop design
- Gate-drive optimization



? **However, at high step ratio, these traditionally separate design domains become strongly coupled.**

[1] B. Zhao et al., "Overview of Dual-Active-Bridge Isolated Bidirectional DC–DC Converter," IEEE TPEL, 2014.
[2] L. Gong et al., "Dynamic ZVS-Guaranteed Modulation for DAB Converters," IEEE TPEL, 2022.
[3] H. Wouters and W. Martinez, "Integrated Inductor-Transformers for High-Frequency Converters," IEEE TPEL, 2025.
[4] B. Sun et al., "Power Loop Layout and Parasitic Inductance in GaN Implementation," IEEE TIA, 2021.
[5] H. C. P. Dymond *et al.*, "Active Gate Driver for GaN FETs to Combat Overshoot, Ringing, and EMI," *IEEE TPEL*, 2018.
[6] Z. Qin *et al.*, "Transformer Current Ringing in Dual Active Bridge Converters," *IEEE TIE*, 2021.

High-Step-Ratio DAB: Application Space and Research Gap

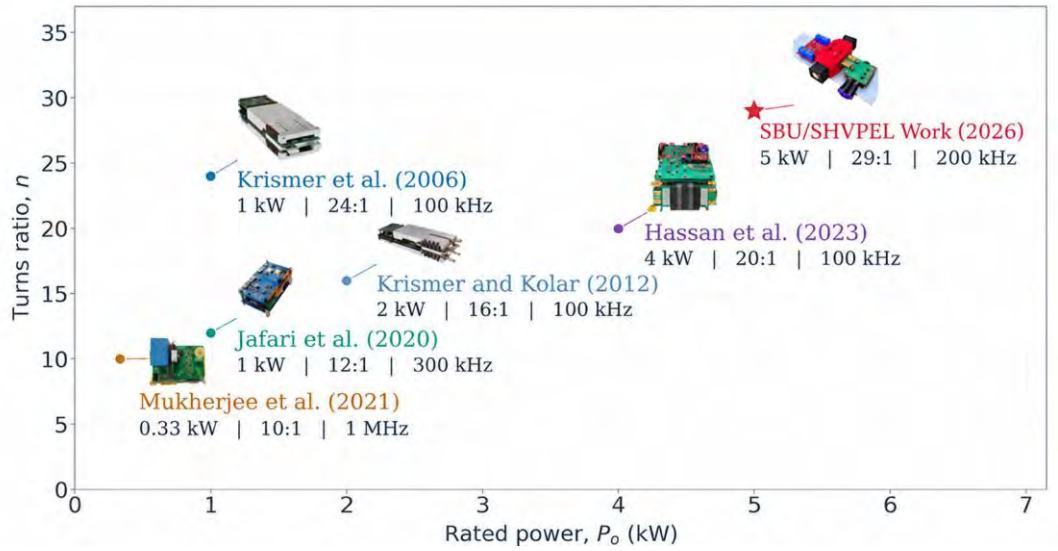
- **Literature becomes increasingly sparse toward the simultaneous high-power, high-step-ratio operating region.**
- **Our target applications push the DAB into high-step-ratio, high-current and high voltage operating region simultaneously.**

? In high-step-ratio DABs

- High dv/dt and high di/dt coexist in the same converter
- Parasitic and electromagnetic coupling become first-order design parameters

Research Need: Limited work systematically identifies high-step-ratio DAB challenges and translates them into design guidelines and mitigation strategies.

- **State-of-the-art high-step-ratio DAB convertors**



SBU/SHVPEL platform: 5 kW | 28 V ↔ 800 V | 200 kHz | 1:29

[1] B. Zhao et al., "Overview of Dual-Active-Bridge Isolated Bidirectional DC–DC Converter," IEEE TPEL, 2014.
[2] L. Gong et al., "Dynamic ZVS-Guaranteed Modulation for DAB Converters," IEEE TPEL, 2022.
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[6] Z. Qin *et al.*, "Transformer Current Ringing in Dual Active Bridge Converters," *IEEE TIE*, 2021.

Converter Development: Device Selection

Problem Statement:

- Need for high-step-ratio power conversion to interface low-voltage distribution buses with emerging high-voltage DC architectures.

Primary Research Objectives:

1. High-Step-Ratio DAB Development

- 28 V to 800 V, 5 kW, 200 kHz, 1:29
- High-frequency transformer + high-current LV GaN stage

2. Identify Design Challenges

- Planar magnetics for high step ratio.
- High LV side current and high di/dt
- High HV side dv/dt.

3. Characterize Coupled Parasitic Effects

- Power-loop-to-gate near-field coupling
- HV-to-LV cross-isolation coupling
- LV conducting-path voltage drop

4. Develop Design Remedies

- Transformer design comparisons and optimization to reduce dv/dt interaction.
- Power stage layout improvement to reduce di/dt interaction

Additional Research Objectives (ongoing):

5. Power Density and Hardware Integration

– **Single PCB integration:** power density ($> 300\ W/in^3$).

Design Specifications:

Parameter	Value
Input Voltage Vin	28
Output Voltage V_{out}	800
Transformer Turns Ratio	1 : 29
Output Power Pout	5 kW
witching Frequency f_{sw}	200 kHz
Target Efficiency	> 97%
LV Side Devices	GaN FETs
HV side devices	SiC MOSFETs
Modulation	Single Phase Shift (SPS)

Converter Development: LV-Side Device Selection

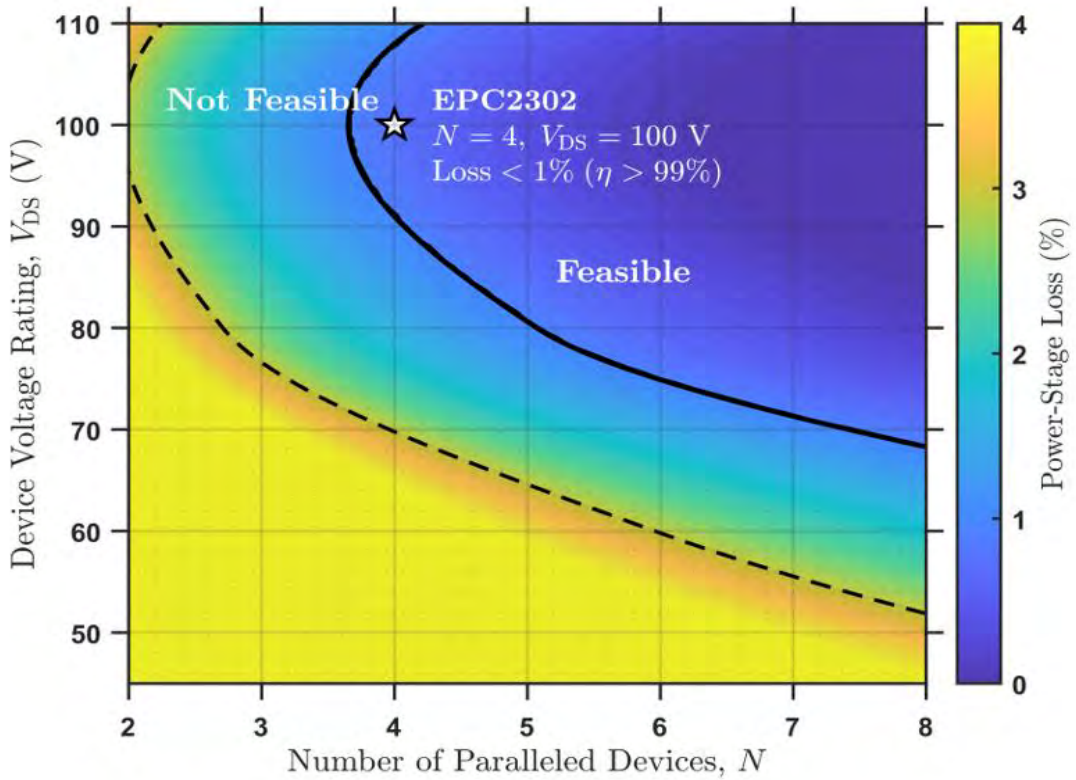
At high current (~180 A), LV-device selection must minimize conduction and reverse-recovery losses while maintaining lowest footprint and lowest thermal resistance.

➢ Comparison of 100-V LV Candidate Switches

Selection Parameter	EPC2302 GaN	CSD19532Q5BT Si MOSFET	RS6P100BHTB1 Si MOSFET
Technology	GaN	Si	Si
VDS	100 V	100 V	100 V
RDS(on)	**1.8 mΩ**	4.6 mΩ	5.9 mΩ
ID,cont	101 A	140 A	100 A
Qrr	**0 nC**	249 nC	260 nC
Coss	1250 pF	706 pF	550 pF
VGS	−4 / +6 V	−20 / +20 V	−20 / +20 V
Vth	1.3 V	2.6 V	2 / 4 V
Footprint	**3 × 5 mm** **15 mm²**	5 × 6 mm 30 mm²	6.0 × 4.9 mm 29.4 mm²
Heat extraction	Top-side cooled	Case / tab	PCB cooled
Rth,JC	**0.2 K/W**	0.8 K/W	1.2 K/W

✓ **Selected LV switch: EPC2302**

➢ PLECS Loss-Based Device Count Selection



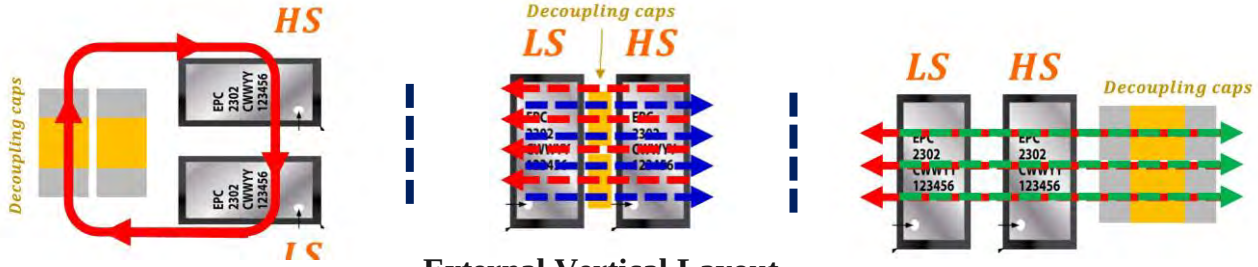
N = 4 satisfies **Ploss, LV < 1%**.

[1] Efficient Power Conversion (EPC), GaN Transistor Fundamentals, Application Note, El Segundo, CA, USA.
[2] A. Muneeb, M. U. Hassan, A. Anwar, and F. Luo, "Design and Analysis of a High Current GaN Based PCB for Dual Active Bridge Converter for Electric Aircraft Applications," Proc. IEEE APEC, 2024, pp. 3135–3139.

LV GaN Power Stage: EPC2302 Device Placement Optimization

With 4× EPC2302 selected per switch position, placement is optimized in two steps: loop geometry and device spacing.

1. Select the Low-Inductance HS–LS Arrangement:



Lateral Layout

- Longer lateral current path

External Vertical Layout

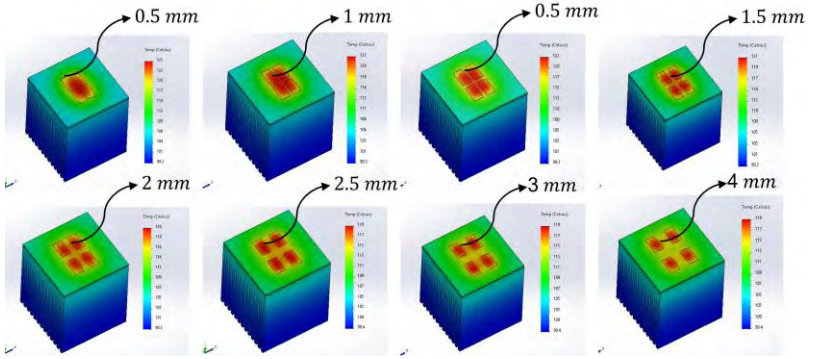
- Loop depends strongly on PCB thickness

✓ Internal Vertical Layout

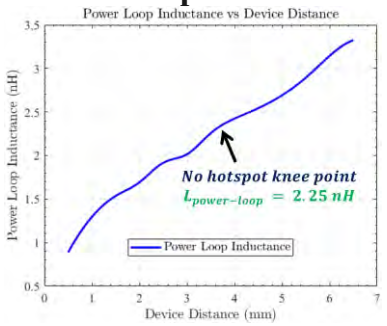
- Overlapped current/return paths provides strongest inductance cancellation

2. Optimize Device Spacing: Thermal Separation vs. Power-Loop Inductance

SOLIDWORKS Thermal Sweep

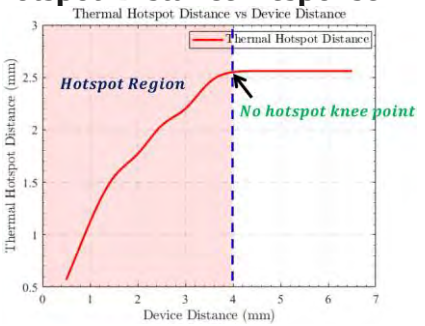


Power-Loop Inductance



Beyond the knee point, power-loop inductance continues to increase with spacing.

Hotspot-Distance Response



Thermal knee occurs near **d ≈ 3.5 mm**.

Hotspot separation improves with spacing.

✓ **Internal vertical arrangement selected for the lowest power-loop inductance.**

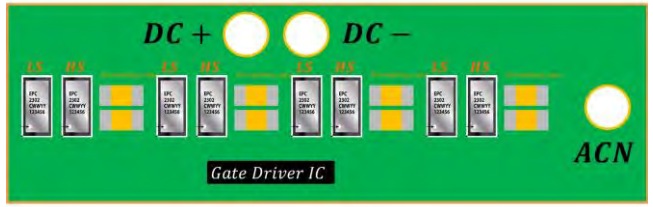
✓ **Final selected placement: Internal-vertical HS–LS arrangement with d = 4 mm spacing.**

[1] A. Muneeb, M. U. Hassan, A. Anwar, and F. Luo, "Design and Analysis of a High Current GaN Based PCB for Dual Active Bridge Converter for Electric Aircraft Applications," IEEE APEC, 2024, pp. 3135–3139.
[2] D. Reusch and J. Strydom, "Understanding the Effect of PCB Layout on Circuit Performance in a High Frequency Gallium Nitride Based Point of Load Converter," IEEE APEC, 2013.

LV GaN Power Stage: Parallel-Device Arrangement

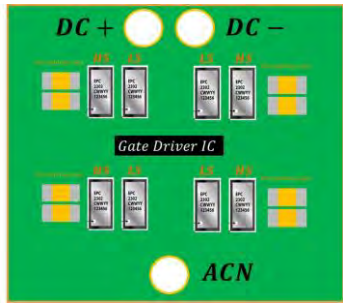
With 4× EPC2302 and 4 mm HS–LS spacing established, the parallel branches must maintain symmetric electrical paths for simultaneous switching and balanced current sharing.

➢ **Literature Survey: Device Paralleling Layout Comparison**



➢ **Lateral Paralleling Layout**

✓ Straightforward implementation
✓ Unequal branch path lengths
? Current-sharing imbalance
? Gate drive path imbalance

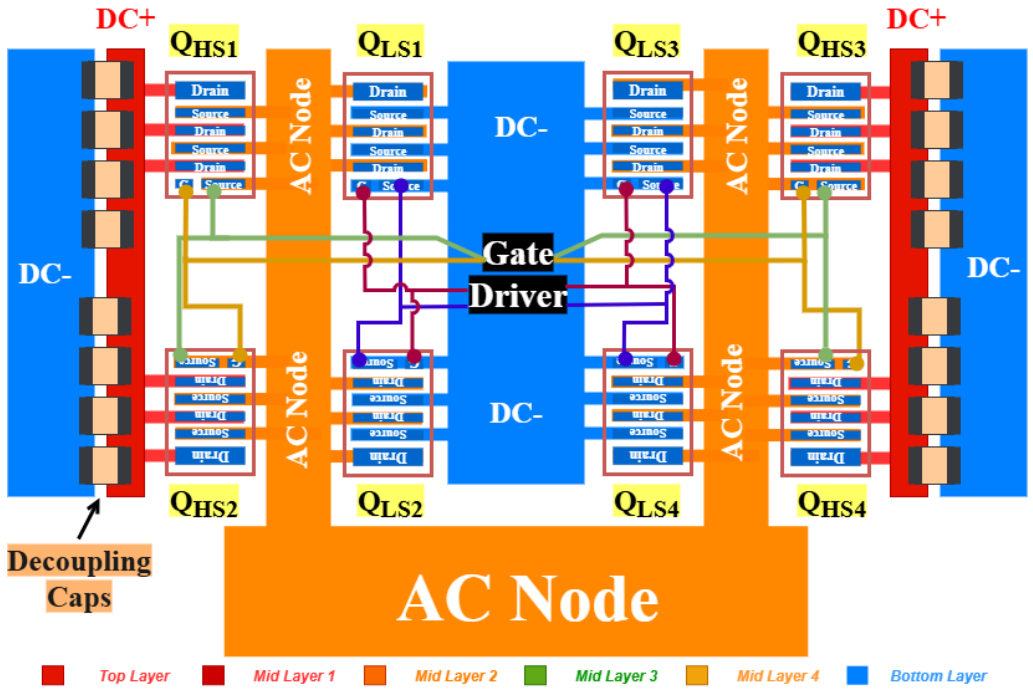


➢ **Butterfly Paralleling Layout**

✓ Symmetric layout
✓ Better current sharing
✓ Middle ground (DC-/return) island for gate drive
✓ Gate drive path symmetry
? Routing complexity

✓ **Selected LV paralleling structure: Symmetrical Butterfly Layout**

➢ **Representative Butterfly Layout**



➢ **4x identical cells surround the central gate-driver / common-return region, preserving branch symmetry.**

[1] Efficient Power Conversion (EPC), GaN Transistor Fundamentals, Application Note, El Segundo, CA, USA.
[2] M. Wattenberg, O. Lorenz and J. Sanchez, "Efficiently Paralleling GaN-Transistors for High Current and High Frequency Applications Using a Butterfly Layout," 2022 24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe), Hanover, Germany, 2022, pp. 1-10.

LV GaN Power Stage: High-Current PCB Implementation

➢ **The selected 4× EPC2302 butterfly arrangement must now carry the rated LV current through the device pads and PCB with low electrical and thermal resistance.**

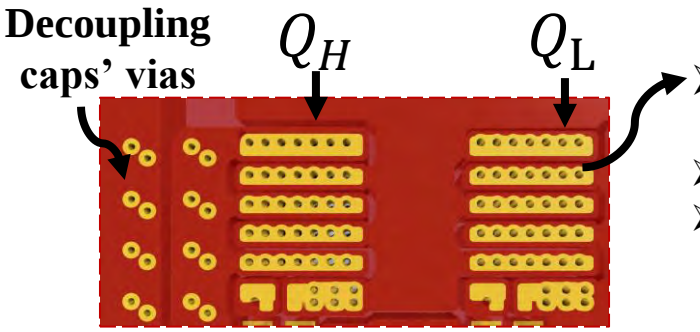
➢ **Layer thickness/count**

EPC2302 current-pad width: 0.37 mm → current must be spread through parallel PCB layers.

Candidate	Parallel Cu Layers	Copper Weight	Assessment
A	20	2 oz	High layer count
B	**8**	**3 oz**	**Selected**
C	6	4 oz	Higher Cu weight

8 layers × 3 oz Cu selected implementation as per IPC-2221.

➢ **Device-Pad Current & Thermal Spreading**

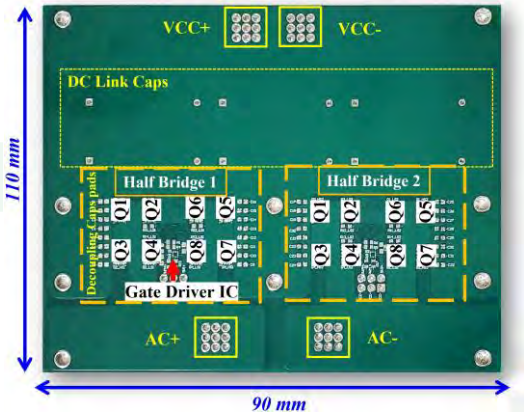


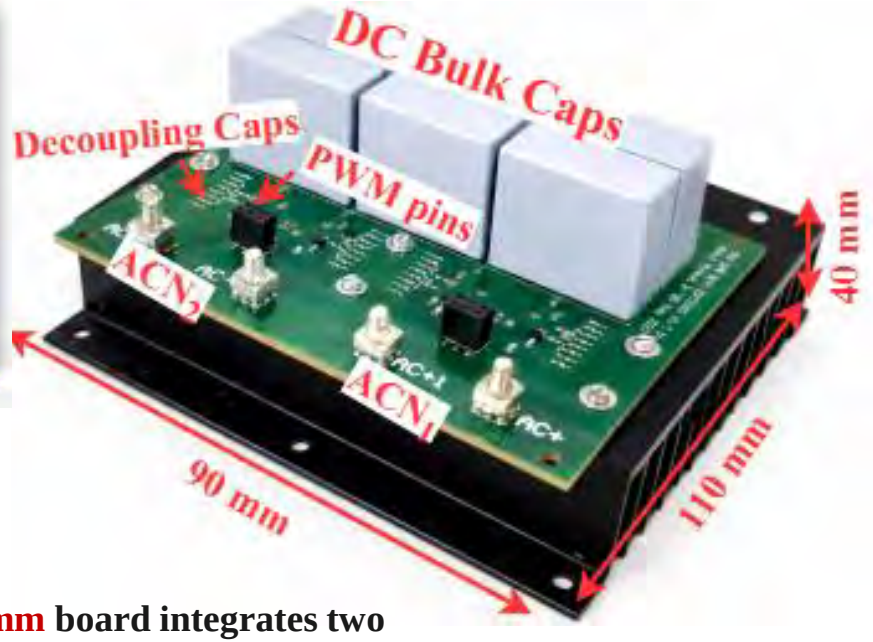
➢ **On-pad vias** connect the compact EPC2302 pads directly into the parallel copper layers.

➢ **33% lower current-transfer resistance [1]**

➢ **Improved heat spreading**

➢ **Final LV Power-Stage Realization**





90 mm × 110 mm x 40 mm board integrates two symmetric half-bridges, DC-link / decoupling capacitors, and the gate-driver region.

✓ **Final LV PCB implementation: 8-layer, 3-oz Cu + on-pad vias + symmetric butterfly routing for high-current operation.**

[1] Efficient Power Conversion (EPC), GaN Transistor Fundamentals, Application Note, El Segundo, CA, USA.

[2] M. Wattenberg, O. Lorenz and J. Sanchez, "Efficiently Paralleling GaN-Transistors for High Current and High Frequency Applications Using a Butterfly Layout," 2022 24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe), Hanover, Germany, 2022, pp. 1-10.

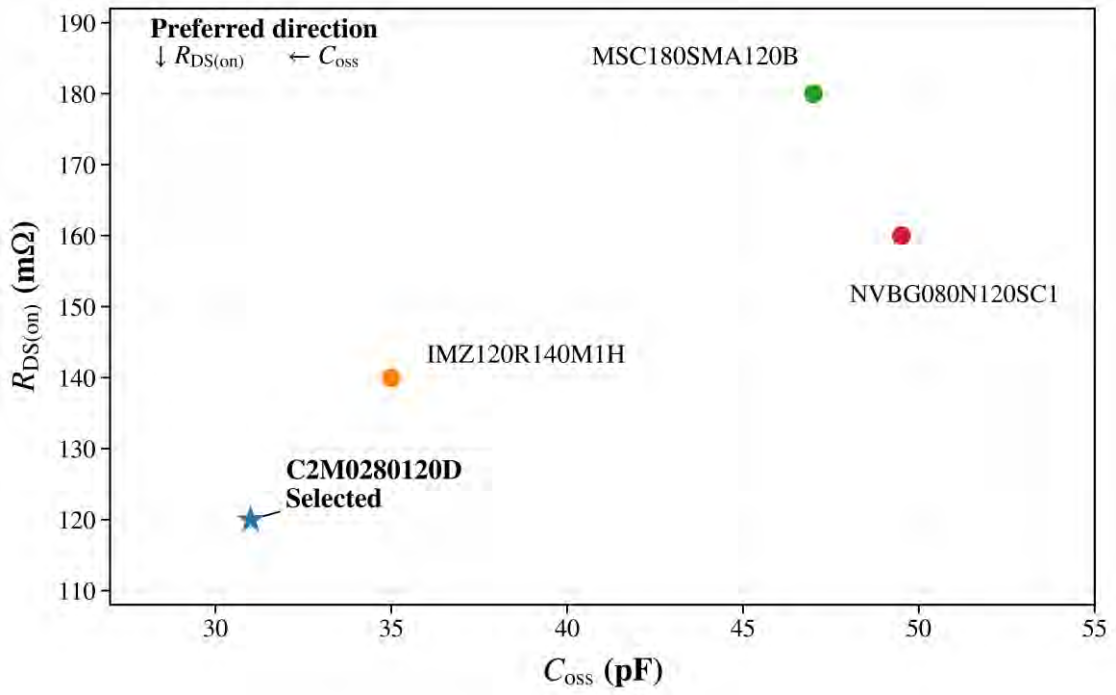
Converter Development: HV-Side Device Selection

- **At 800 V and ~6–7 A, HV-side device selection is driven primarily by switching loss so HV side switch should be selected to minimize C_{oss} along with the Rds_{on}**

- **Comparison of HV Candidate Switches**

Selection Parameter	C2M0280120D Wolfspeed	NVBG080N120SC1 onsemi	MSC180SMA120B Microchip	IMZ120R140M1H Infineon
VDS	1200 V	1200 V	1200 V	1200 V
RDS(on)*	**120 mΩ**	160 mΩ	180 mΩ	140 mΩ
Coss*	**31 pF**	49.5 pF	47 pF	35 pF
Qg*	19 nC	34 nC	36 nC	13 nC
Package	TO-247-3L	D2PAK-7L	TO-247-3L	TO-247-4
Kelvin / driver source	No	Yes	No	Yes
Selection assessment	**Best overall balance**	Low RDS(on), higher Coss/Qg	Highest RDS(on)/Qg	Lowest Qg, slightly higher Coss

- **Loss-Relevant Device Trade Space**



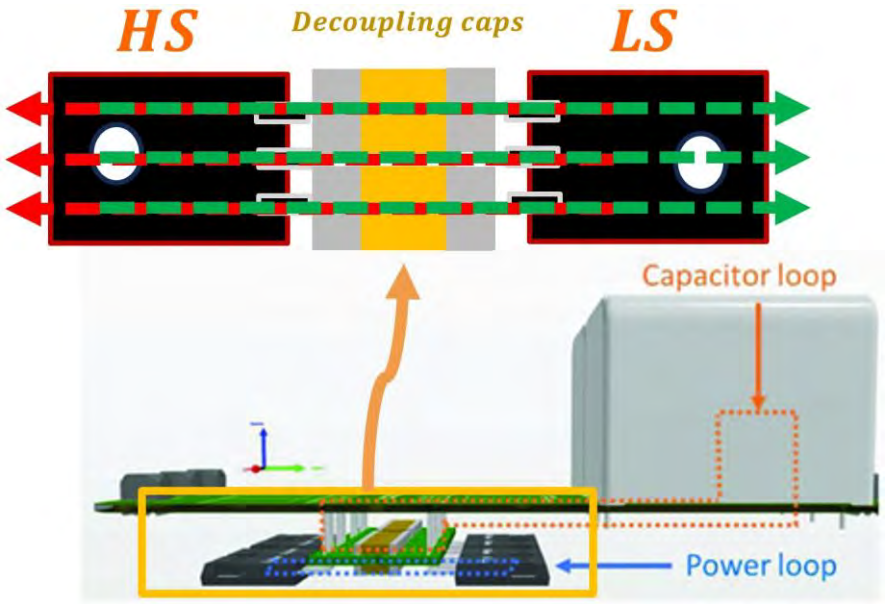
✓ **Selected HV switch: C2M0280120D**

[1] X. Li et al., IEEE WiPDA, 2015, pp. 257–262.
[2] X. Li et al., IEEE ISPSD, 2019, pp. 231–234.
[3] Manufacturer datasheets: C2M0280120D, NVBG080N120SC1, MSC180SMA120B, IMZ120R140M1H.

HV SiC Power Stage: Power-Loop Layout Optimization

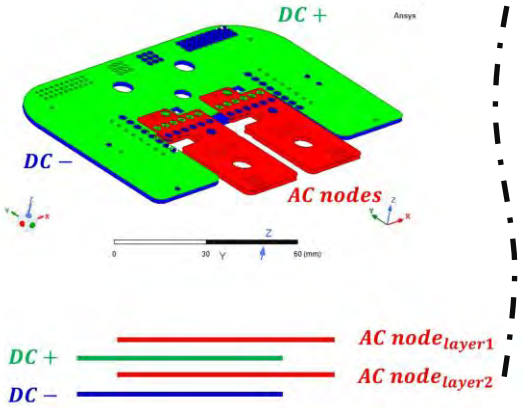
➢ **With the 1200-V SiC switch selected, the HV power stage is optimized in two steps: power-loop geometry and PCB stack-up.**

➢ **Literature Study: Low-Inductance Power-Loop Geometry**

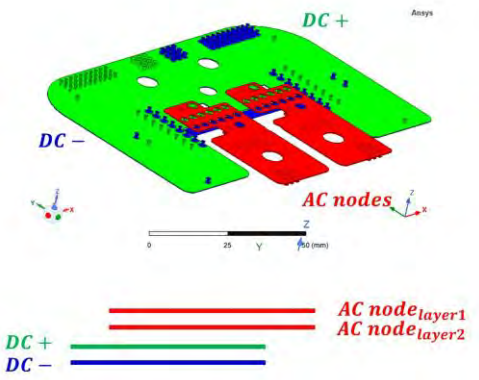


➢ **Literature Study: Low-Inductance Power-Loop Geometry**

➢ **Interleaved**



➢ **Non-Interleaved**



$L_{power-loop}$	$C_{PCB}: DC+ \rightarrow AC$	$Stack-Up$	$Stack-Up$
Interleaved	1.37 nH	73.87 pF	67.77 pF
Non-interleaved	3.77 nH	10.004 pF	7.800 pF

✓ **Lateral TO-247 Arrangement: Decoupling caps are placed directly between HS and LS devices to form a short power-loop path.**

➢ **C_{PCB} eventually increases the switching losses which are dominant on the HV side.**

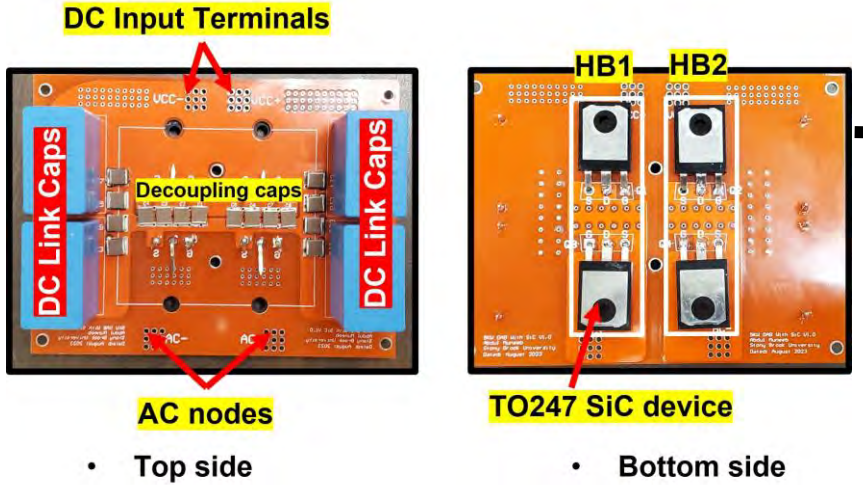
✓ **Non-interleaving Selected: It increases power-loop inductance from 1.37 nH → 3.77 nH, however reduces C_{PCB} by 86.5% / 88.5%.**

[1] Z. Chen, C. Chen, Q. Huang, and A. Q. Huang, "Design of High Power Converter with Single Low R_{on} Discrete SiC Device," IEEE WiPDA, 2022, pp. 209–214.
[2] X. Li et al., "Understanding Switching Losses in SiC MOSFET: Toward Lossless Switching," IEEE WiPDA, 2015, pp. 257–262.

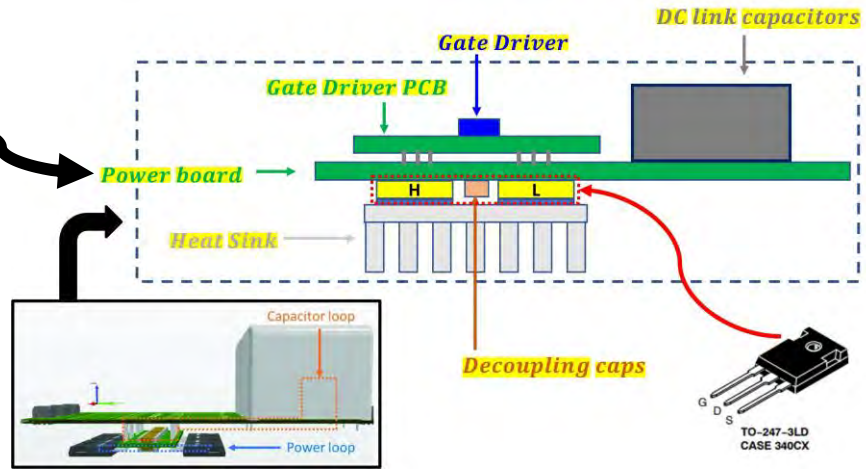
HV SiC Power Stage: Power-Loop Layout Optimization

➢ **With the power-loop geometry and PCB stack-up established, the final HV implementation now focuses on minimizing the gate loop and integrating the isolated driver.**

➢ **Directly integrated HV power stage**



➢ **HV Power PCB and Physical Stack**



✓ DC-link and **decoupling capacitors** are kept close to the two half-bridges to preserve the short power-loop and commutation loops.

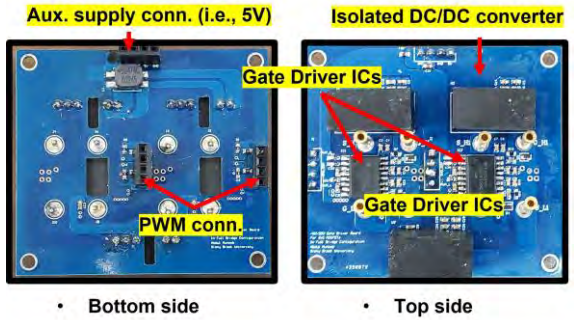
✓ **Gate-driver PCB sits directly on the SiC pins → minimum gate-loop length**.

➢ **Comparison of the Gate Drive ICs**

Parameter	NCV51563	UCC21530-Q1
Isolation voltage	5000 Vrms	**5700 Vrms**
CMTI	>200 V/ns	**>100 V/ns**
Peak source current	4.5 A	**4 A**
Rise / fall time	11 / 10 ns	**6 / 7 ns**

✓ **Selected: UCC21530-Q1** → 6 ns / 7 ns rise-fall times and 5700-Vrms isolation.

➢ **Designed isolated gate-driver PCB**



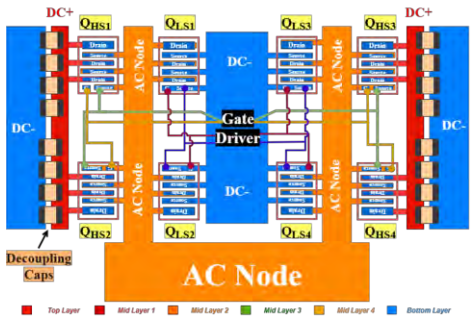
✓ **Final HV architecture: optimized SiC power board + directly mounted UCC21530-Q1 driver board → short commutation and gate-drive loops.**

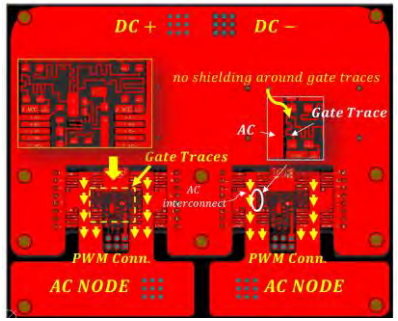
[2] Texas Instruments, "UCC21530-Q1 4-A/6-A, 5.7-kV$_{RMS}$ Isolated Dual-Channel Gate Driver," Datasheet.
[3] Murata Power Solutions, "MGJ2 Series 5.2-kVDC Isolated Gate-Drive Power Supply," Datasheet.

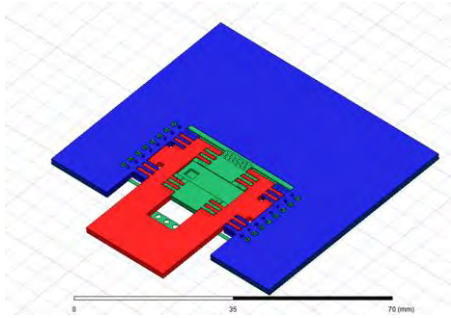
LV GaN Power Stage: Q3D Extraction and DPT Validation

After completing the LV GaN-side hardware, Q3D extraction and DPT were used to verify the power-loop parasitics and the measured switching transient.

➢ **Ansys Q3D Parasitic Extraction**





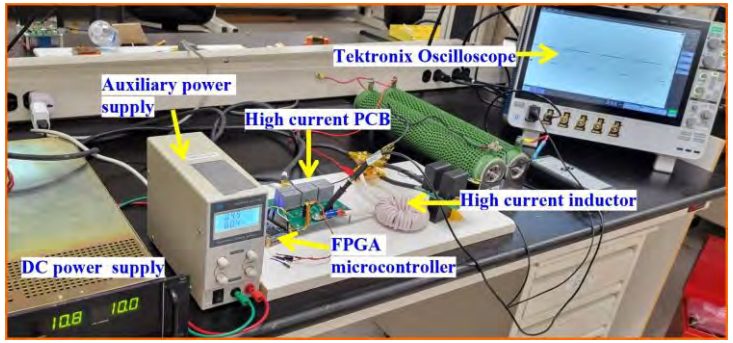


➢ **Butterfly Paralleling Layout**

➢ **Design of the PCB Layout: Altium PCB Designer**

➢ **Simplified power loop geometry in Ansys Q3D environment**

➢ **DPT and Switching-Model Correlation**

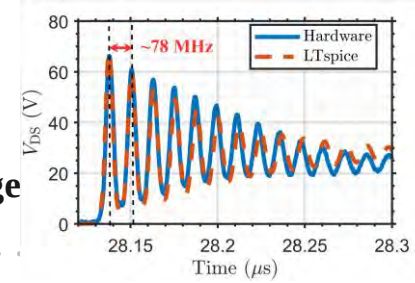


➢ **LV DPT hardware setup**

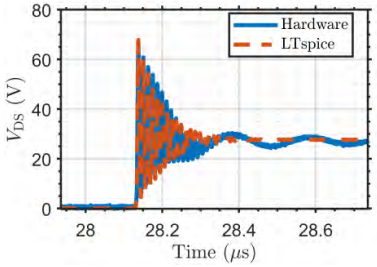
Extracted Parameter	Result
Power-loop inductance	≈ 3.2 nH / bridge
CPCB, DC±→AC	≈ 62–78 pF
EPC2302 Coss	≈ 1200 pF / device

$V_{DS,peak}$ ≈ 66.26 V | f_{ring} ≈ 78 MHz | di/dt ≈ 7.5 A/ns per half bridge
4× effective di/dt ≈ 30 A/ns | LV dv/dt ≈ 4 V/ns

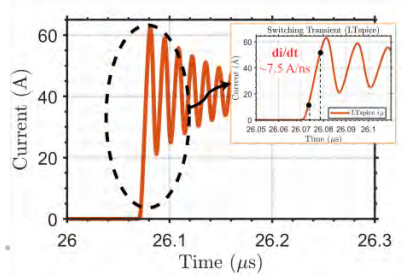
➢ **Ringing-frequency correlation**



➢ **Measured switching transition**



➢ **I_d and di/dt**

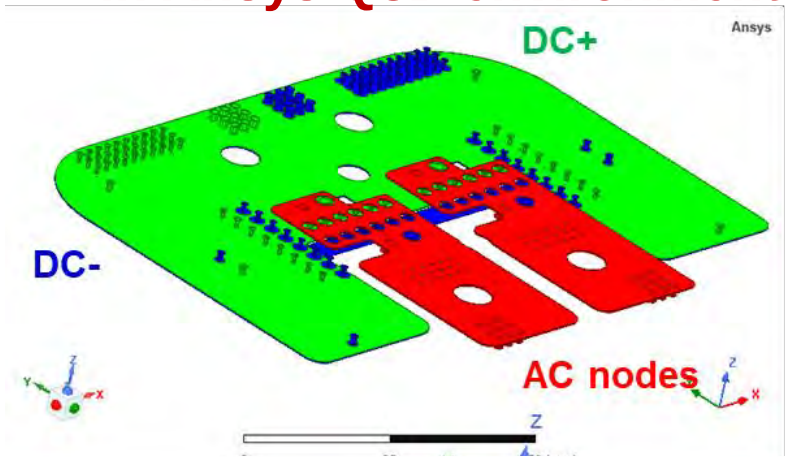


FAR BEYOND

HV SiC Power Stage Characterization with DPT

➢ The final non-interleaved HV board was characterized using Q3D and DPT.

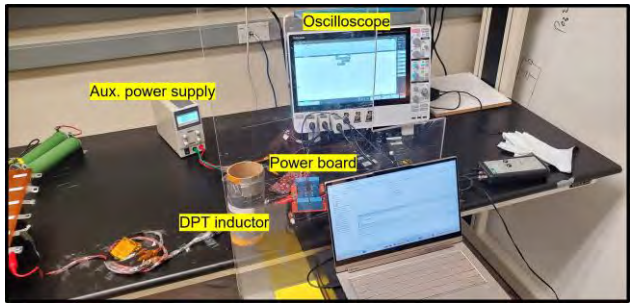
➢ **Simplified power loop geometry in Ansys Q3D environment**

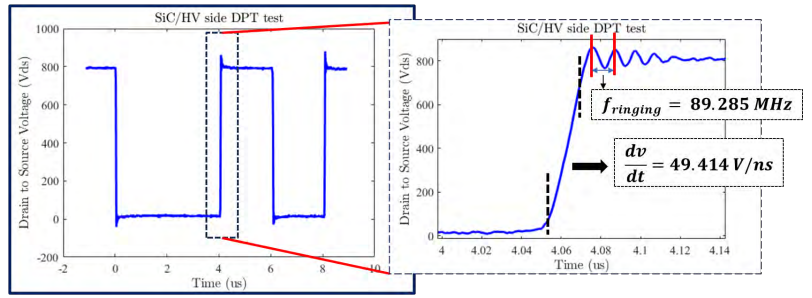


Extracted Parameter	Result
Power-loop inductance	3.77 nH
CPCB: DC+→AC	10.004 pF
CPCB: DC−→AC	7.800 pF

CPCB reduction: 141.64 → 17.80 pF (−87.4%)
PLECS loss simulation: 51.4 → 35.6 W (−30.8%)

➢ **Double-Pulse Test at 800 V**





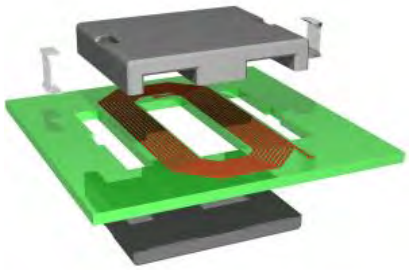
Measured Metric	DPT Result
dv/dt	49.414 V/ns
di/dt	6.9 A/ns
Ringing frequency	89.285 MHz
Bus voltage	800 V

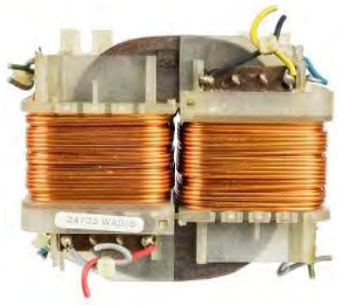
➢ **Ringing-Frequency Validation** $f_{ring} \approx 89.3\ MHz$ confirms the **combined $C_{oss} + C_{PCB}$ and L_{eff}, dominated by TO-247 lead** inductance (15– 20nH) over PCB inductance (3.77nH).

[1] A. B. Mirza, A. Castiblanco, A. Muneeb, Y. Xie, S. S. Vala and F. Luo, "Impact of PCB Parasitic Capacitance on Switching Transients in Chopper and Half-Bridge Configurations Utilizing TO-247 SiC Devices," in IEEE Transactions on Industry Applications, vol. 61, no. 4, pp. 6618-6631, July-Aug. 2025,

High-Step-Ratio Transformer: Planar Magnetics Selection

At 5 kW, 200 kHz and 1:29, the transformer must combine high-frequency operation, high LV current and high HV turn count within a compact isolated structure.





PCB-Based Planar	Traditional Wire-Wound
Low-profile structure	Higher profile
Controlled PCB geometry	More assembly dependent
Highly repeatable	More difficult to reproduce
Well suited to PCB integration	More complex
Structured and reproducible	More assembly dependent

For High Step Ratio DAB:

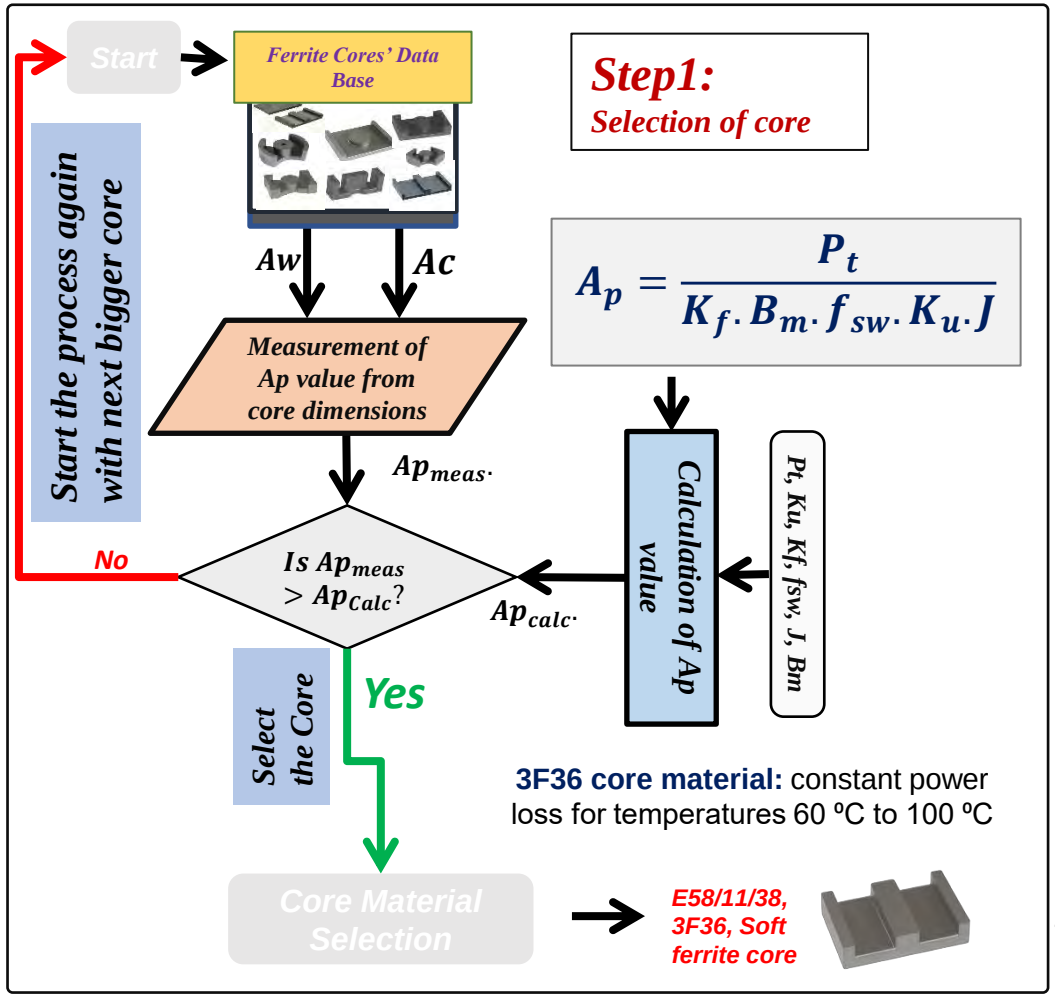
- ? **Leakage Inductance**
  → directly affects DAB transfer gain
- ? **Winding Resistance / AC Loss**
  → high LV current + long HV winding
- ? **Parasitic Capacitance**
  → increases with PCB-layer overlap / interleaving

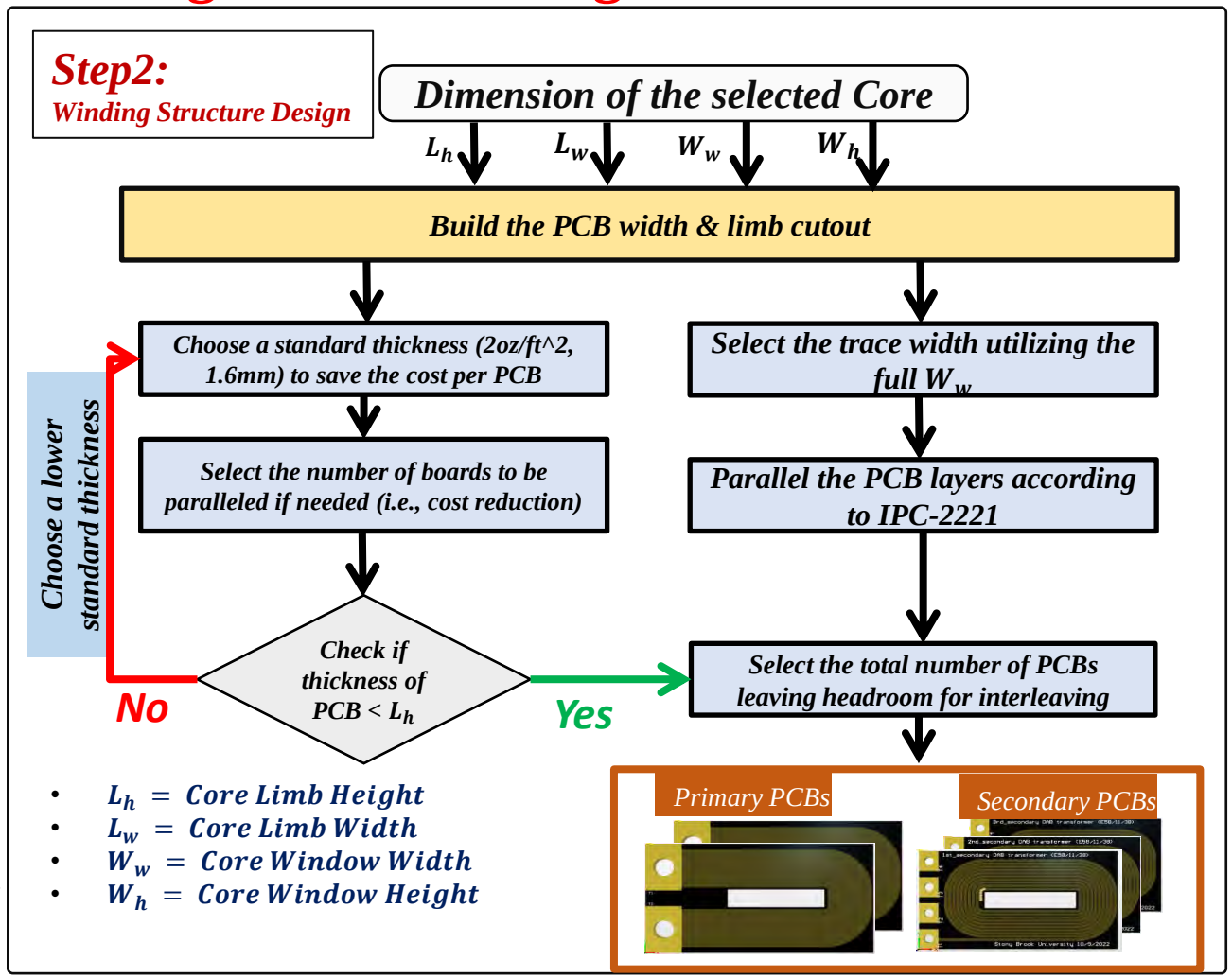
➢ **These Challenges can become layout design bottlenecks and can get exacerbate at higher step ratios: needs geometry-based comparison for initial design selection.**

[1] A. B. Mirza, A. Castiblanco, A. Muneeb, Y. Xie, S. S. Vala and F. Luo, "Impact of PCB Parasitic Capacitance on Switching Transients in Chopper and Half-Bridge Configurations Utilizing TO-247 SiC Devices," in IEEE Transactions on Industry Applications, vol. 61, no. 4, pp. 6618-6631, July-Aug. 2025,

High-Step-Ratio Planar Transformer: Two-Step Design Flow

➢ **The 1:29 planar transformer is developed in two sequential steps: core selection followed by PCB winding-structure design.**

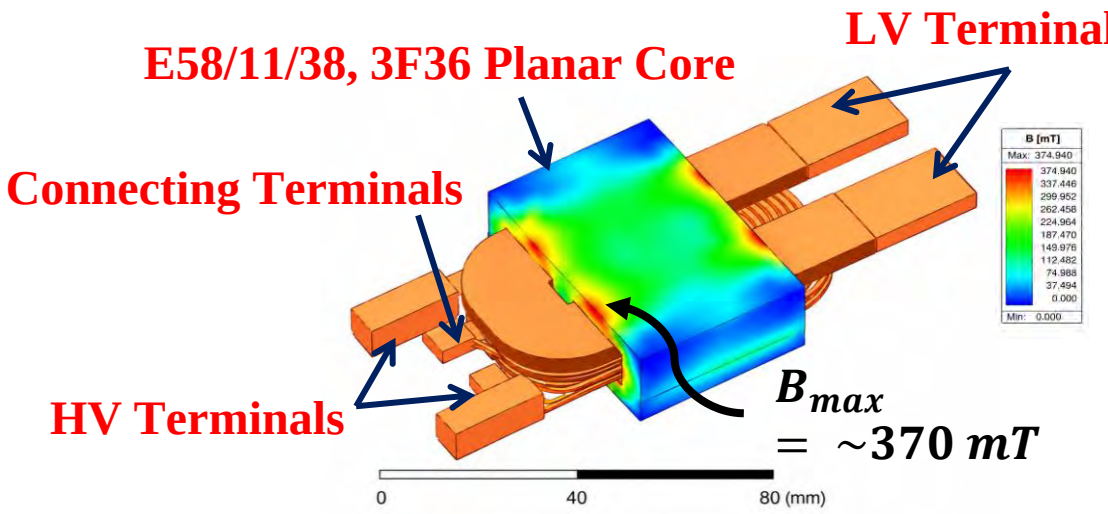


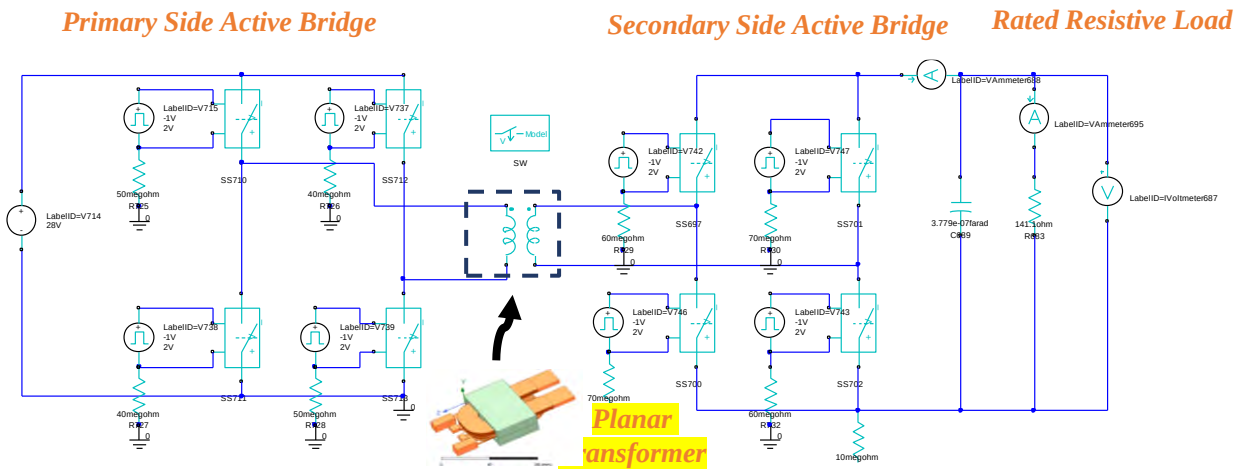


High-Step-Ratio Planar Transformer: FEA Analysis

FEA transient simulations were performed with the complete DAB model to compare transformer winding arrangements and quantify their loss impact.

- Transformer in FEA environment
- FEA Transient Solver circuit simulation setup





Two extreme cases has been simulated:

Case 1: No interleaving
(LV and HV windings are placed apart)

Case 2: Full interleaving
(LV and HV windings are placed on top of each other)

Parameters	Case 1	Case 2	%age Change
$P_{loss\,LV}$	51.88 W	39.75 W	23.3 %
$P_{loss\,HV}$	76.68 W	51.88 W	32.3 %
$CoreLoss$	20.77 W	29.55 W	42.2 %

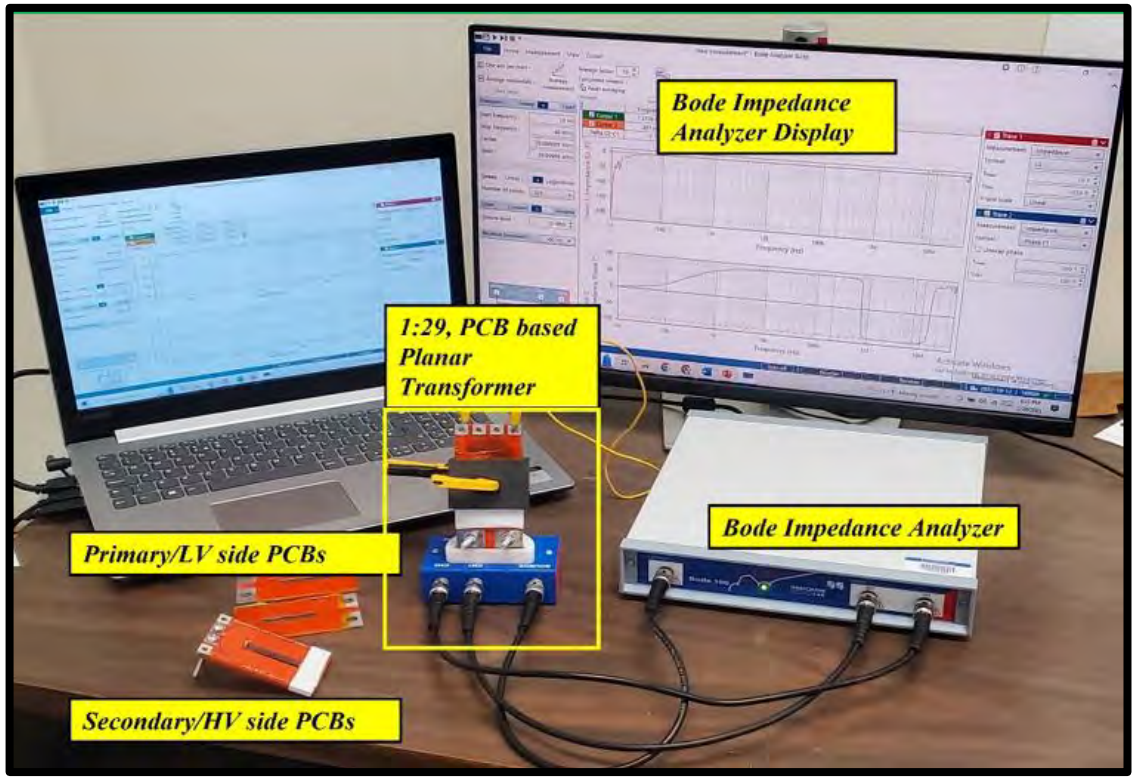
- Transformer power efficiency
  - Case 1: 97.02%
  - Case 2: 98.10%
- ✓ Selected Case 2: Full interleaving

[1] A. B. Mirza, A. Castiblanco, A. Muneeb, Y. Xie, S. S. Vala and F. Luo, "Impact of PCB Parasitic Capacitance on Switching Transients in Chopper and Half-Bridge Configurations Utilizing TO-247 SiC Devices," in IEEE Transactions on Industry Applications, vol. 61, no. 4, pp. 6618-6631, July-Aug. 2025,

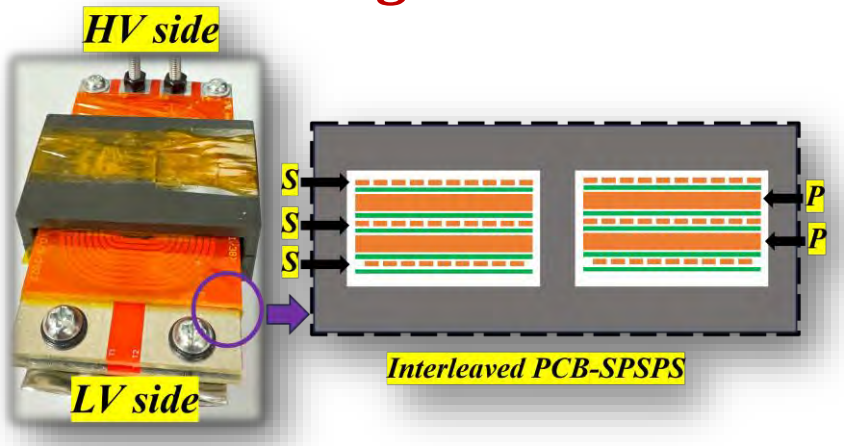
High-Step-Ratio Planar Transformer: Characterization

- **Interleaved winding structure SPSPS winding structure was prototyped and characterized with the Bode 100 Analyzer.**

Impedance Analysis Setup



PCB-SPSPS winding structure



Specifications:

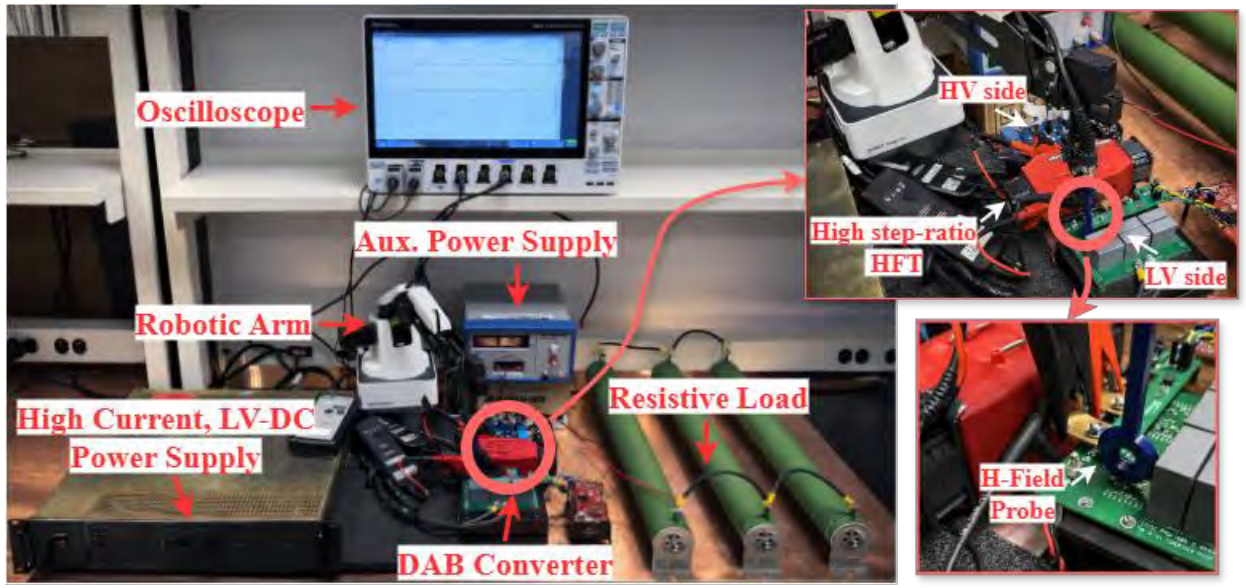
Parameter	LV	HV
Magnetizing Inductance	5.99 µH	4.98 mH
Leakage Inductance	56.25 nH	4.75 µH
Winding Resistance (dc)	1.45 mΩ	1.12 Ω
Isolation Capacitance	~288 pF	~288 pF
Intra-Winding Capacitance	103.4 nF	123.6 pF

[1] A. Muneeb, A. B. Mirza, M. Ul Hassan, A. Anwar, A. Castiblanco and F. Luo, "Parasitic Capacitances in High Step Ratio Planar Transformers for Dual Active Bridge Converters: Cause and Effect," IECON 2024 - 50th Annual Conference of the IEEE Industrial Electronics Society, Chicago, IL, USA, 2024

DAB Testing and Analysis

- Following individual stage characterization, the **LV GaN bridge HV SiC bridge, and 1:29 planar transformer** were assembled and tested under continuous DAB operation.

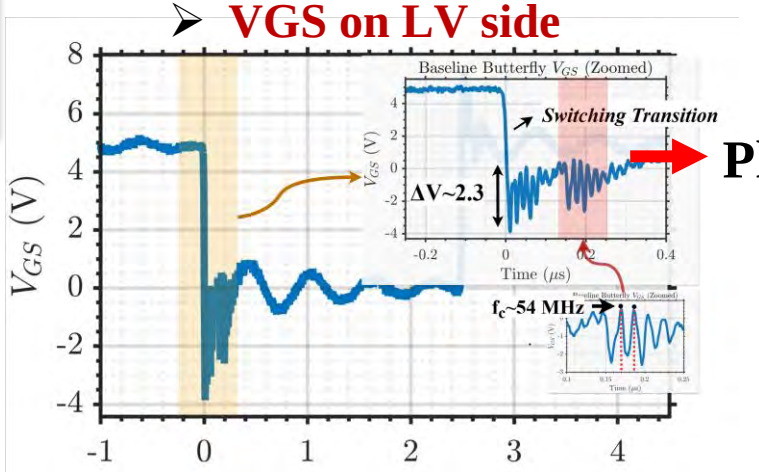
DAB Converter hardware setup



Test Conditions

Parameter	Value
LV / HV DC Voltage	27.34 / 786.5 V
LV / HV AC Current (rms)	175.9 / 6.488 A
Output Power	4.758 kW
Switching Frequency	200 kHz
Modulation	SPS
Phase Shift	28.6°
LV / HV Dead Time	30 / 100 ns
Turns Ratio	1 : 29

VGS on LV side



Phase shift transition

LV side VGS

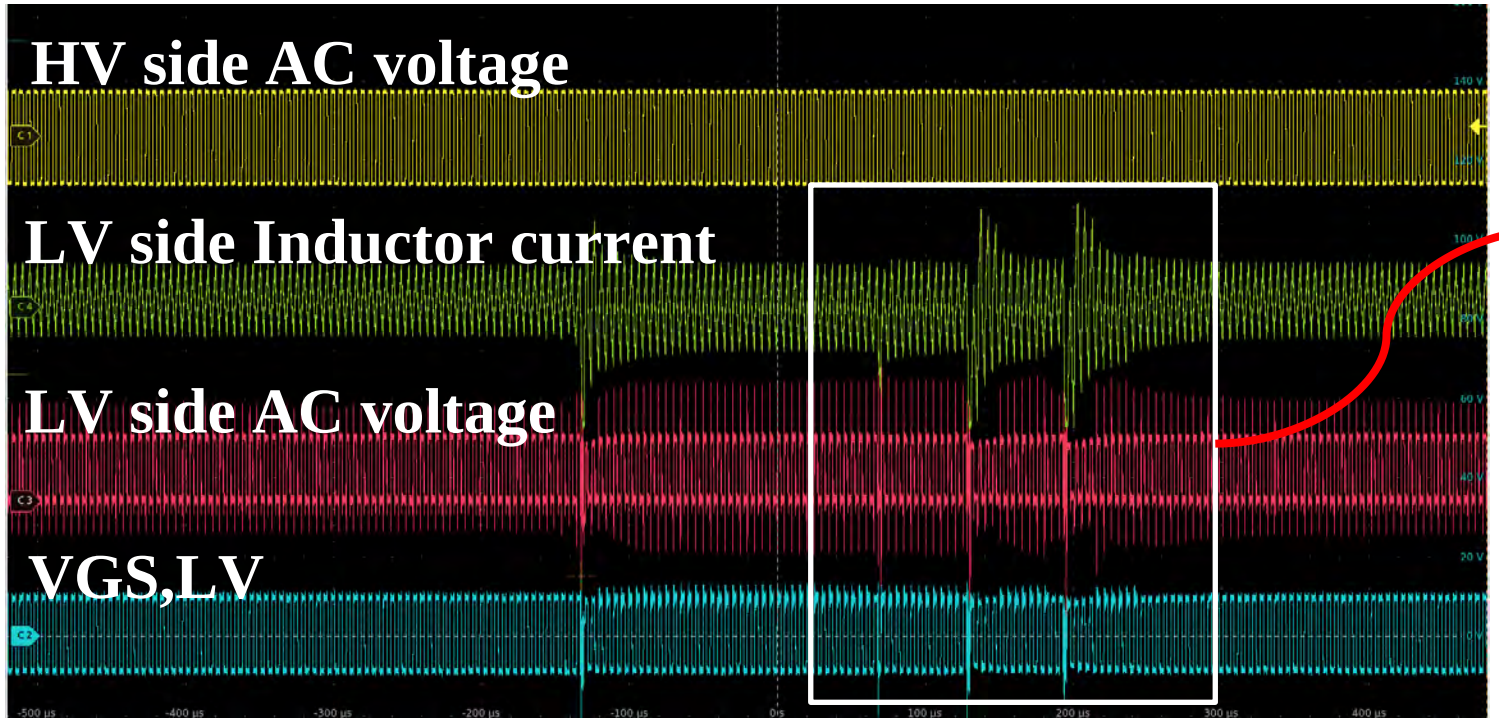
$$f_c = 54\ MHz$$

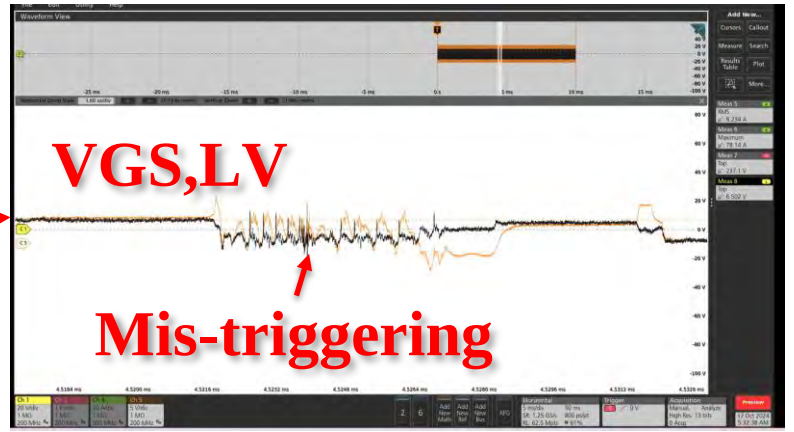
- At near rated conditions, **the converter's LV side AC node voltage started showing another high magnitude ringing after the switching transition.**

[1] A. Muneeb, A. B. Mirza, M. Ul Hassan, A. Anwar, A. Castiblanco and F. Luo, "Parasitic Capacitances in High Step Ratio Planar Transformers for Dual Active Bridge Converters: Cause and Effect," IECON 2024 - 50th Annual Conference of the IEEE Industrial Electronics Society, Chicago, IL, USA, 2024

DAB Testing and Analysis

- As **converter power increased**, the previously observed **LV-side ringing intensified** and propagated into the LV gate-drive waveform.





- VGS shows the coupling form AC to the gate voltage.
- HV side AC voltage remains clean.

[1] A. Muneeb, A. B. Mirza, M. Ul Hassan, A. Anwar, A. Castiblanco and F. Luo, "Parasitic Capacitances in High Step Ratio Planar Transformers for Dual Active Bridge Converters: Cause and Effect," IECON 2024 - 50th Annual Conference of the IEEE Industrial Electronics Society, Chicago, IL, USA, 2024

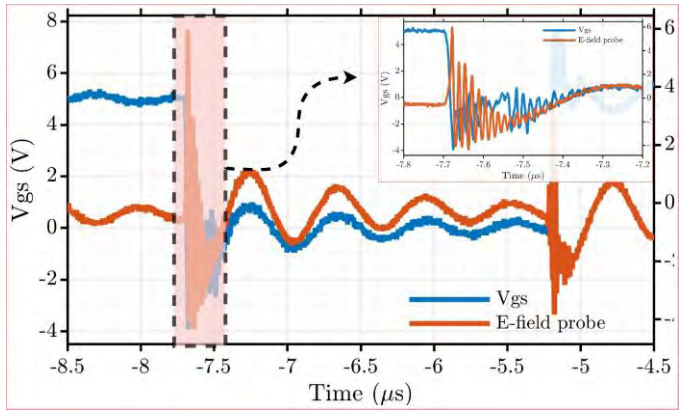
Identifying The Coupling Mechanism

Q3D Extracted gate- and power-loop were used to predict their resonant frequencies and compare them with the observed ~54 MHz gate disturbance.

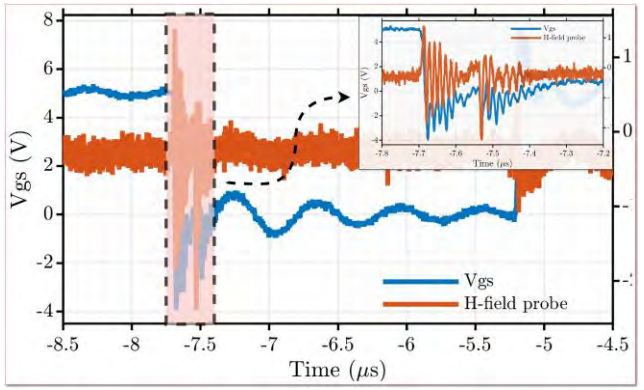
➢ **Q3D Extracted Gate/Power-Loop Parameters**

Network / Path	Inductance	Dominant C	Calculated f_0	Measured / Observed
Gate-source loop	**2.96 nH**	Ciss ≈ 3.2 nF	**≈ 51.7 MHz**	**VGS: 54–56 MHz**
Power / commutation loop	**2.80 nH**	Coss ≈ 1 nF	**≈ 78 MHz**	**VDS: 78 MHz**

➢ **AC node field probes placement**



➢ **VGS and E-field**



➢ **VGS and H-field**

- The ringing frequency sits between the Power loop and gate loop indicating a near field coupling exists.
- This was further validated by placing E-/H-Field probes directly on the AC trace near the gate loop.
- A strong H-Field signature observed with same frequency indicating H-field coupling due to high di/dt.

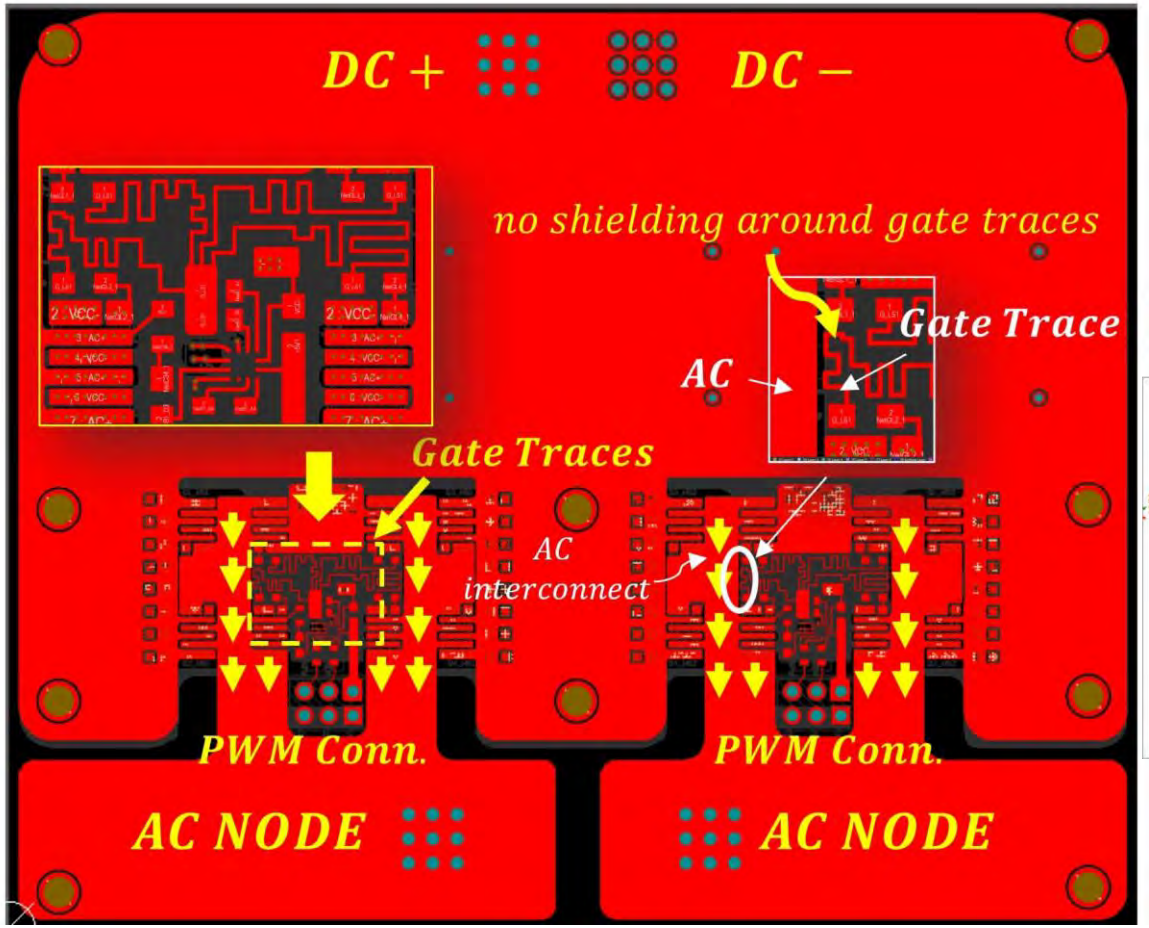
*dv/dt is small so the capacitive cross talk has negligible impact.

*Due to high di/dt has inductive near field coupling/cross-talk has more impact.

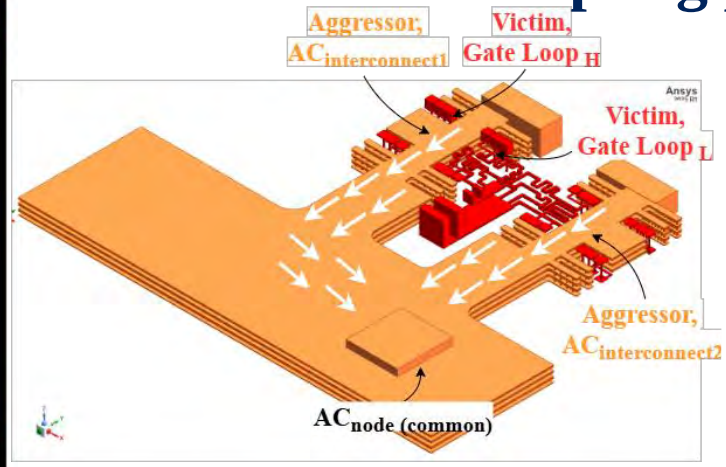
[1] A. Muneeb, A. Anwar, A. B. Mirza, Y. Li, S. Deng, M. Hijikata, and F. Luo, "Near-Field Coupling in Butterfly-Layout Paralleled GaN Power Stages for High Step-Ratio Power Conversion," IEEE Transactions on Power Electronics, submitted for publication, 2026.

Identifying The Coupling Mechanism

➢ Baseline Butterfly Layout



➢ The butterfly layout improves device symmetry but routes the high-di/dt AC interconnect close to the central gate-drive region, creating an unintended magnetic coupling path.



Parameter	Extracted Value
MAC,int→Gate,H	0.822 nH
MAC,int→Source,H	0.638 nH
Mdiff,H	0.184 nH
Lg,HS	2.96 nH

➢ Q3D identifies the AC-interconnect → high-side gate path as the dominant magnetic coupling path, with M = 0.822 nH.

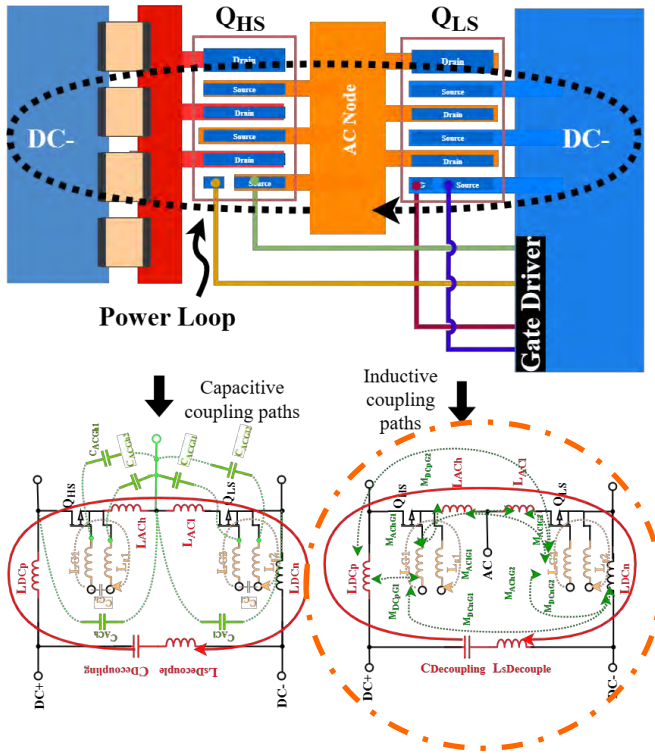
*Due to high di/dt has inductive near field coupling/cross-talk has more impact.

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Coupling-Path Modeling: LV and Transformer Parasitics

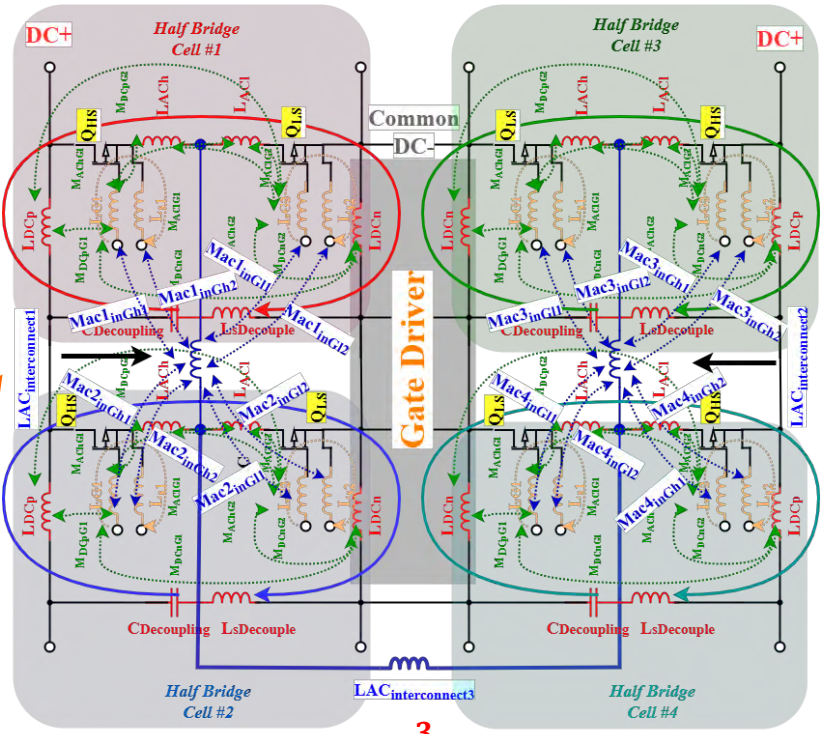
- **Following the near-field measurements, progressive parasitic models were developed to identify how the disturbance propagates from the converter power stage to the LV gate loop.**

Single Cell model



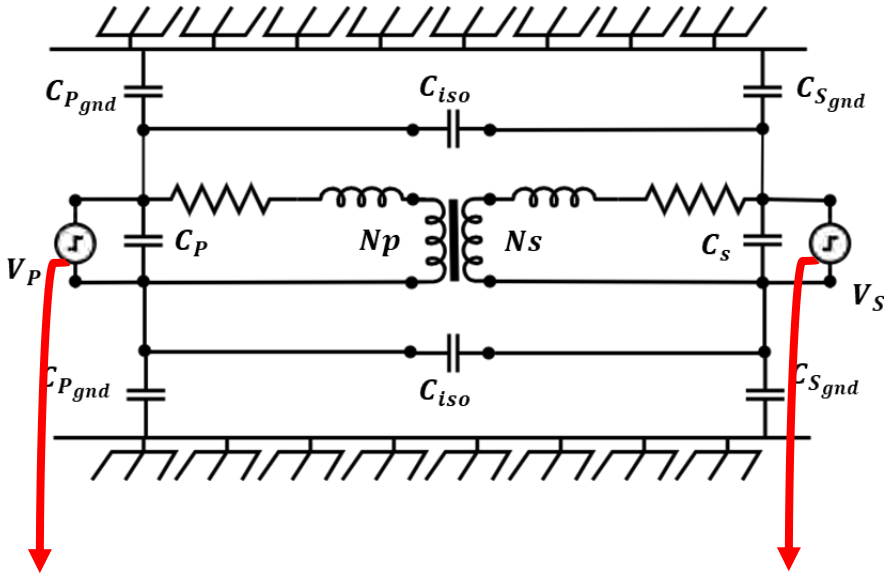
$$i_{ind}(t) = C_{AC \to G} \frac{dV_{AC}}{dt}$$

4 Cell model: AC interconnect effect



$$v_{g(y,x),ind}(t) = v_{g(y,x),ind,cell}(t) + \sum_{k=1}^{3} M_{int,k}^{(y,x)} \frac{di_{int,k}}{dt}$$

Transformer Model



$\uparrow\uparrow di/dt$

$\uparrow\uparrow\uparrow dv/dt$

$$i_{coup,LV}(t) \approx C_{iso} \frac{dv_{HV}(t)}{dt}$$

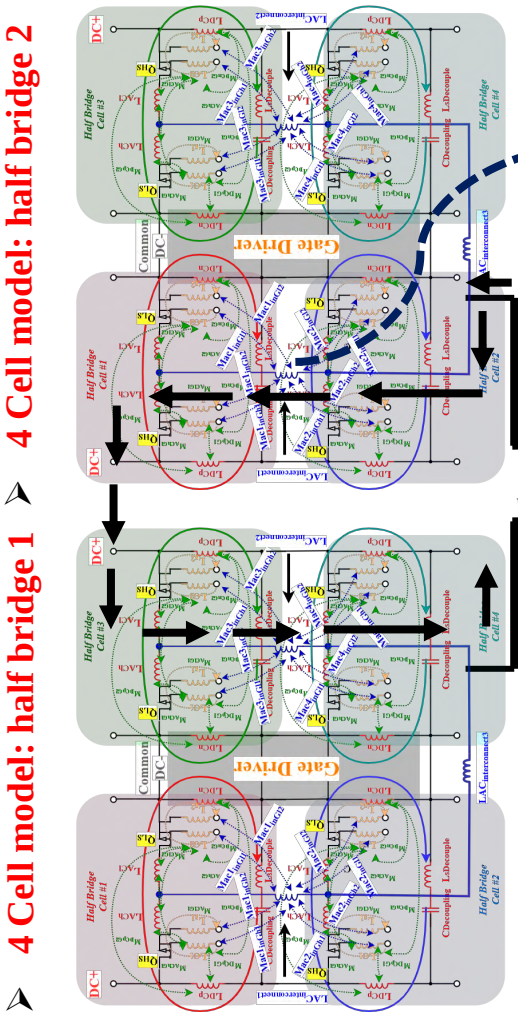
***dv/dt is small so the capacitive cross talk has negligible impact.**

***Due to high di/dt has inductive near field coupling/cross-talk has more impact.**

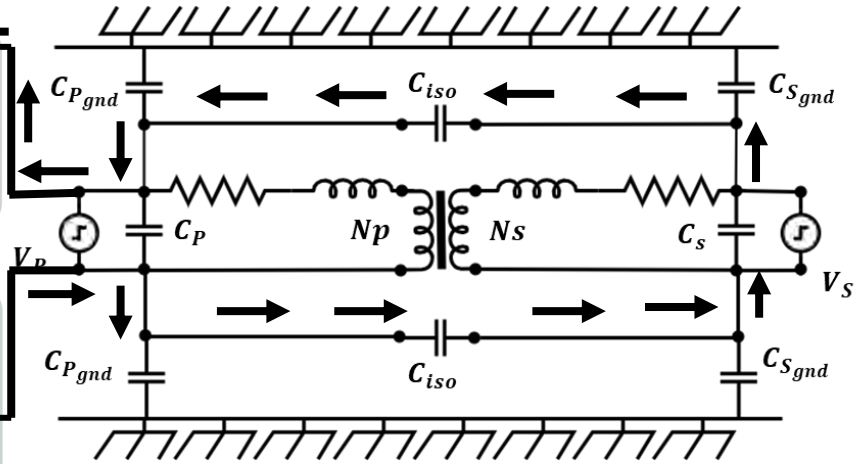
[1] A. Muneeb, A. Anwar, A. B. Mirza, Y. Li, S. Deng, M. Hijikata, and F. Luo, "Near-Field Coupling in Butterfly-Layout Paralleled GaN Power Stages for High Step-Ratio Power Conversion," IEEE Transactions on Power Electronics, submitted for publication, 2026.

DAB Converter Parasitic Model

LTspice modeling identified the complete disturbance path from the HV switching transition to the LV gate loop.



Noise injection into LV gate trace routed close to AC interconnect carrying high di/dt current



Due to high step ratio:

When $Cs, gnd < Ciso$, For high frequency series inject displacement current through the **Ciso**:

$Cs < Cp$

$Llk,HV > Llk,LV$

$Z,LV < Z,HV$

Key Culprits:

❑ M_{eff} ❑ C_{iso}

- **HV-side dv/dt** generates displacement current through $Ciso$.
- That current is injected into the LV AC-node structure.
- On the LV side, the **current enters a low-impedance high-di/dt commutation** region.
- the resulting current disturbance in the LV AC interconnect couples into the nearby gate loop through mutual inductance.
- this appears as gate disturbance, ringing, or false turn-on tendency.

$$\frac{dv_{HV}}{dt} \rightarrow i_{disp}(t) \rightarrow i_{AC,LV}(t) \rightarrow v_{g,ind}(t)$$

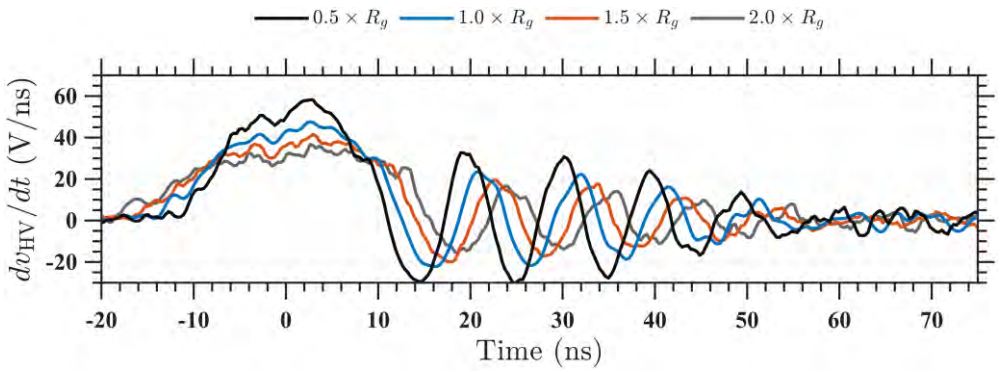
[1] A. Muneeb, A. Anwar, A. B. Mirza, Y. Li, S. Deng, M. Hijikata, and F. Luo, "Near-Field Coupling in Butterfly-Layout Paralleled GaN Power Stages for High Step-Ratio Power Conversion," IEEE Transactions on Power Electronics, submittedfor publication, 2026.

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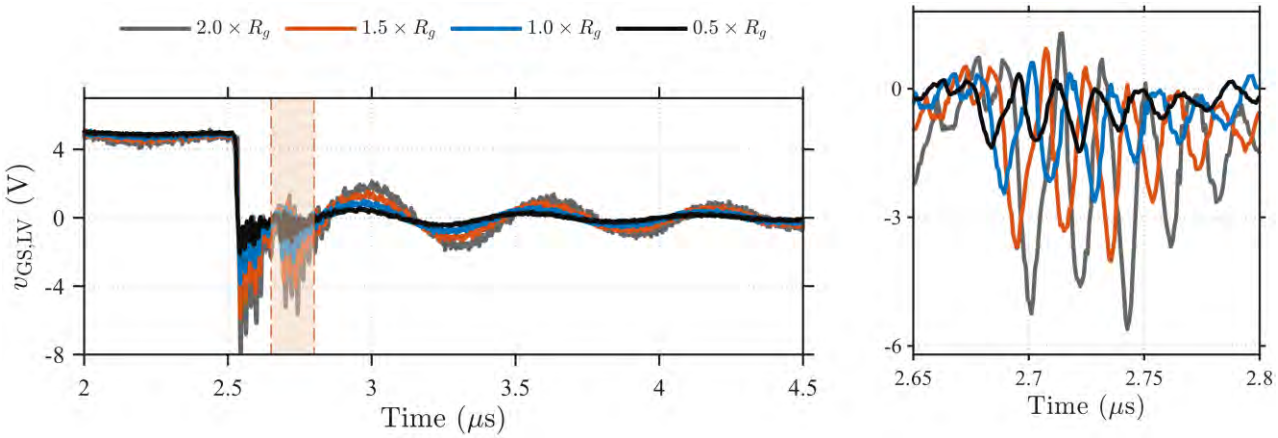
HV dv/dt-Induced LV Gate Disturbance: Experimental Validation

- **To isolate the excitation source, the LV network was held fixed while $R_{g,HV}$ was varied to sweep the HV switching-node dv/dt.**

- **DPT-Measured HV dv/dt**



- **Observed VGS**



- **Measured Validation Data**

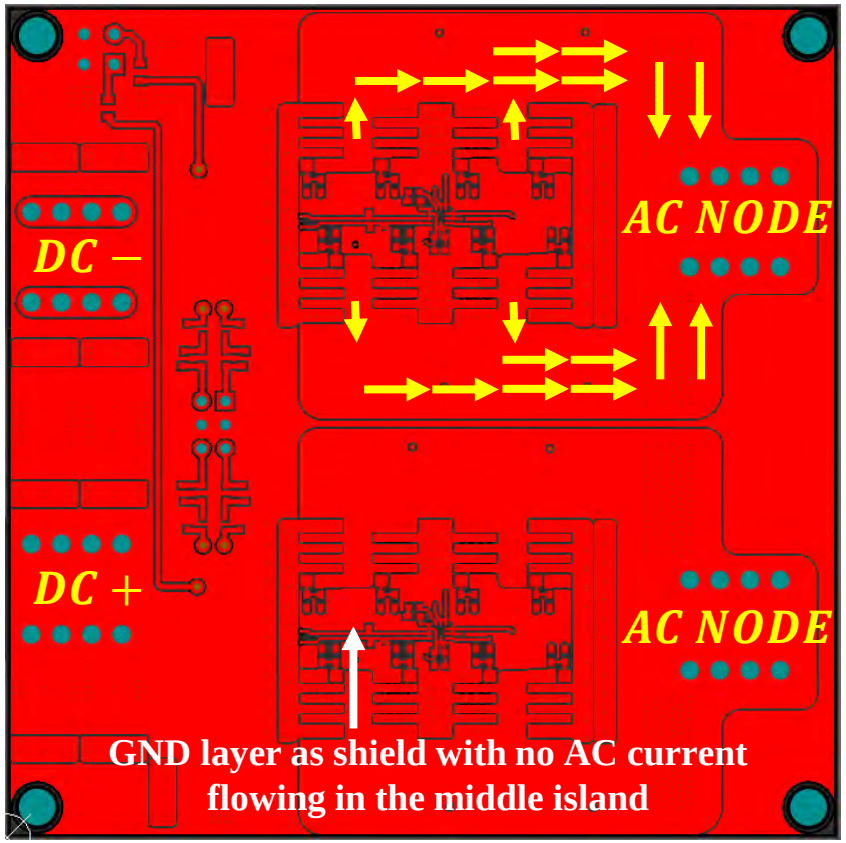
$R_{g,\mathrm{HV}}$	dv_{HV}/dt	$VGS_{ind,\mathrm{LV}}$
1.1 Ω (0.5×)	**58.2 V/ns**	~6.90 Vpp (max)
2.2 Ω (nom.)	**47.6 V/ns**	~2.3 Vpp
3.3 Ω (1.5×)	**41.6 V/ns**	~2.05 Vpp
4.4 Ω (2×)	**36.6 V/ns**	~1.80 Vpp (min)

- **With the LV network unchanged, increasing dv_{HV}/dt from 36.6 to 58.2 V/ns increased the LV gate disturbance from 1.80 to 6.90 V_{pp}, identifying the HV phase-shift transition as the upstream excitation source.**

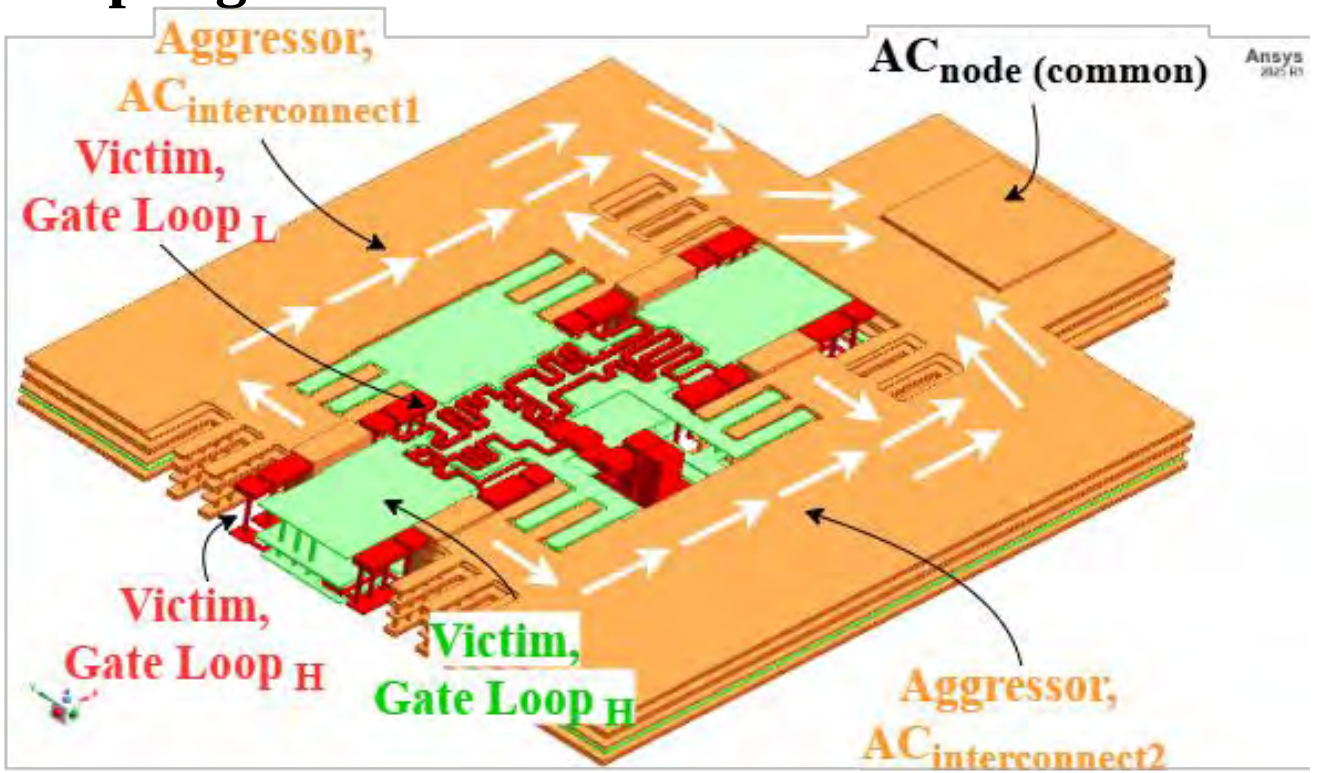
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Near Field Coupling Mitigation: Proposed SSAB

- **Baseline butterfly layout is prone to noise and not suitable for the high di/dt operation.**
- **SSAB (Shielded Split-AC Butterfly) layout is proposed to mitigate the near field coupling.**



- SSAB Layout: PCB top layer view

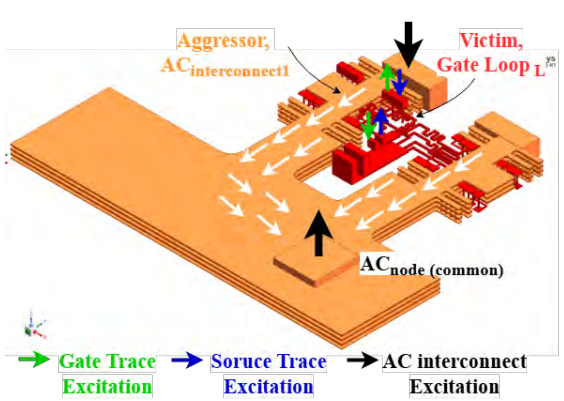


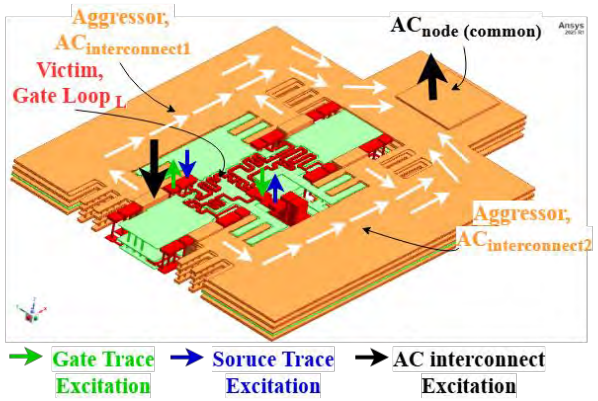
- SSAB Layout: Q3D simplified geometry

[1] A. Muneeb, A. Anwar, A. B. Mirza, Y. Li, S. Deng, M. Hijikata, and F. Luo, "Near-Field Coupling in Butterfly-Layout Paralleled GaN Power Stages for High Step-Ratio Power Conversion," IEEE Transactions on Power Electronics, submitted for publication, 2026.
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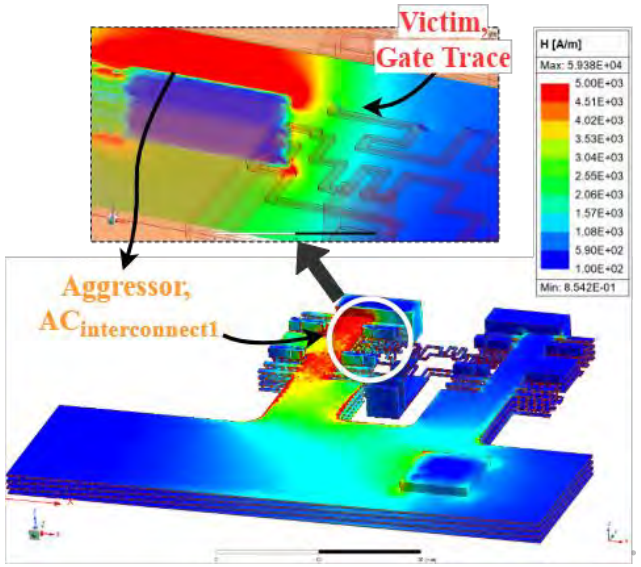
Near Field Coupling Mitigation: Ansys Maxwell 3D

➢ **Baseline and SSAB Layout: Maxwell 3D Excitation**

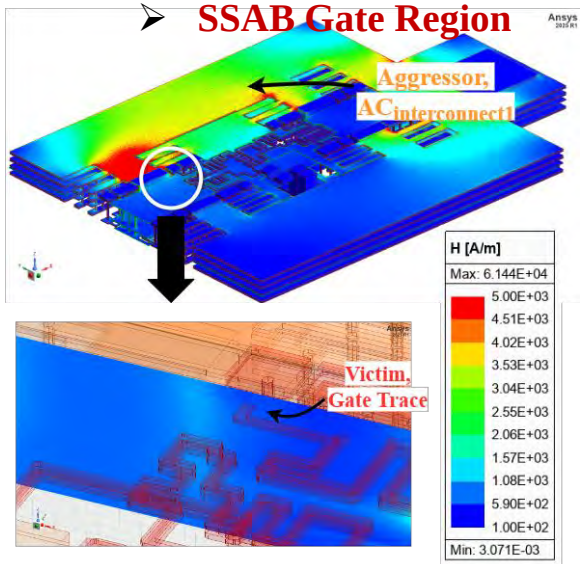




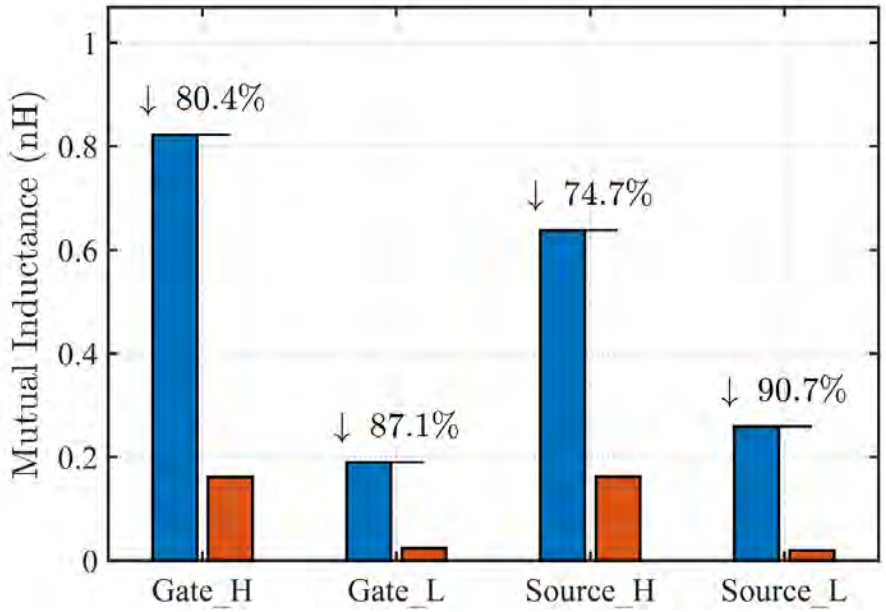
➢ **Baseline Hotspot Region**



➢ **SSAB Gate Region**



➢ **Mutual Inductance reduction**



M_{eff} **in Baseline butterfly layout**

75–91% ***reduction***

M_{eff} **in SSAB layout**

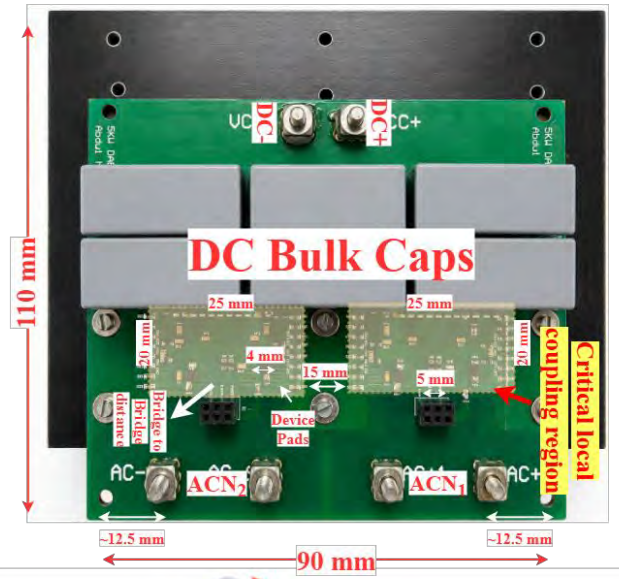
➢ **SSAB achieves >75% reduction in Meff without changing the power loop and without increasing PCB footprint.**

[1] A. Muneeb, A. Anwar, A. B. Mirza, Y. Li, S. Deng, M. Hijikata, and F. Luo, "Near-Field Coupling in Butterfly-Layout Paralleled GaN Power Stages for High Step-Ratio Power Conversion," IEEE Transactions on Power Electronics, submitted for publication, 2026.

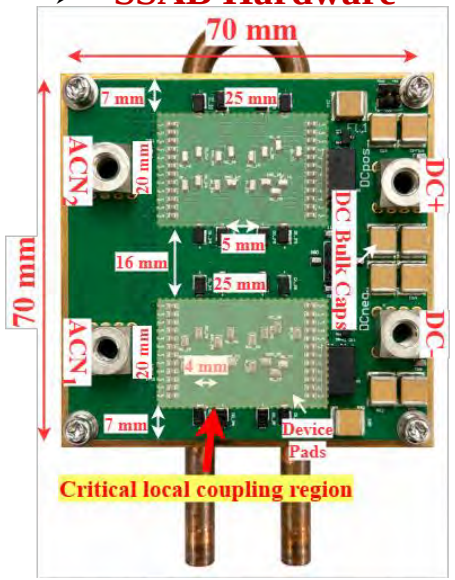
[2] [1] A. Muneeb, A. B. Mirza, Samuel Defaz, and F. Luo, "Impact of high dv/dt on the high step ratio DAB converter," IEEE Transactions on Power Electronics, accepted for publication, 2025.

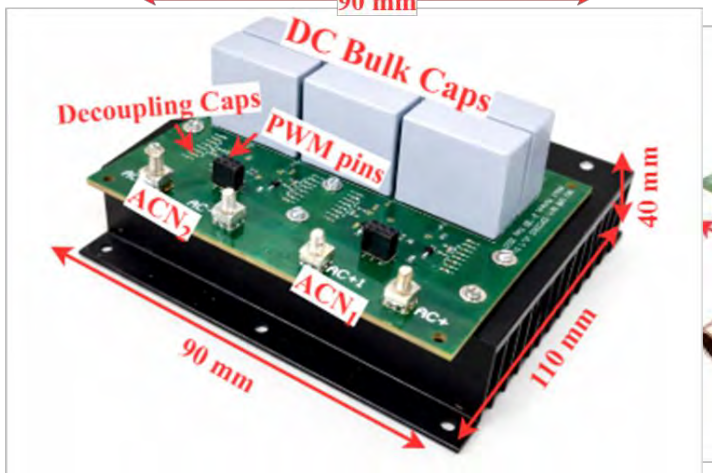
Stony Brook University Cross-talk Mitigation: Transformer

➢ Baseline Butterfly Hardware



➢ SSAB Hardware







➢ Hardware Comparison

Parameter	Baseline	SSAB	Status
Device count	4× EPC2302	4× EPC2302	Same
PCB stack-up	10L, 2oz/3oz Cu	10L, 2oz/3oz Cu	Same
Gate drive / Rg	Identical	Identical	Same
Electrical test condition	Identical	Identical	Same
AC routing	Central butterfly	Split peripheral	Changed
Gate region	Near AC path	Isolated + shielded	Changed
Return-path control	Central/shared	Outer-path confined	Changed
Coupling strategy	Symmetry-based	Geometry-based	Changed

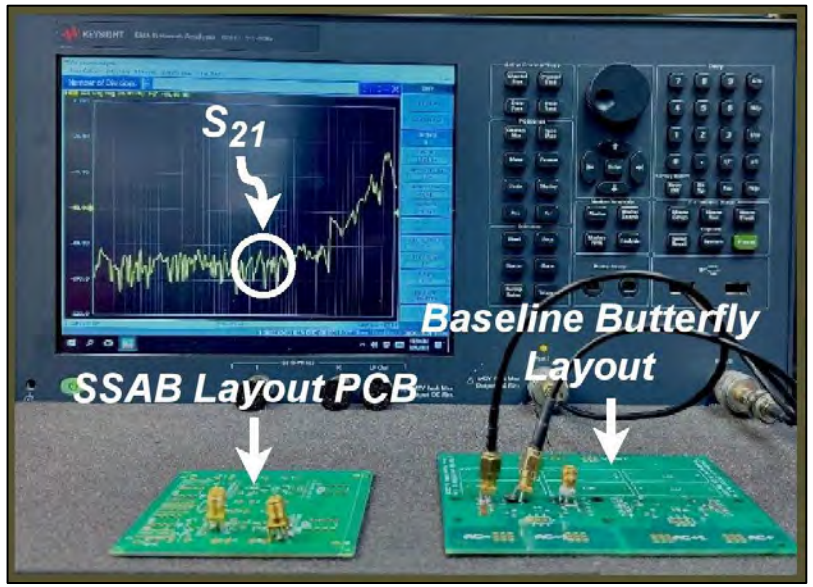
Comparison Boundary: device placement, gate drive and operating conditions remain fixed; the local electromagnetic geometry is the controlled change.

FAR BEYOND

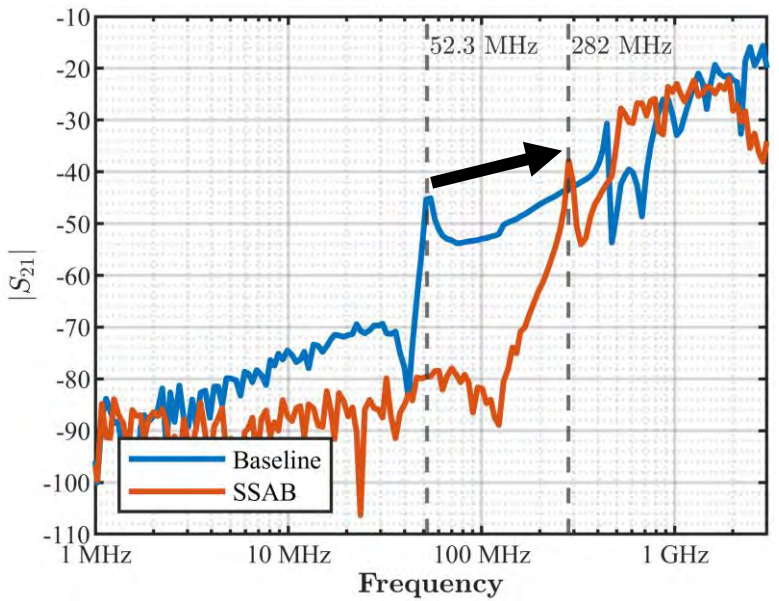
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Cross-talk Mitigation: Transformer

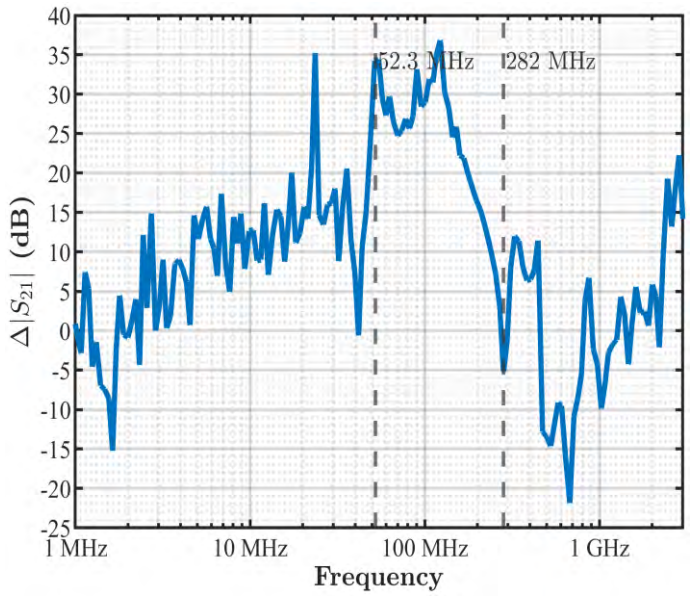
- **Keysight ENA E5061B Vector Network Analyzer (VNA) was used to measure S_{21} and experimentally quantify the AC-interconnect-to-gate coupling.**
  - **S_{21} Measurement Setup**



  - **S_{21}: Baseline Vs SSAB**



  - **▲ S_{21}**



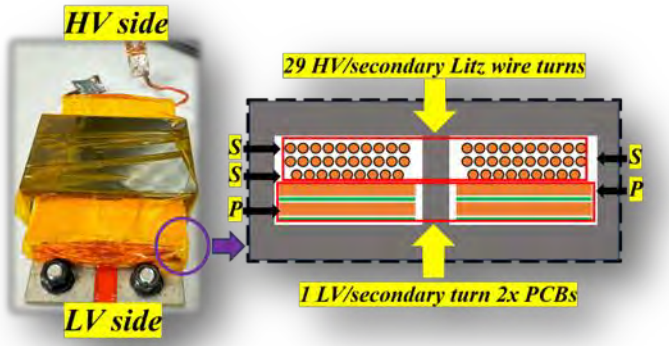
  - **The baseline layout exhibits a strong coupling feature at 52.3 MHz, closely matching the measured 54–56 MHz gate-voltage disturbance.**
  - **SSAB suppresses coupling in the critical 50–60 MHz gate-sensitive band by > 30 dB; the remaining ≈ 282 MHz feature is a higher distributed coupling mode.**

FAR BEYOND

[1] A. Muneeb, A. Anwar, A. B. Mirza, Y. Li, S. Deng, M. Hijikata, and F. Luo, "Near-Field Coupling in Butterfly-Layout Paralleled GaN Power Stages for High Step-Ratio Power Conversion," IEEE Transactions on Power Electronics, submitted for publication, 2026.
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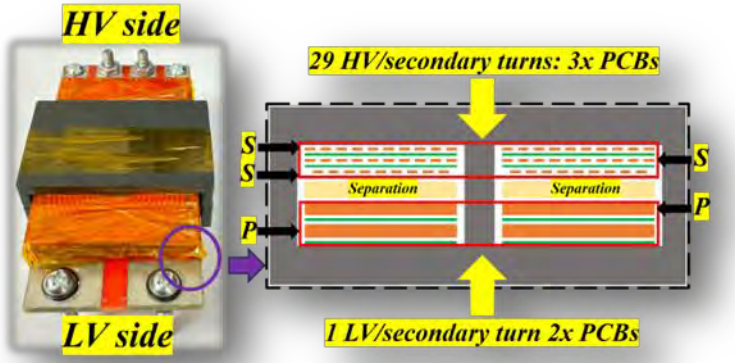
Cross-talk Mitigation: Transformer

- **To reduce the dv/dt noise crossing into the LV side the C_{iso} is needed to be reduced**



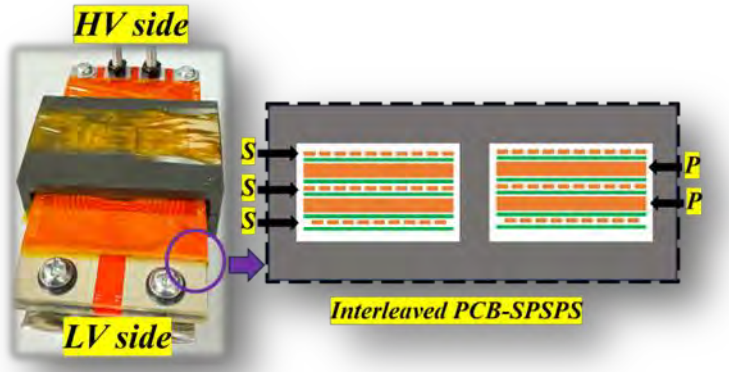
- **Hybrid PCB-Litz winding structure.**

- Moderate AC resistance.
- Moderate Ciso .
- Moderate Leakage inductance.
- Resonance point shifted to high frequency.
- Low Cs.



- **PCB-PP-SEP-SSS winding structure.**

- Moderate AC resistance.
- **Least Ciso.**
- Moderate Leakage inductance.
- Resonance point shifted to high frequency.
- Low Cs.



- **PCB-SPSPS winding structure.**

- Least AC resistance.
- Highest Ciso.
- Least Leakage inductance.
- Resonance point shifted to low frequency.
- High Cs.

Extracted parameter	PCB-SPSPS	Hybrid PCB-Litz	PCB-PP-SEP-SSS
Ciso (pF)	288.00	84.53	**35.79**
Llk,LV (nH)	37.61	19.35	32.53
Cp,LV (nF)	21.18	22.05	65.03
Lmag,LV (µH)	3.56	9.27	5.32

- **C_{iso} was reduced to ~37 pF from ~288 pF**

SPSPS to PP-SEP-SSS, at identical dv_{iso}/dt

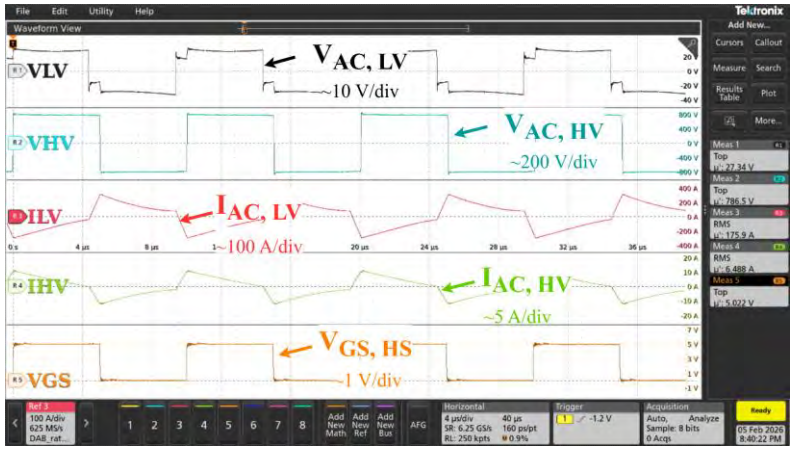
87.57% lower injection

[1] A. Muneeb, A. Anwar, A. B. Mirza, Y. Li, S. Deng, M. Hijikata, and F. Luo, "Near-Field Coupling in Butterfly-Layout Paralleled GaN Power Stages for High Step-Ratio Power Conversion," IEEE Transactions on Power Electronics, submitted for publication, 2026.
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[3] A. Muneeb, A. B. Mirza, M. Ul Hassan, A. Anwar, A. Castiblanco and F. Luo, "Parasitic Capacitances in High Step Ratio Planar Transformers for Dual Active Bridge Converters: Cause and Effect," IECON 2024 - 50th Annual Conference of the IEEE Industrial Electronics Society, Chicago, IL, USA, 2024

High Step Ratio DAB: Continuous operation

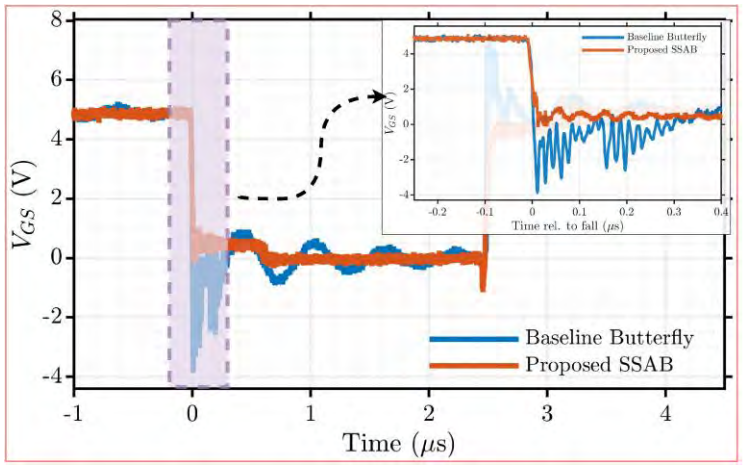
- **Reduced Ciso limits injection; reduced Meff suppresses the local power-to-gate coupling path.**

Continuous DAB operation



5 kW · 200 kHz · $I_L V = 188 ARMS$

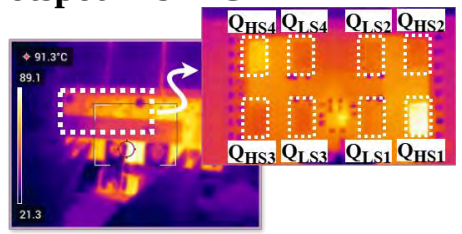
Baseline vs. SSAB gate response



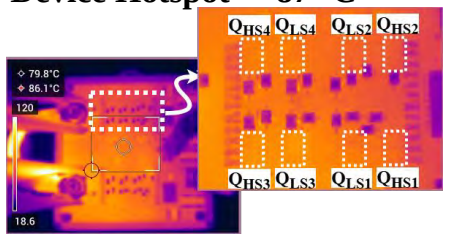
✓ **Resonance-driven gate ringing suppressed**

Board thermal comparison

- **Baseline Butterfly Layout, Device Hotspot= ~91 °C**



- **SSAB, Device Hotspot= ~87 °C**



Measured metric	Baseline	SSAB	Result
VGS disturbance at 200% load	6.919 Vpp	0.464 Vpp	93.3% lower
Peak efficiency	≈97.1%	≈96.9%	Comparable
Board hotspot temperature	91.3°C	87.1°C	5.°C lower

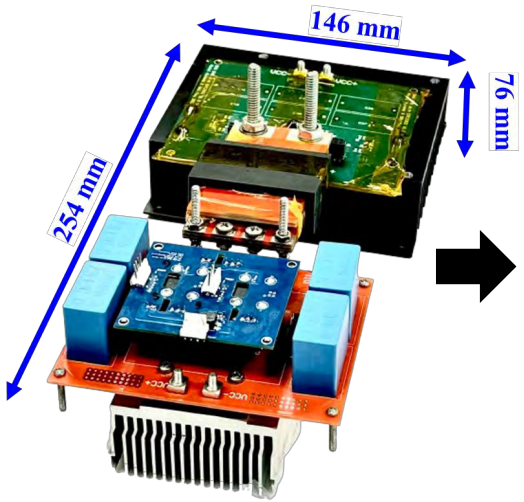
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[3] A. Muneeb, A. B. Mirza, M. Ul Hassan, A. Anwar, A. Castiblanco and F. Luo, "Parasitic Capacitances in High Step Ratio Planar Transformers for Dual Active Bridge Converters: Cause and Effect," IECON 2024 - 50th Annual Conference of the IEEE Industrial Electronics Society, Chicago, IL, USA, 2024

Power Density Improvement: Ongoing and Future work

➢ High Power Density Achievement: IPhone Pro Max DAB

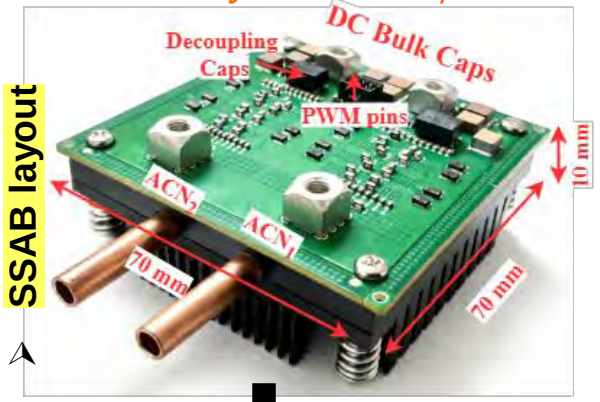
Gen 1.0:

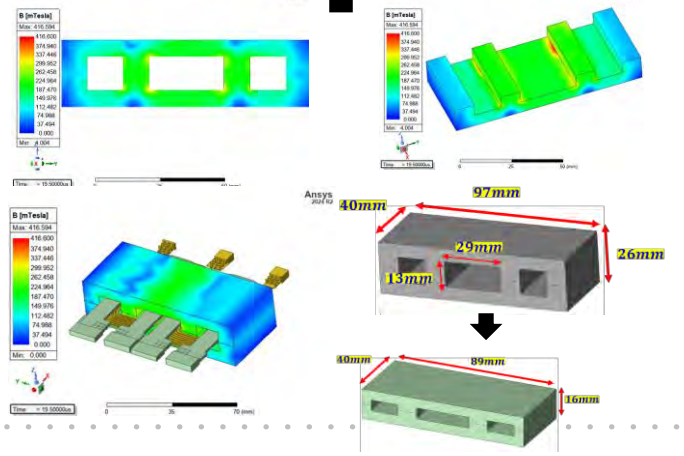
$Power\ Density \approx 60\ W/in^3$



Gen 1.1:

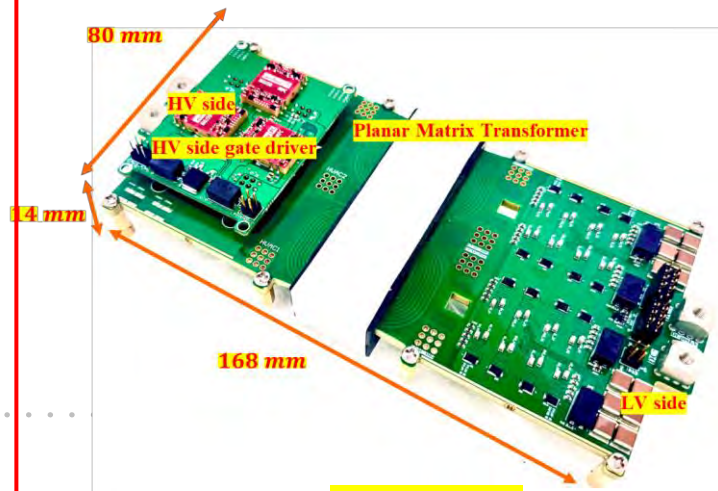
$PowerDensity \approx 100.2W/in^3$





➢ Matrix Flux cancellation optimization



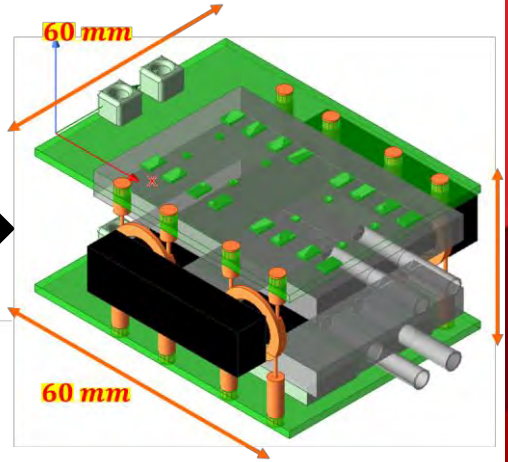


Gen 2.0:

$Research\ Milestone \rightarrow\rightarrow PowerDensity \approx 436W/in^3$

Gen 3.0:

$PowerDensity \approx 572\ W/in^3$



➢ Central limb CC-Matrix flux cancellation magnetics-based DAB converter

FAR BEYOND

Acknowledgement

Sponsors:



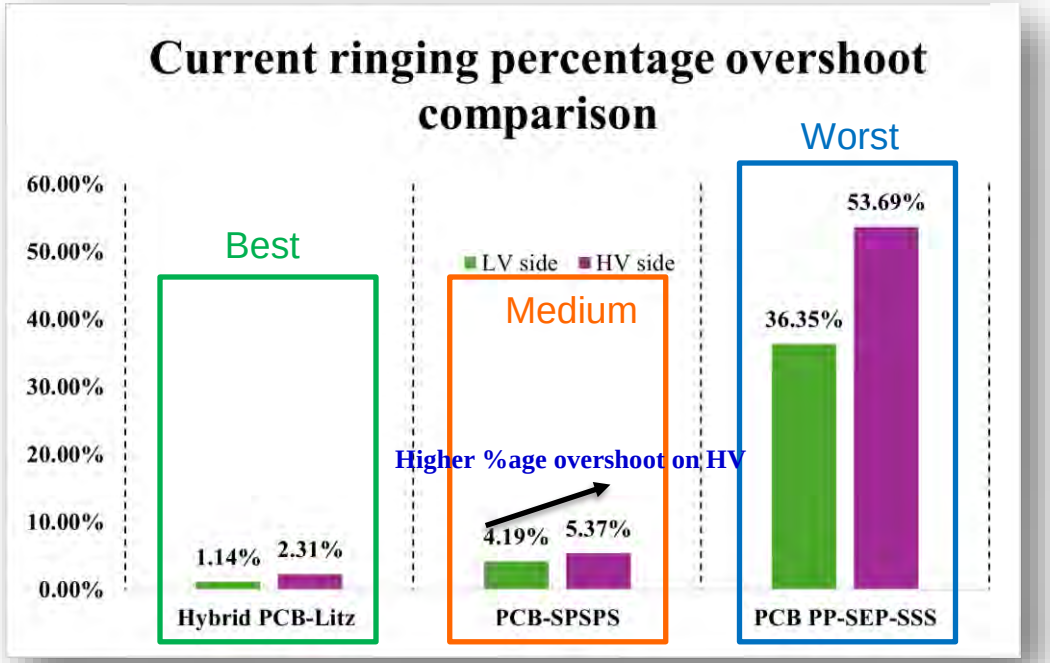
GE Aerospace

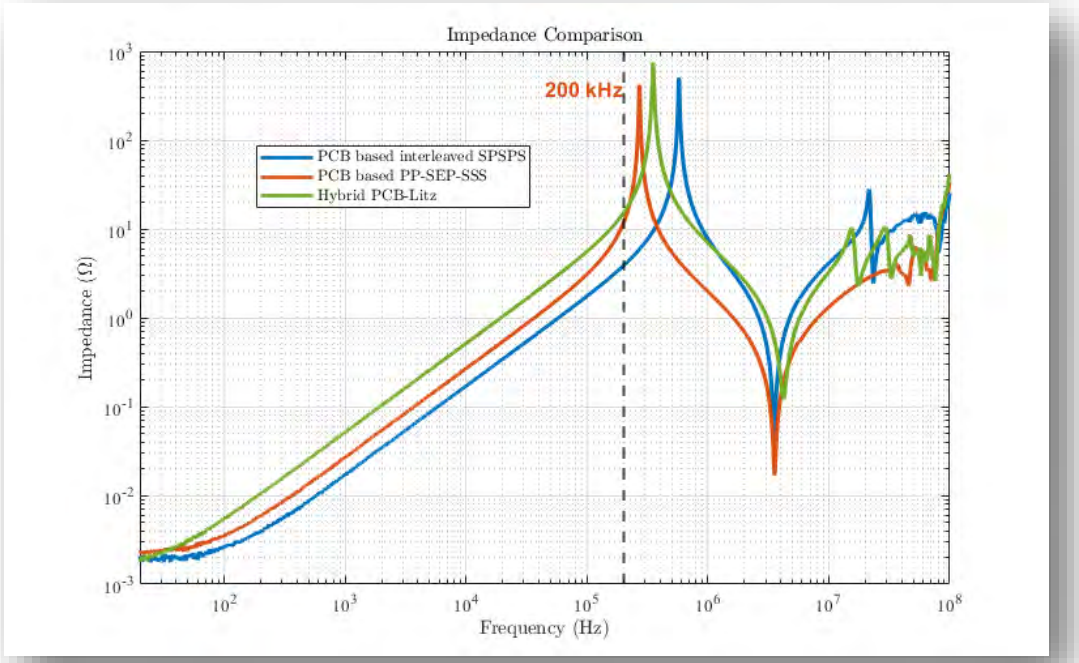
Thanks

Questions?

Magnetics: Transformer comparison

- **In high step ratio DAB converters, the parasitic capacitance produces the current ringing with high overshoots especially on HV side.**





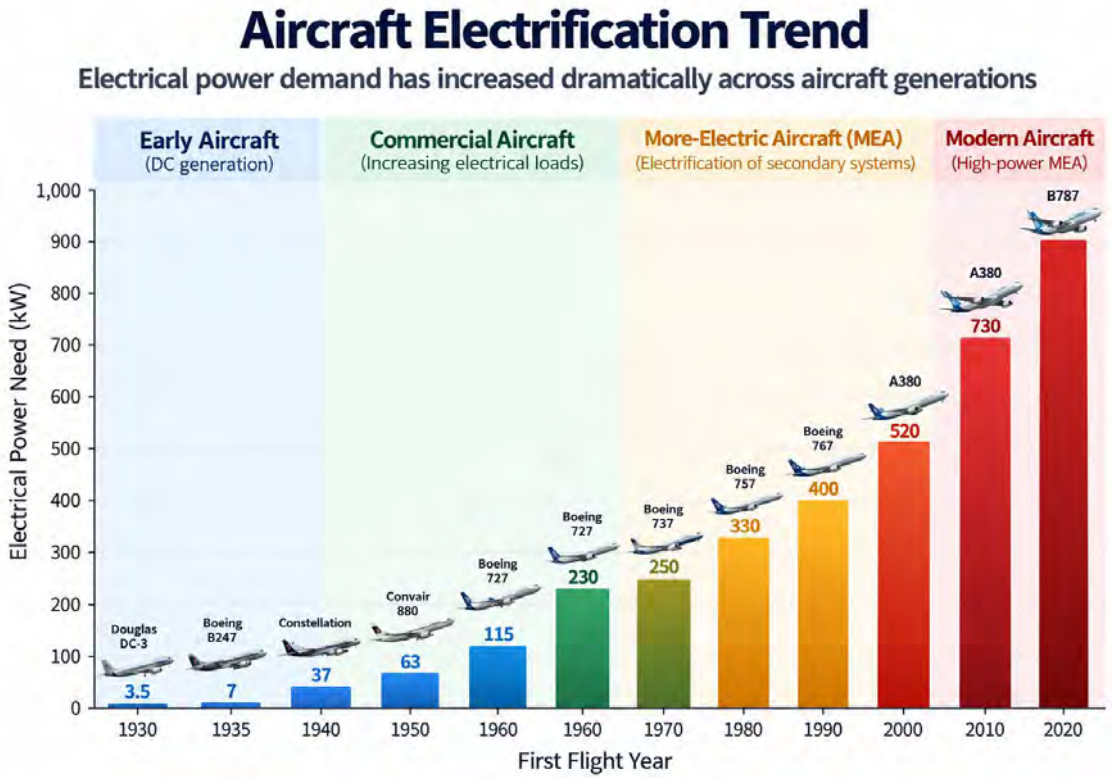
- **Effect of intra-winding capacitance can be depicted by the resonance frequency points:**

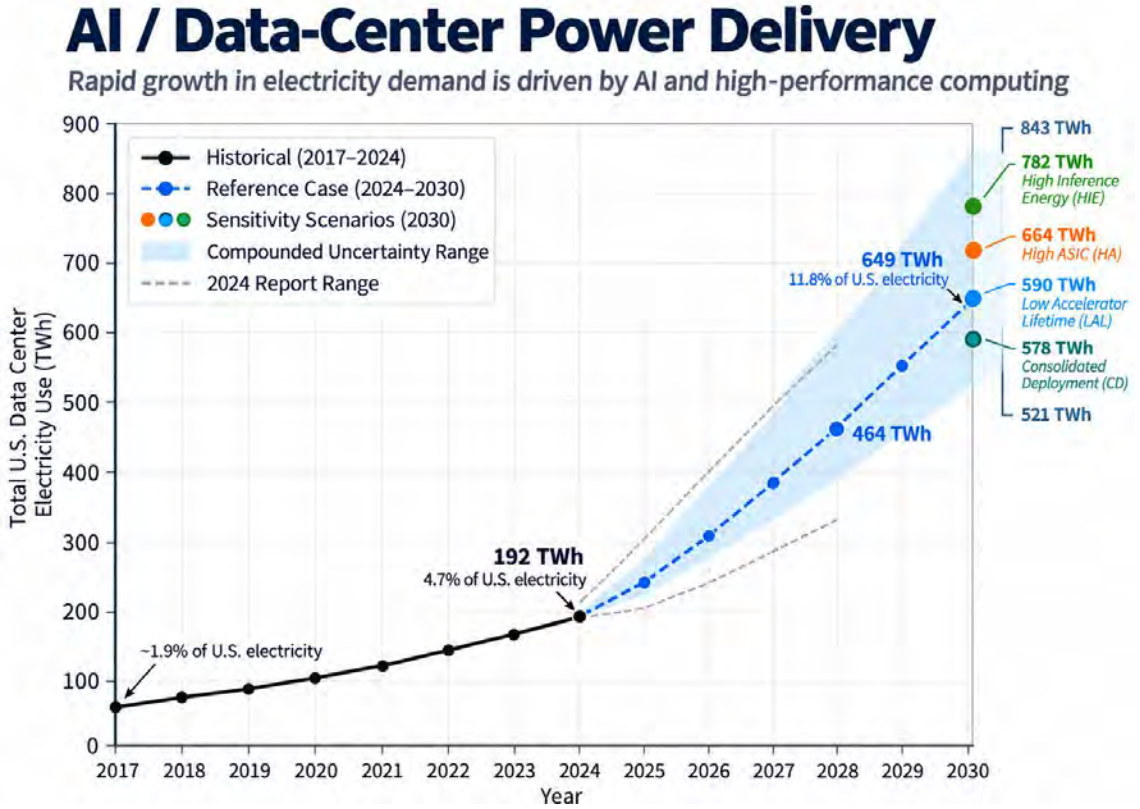
SPSPS<HLPCB<PP-SEP-SSS

[1] D. Deschrijver, M. Mrozowski, T. Dhaene, and D. De Zutter, "Macromodeling of multiport systems using a fast implementation of the vector fitting method," IEEE Microwave and Wireless Components Letters, vol. 18, no. 6, pp. 383–385, 2008.

Motivation: Growing Electrical Power Demand

- **Electrification is rapidly increasing electrical power demand in both modern aircraft and AI data centers.**



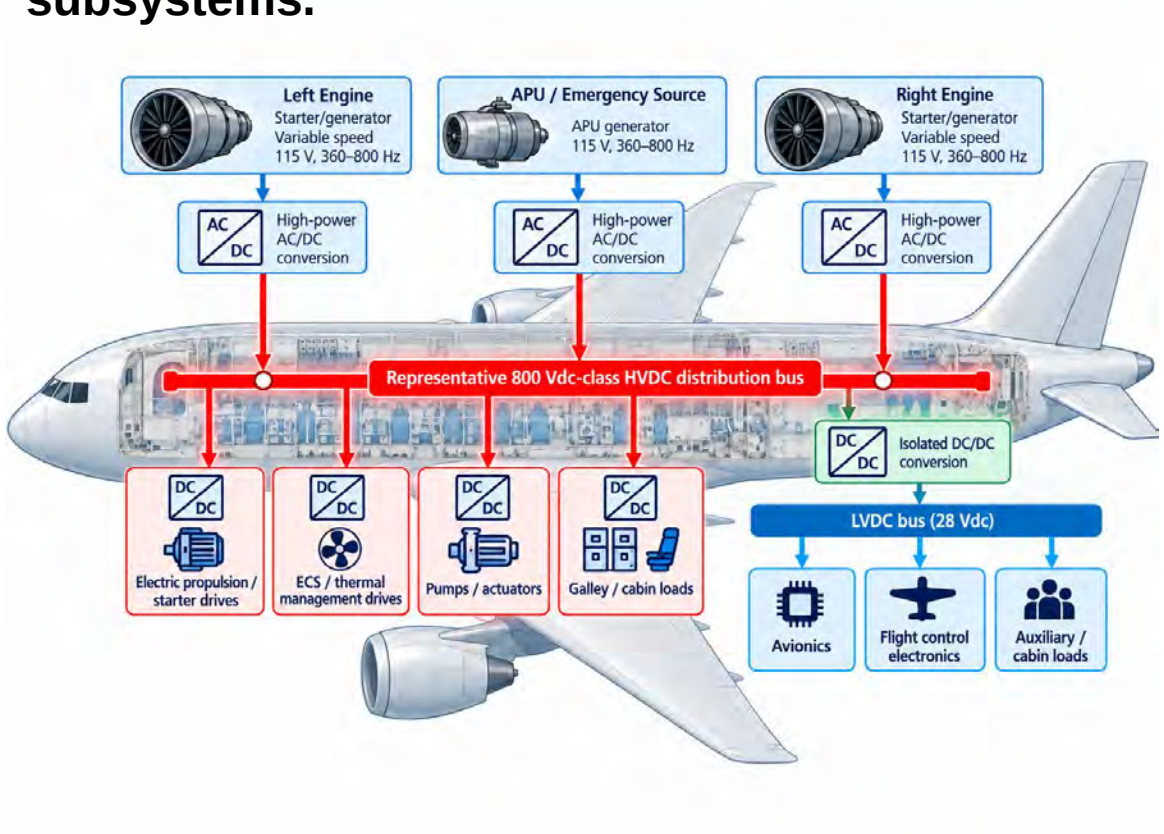


- ✓ Aircraft electrical power demand has increased from **~3.5 kW to ~900 kW, a >250× increase across successive** generations.

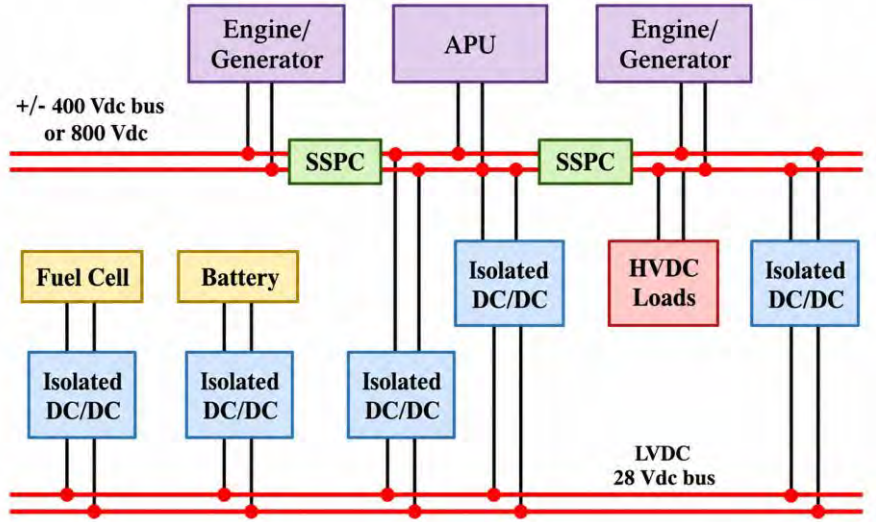
[1] D. Deschrijver, M. Mrozowski, T. Dhaene, and D. De Zutter, "Macromodeling of multiport systems using a fast implementation of the vector fitting method," IEEE Microwave and Wireless Components Letters, vol. 18, no. 6, pp. 383–385, 2008.

Motivation: Aircraft Power Architecture

- **Increasing onboard power demand is driving aircraft electrical systems toward HVDC distribution, where power-electronic converters interconnect high-voltage buses with lower-voltage loads and subsystems.**



- **Representative 800-V-Class Aircraft HVDC Architecture**

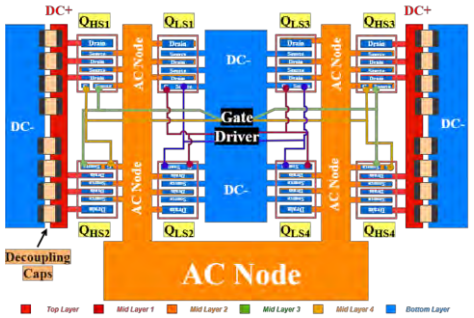


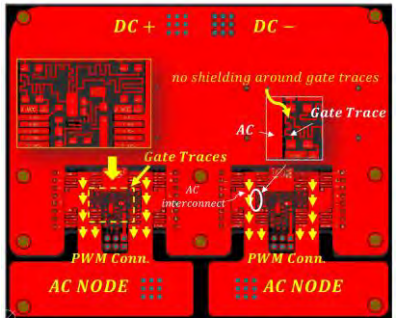
- **Multi-Source HVDC/LVDC Aircraft Architecture**

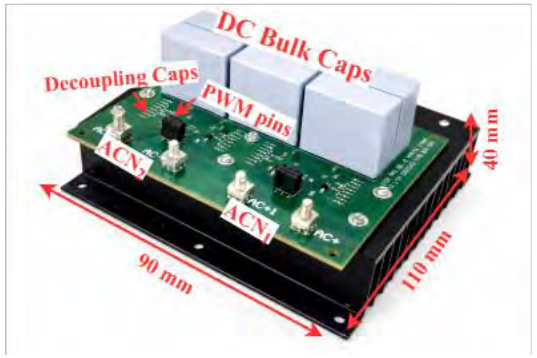
Centralized HVDC distribution supplies high-power loads while isolated DC/DC conversion interfaces the 28-V low-voltage domain.

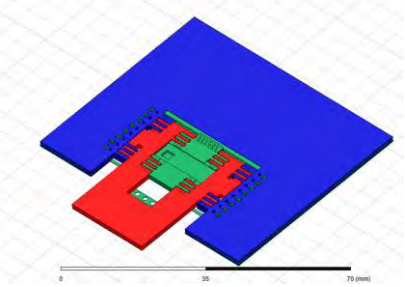
[1] S. J. Smith, A. Hubbard, A. Newkirk, M. Ganeshalingam, B. Holecek, D. A. Sartor, M. Mills, and A. Shehabi, United States Data Center Energy Usage Report: 2025 Update, Lawrence Berkeley National Laboratory, Berkeley, CA, USA, LBNL-2001758, Jun. 2026.

LV-Side Design and Analysis









➢ **Simplified power loop geometry in Ansys Q3D environment**

➢ Power Stage Validation: DPT Testing

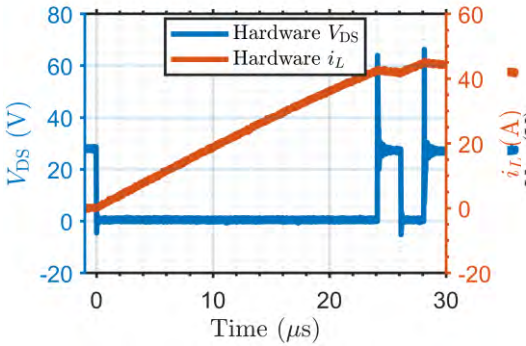
➢ LTspice model is built to compare the DPT (Double pulse test) results.

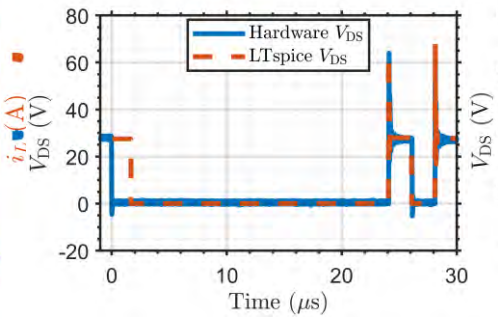
➢ The di/dt is estimated with the model compared with hardware results.

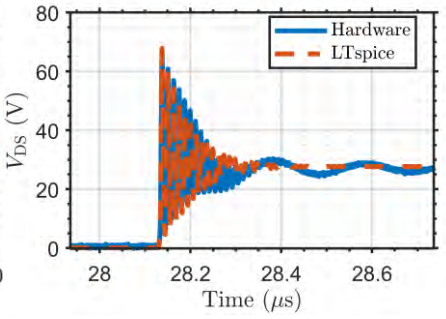
Ansys Q3D Simulation Res

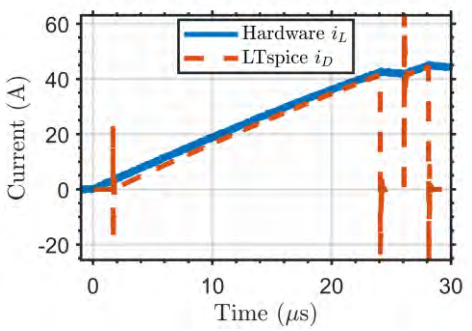
r bridge

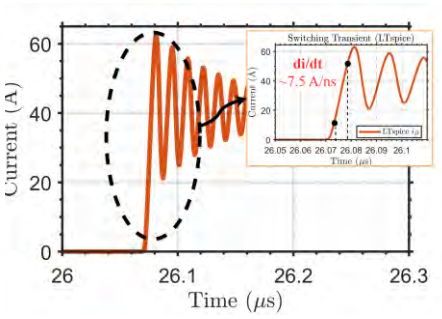
200 pF











➢ **Measured DPT waveform showing Vds and i_L**

➢ **Vds comparison between hardware and LTspice**

➢ **Zoomed Vds switching transition**

➢ **Id ringing used for power loop inductance**

➢ **di/dt estimation with Ltspice model**

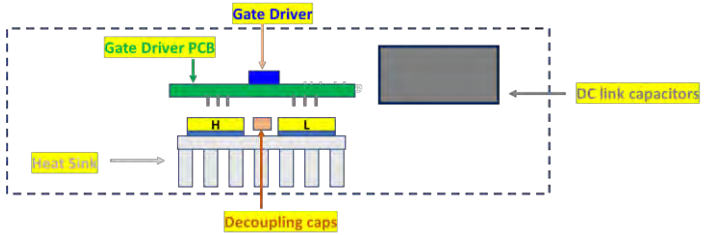
FAR BEYOND

The **4x effective dv/dt** is lower on LV side due to low voltage swing **(0-28V) ~ 4 V/ns**

di/dt ~ 7.5 A/ns (per half bridge) (0- 45 Amps)

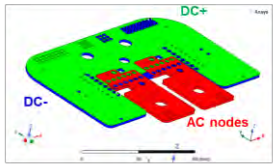
4x Effective di/dt = 30 A/ns

HV-Side Design and Analysis



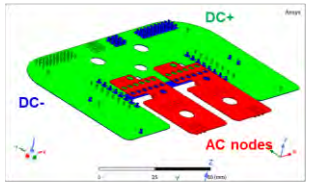
- Due to **high voltage swing (i.e., 0-800V)** the power loop parasitic capacitances were needed to be reduced.

- Design 1: interleaved





- Design 2: without interleaving





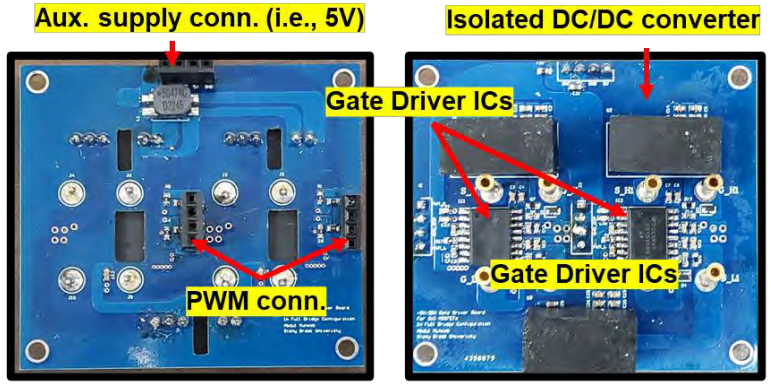
- **Simplified power loop geometry in Ansys Q3D environment**

$L_{Powerloop} = 1.37\ nH$
$C_{stray} = 73.87\ pF\ (Vcc + to\ AC)$
$C_{stray} = 67.77\ pF\ (Vcc - to\ AC)$

$L_{Powerloop} = 3.77\ nH$
$C_{stray} = 10.004\ pF\ (Vcc + to\ AC)$
$C_{stray} = 7.800\ pF\ (Vcc - to\ AC)$

SiC device's Coss is ~78 pF which is comparative to the stray capacitances, and it can induce high switching losses [1]

- **Design 2: without interleaving was selected.**



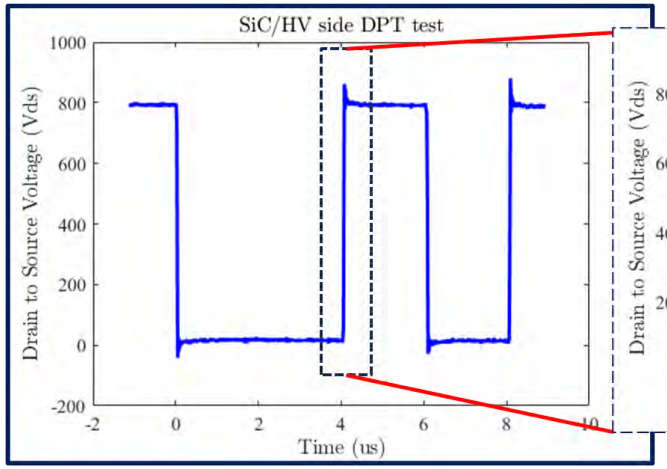
- Bottom side
- Top side

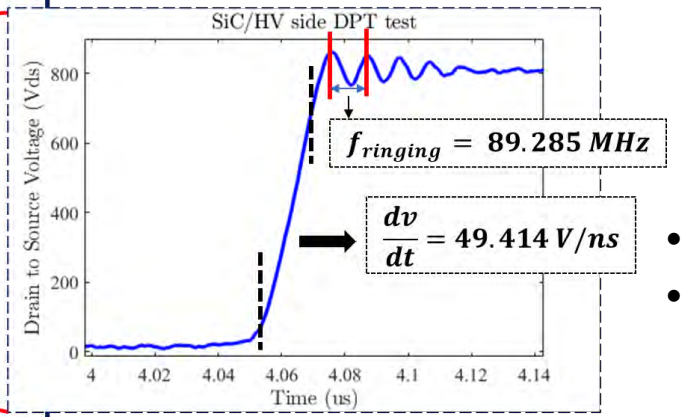
- **Gate Driver board**



- Top side
- Bottom side

- **Power board**



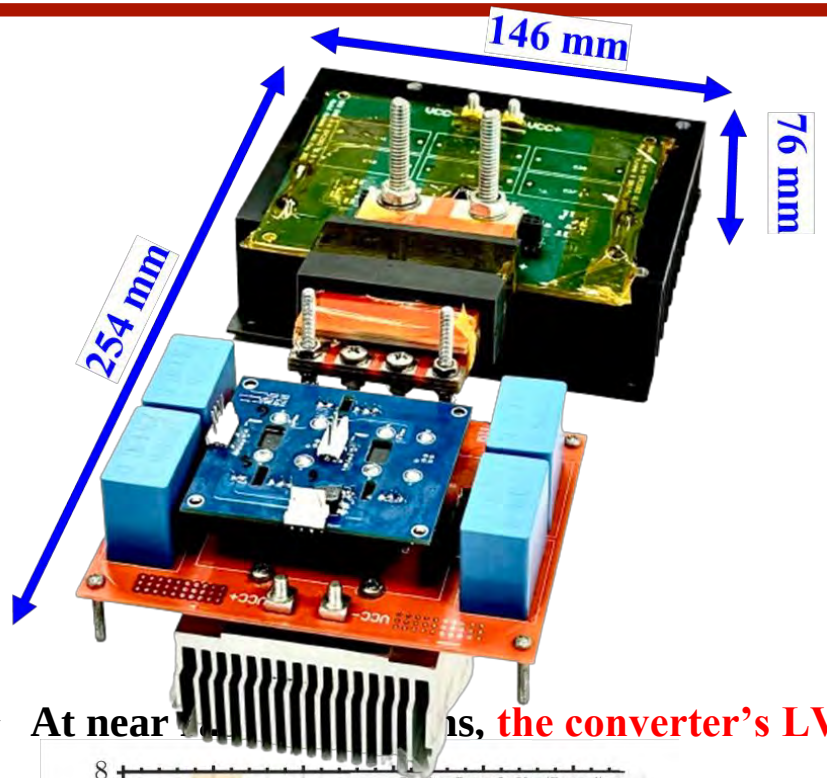


DPT test was performed:

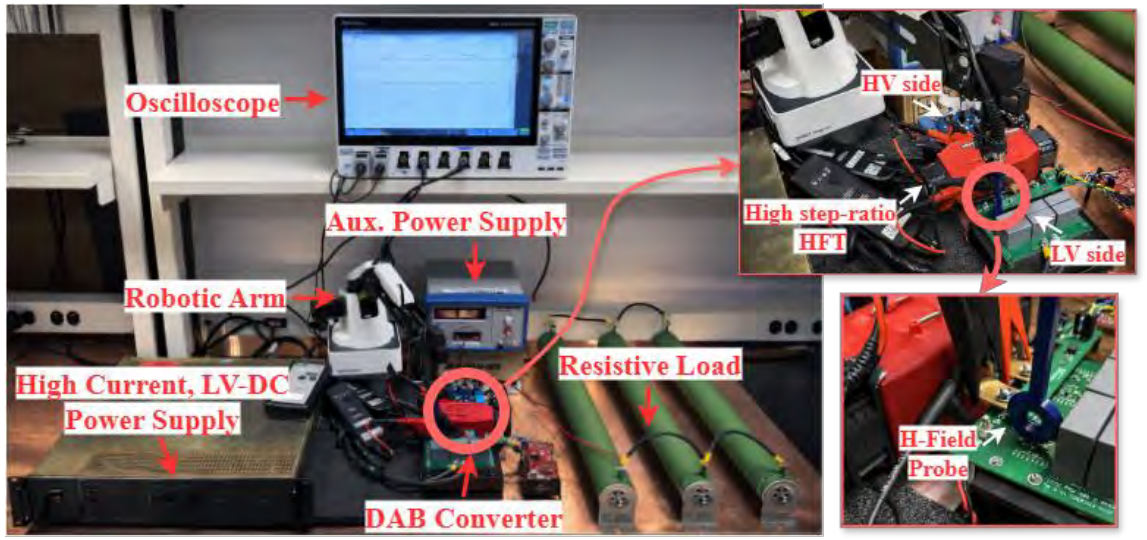
- **dv/dt = 49.414,**
- **di/dt= 6.9 A/ns**

[1] A. B. Mirza, A. Castiblanco, A. Muneeb, Y. Xie, S. S. Vala and F. Luo, "Impact of PCB Parasitic Capacitance on Switching Transients in Chopper and Half-Bridge Configurations Utilizing TO-247 SiC Devices," in IEEE Transactions on Industry Applications, vol. 61, no. 4, pp. 6618-6631, July-Aug. 2025,

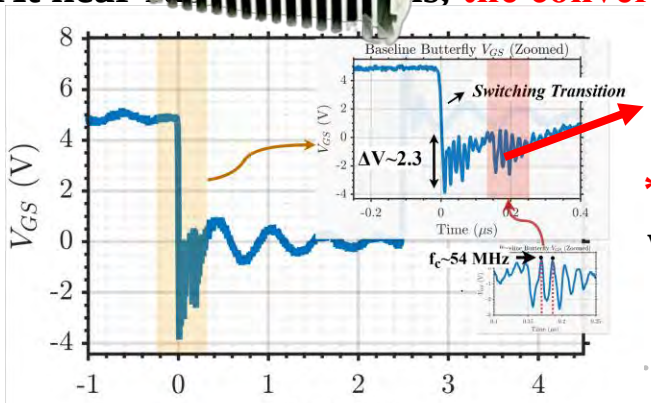
DAB Testing and Analysis



➢ **Hardware setup: Continuous DAB converter operation was tested**



➢ **At near [illegible]s, the converter's LV side AC node voltage started showing another ringing after the switching transition.**

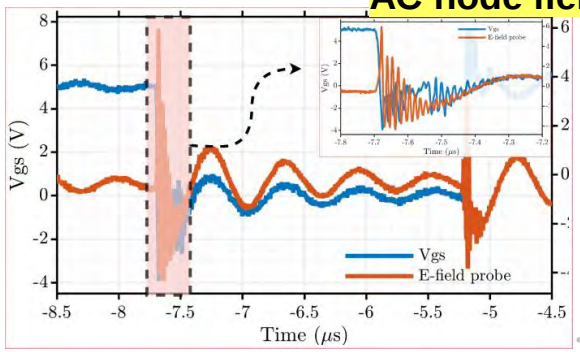


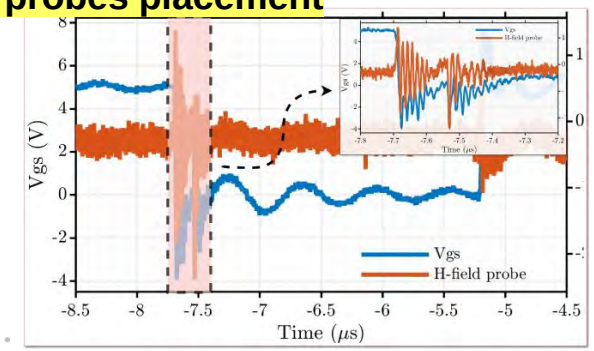
Phase shift transition.

***Same frequency ringing was observed on LV side VGS**

$$f_c = 54\ MHz$$

AC node field probes placement





➢ **VGS on LV side**

➢ **VGS and E-field**

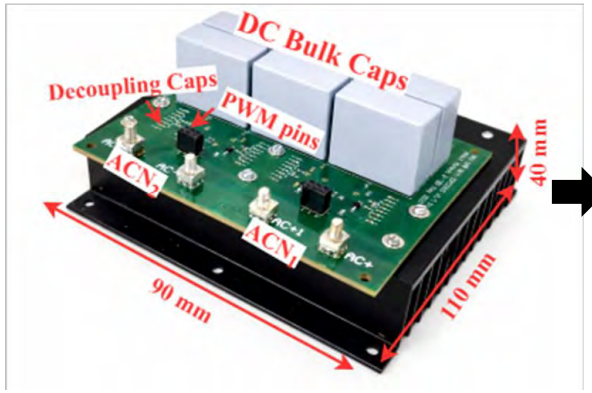
➢ **VGS and H-field**

FAR BEYOND

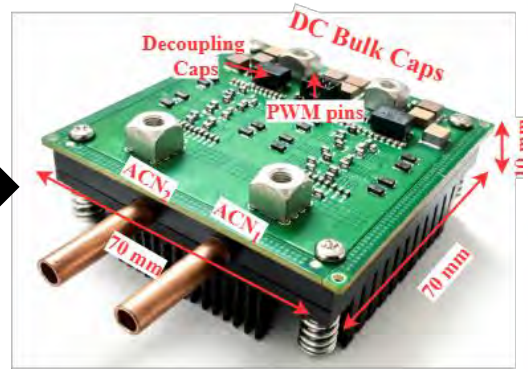
[1] A. Muneeb, A. B. Mirza, M. Ul Hassan, A. Anwar, A. Castiblanco and F. Luo, "Parasitic Capacitances in High Step Ratio Planar Transformers for Dual Active Bridge Converters: Cause and Effect," IECON 2024 - 50th Annual Conference of the IEEE Industrial Electronics Society, Chicago, IL, USA, 2024

Cross-talk Mitigation: Transformer

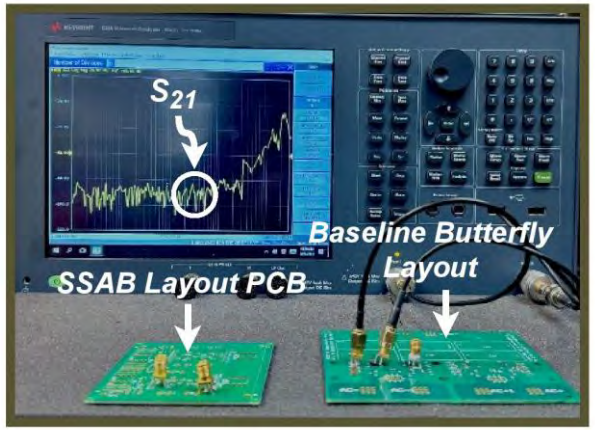
- **After transformer and PCB layout optimization the hardware was tested with VNA and S21 measurement was compared.**

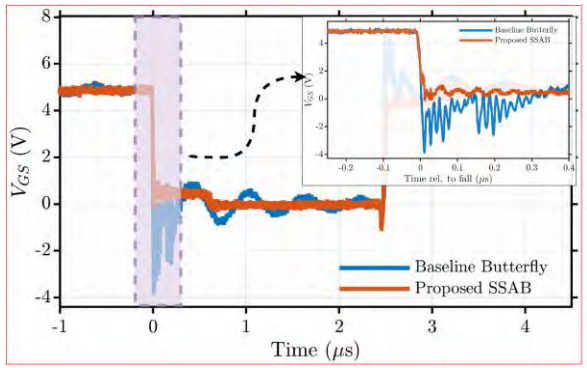


- **Baseline butterfly layout**

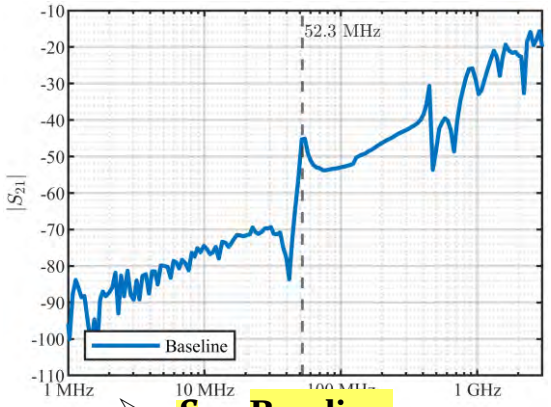


- **SSAB layout**

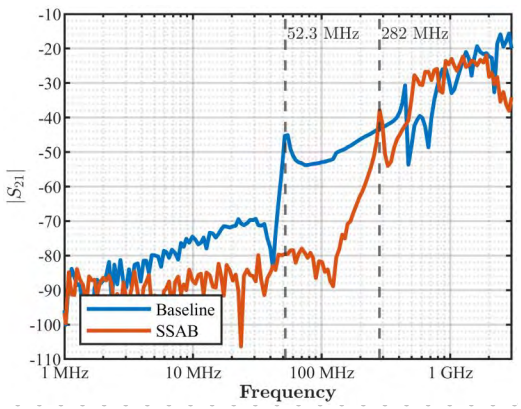




- **VGS SSAB layout**

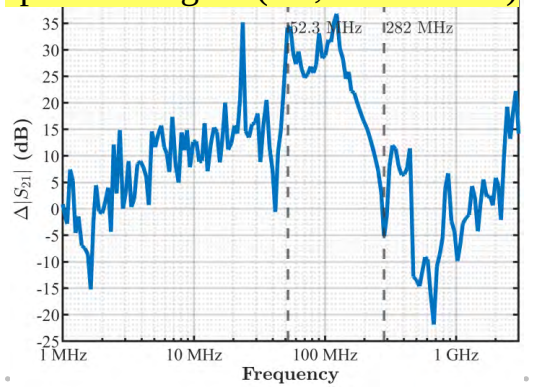


- **S_{21}: Baseline butterfly layout**

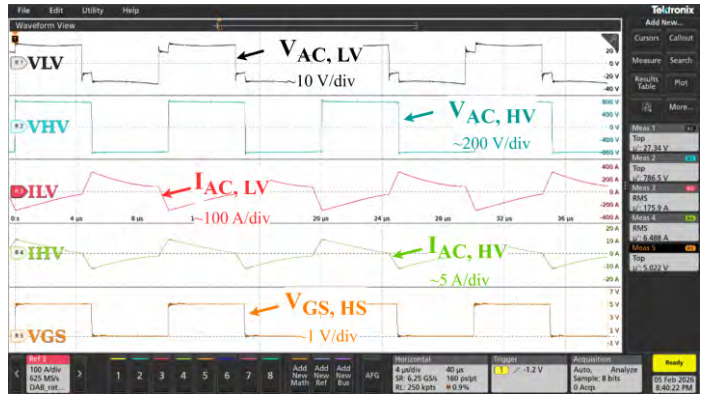


- **S_{21}: Baseline Vs SSAB**

~30 dB difference int e gate resonance spectrum region (i.e., 51-63 MHz)



- **▲ S_{21}**

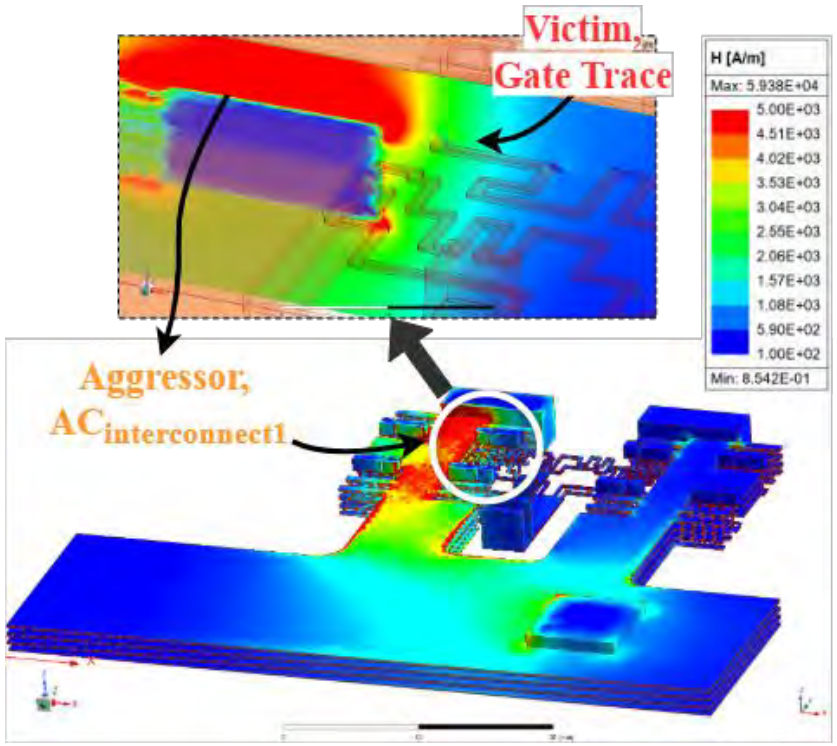


- **Rated DAB converter operation: Stable VGS**

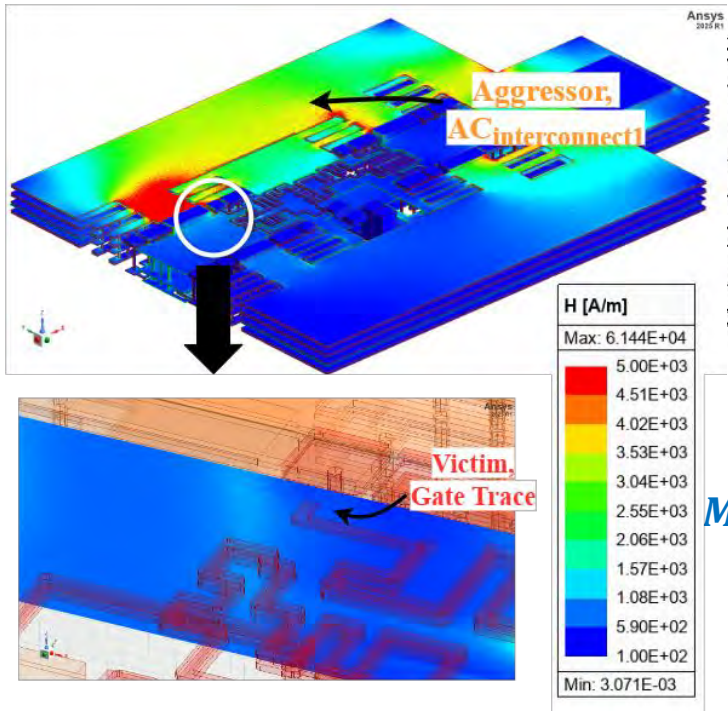
[1] A. Muneeb, A. Anwar, A. B. Mirza, Y. Li, S. Deng, M. Hijikata, and F. Luo, "Near-Field Coupling in Butterfly-Layout Paralleled GaN Power Stages for High Step-Ratio Power Conversion," IEEE Transactions on Power Electronics, submitted for publication, 2026.
[2] [1] A. Muneeb, A. B. Mirza, Samuel Defaz, and F. Luo, "Impact of high dv/dt on the high step ratio DAB converter," IEEE Transactions on Power Electronics, accepted for publication, 2025.

Cross-talk Mitigation: LV side PCB

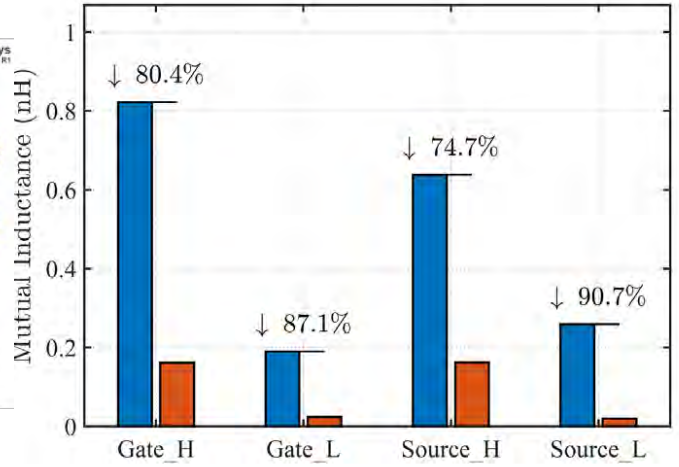
- **Ansys Maxwell simulations were conducted to visualize the H-field on the gate regions**



- **Baseline Butterfly Layout**



- **SSAB Layout**



M_{eff} in Baseline butterfly layout

↓ $75–91\%$ *reduction*

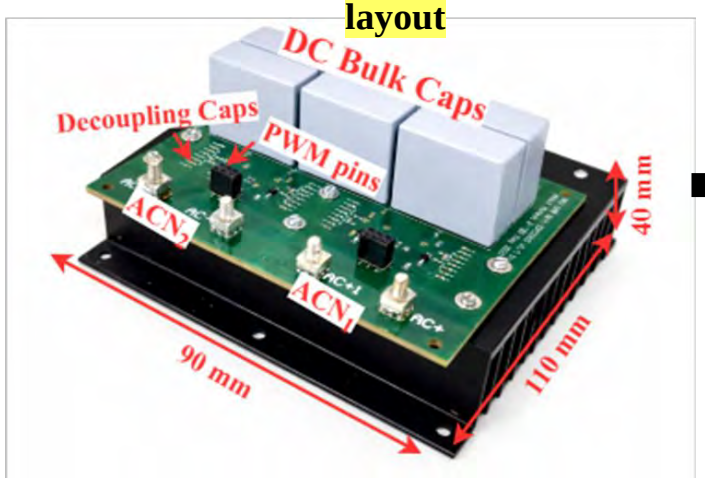
M_{eff} in SSAB layout

SSAB achieves >75% reduction in Meff wihtout changing the power loop and without increasing PCB footprint.

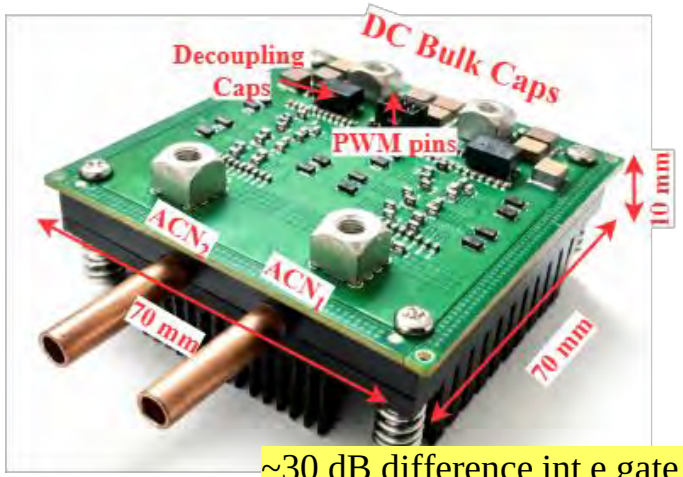
[1] A. Muneeb, A. Anwar, A. B. Mirza, Y. Li, S. Deng, M. Hijikata, and F. Luo, "Near-Field Coupling in Butterfly-Layout Paralleled GaN Power Stages for High Step-Ratio Power Conversion," IEEE Transactions on Power Electronics, submitted for publication, 2026.
[2] [1] A. Muneeb, A. B. Mirza, Samuel Defaz, and F. Luo, "Impact of high dv/dt on the high step ratio DAB converter," IEEE Transactions on Power Electronics, accepted for publication, 2025.

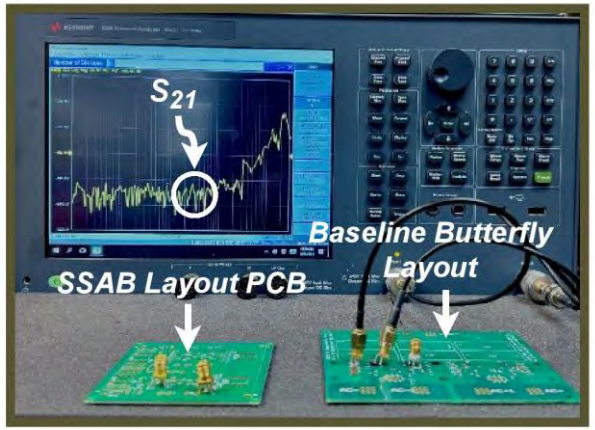
Cross-talk Mitigation: Transformer

➢ **Baseline butterfly layout**

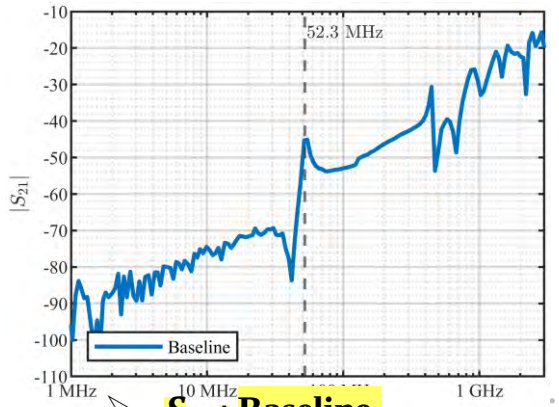


➢ **SSAB layout**

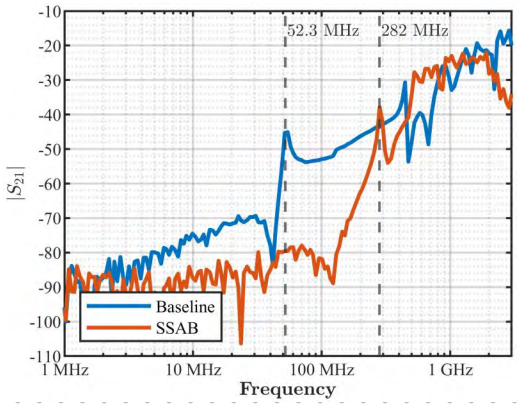




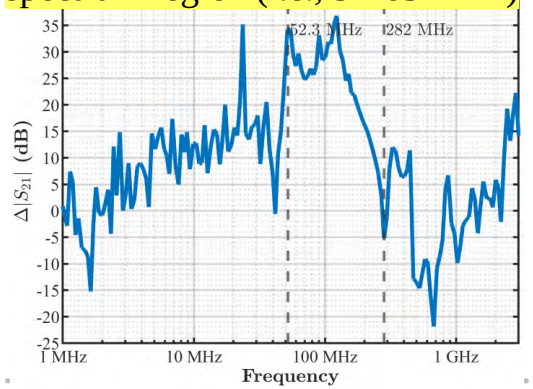
~30 dB difference int e gate resonance spectrum region (i.e., 51-63 MHz)



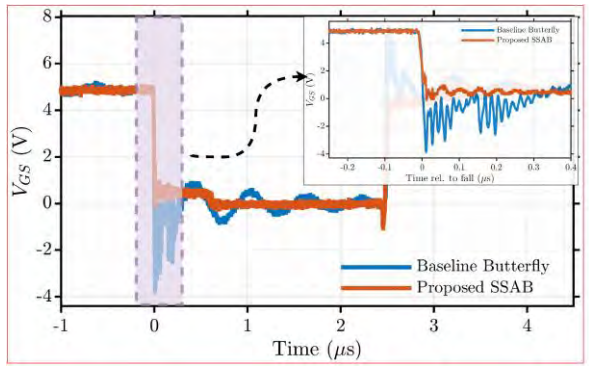
➢ S_{21}: **Baseline butterfly layout**



➢ S_{21}: **Baseline Vs SSAB**



➢ ▲ S_{21}

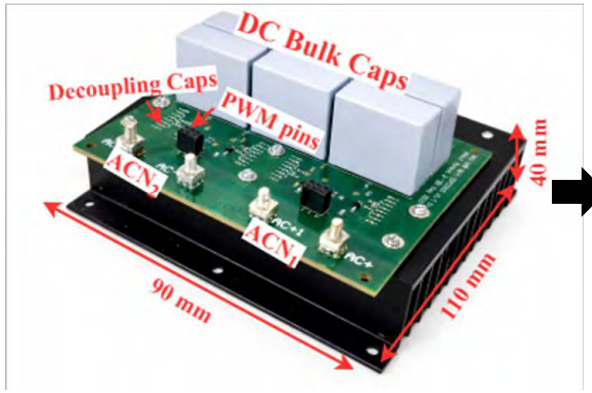


➢ **VGS SSAB layout**

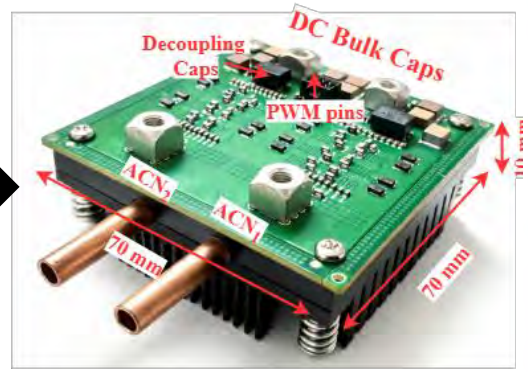
[1] A. Muneeb, A. Anwar, A. B. Mirza, Y. Li, S. Deng, M. Hijikata, and F. Luo, "Near-Field Coupling in Butterfly-Layout Paralleled GaN Power Stages for High Step-Ratio Power Conversion," IEEE Transactions on Power Electronics, submitted for publication, 2026.
[2] [1] A. Muneeb, A. B. Mirza, Samuel Defaz, and F. Luo, "Impact of high dv/dt on the high step ratio DAB converter," IEEE Transactions on Power Electronics, accepted for publication, 2025.

Cross-talk Mitigation: Transformer

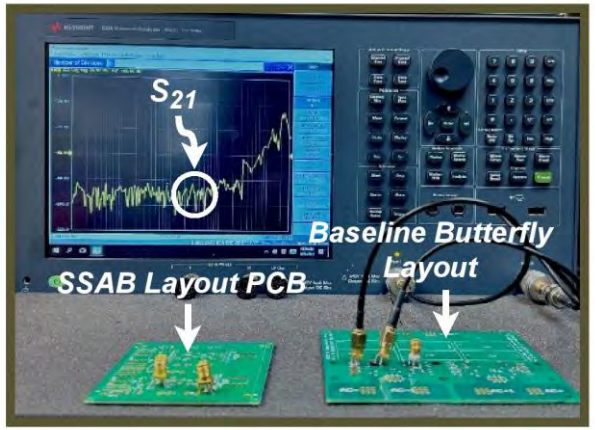
- **After transformer and PCB layout optimization the hardware was tested with VNA and S21 measurement was compared.**

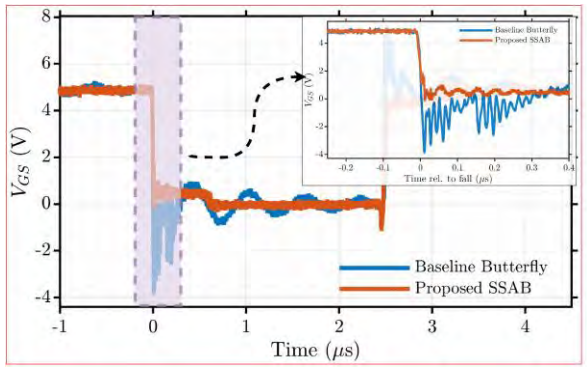


- **Baseline butterfly layout**

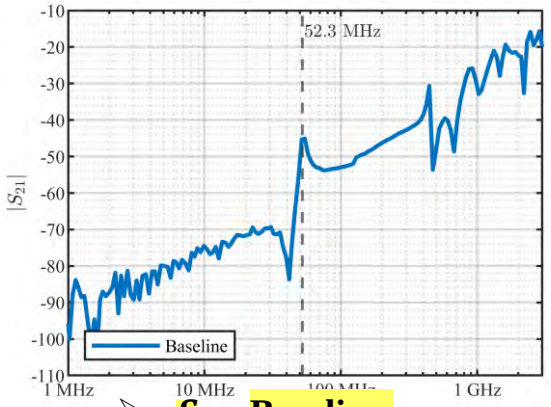


- **SSAB layout**

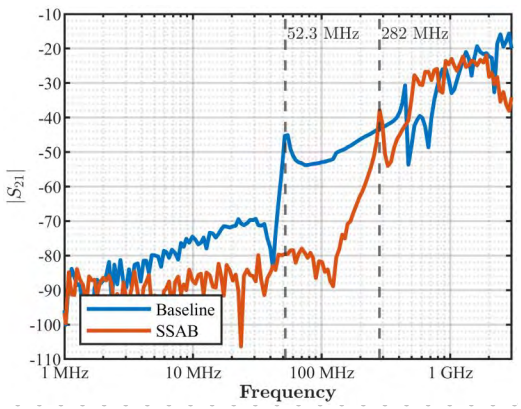




- **VGS SSAB layout**

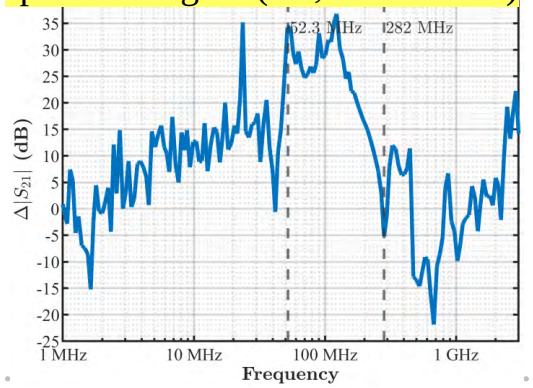


- **S_{21}: Baseline butterfly layout**

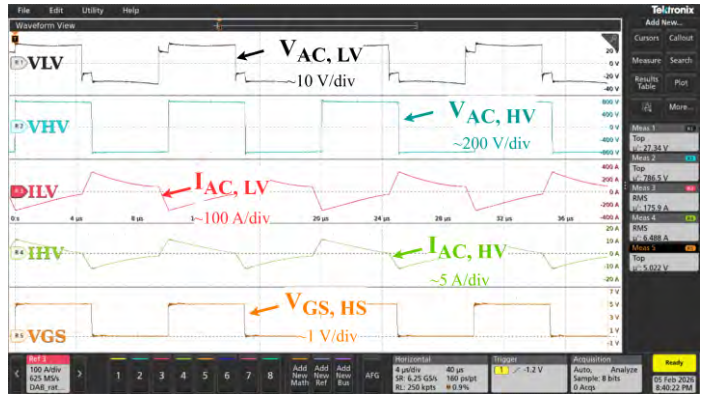


- **S_{21}: Baseline Vs SSAB**

~30 dB difference int e gate resonance spectrum region (i.e., 51-63 MHz)



- **▲ S_{21}**



- **Rated DAB converter operation: Stable VGS**

[1] A. Muneeb, A. Anwar, A. B. Mirza, Y. Li, S. Deng, M. Hijikata, and F. Luo, "Near-Field Coupling in Butterfly-Layout Paralleled GaN Power Stages for High Step-Ratio Power Conversion," IEEE Transactions on Power Electronics, submitted for publication, 2026.
[2] [1] A. Muneeb, A. B. Mirza, Samuel Defaz, and F. Luo, "Impact of high dv/dt on the high step ratio DAB converter," IEEE Transactions on Power Electronics, accepted for publication, 2025.