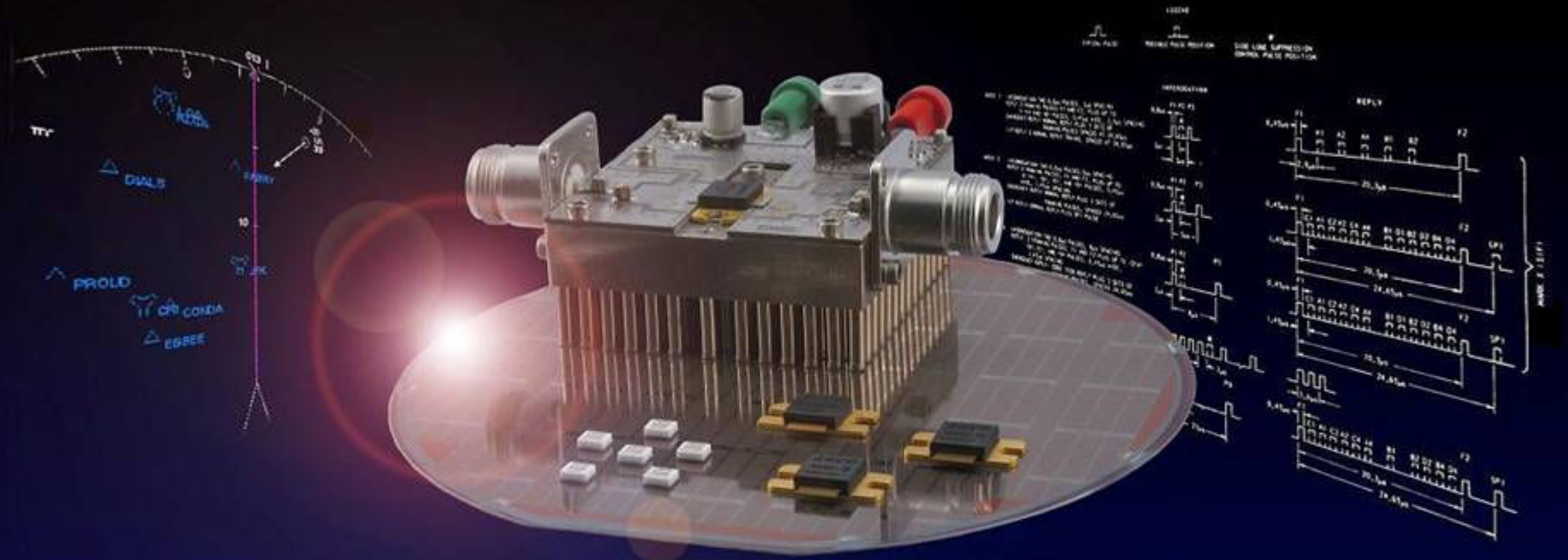
Introducing the High Voltage Vertical Technology for High Power Applications



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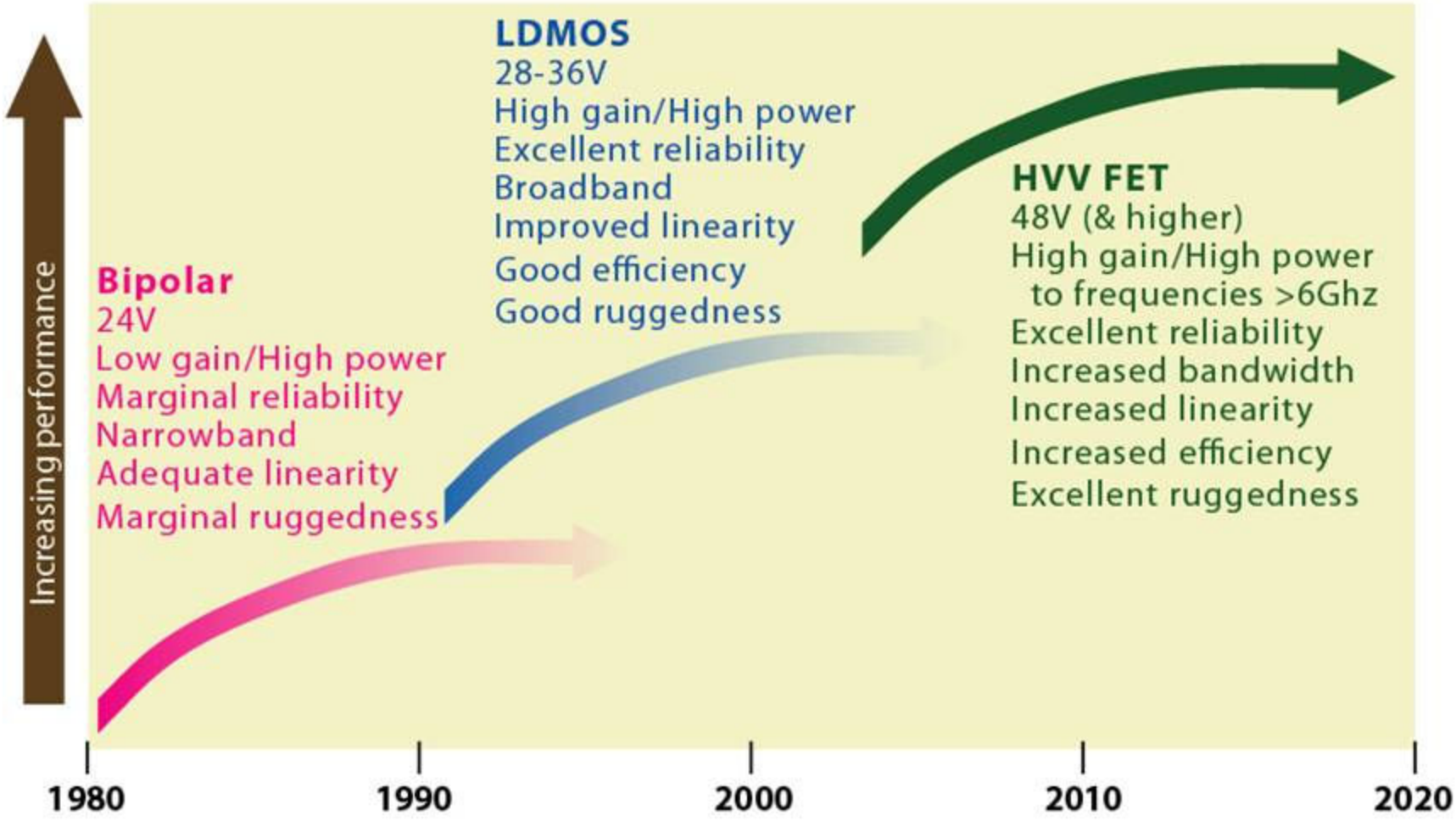
HVVi Semiconductors

Phoenix, AZ

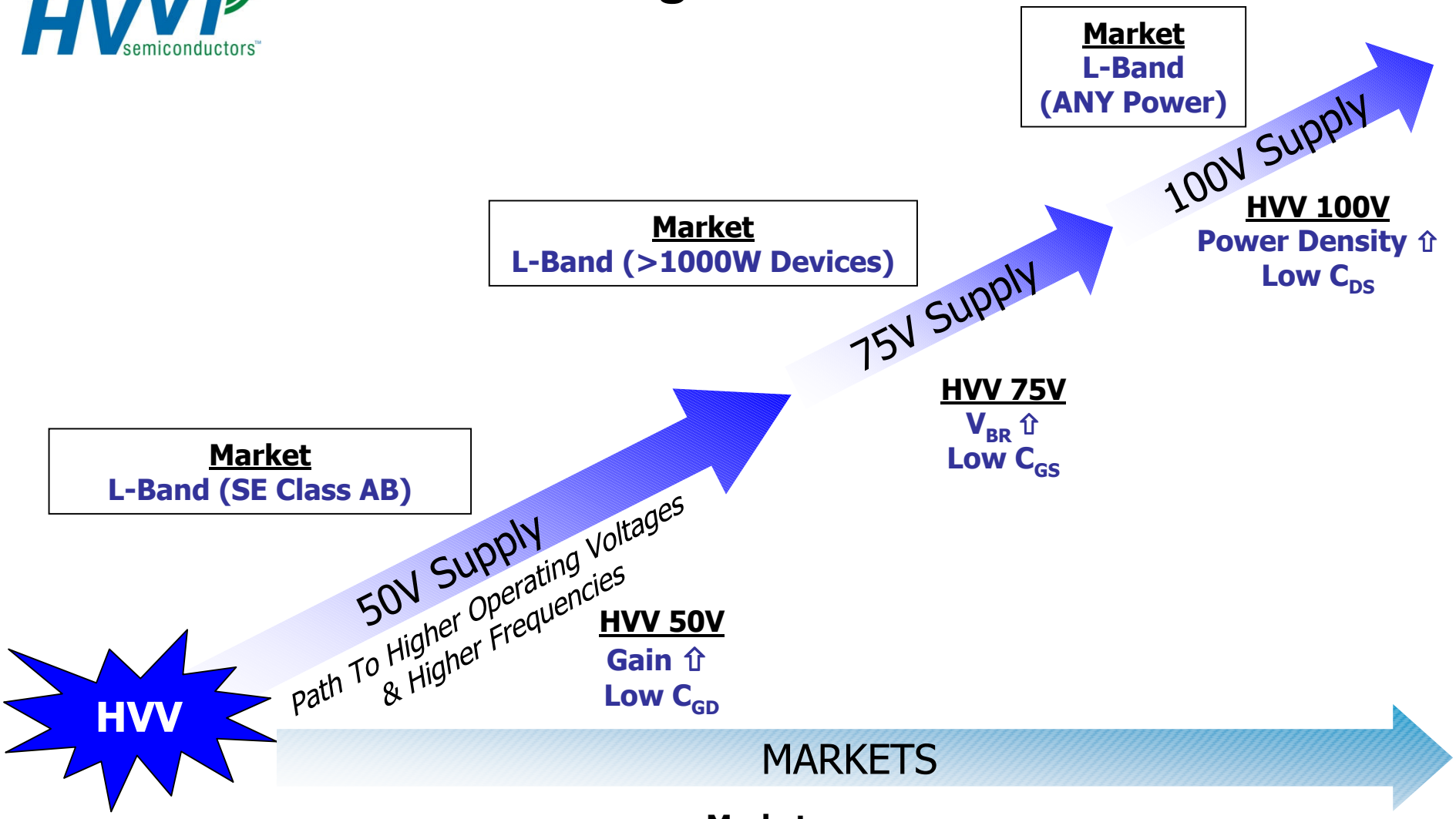
AGENDA

Background
Device Overview
Packaging Strategy
HVVFET Advantages
Transistor Performance
Reliability
Summary

Silicon Technology History



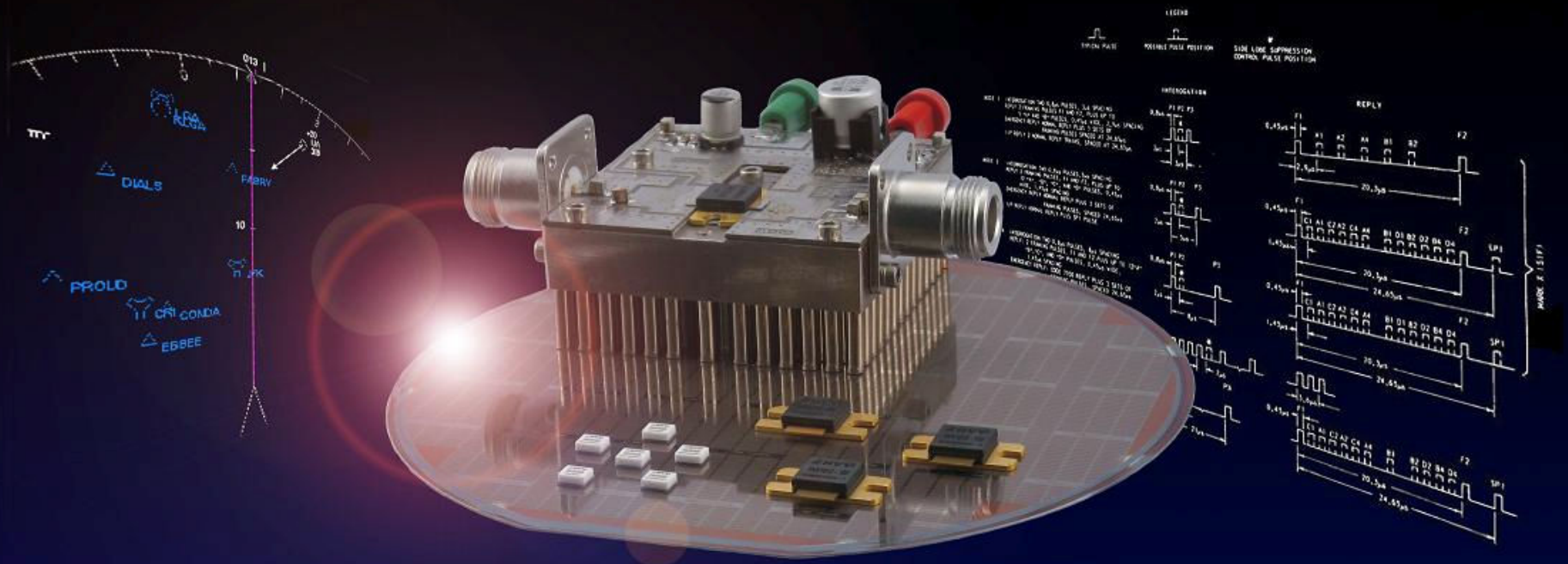
Breakthrough Product Differentiation



Markets

L-Band (Avionics & Radar) Rugged Power and Efficiency, Low Bandwidth

Vertical Device Structure Overview



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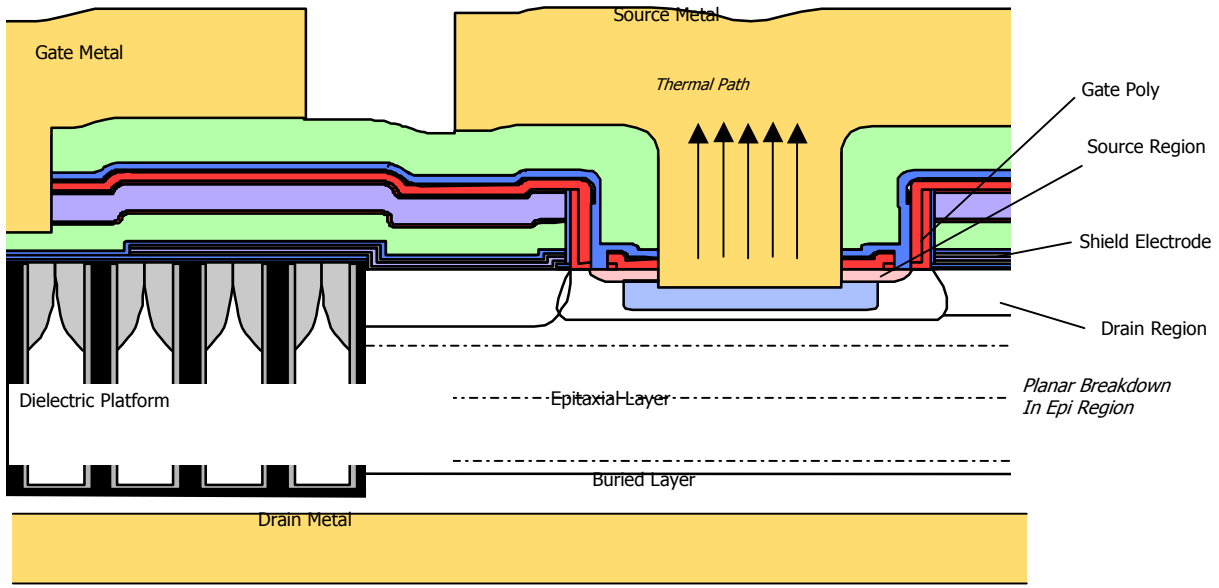
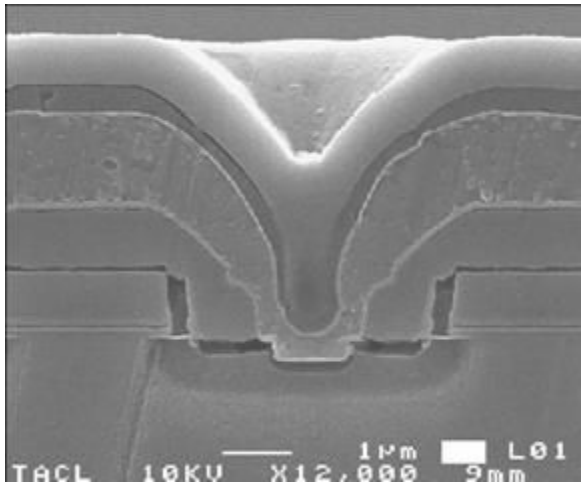
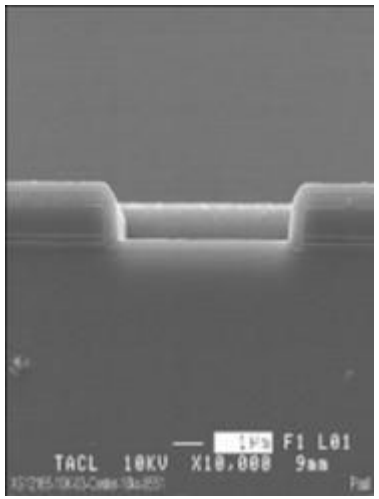
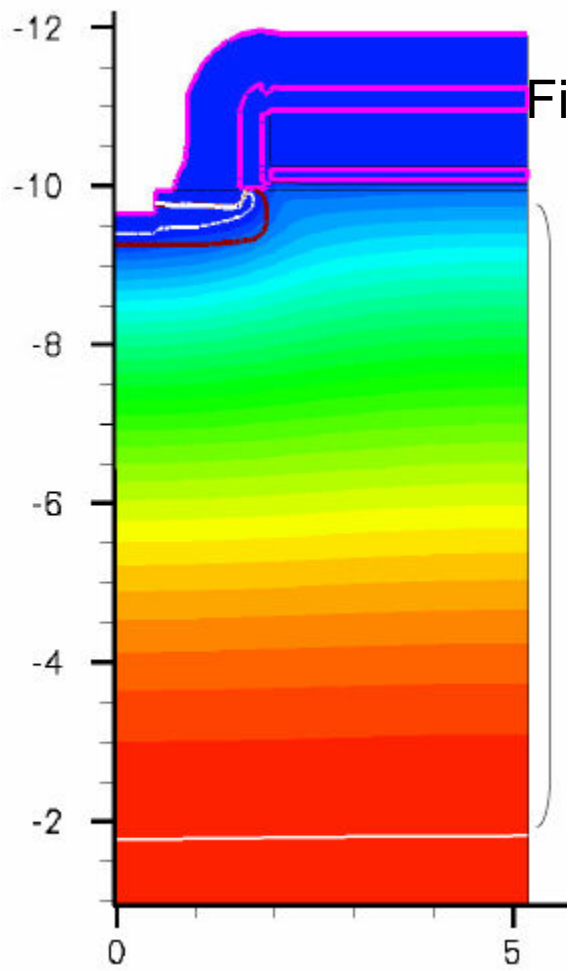
Vertical Device Structure and Cross Sections







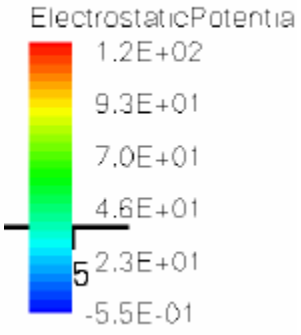
Vertical Device Characteristics - BVDSS



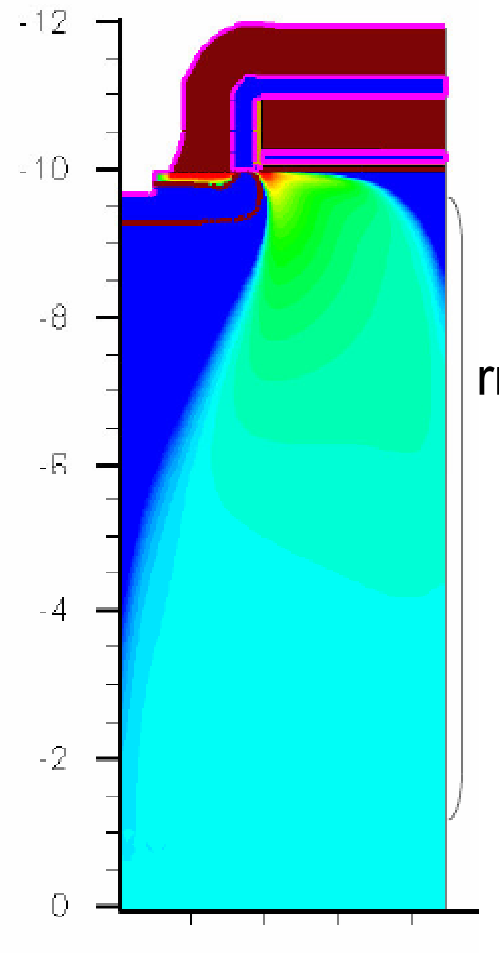
First Generation Breakdown Voltage

120V Breakdown
~ 8um of Epi

Equal Potential Lines



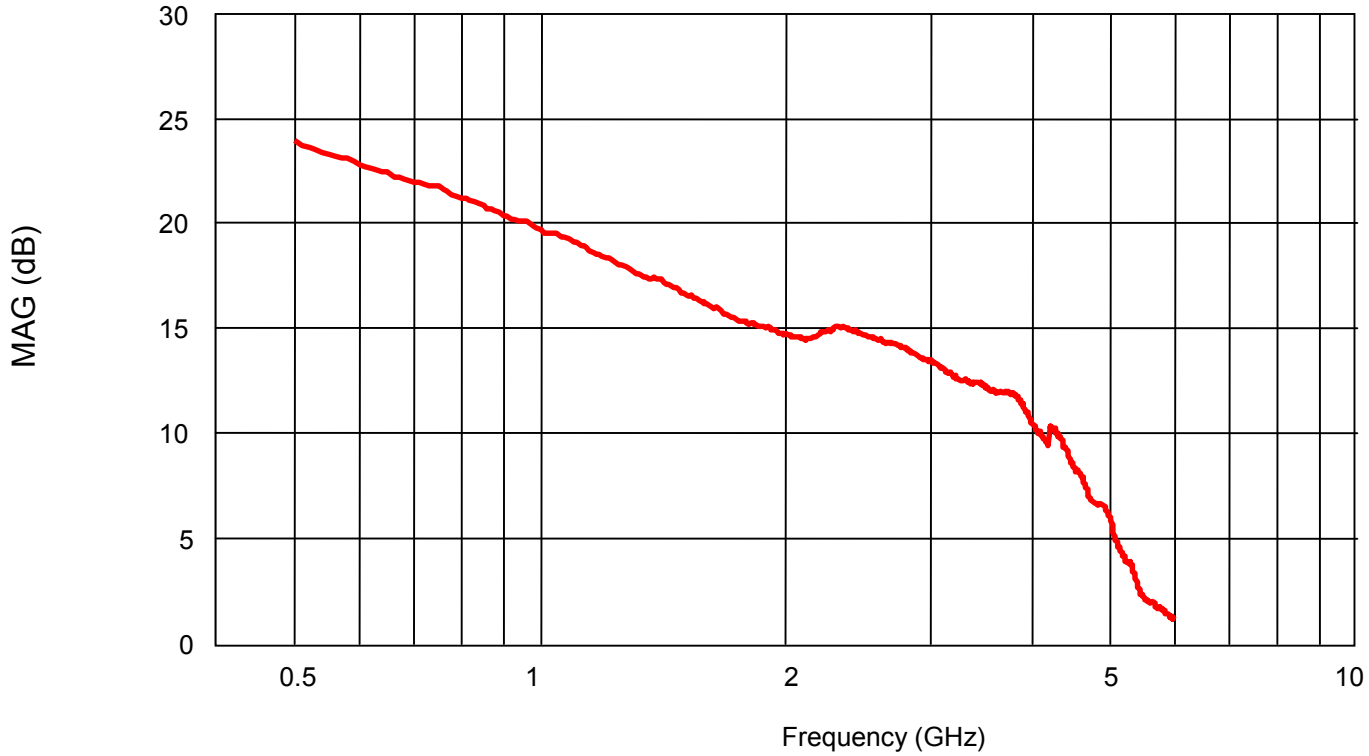
Vertical Device Current Path



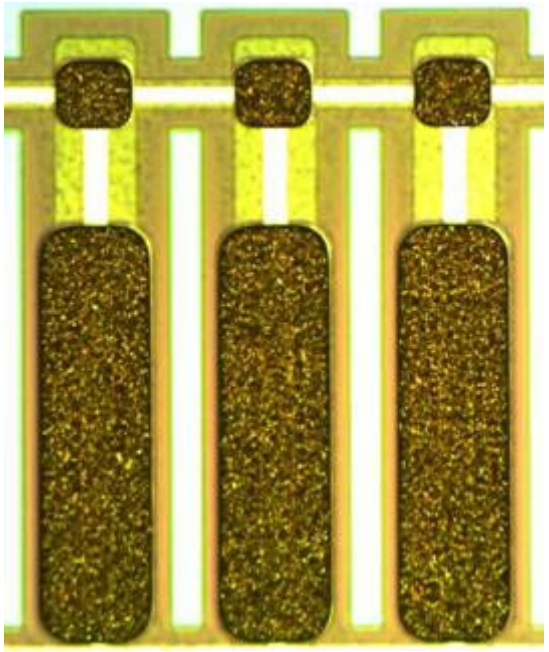
rrent Flow in Epitaxial Region

Vertical Device Characteristics

Maximum Available Gain

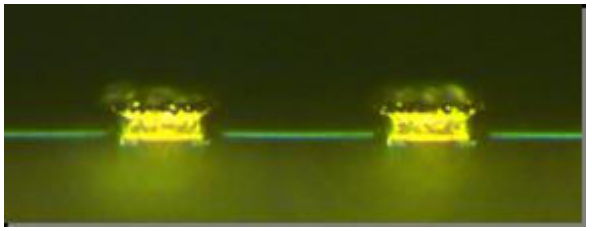


Unique Device Characteristics



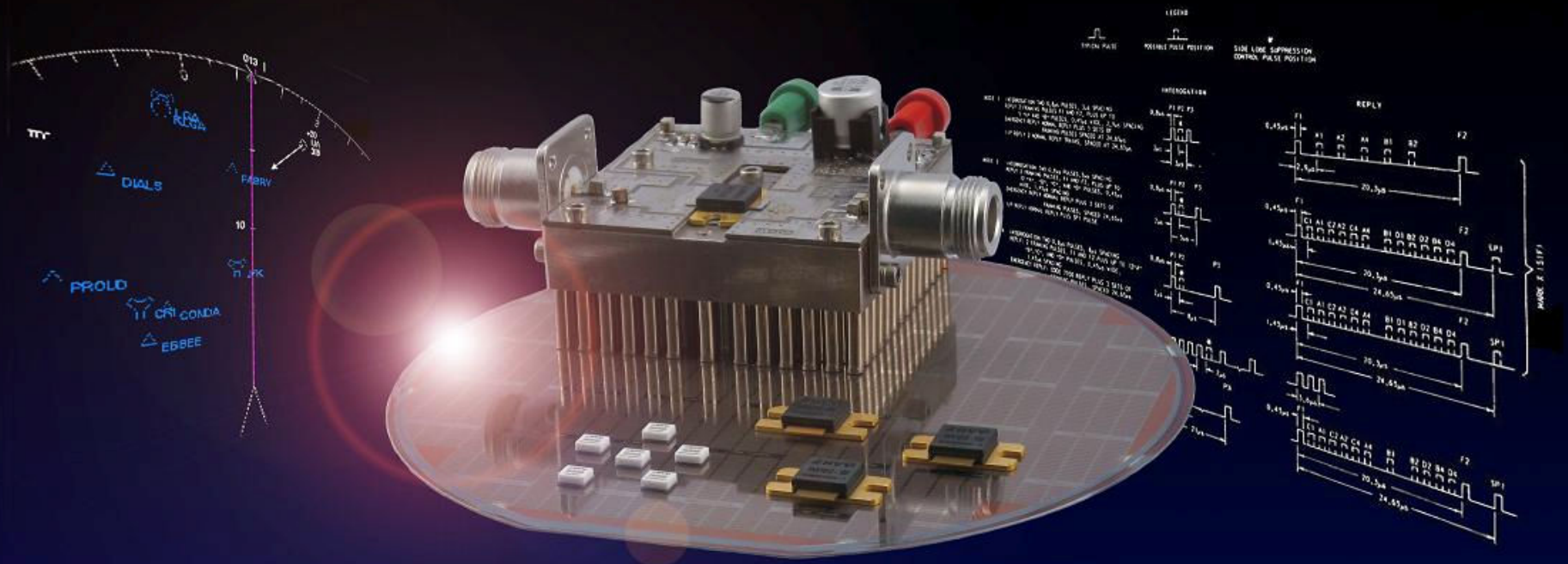
Gate Terminal Bumps

Source Terminal Bumps



Bump Cross-Section

High Power Package Overview



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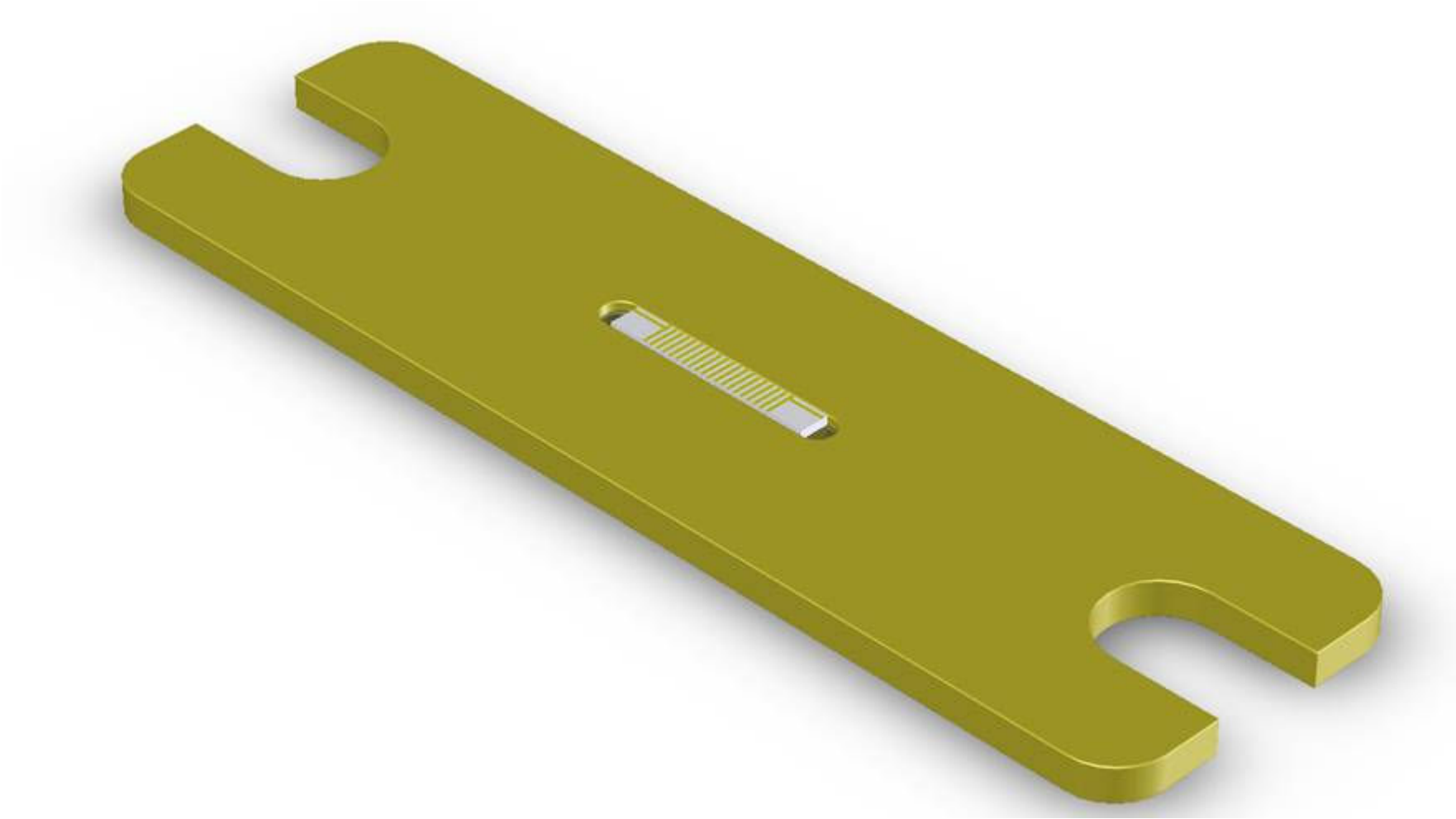
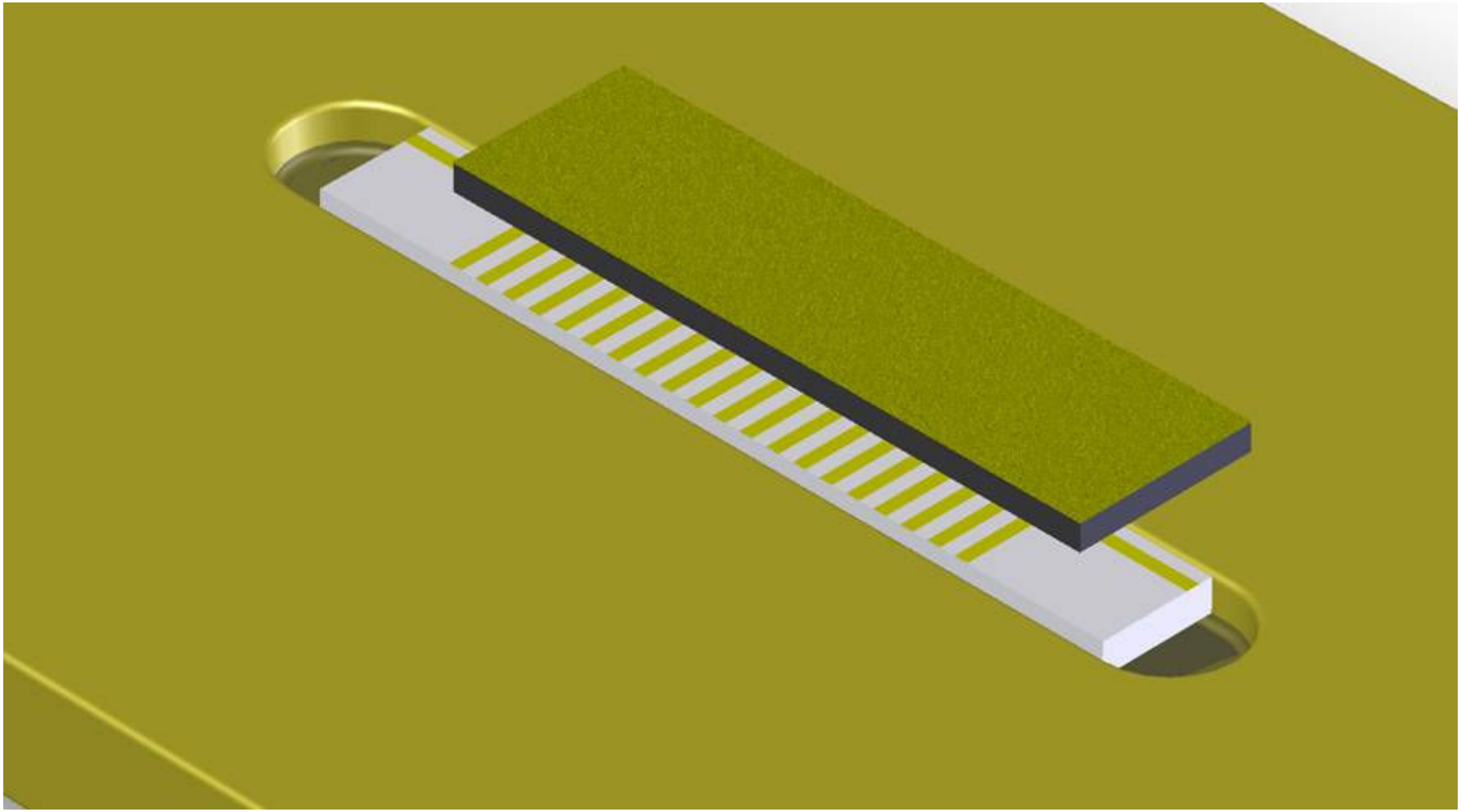
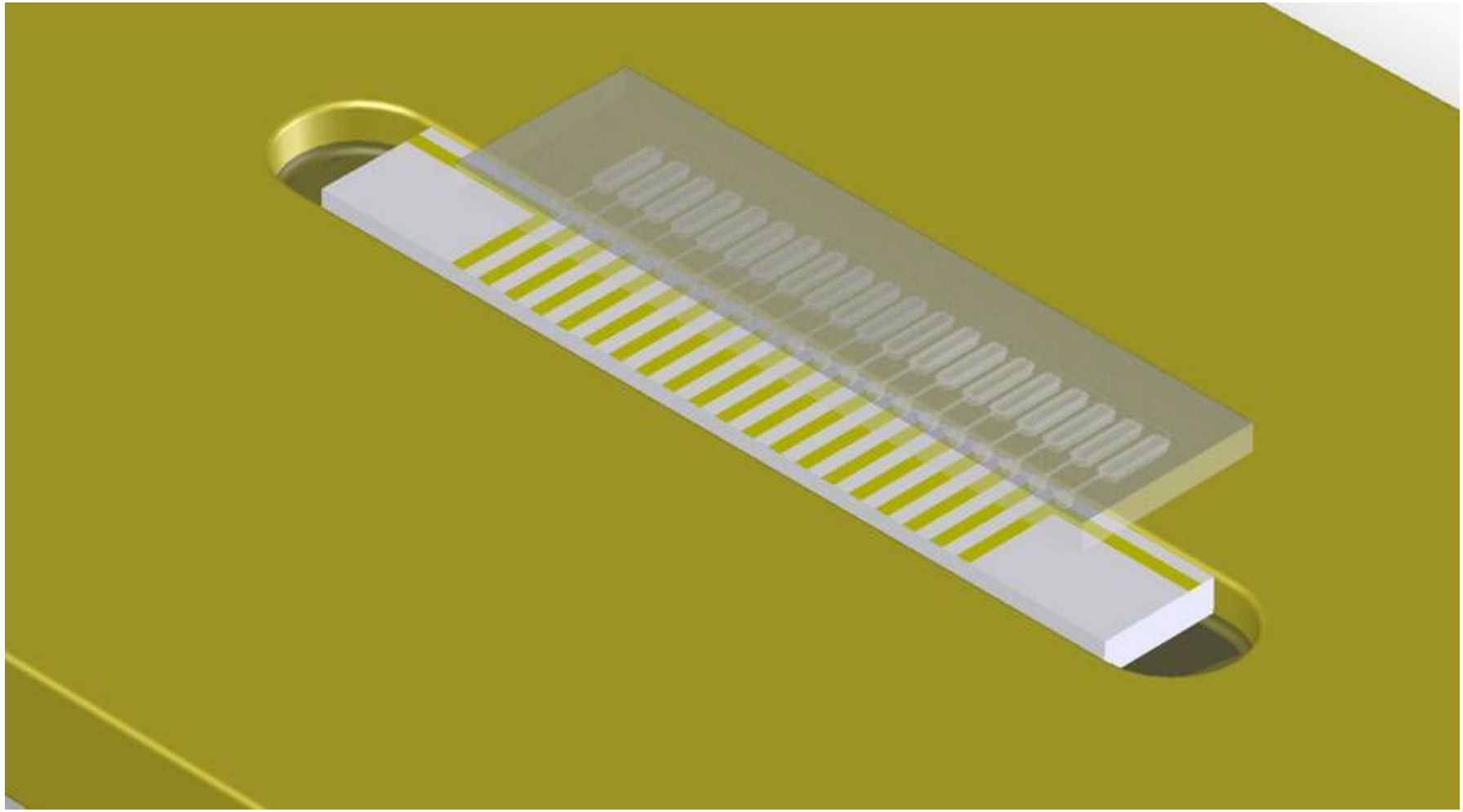
1 – Flange with interposer attached



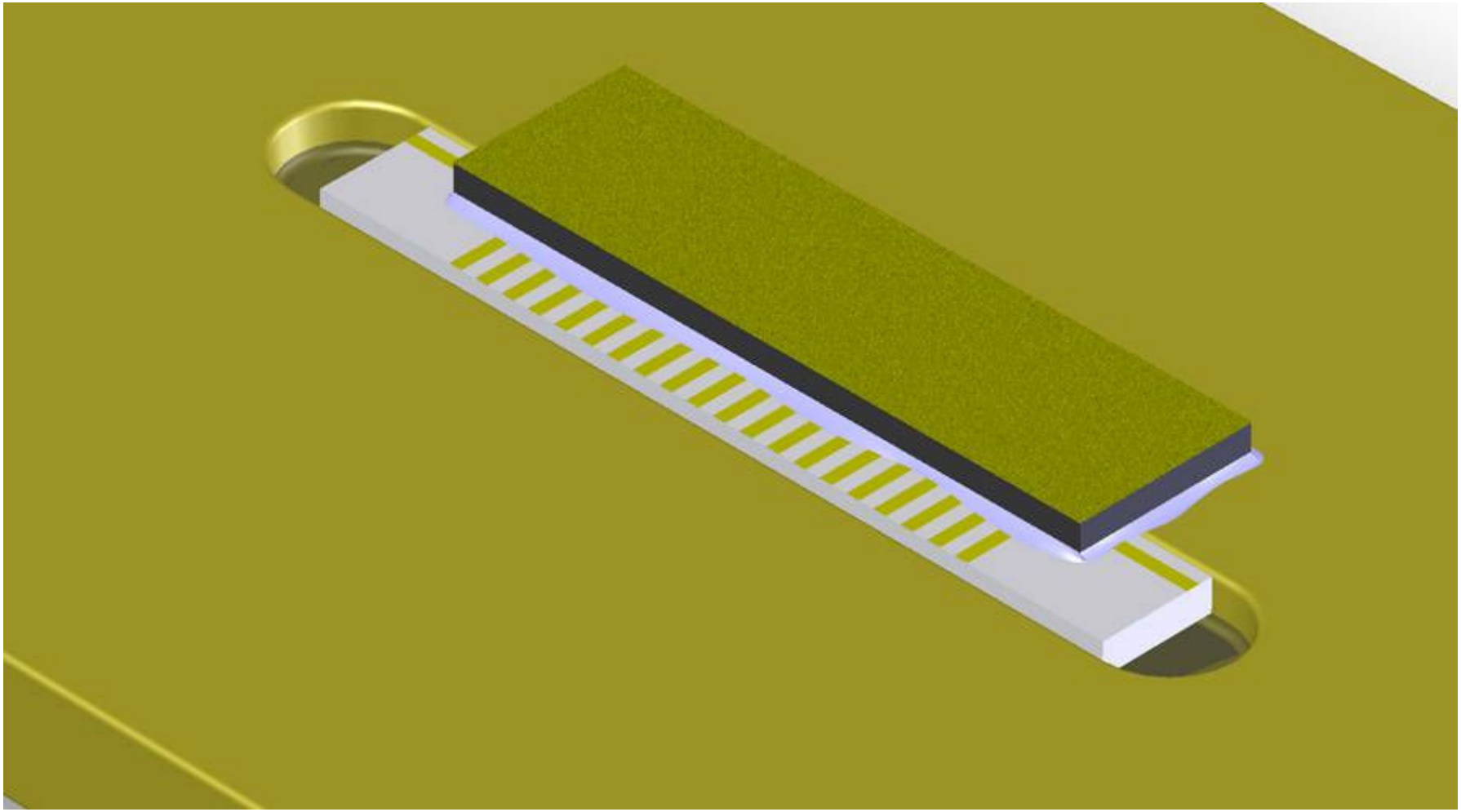
2A – Die attach, AuSn eutectic



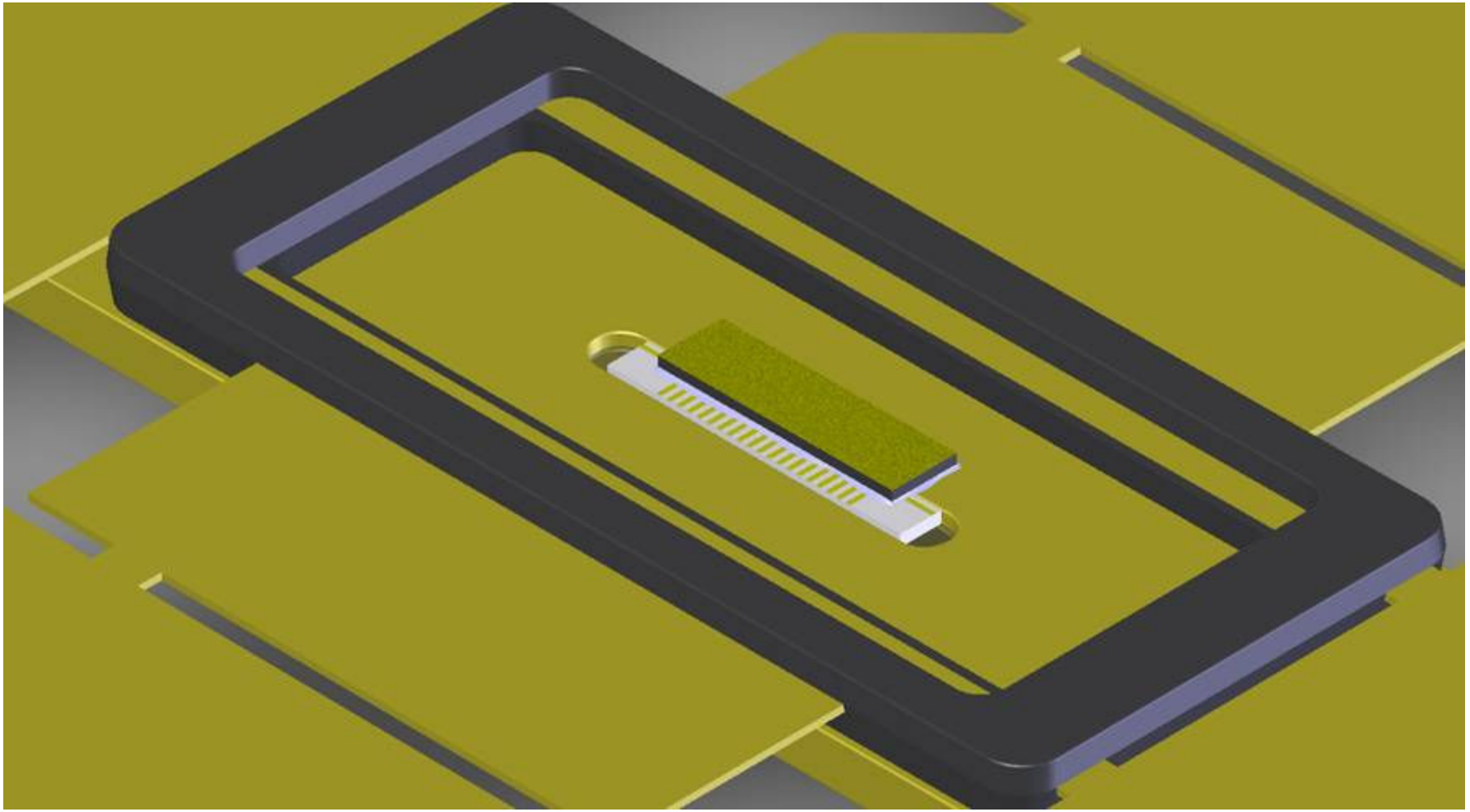
2B – Die attach, AuSn eutectic - transparent



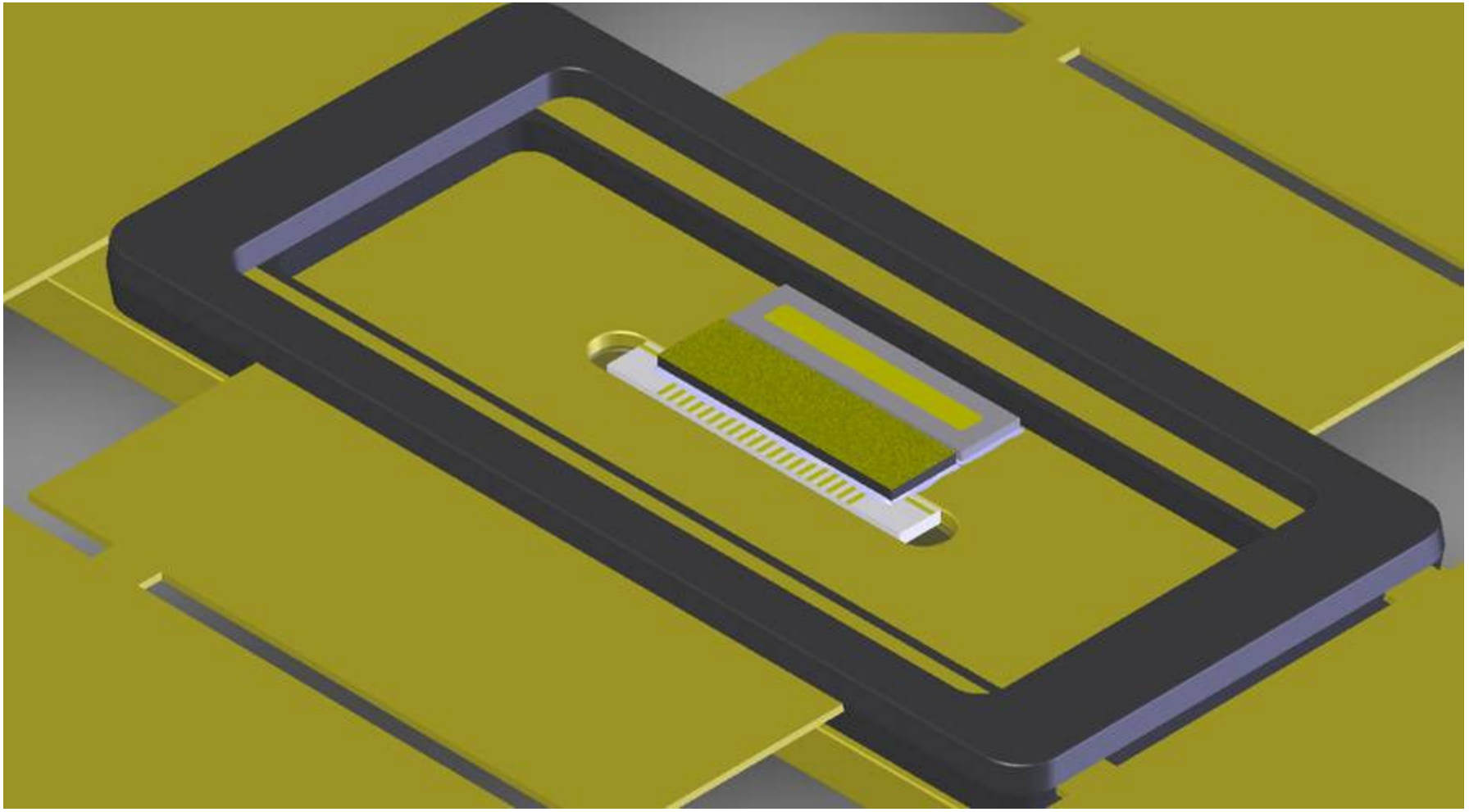
3 – Underfill application and cure



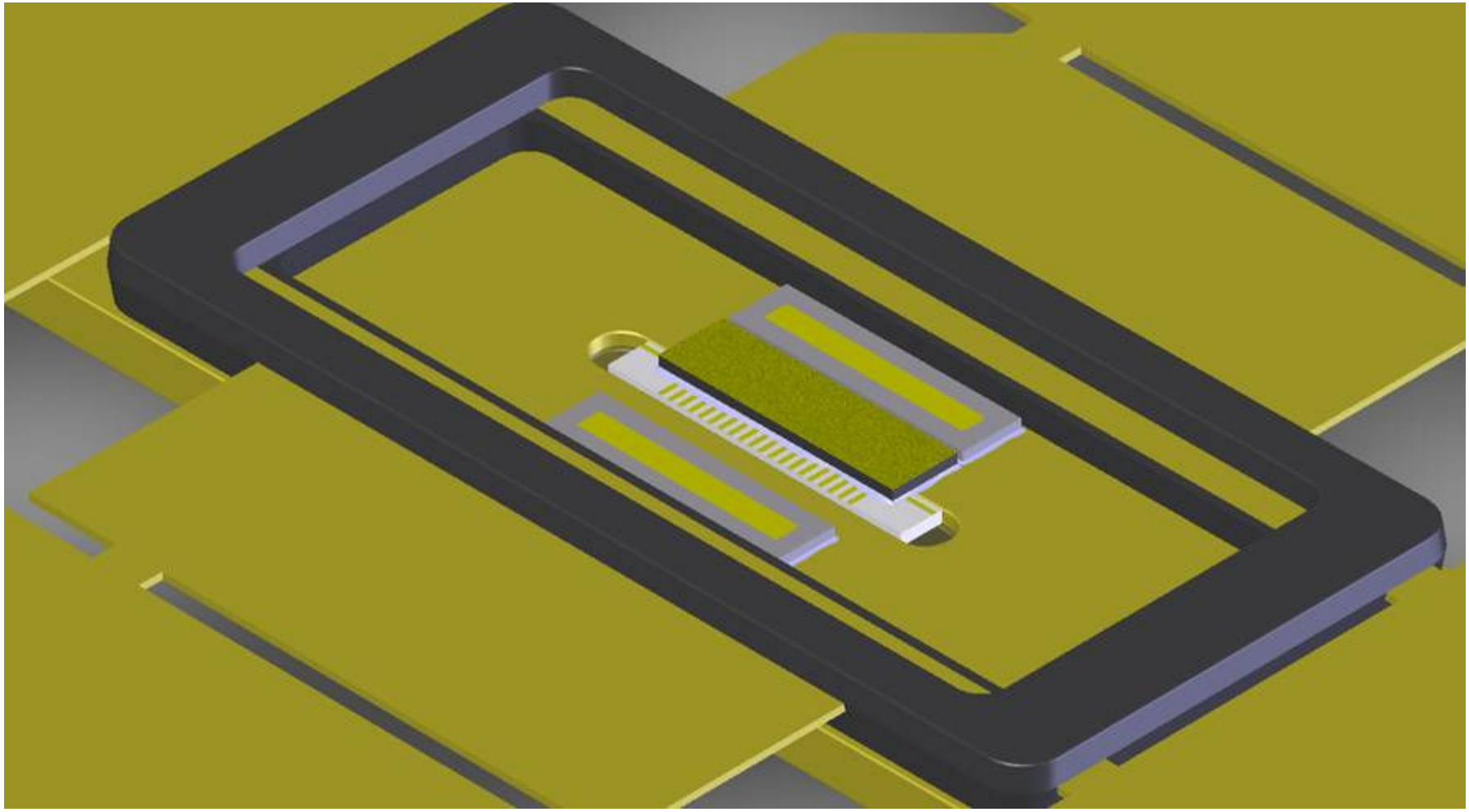
4 – Seal leadframe to flange



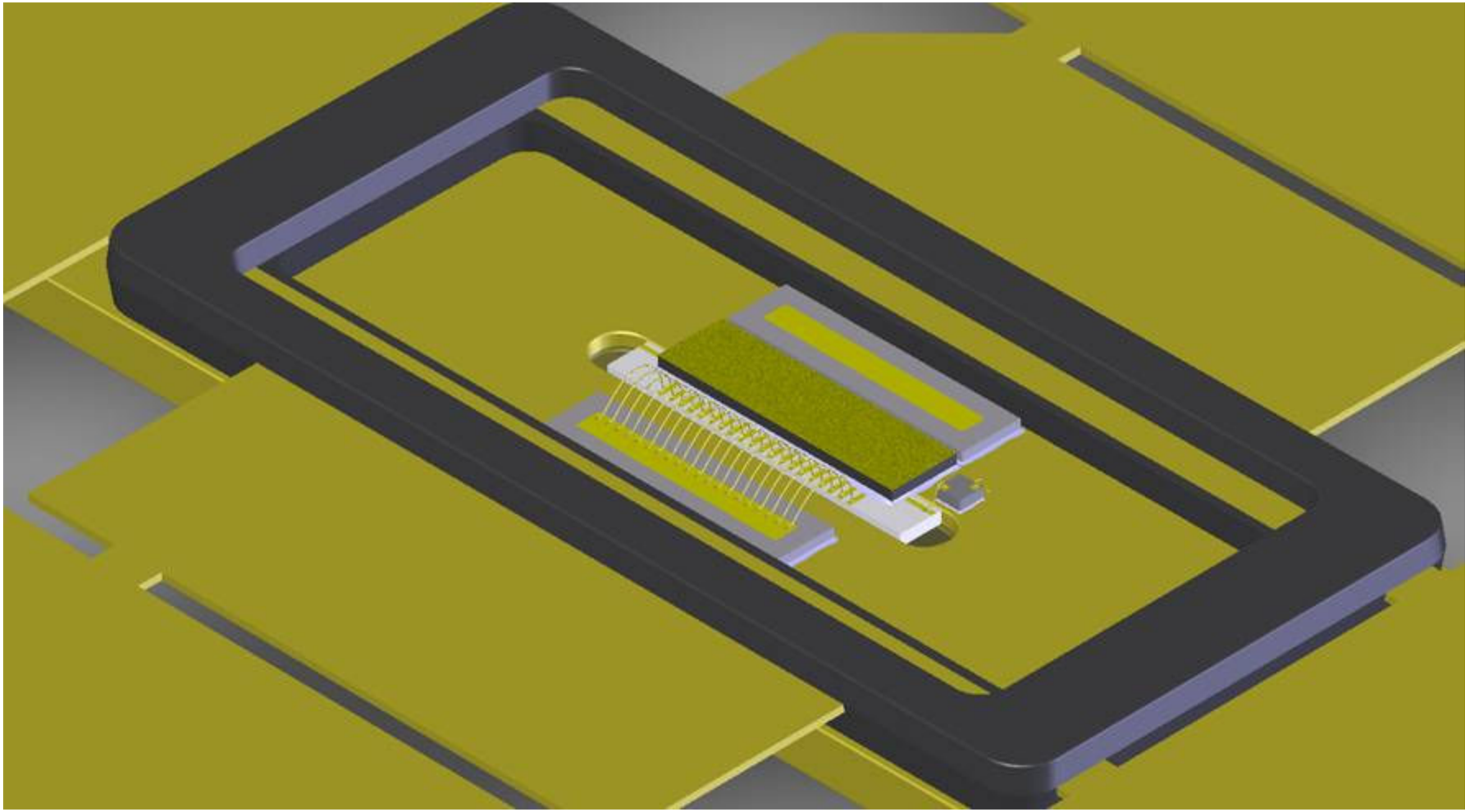
5 – Output MOSCAP attach – Ag epoxy



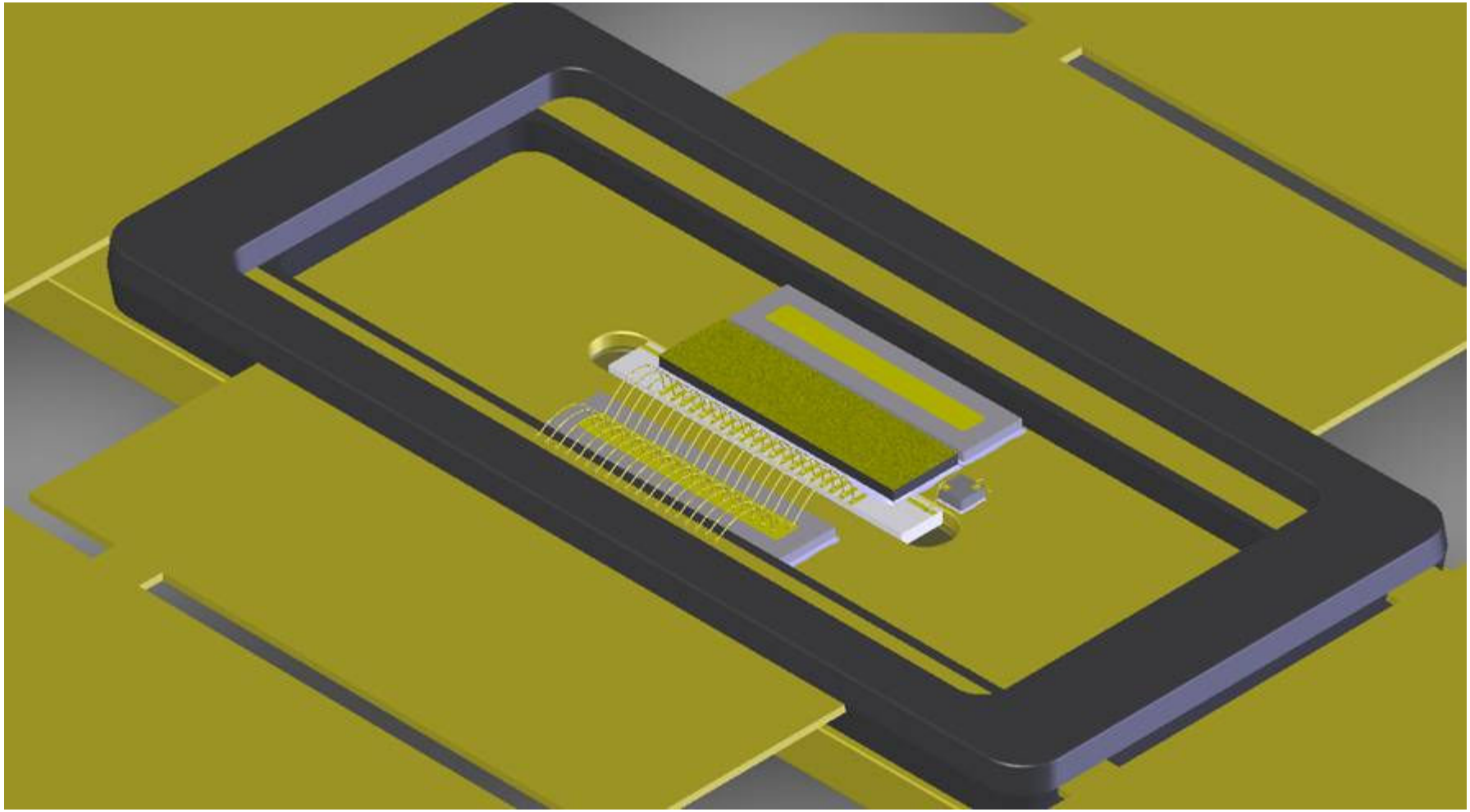
6 – Input MOSCAP attach – Ag epoxy



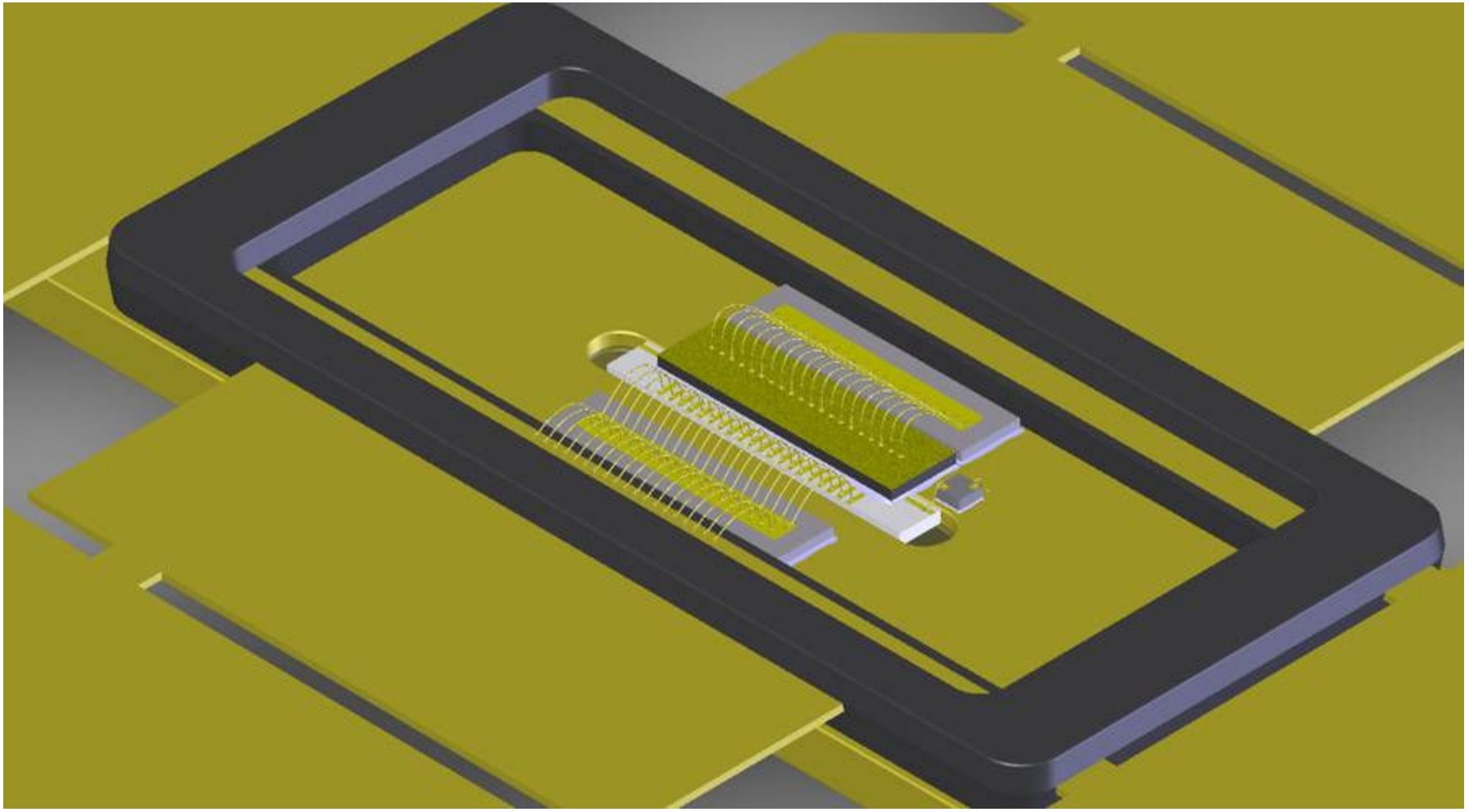
7 – Wirebond from Interposer to Input MOSCAP – 1mil Au wire



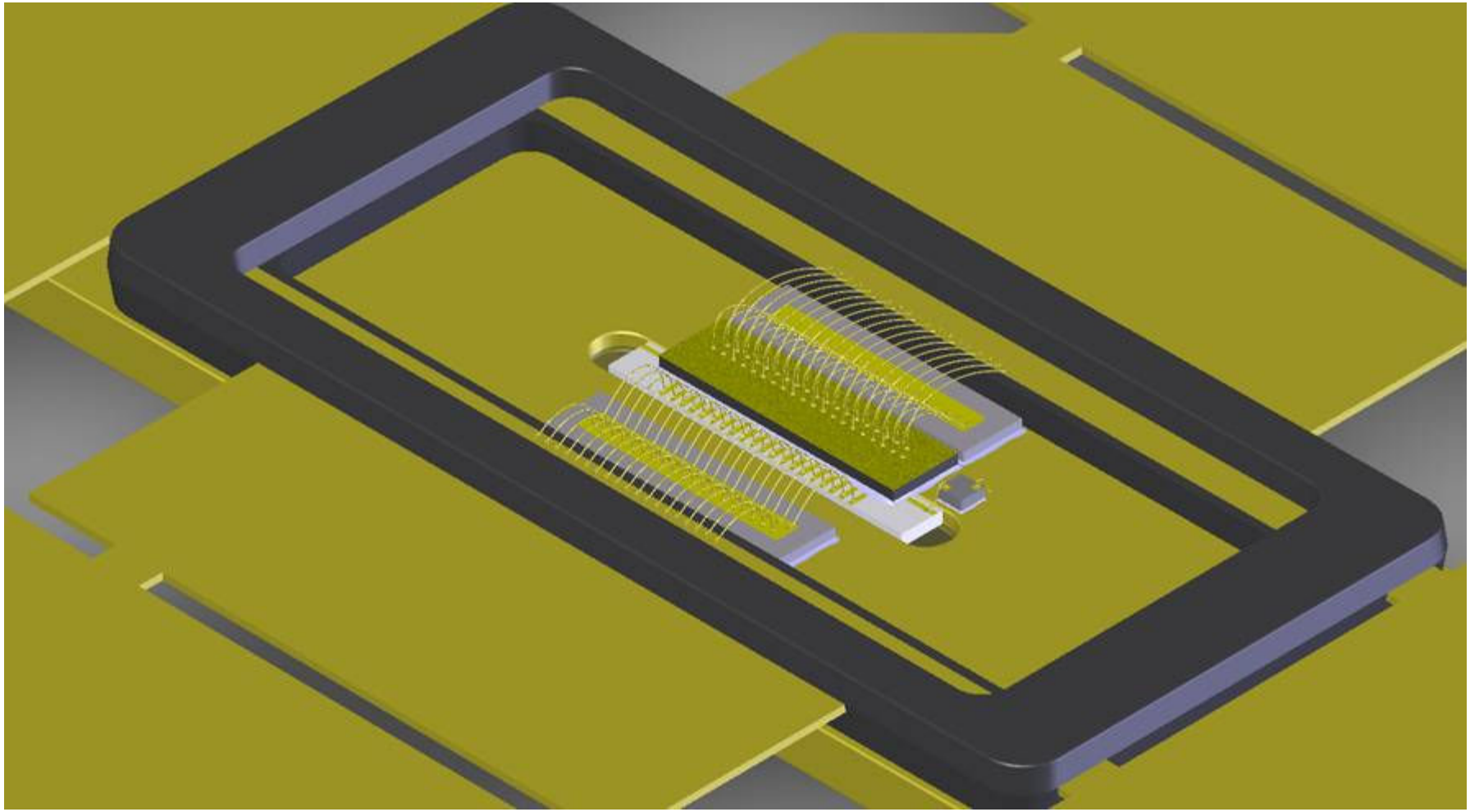
8 – Wirebond from Input MOSCAP to Input Lead – 1mil Au wire



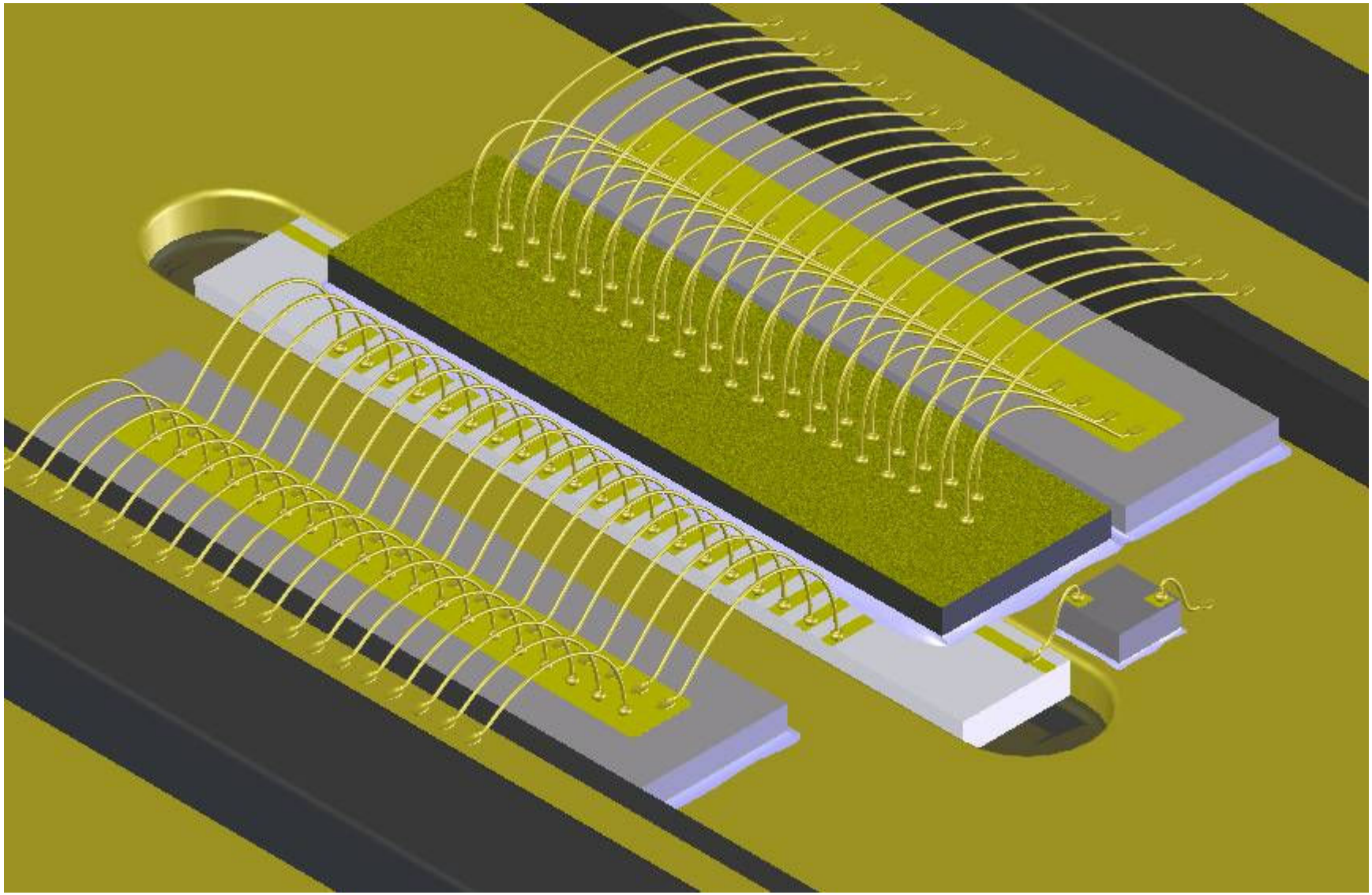
9 – Wirebond from DIE to Output MOSCAP – 1mil Au wire



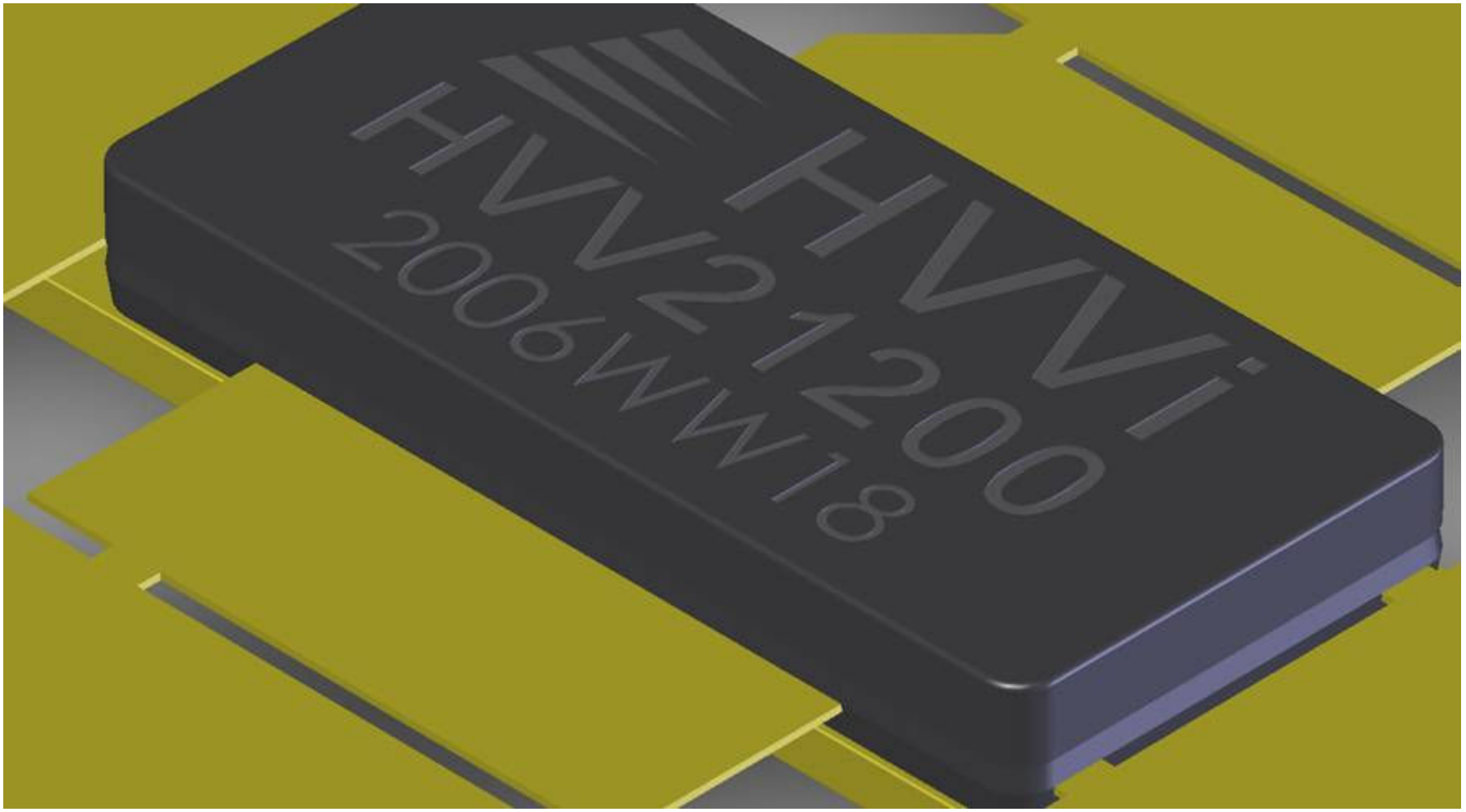
10 – Wirebond from DIE to Output Lead – 1mil Au wire



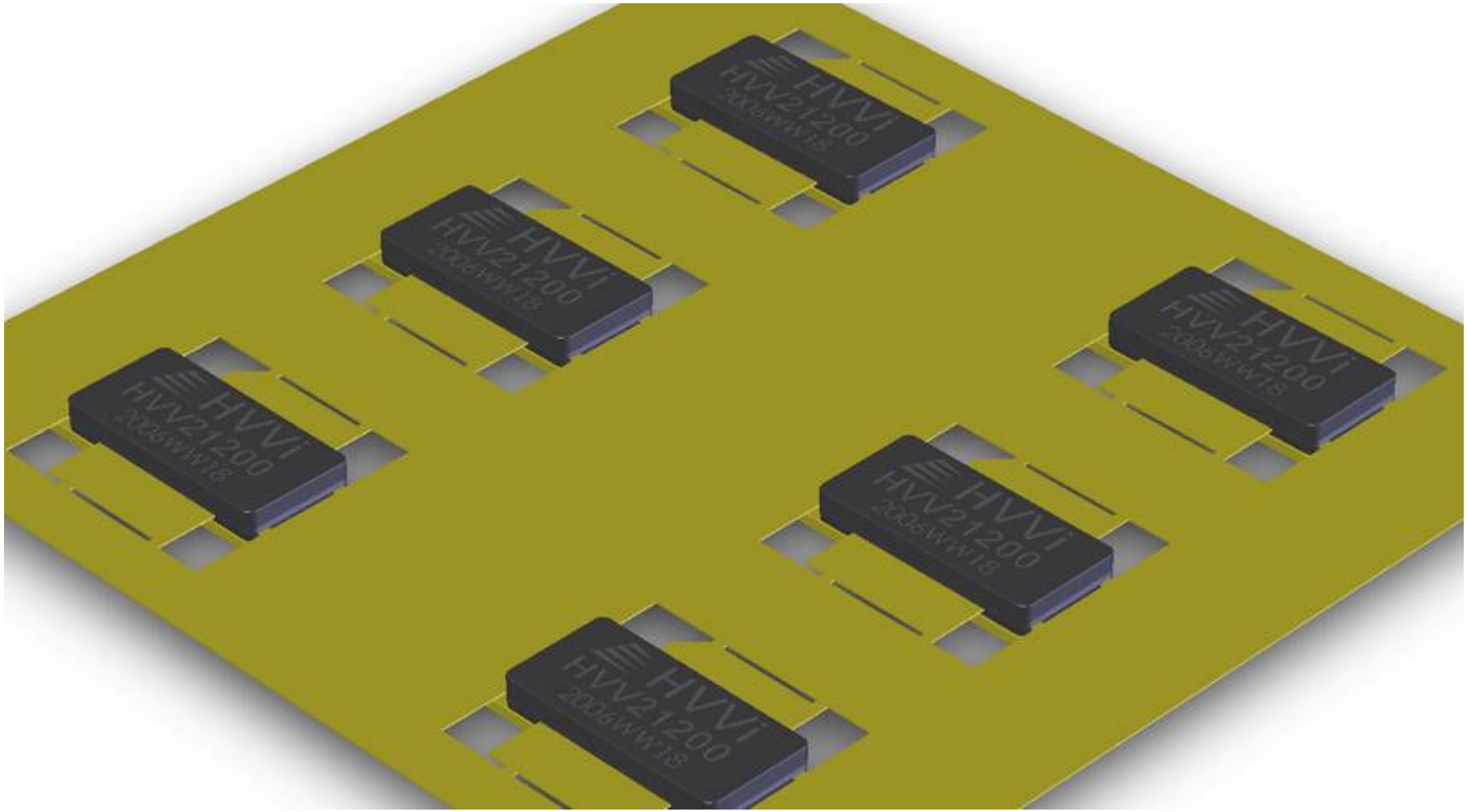
11 – Completed die and wirebond - closeup



12 – Attach Lid & Mark

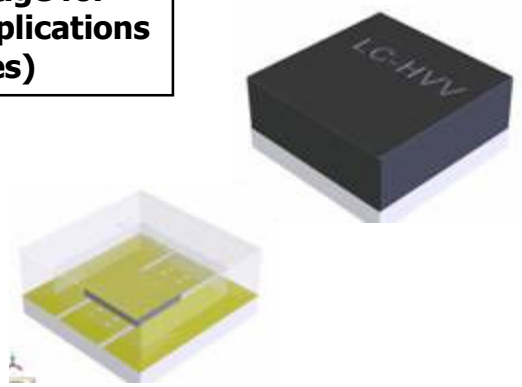


13 – Attach Lid & Mark - Array



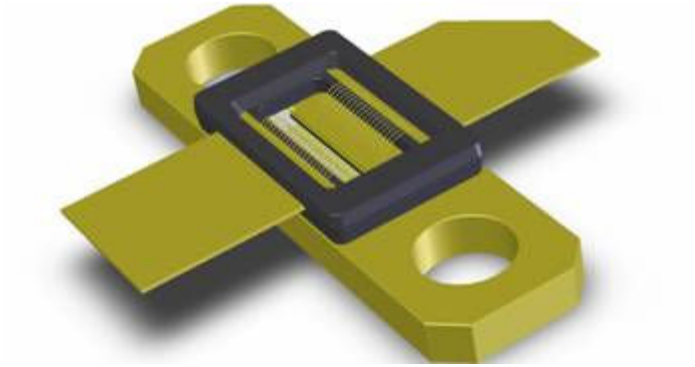
Package Types

Low cost AlN package for predriver & driver applications (all frequencies)

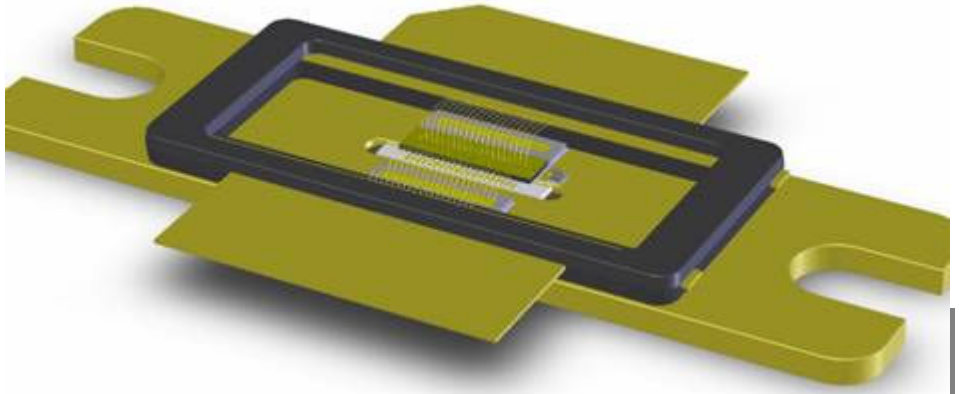


HVV planar package for high power, high frequency applications.

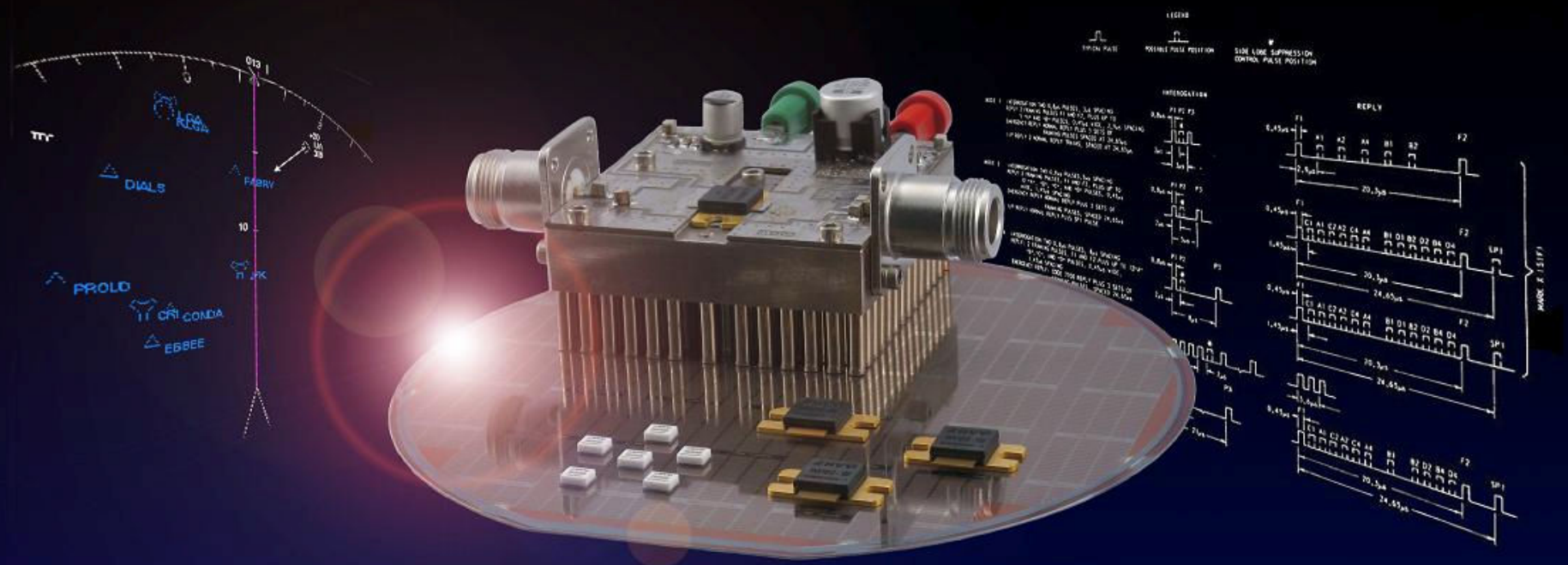
Un-matched



Matched



HVVFET Advantages



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High Voltage Advantages

ELECTRICAL CHARACTERISTICS

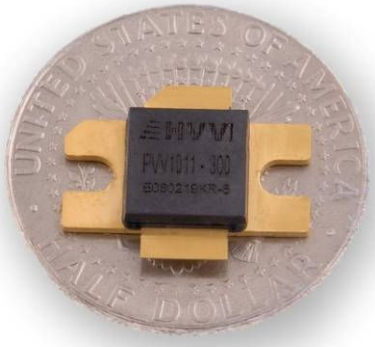
Symbol	Parameter	Conditions	Min	Typical	Max	Unit
$V_{BR(DSS)}$	Drain-Source Breakdown	VGS=0V,ID=5mA	95	102	-	V
I_{DSS}	Drain Leakage Current	VGS=0V,VDS=50V	-	50	200	μA
I_{GSS}	Gate Leakage Current	VGS=5V,VDS=0V	-	1	5	μA
G_P[1]	Power Gain	F=1090MHz	16	18	-	dB
IRL[1]	Input Return Loss	F=1090MHz	-	-12	-8	dB
η_D[1]	Drain Efficiency	F=1090MHz	43	45	-	%
VGS(Q)[2]	Gate Quiescent Voltage	VDD=50V,IDQ=100mA	1.1	1.45	1.8	V
VTH	Threshold Voltage	VDD=5V, ID=300μA	0.7	1.2	1.7	V

- High voltage solutions
  - Increases power density
  - Lower current improves reliability
  - Increased output impedance
- Single power supply
- Capable of operating at lower voltages (down to 24V) to provide flexibility to the customers.

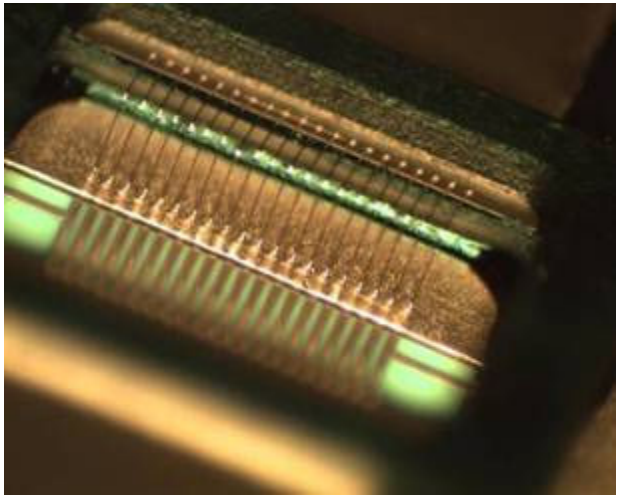
High Power Density = Smaller Packages

25W

300W

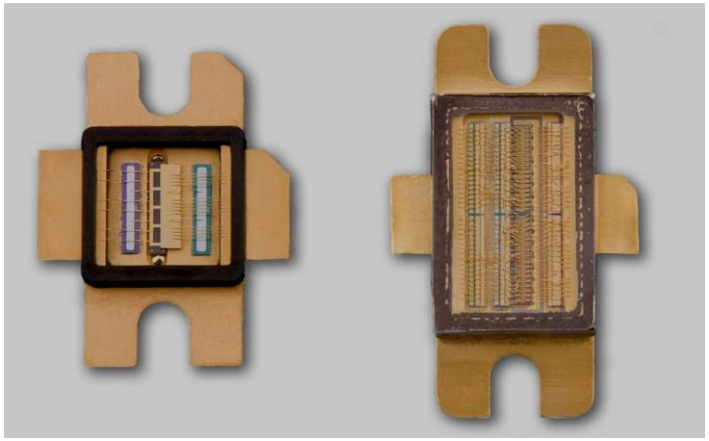


High Power in Small Packages



300W Comparison

HVVFET LDMOS

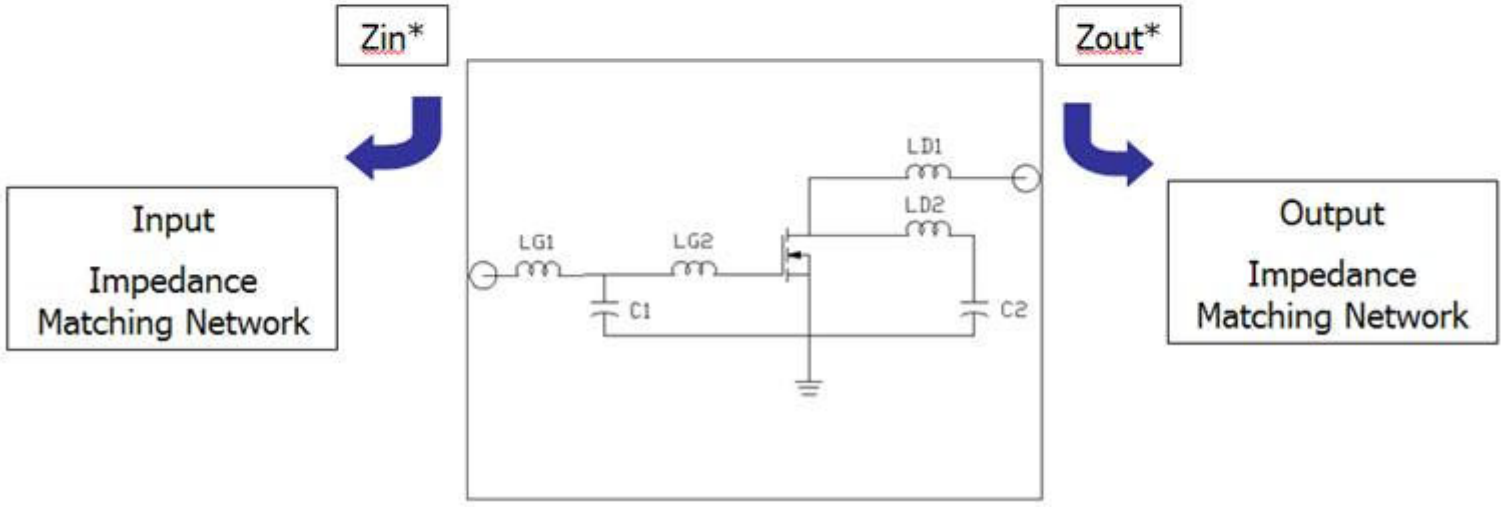


- HVVFET is ½ the size
- Simpler Device for Improved Reliability

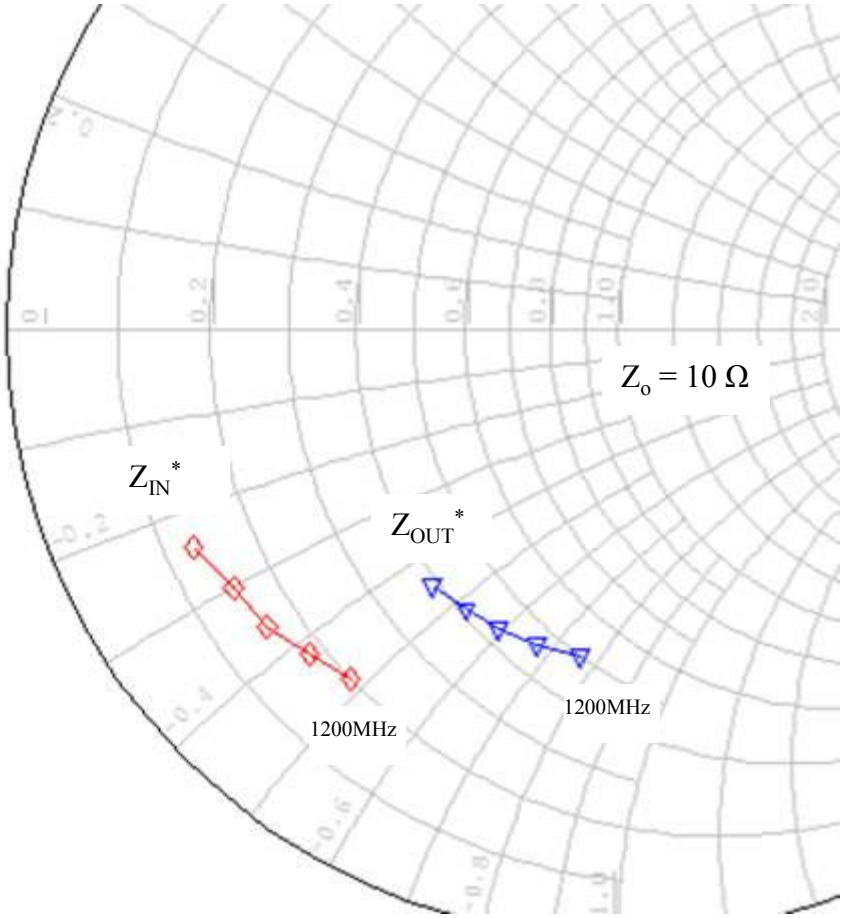
Internal Matching Networks
100W L-Band Radar Device

Test Circuit Impedance

Frequency	Zin*(ohms)	Zout*(ohms)
1200MHz	2.0-j4.8	5.0-j7.6
1250MHz	1.8-j4.2	4.6-j6.7
1300MHz	1.6-j3.6	4.3-j5.9
1350MHz	1.5-j3.0	4.1-j5.2
1400MHz	1.3-j2.4	3.9-j4.5

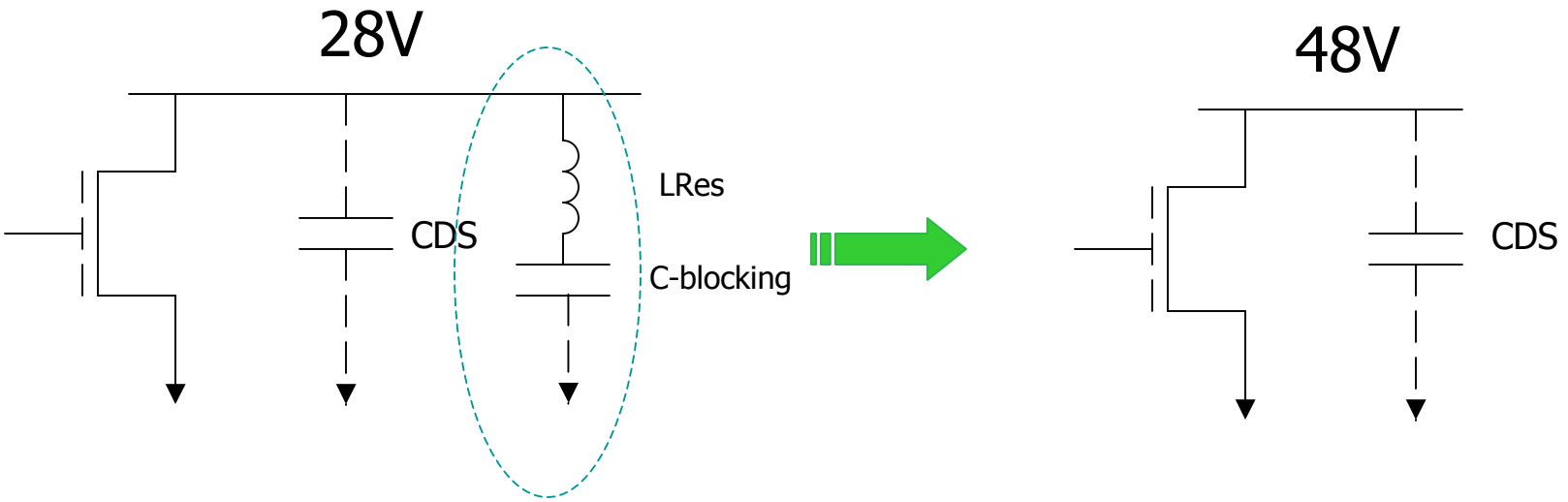


Impedance Data
100W L-Band Radar Device



Design Flexibility

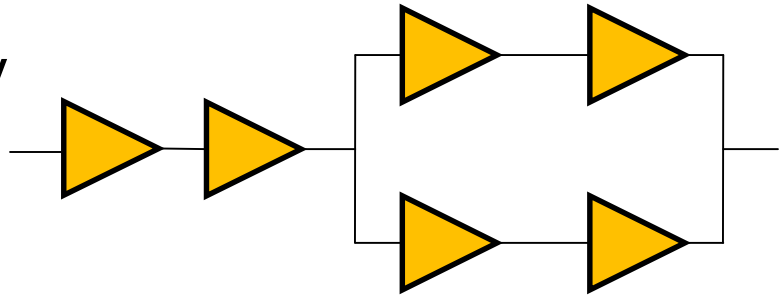
- Higher Zout→ Eliminate output Shunt Blocking Cap
- Flexibility to do external harmonic terminations
- Improve Doherty Amplifier performance



HVVFET vs Bipolar Solutions

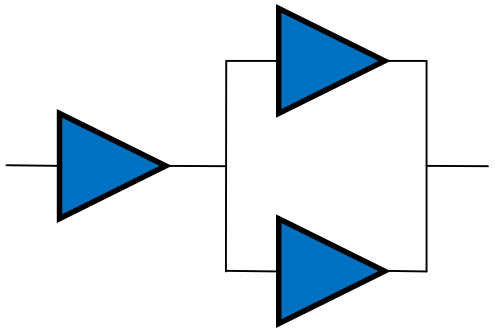
Lower System Costs with High Gain & High Power Density

- Higher gain reduces number of stages
- High power density packages reduces the PCB area
- Lower number of passive components
- Single 48V Supply line-up
  - Higher output impedance



0912-7	0912-25	MDS170L	MDS350L
8.5dB, 25%	8.5dB, 45%	7dB, 35%	8dB, 47%
Bipolar	Bipolar	Bipolar	Bipolar

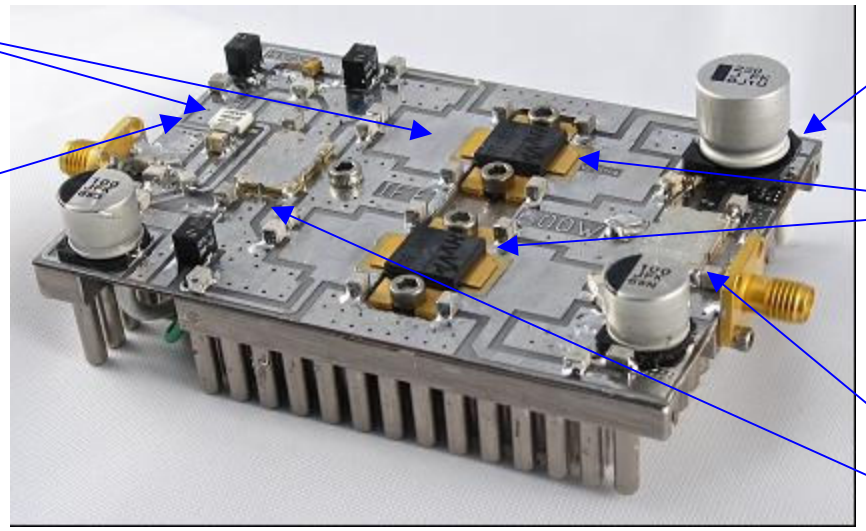
Four stage Bipolar Lineup



HVV1011-035	HVV1011-300
19dB, 48%	16dB, 48%
HVVFET	HVVFET

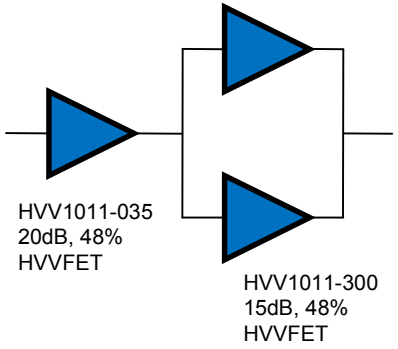
Two stage HVVFET Lineup

Design Example: 600W Live Demo @ MTT-S

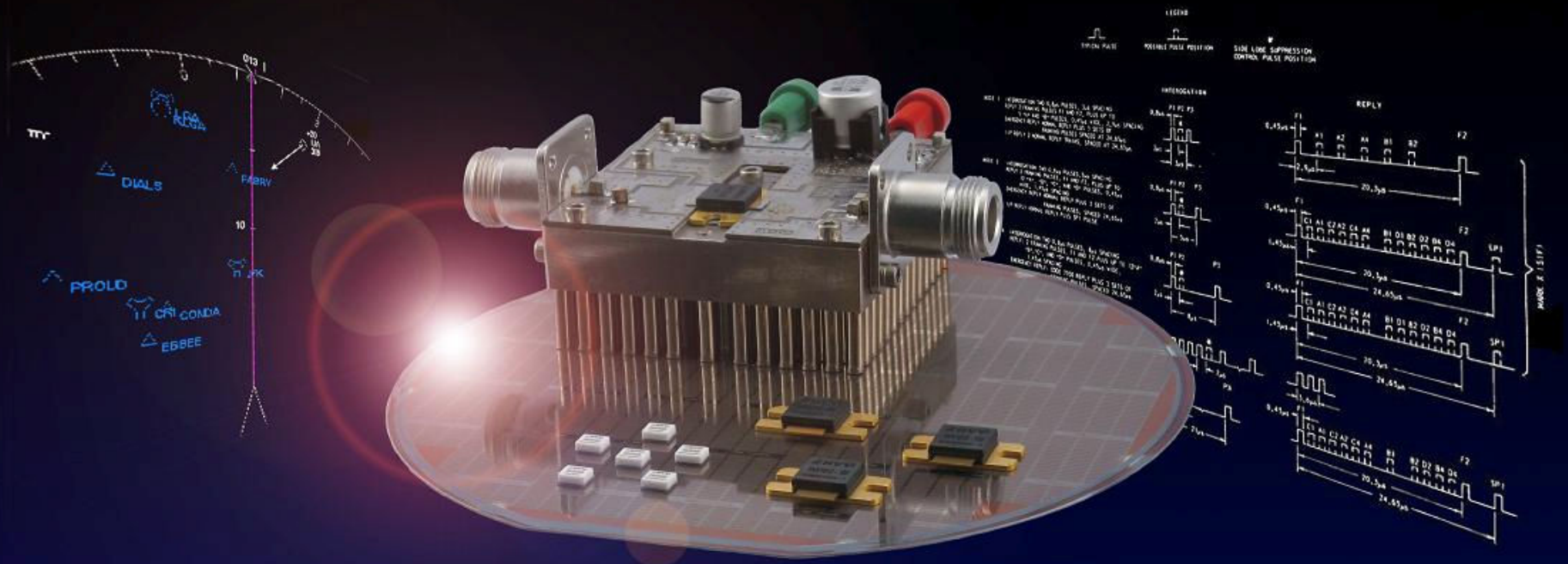


PCB footprint of 2.5” X 3.5” with low cost material (er =2.55)

Parameter	Value	Unit
Frequency	1090	MHz
Output Power	600	Watts
Gain	34	dB
Efficiency	47	%



Transistor Performance



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HVVFET Model Performance

Good Agreement on DC IV Curves for small device (4W).

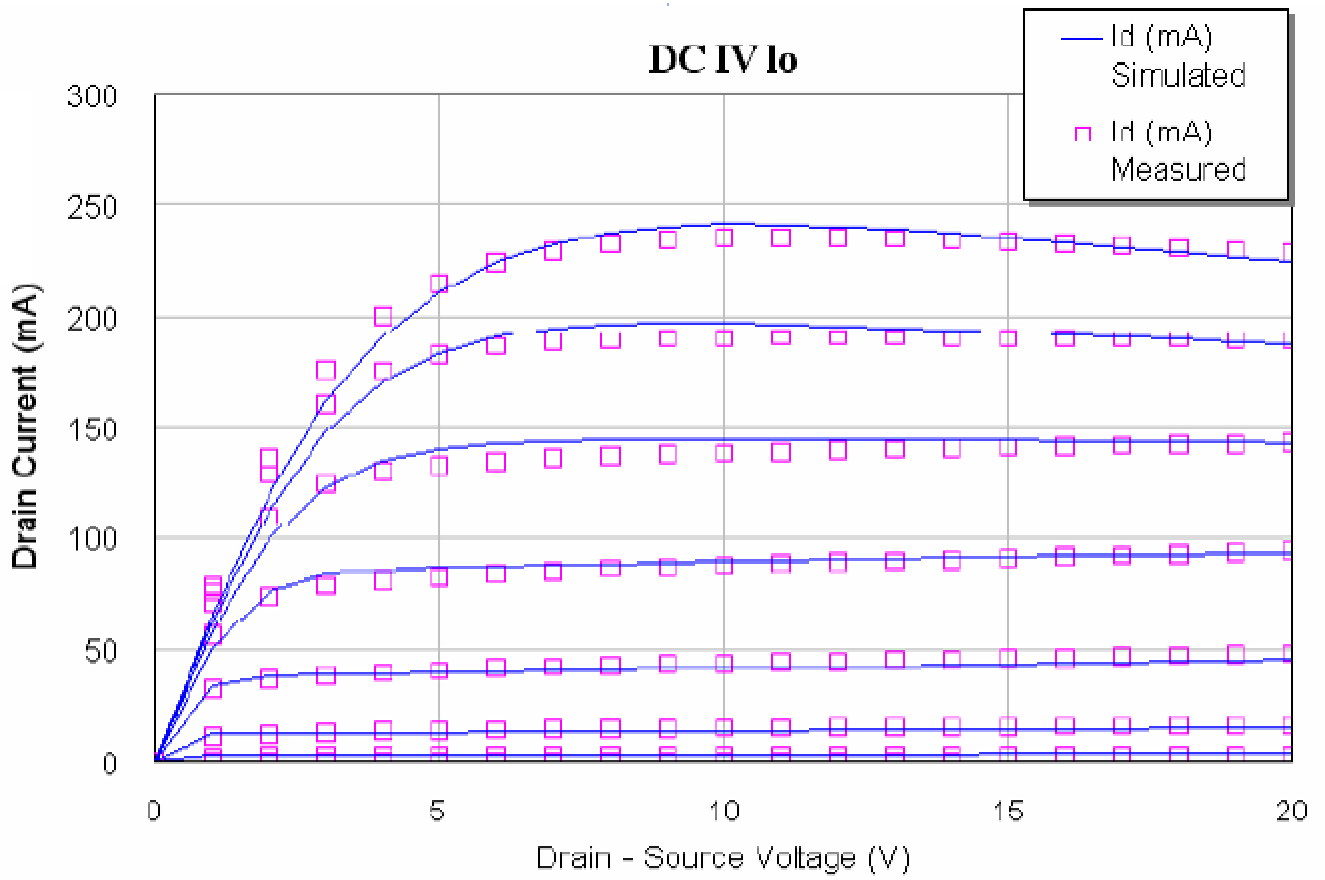
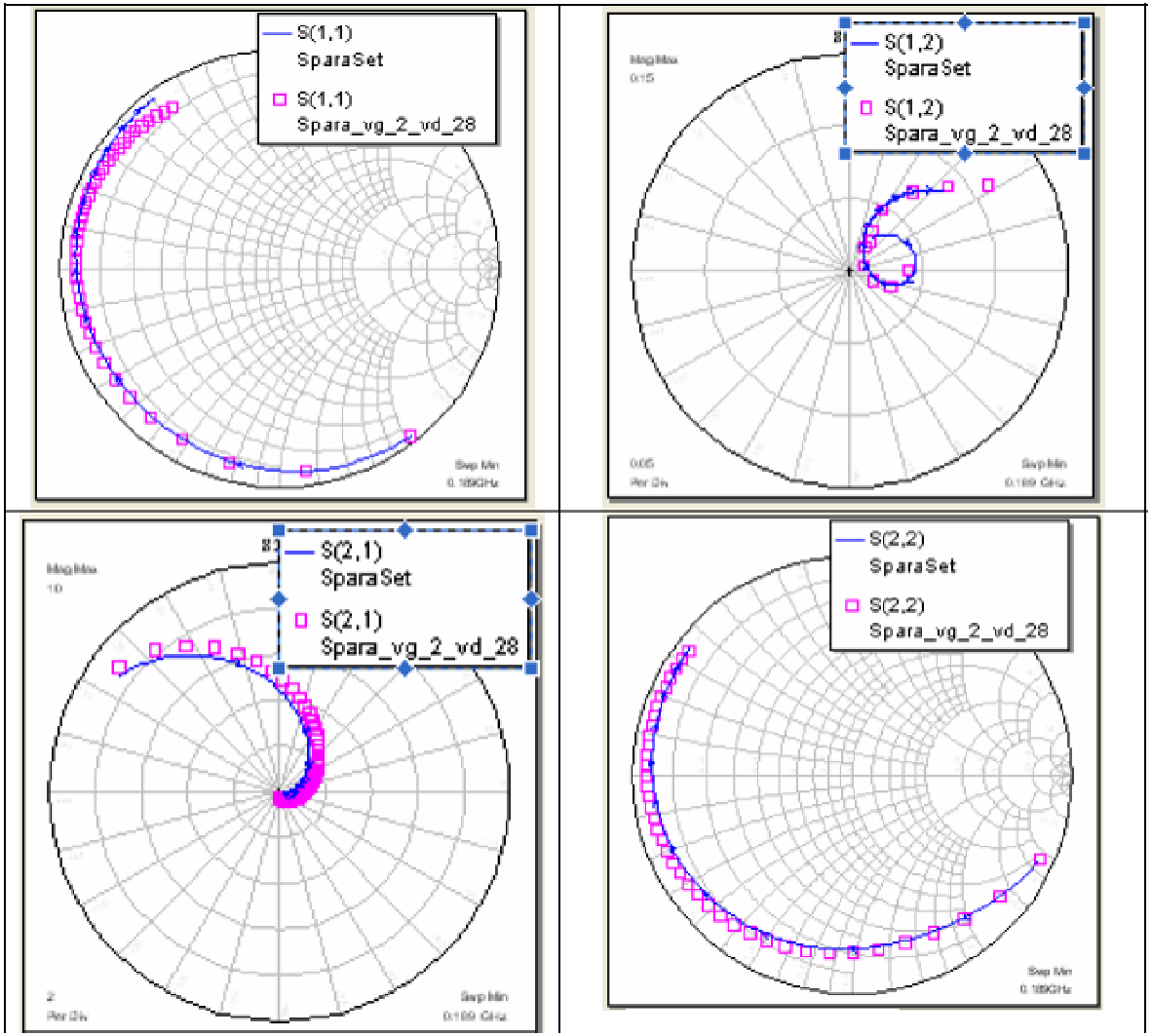


Figure 3 – Displayed is the static I-V comparison between the model (solid line) and measured data (symbol) for sample 1 of the 4W device. Vds = 0, 1, … 20V, Vgs = 1.4, 1.6, 3 V bottom up and Rth parameter = 20.

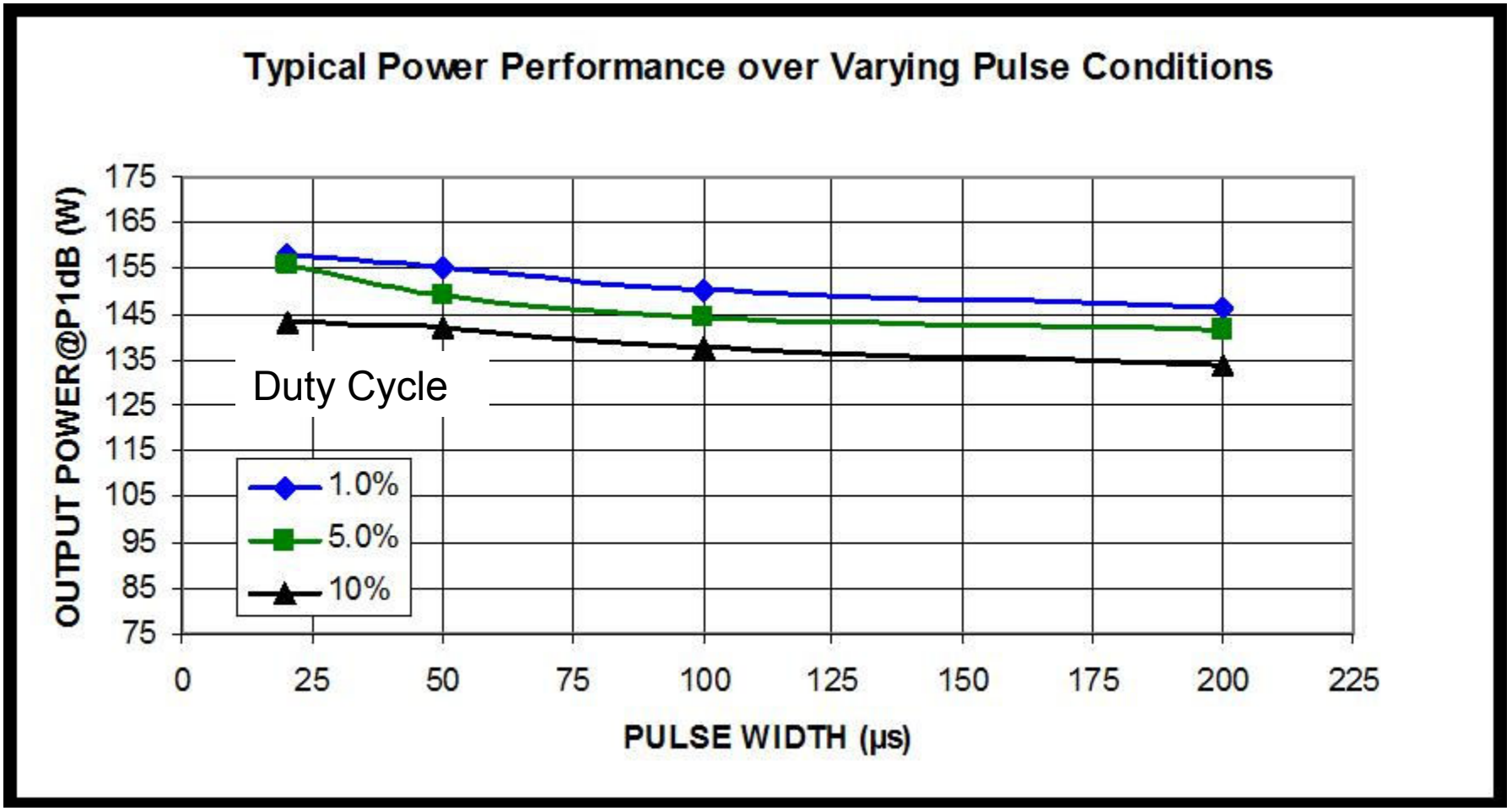
Modeling Efforts by Modelithics

HVVFET Model Performance



Modeling Efforts by Modelithics

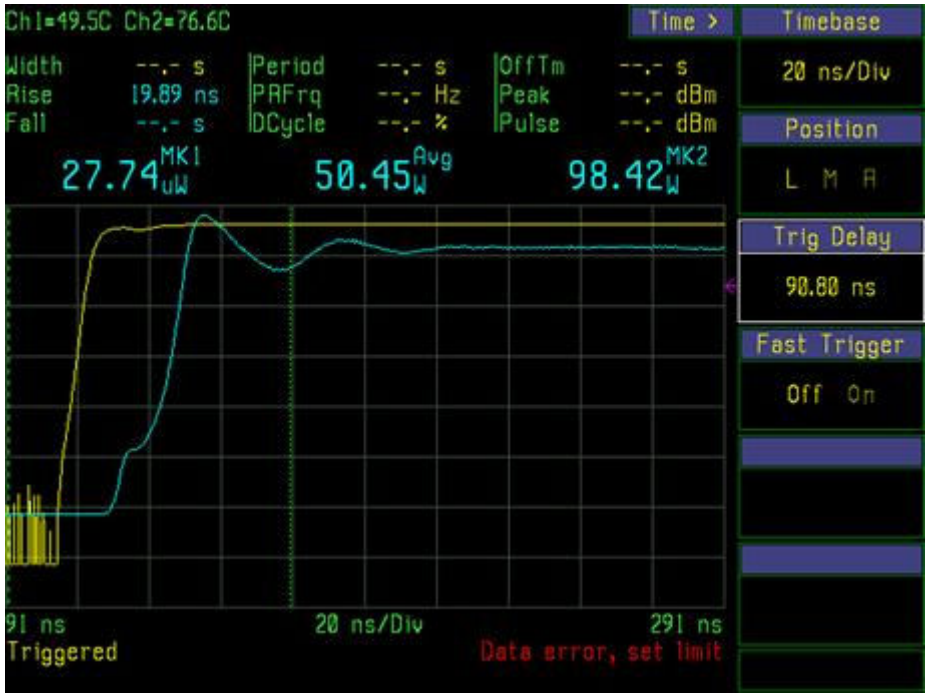
HVVFET Pulsed Performance

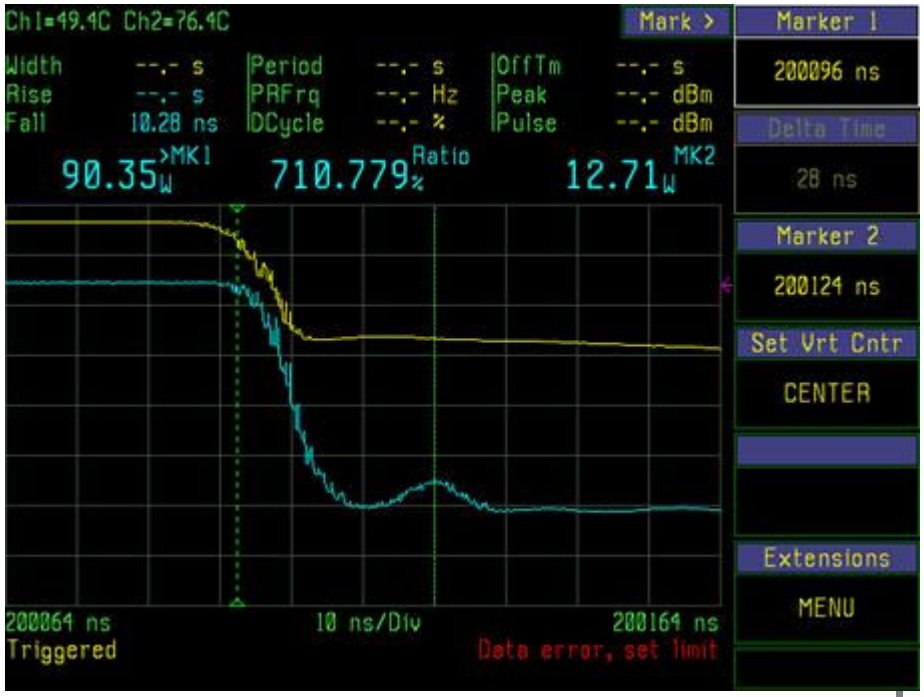


HVVFET Pulse Response

PULSE CHARACTERISTICS

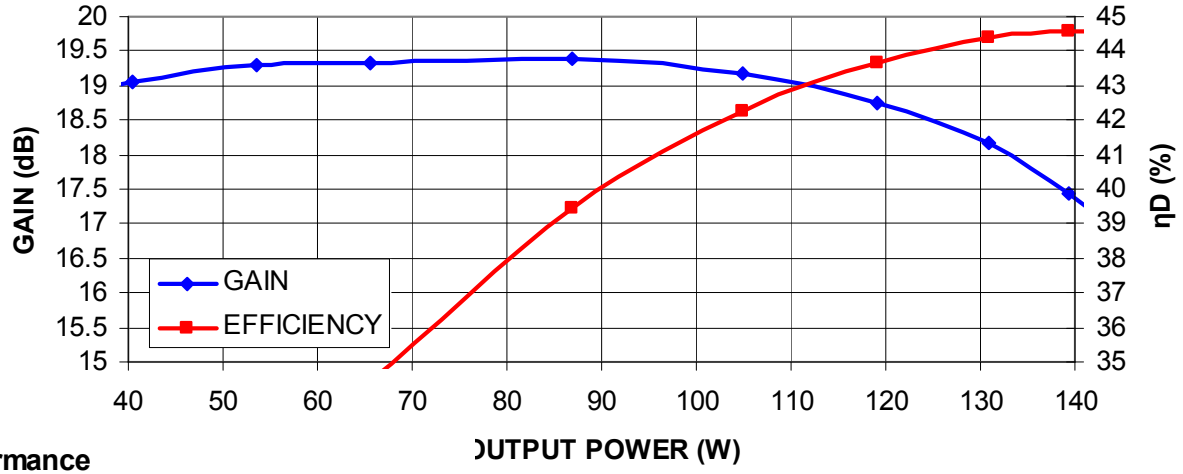
Symbol	Parameter	Conditions	Min	Typical	Max	Unit
T_r[1]	Rise Time	F=1090MHz	-	<35	50	nS
T_f[1]	Fall Time	F=1090MHz	-	<15	50	nS
PD[1]	Pulse Droop	F=1090MHz	-	0.3	0.5	dB



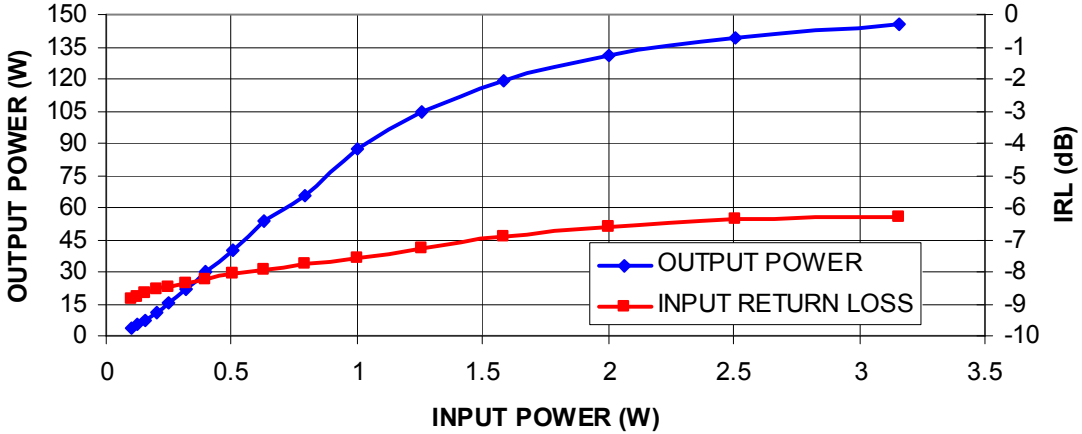


Power Swept Performance

Typical Power Performance
in a Broadband Matched Circuit

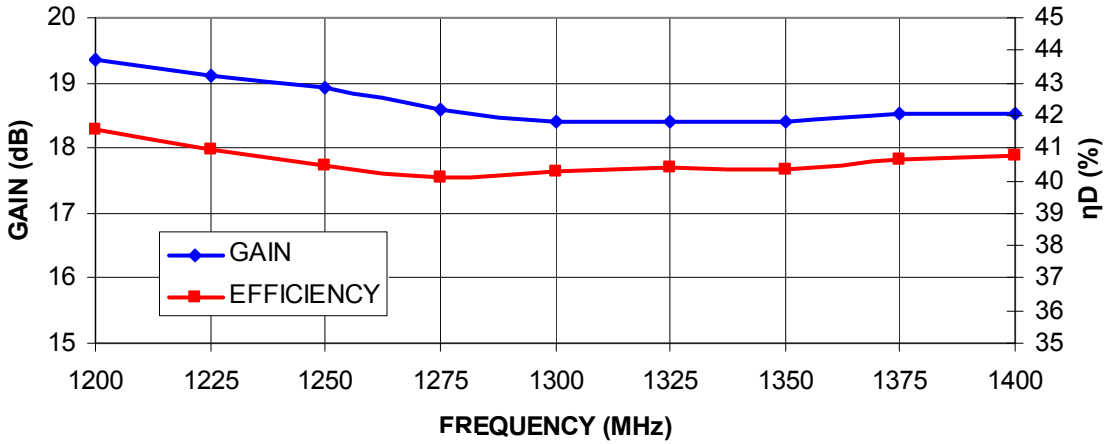


Typical Power Performance
in a Broadband Matched Circuit

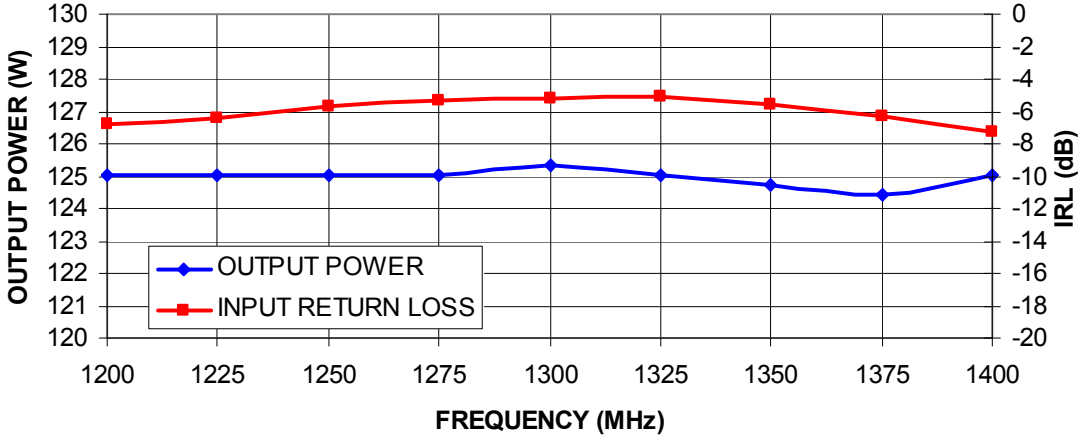


Frequency Response

Typical Frequency Performance in a Broadband Matched Circuit

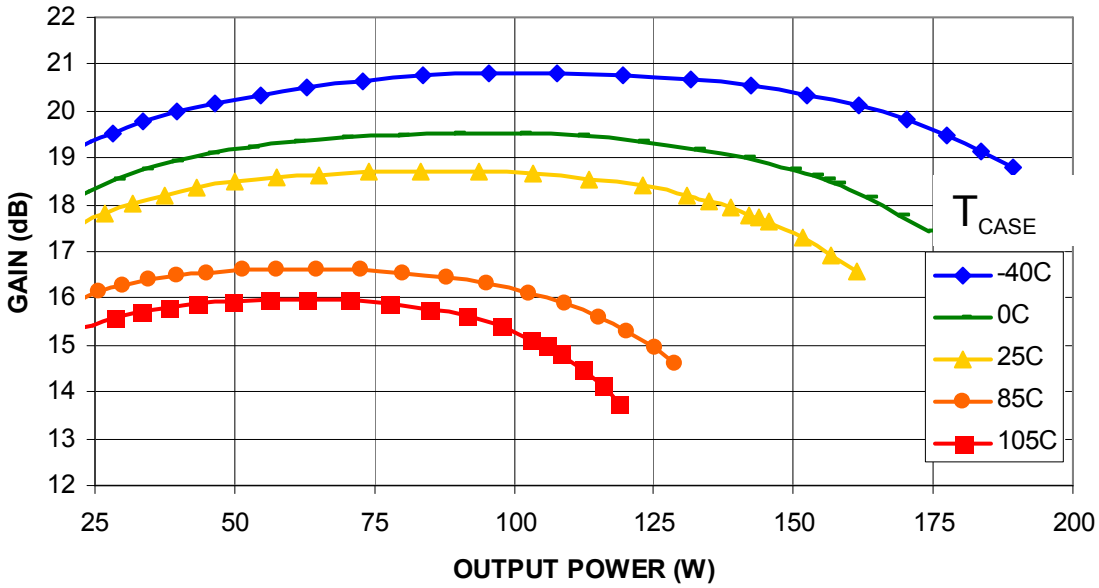


Typical Frequency Performance in a Broadband Matched Circuit



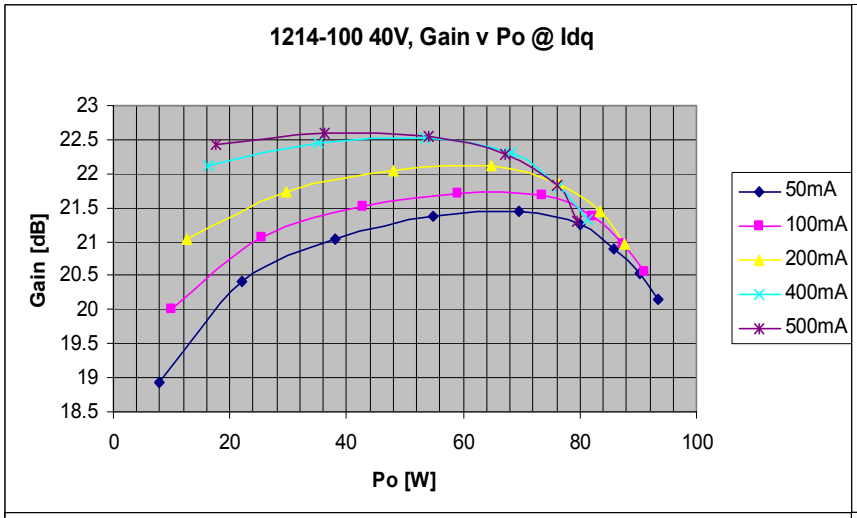
Temperature Response

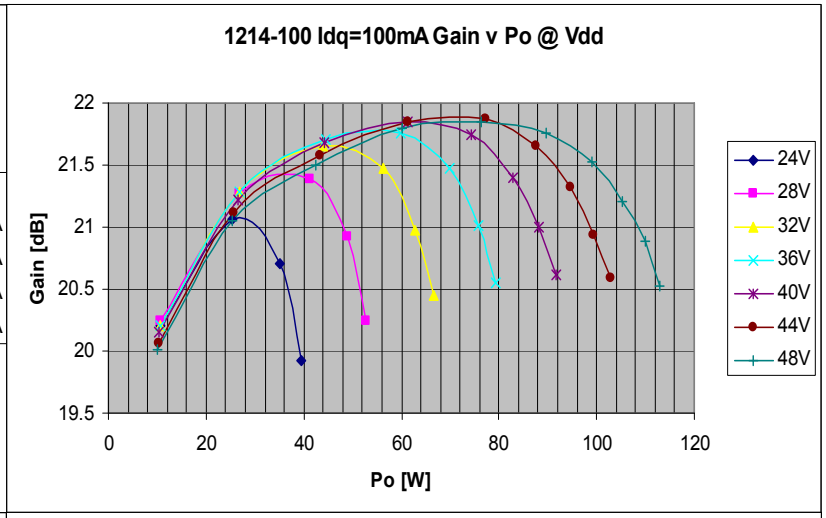
Vertical Technology Temperature Stability

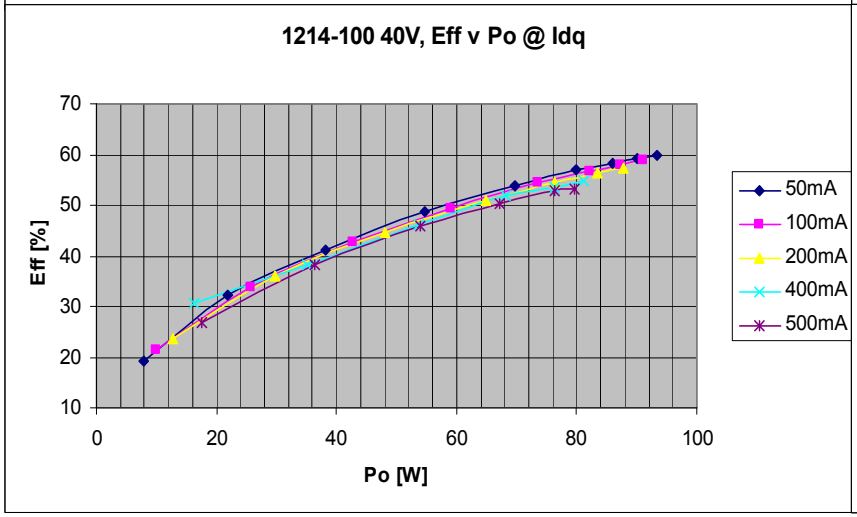


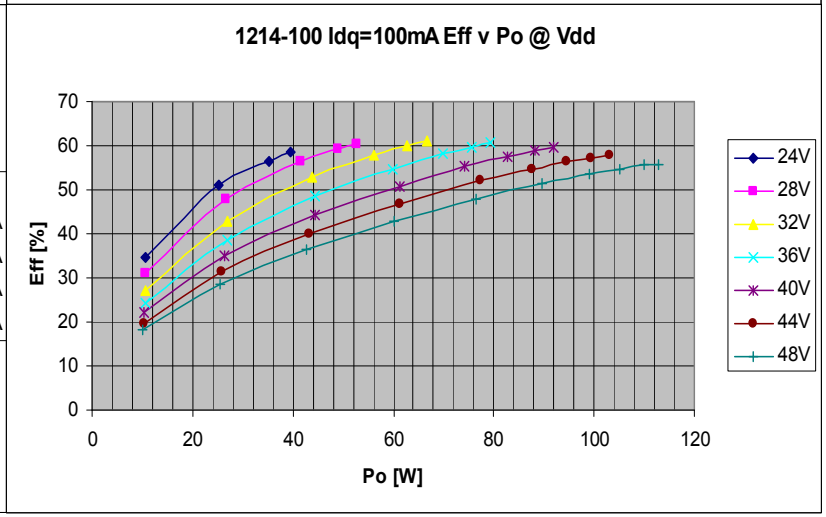
Measured at P1dB Compression Point			
TEMP	**Gain (dB)**	**Power (W)**	**Power (dBm)**
-40C	19.8	170	52.3
0C	18.5	155	51.9
25C	17.7	144	51.6
85C	15.6	115	50.6
105C	15	106	50.3

Bias Characterization







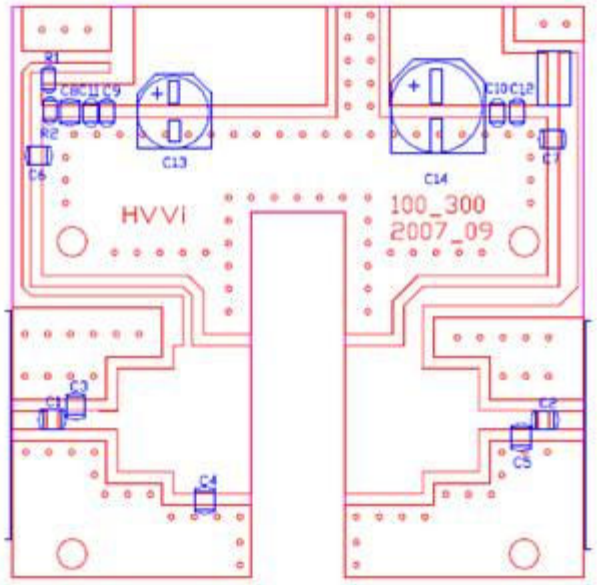


Demonstration Circuit Board (100W)

The innovative Semiconductor Company!

HVV1214-100 HIGH VOLTAGE, HIGH RUGGEDNESS

L-Band Radar Pulsed Power Transistor
1200-1400 MHz, 200µs Pulse, 10% Duty
For Ground Based Radar Applications



Demonstration Board Outline

Demonstration Circuit Board Picture

(AutoCAD Files for Demonstration Board available online at www.hvvi.com/products)

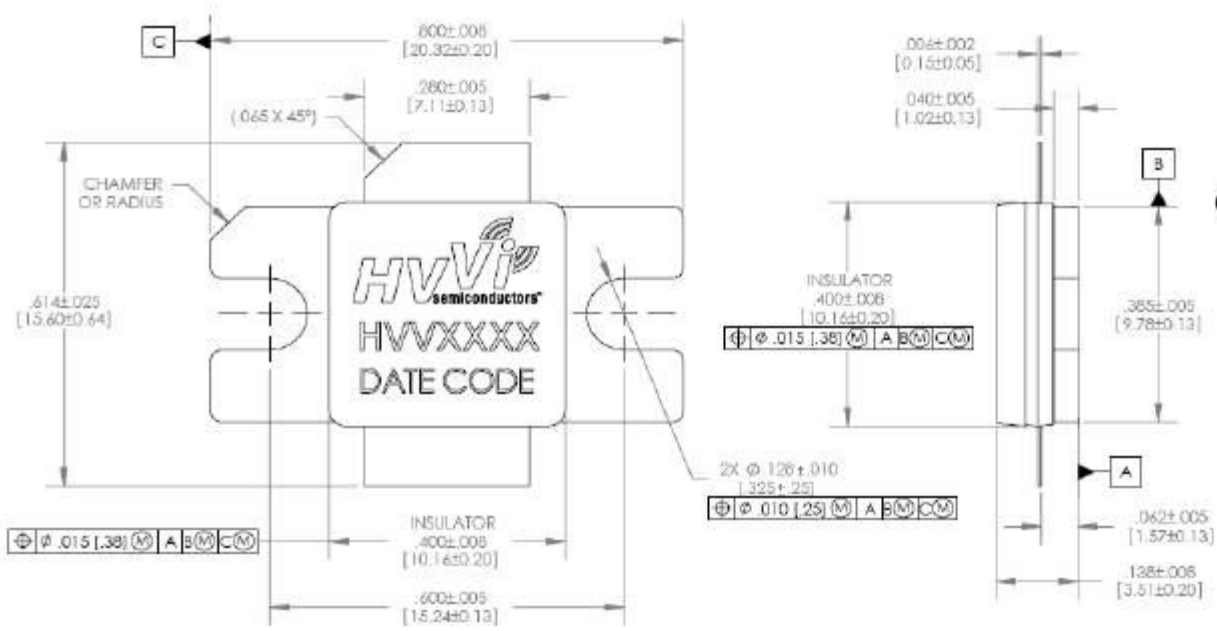
Mechanical Package Dimensions

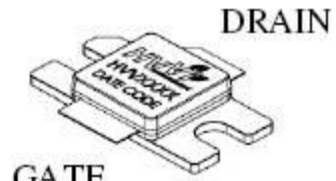
The innovative Semiconductor Company!

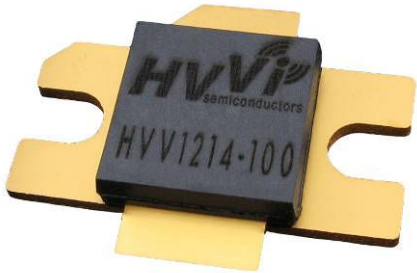
HVV1214-100 HIGH VOLTAGE, HIGH RUGGEDNESS

L-Band Radar Pulsed Power Transistor
1200-1400 MHz, 200µs Pulse, 10% Duty
For Ground Based Radar Applications

PACKAGE DIMENSIONS

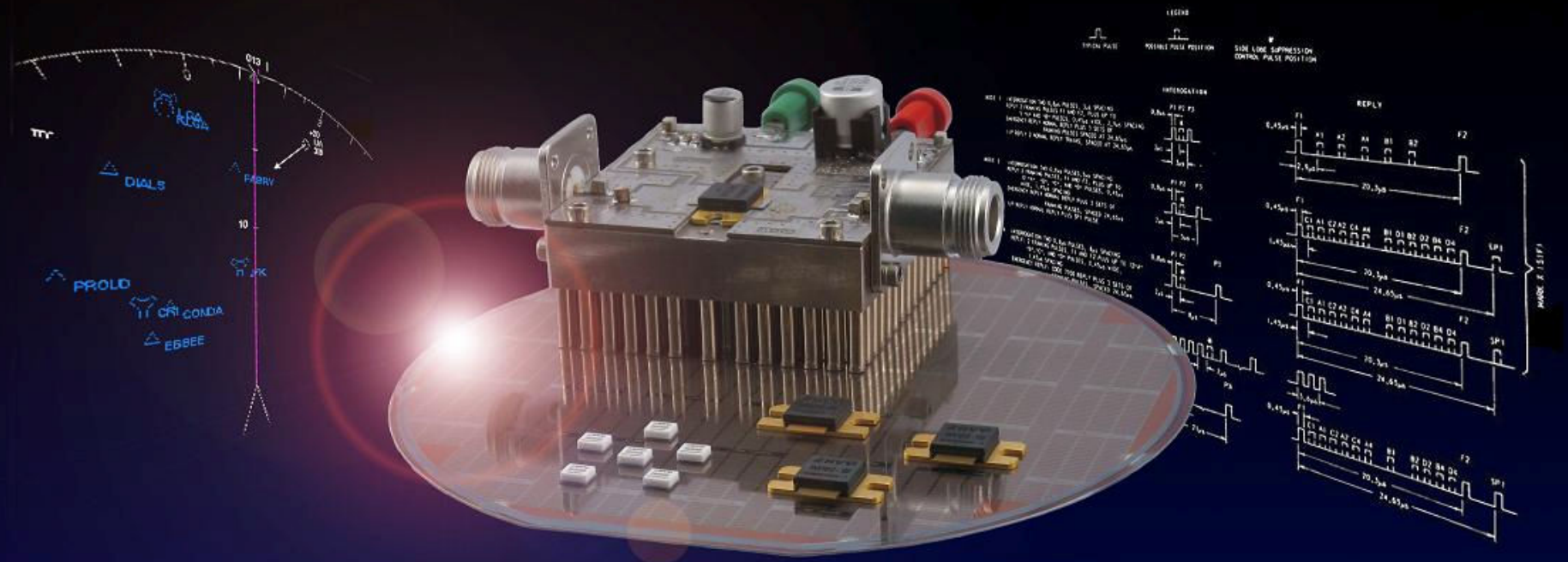






Note: Drawing is not actual size.

Reliability



Brian D. Battaglia

Applications Engineering

HVVi Semiconductors

Phoenix, AZ

Reliability Report

Qualification Tests and Results

The qualification tests were performed per standard test conditions (JEDEC, AEC-101, MIL-STD-883). Sample sizes were chosen per recommended sizes or per Lot Tolerance Percent Defective (LTPD) Sampling based on the Military Standards (5% level).

Table 3. A list of reliability tests completed for the HVV1011-300 qualification.

Stress	Abbv.	Ref.	Conditions	Duration/ Acceptance	Lot A	Lot B	Lot C
Electrical Parameter Assessment	ED	JESD86	Datasheet	Per datasheet	All	All	All
High Temperature Reverse Bias	HTRB	JESD22-A108, JESD85	80% of BVds (max)	1008 hr / 0 Fail	0/45	0/45	0/45
High Temperature Gate Bias	HTGB	JESD22-A108, JESD85	80% of BVgs (max)	1008 hr / 0 Fail	0/45	0/45	0/45
Temperature Cycling	TC	JESD22-A104	-40 °C to +125 °C	1000 cycles / 0 Fail	0/45	0/45	0/45
Temperature/Humidity (Unbiased)	UHAST	JESD22-A118	+130 °C, 85% RH	96 hours / 0 Fail	0/45	0/45	0/45
Thermal Resistance Measurements (Average & Pulsed)	θ_{JC}	JESD24-3	Under spec operating conditions	Characterize device	0/5	0/5	0/5
Solderability	SD	JESD22-B102E	Per std	0 Fail	0/15		
Resistance to Solder Heat	RSH	JESD22-B106C	Per std	0 Fail	0/30		
Variable Vibration Frequency	VVF	JESD22-B103	20 – 2000 Hz, Peak force = 20 g	4 min with 4 travels per axis / 0 fail	0/5		
Mechanical Shock	MS	JESD22-B104	Accel = 1500 g; Duration = 0.5 msec	5 times in both directions of 3 axis (6 directions total) / 0 Fail	0/5		
Constant Acceleration	CA	MIL-STD-833-2001	10000 g	Y1 Direction	0/6		

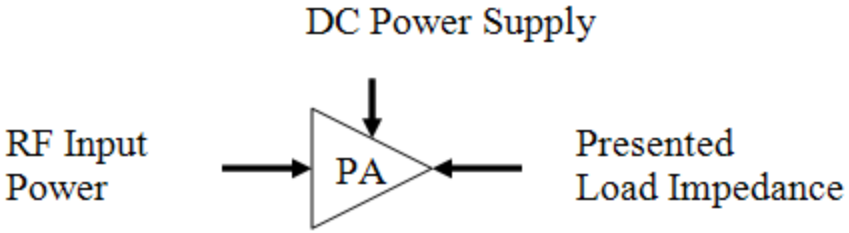
Why is Ruggedness Important?

RUGGEDNESS PERFORMANCE

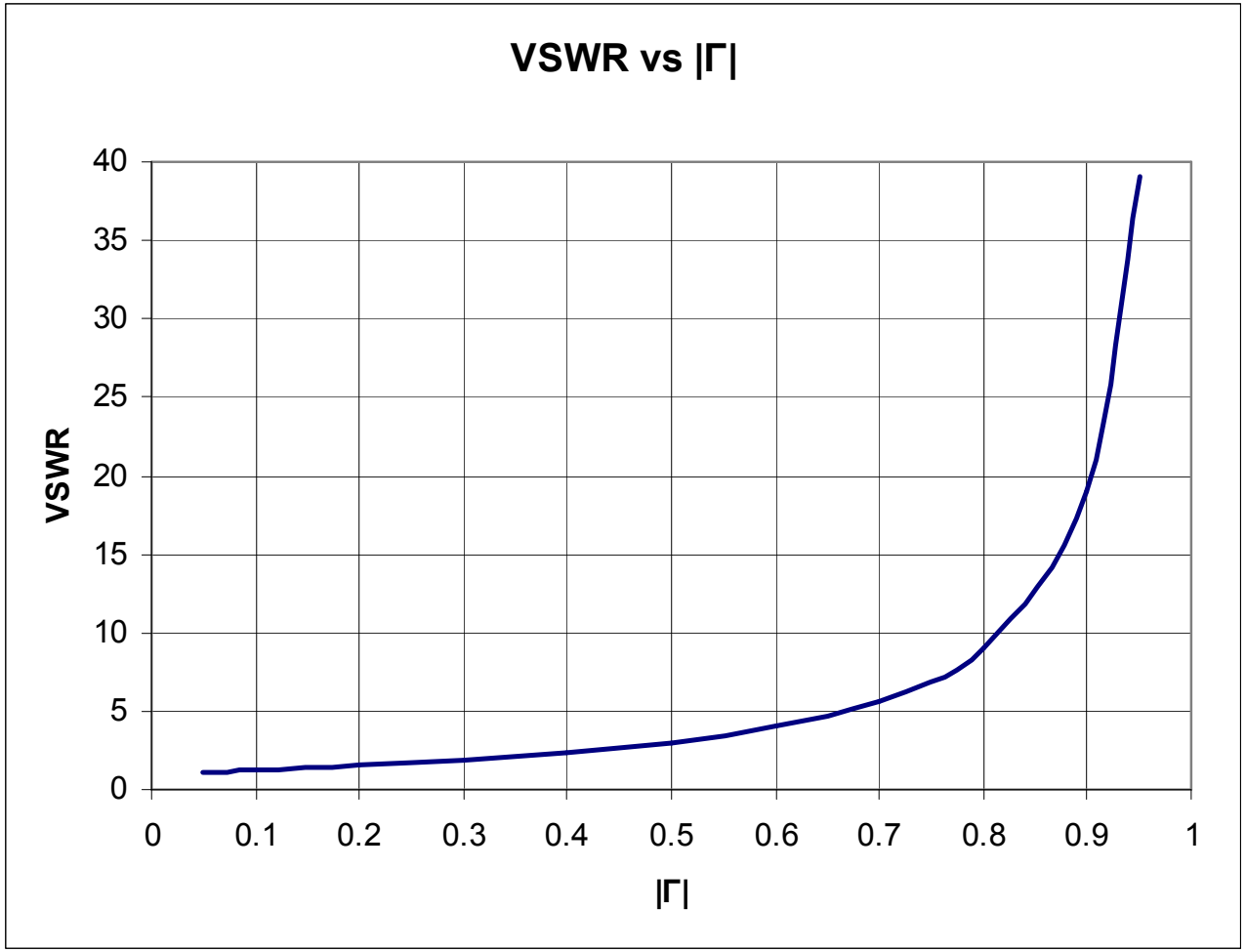
Symbol	Parameter	Test Condition	Max	Units
LMT[1]	Load Mismatch Tolerance	F = 1090 MHz	20:1	VSWR

The HVV1011-300 device is capable of withstanding an output load mismatch corresponding to a 20:1 VSWR at rated output power and nominal operating voltage across the frequency band of operation.

Parameters affecting power amplifier performance



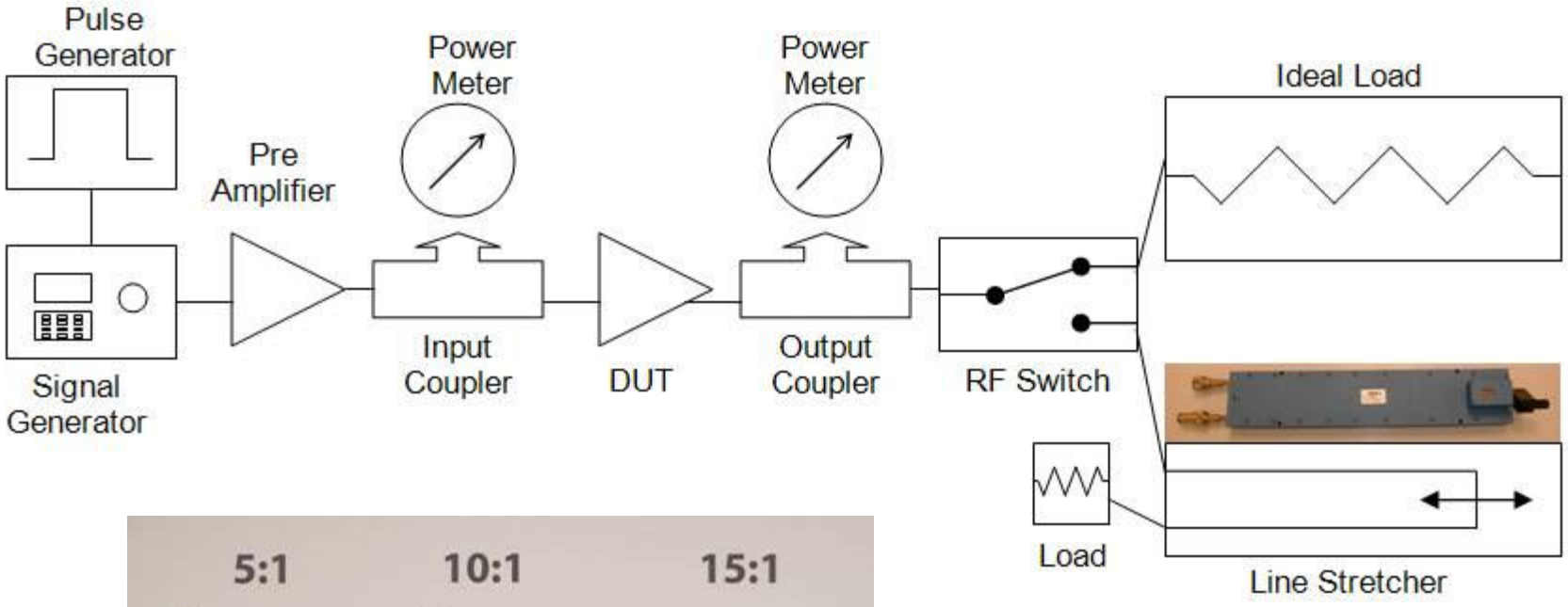
Output Load Termination

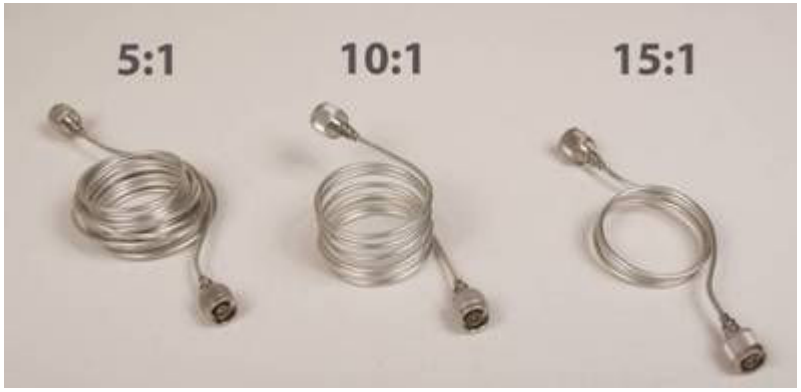


$$VSWR = \frac{1+|\Gamma|}{1-|\Gamma|}$$

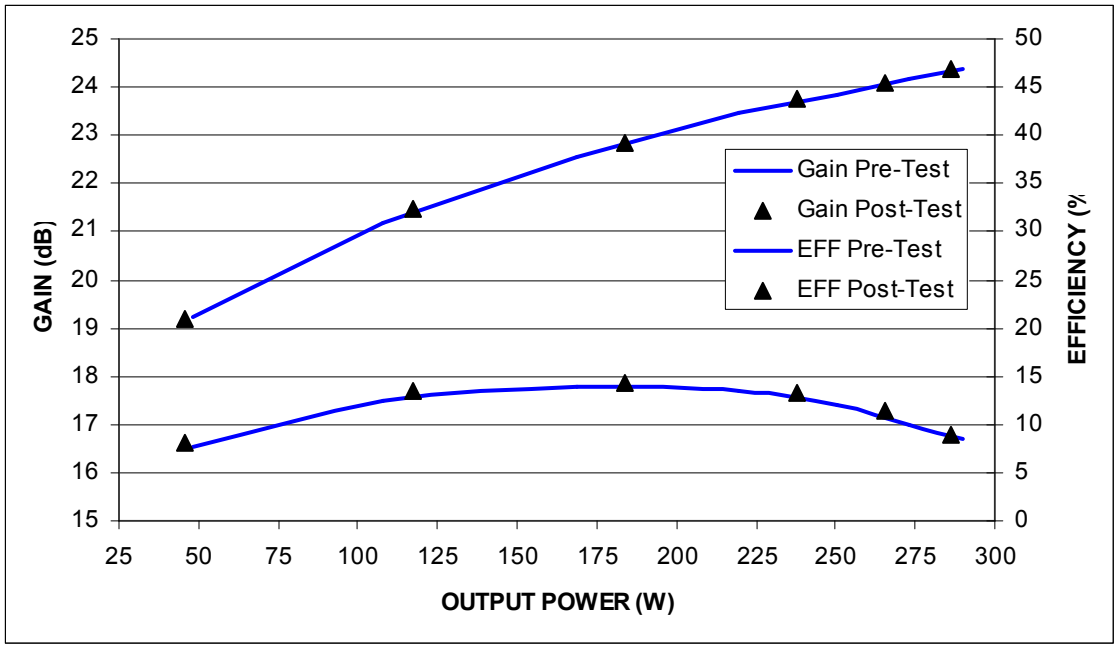
Typical RF Bench Ruggedness Test Set-up

RF Bench Diagram with load and line stretcher





Industry's Highest Ruggedness



Supply	VSWR	VSWR	VSWR
Voltage	5:1	10:1	20:1
VDD	Pass	Pass	Pass
VDD+10%	Pass	Pass	Pass

Table 1: Ruggedness results summary at rated output power.

Supply	VSWR	VSWR	VSWR
Voltage	5:1	10:1	20:1
VDD	Pass	Pass	Pass
VDD+10%	Pass	Pass	Pass

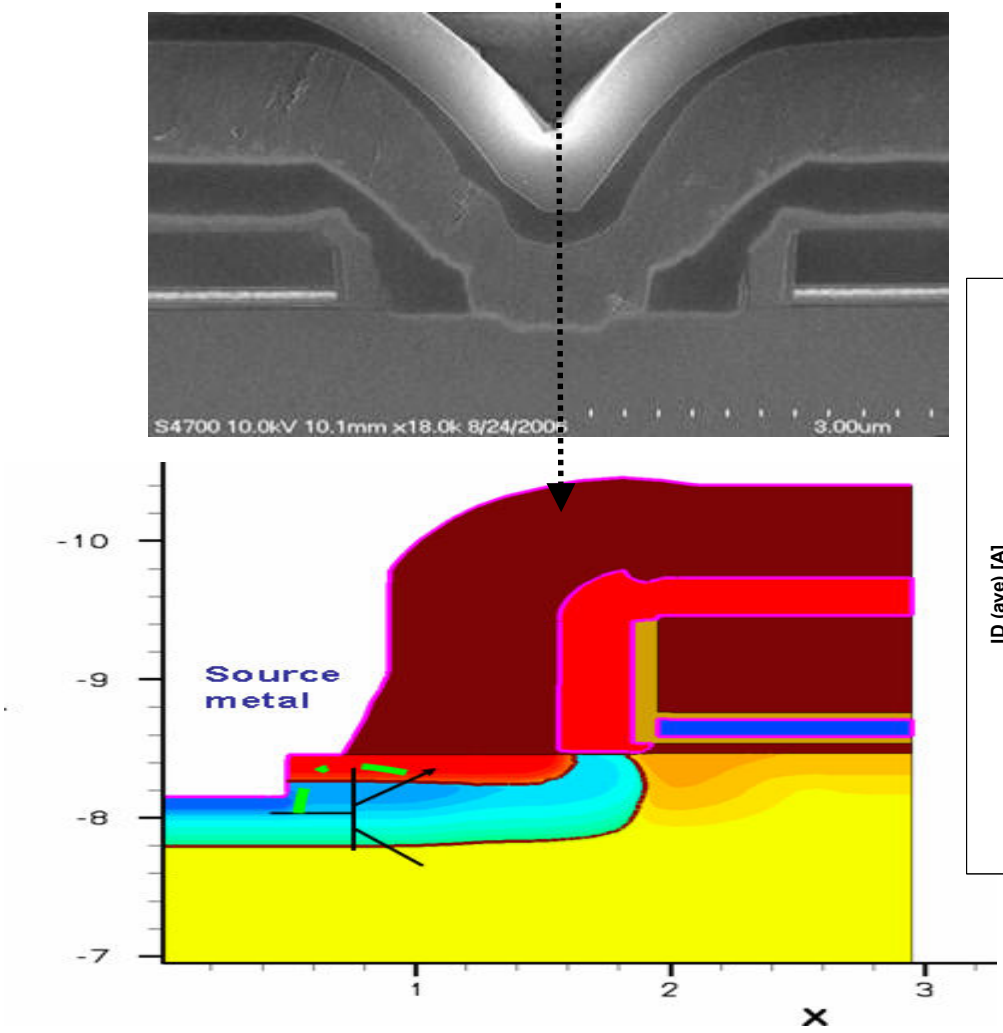
Table 2: Ruggedness results summary at 3dB overdrive.

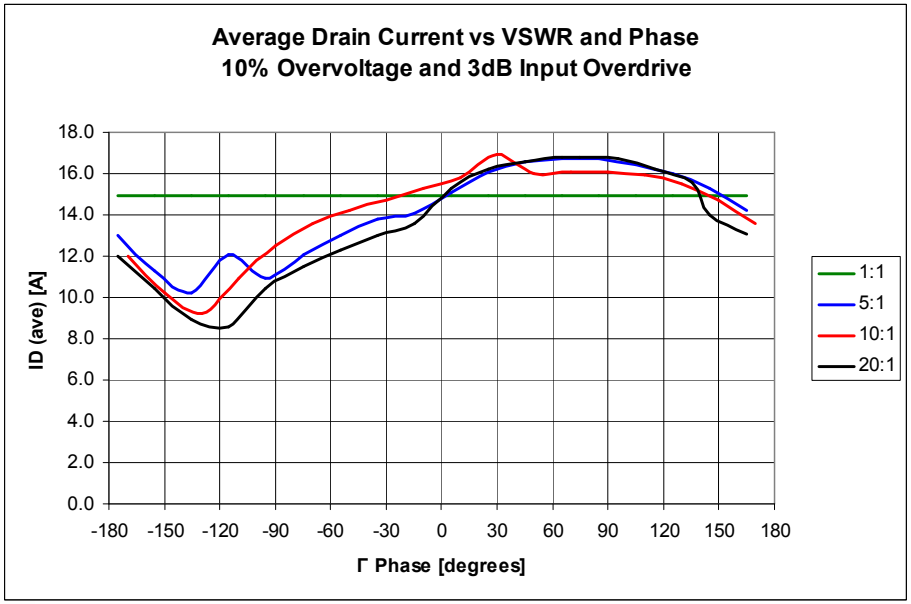
CONDITION	IDSS (µA)	BVDSS (Volts)	VTH (Volts)	RDSON (mOhm)	GM (S)
PRE-TEST	7.3	111.9	1.108	93.2	4.50
POST-TEST	7.3	112.6	1.113	93.3	4.56

Table 3: DC parameters before and after ruggedness test.

Thermal Path enhances device ruggedness

Cross Section Of A Transistor Cell





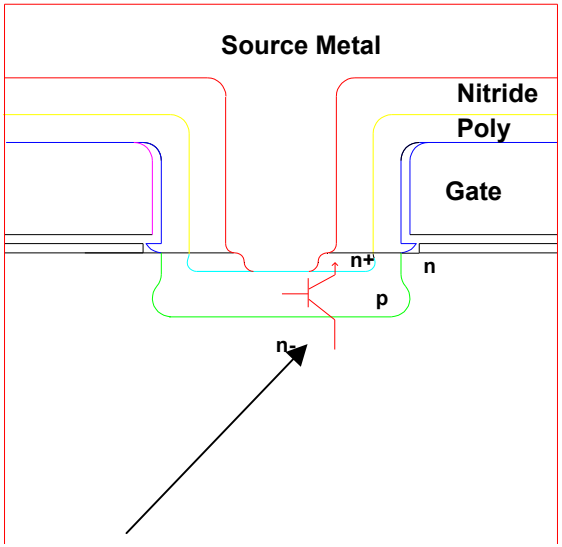
HVVFET vs LDMOS

- The HVVFET has proven to be extremely rugged and stable allowing the designer to have greater freedom in designing their power amplifier
- Eliminates the need of heavy isolators and circulators saving space and weight

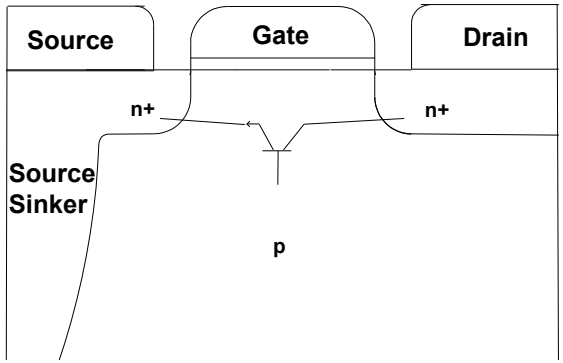
Why is the HVVFET so rugged?

Suppresses parasitic bipolar transistor present in all MOSFETs

HVV FET



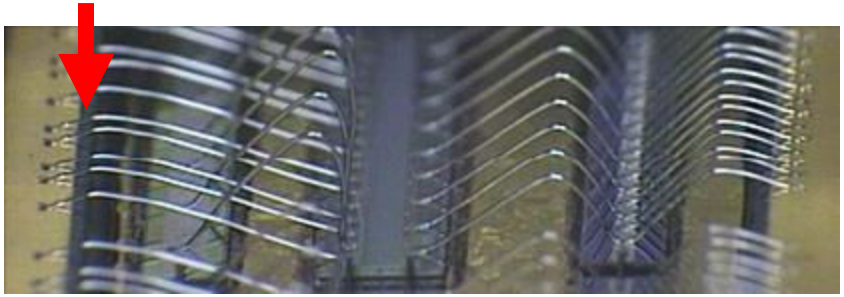
LDMOS



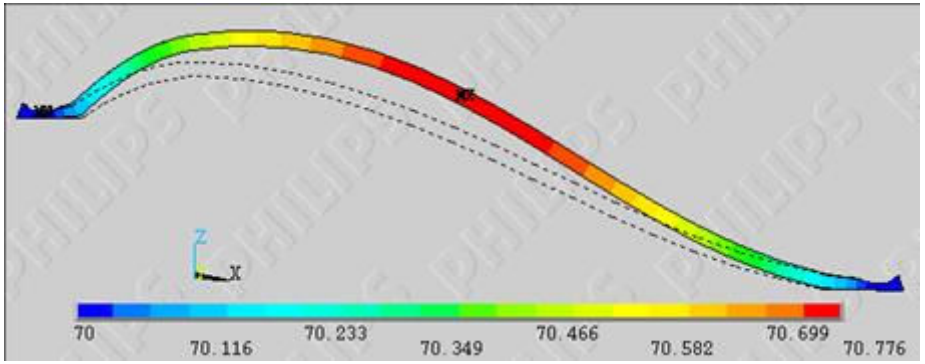
- Parasitic NPN transistor shorted with source metal
- Heat in parasitic NPN removed efficiently

Gold Bonds for Reliable Pulsed Applications

Lateral Device with Aluminum Wires

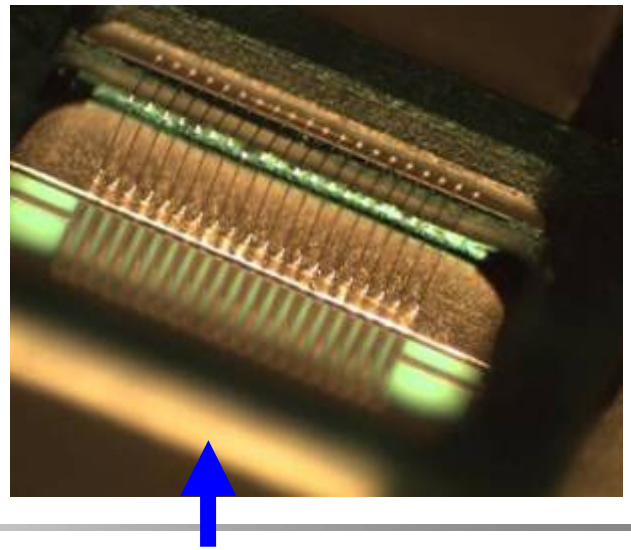


Example of an LDMOS product in air cavity package. Red arrow indicates the critical wire loop shapes that may be susceptible to power-cycling induced high-cycle fatigue.



Joule heating will cause the bond wires to expand and contract in a cyclical manner, leading to mechanical fatigue

- HVVi RF pulse testing to ensure consistent operation under stringent conditions
  - HVV1011-300 device pulsed over 1 Billion times per month



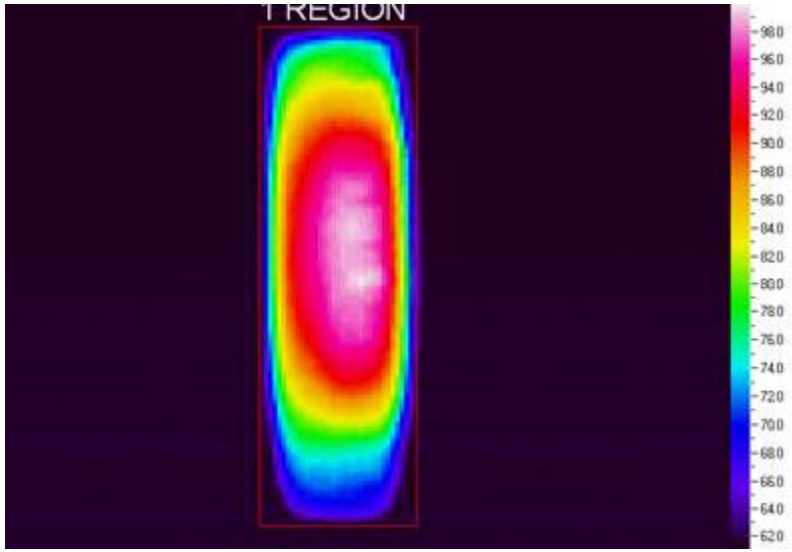
HVVFET Device with Gold Wires

Thermal Measurement Techniques

- Several methods for measuring Rth (jc) or Rth (ja)
  - IR Camera
  - Delta Id
  - Delta Vf
- Measurements
  - Rth(ja)
    - Thermal resistance junction to air is the only measurement that customers are interested in.

Traditional Thermal Measurements

IR Scan of HVVFET



Costly equipment set – Thermal Camera and Liquid Nitrogen

Vertical Device Thermal Measurements

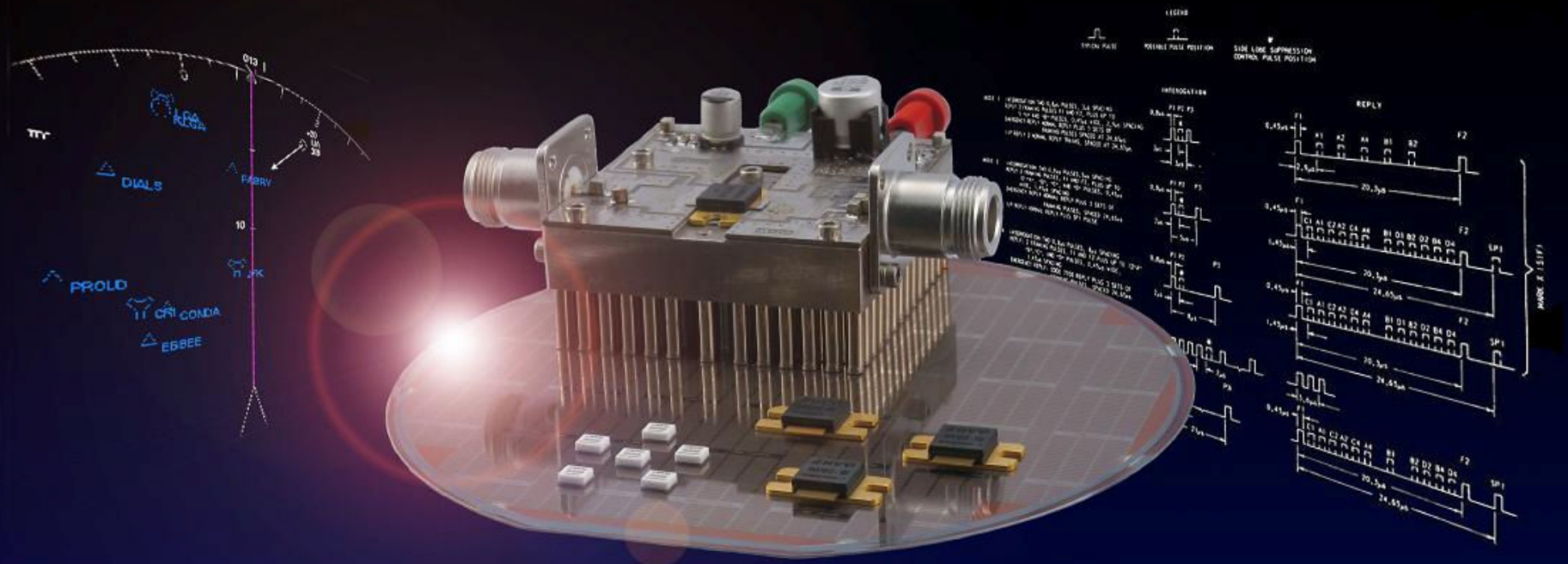
TESEC Measurement Equipment

- Delta Vf Method
  - Not a direct temperature measurement but does represent Max Tj
    - Tj calculated by knowing how Vf of the body diode changes with temperature for a fixed If
    - Can measure transient DC conditions only
    - Can determine Rth junction to air
  - Can derive RC thermal network by recording Vf from various transient conditions
    - Errors of model would be
      - Time delay to acquire a noise free reading
      - Vf v Temperature measurement error
      - Since transient only, it is requires de-embedding of test fixture

THERMAL PERFORMANCE

Symbol	Parameter	Max	Unit
θ_{JC}[1]	Thermal Resistance	0.20	°C/W

Summary



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HVVFET - Best in Class Si Technology for Avionics & Radar Applications

Pulsed Applications	HVVFET	Bipolar	36V LDMOS	50V LDMOS	GaN
High Voltage					
Gain					
Efficiency (drain)					
BW					
Thermal Resistance					
Ruggedness					
Power Density					
System Savings					

The HVVFET™ offers:

- Best in the industry ruggedness (20:1) – at least 2x the best in the industry
- Twice the power in the same package [vs. LDMOS]
- Significant improvements in gain (5x) and efficiency (30%) [vs. Bipolar]
- Ease of design due to ruggedness and higher impedances
- Complete 50V product line that can operate from 5V up to 50V

Vertical Technology Advantages

High Voltage Advantages

- Lower Current (Reliability)
- Lower Current (Dissipated Heat)
- Higher Impedance (Ease of Match)
- High Breakdown Voltage (Ruggedness)

Thermal Advantages

- Shorter Heat Path (Reliability)
- Lower Thermal Resistance (Cooler)
- No Thermal Runaway (Self Regulating)
- Higher Ruggedness (No Parasitic BJT)

System Advantages

- High Packing Density (smaller package footprint, package savings: cost, size and weight)
- Reducing Driver Stage Requirement (system level efficiency savings)
- High Voltage Driver Stage (power supply design savings)
- Extreme Ruggedness Rating (eliminates isolators reducing cost and weight)