Hysteresis Loss in High Voltage MOSFETs:
Findings and effects for high frequency AC-DC converters

What will I get out of this session?

Purpose:

- Highlight Coss hysteresis loss
  - Occurs for all SJ MOSFETs, from ALL manufacturers, but to greater/lesser extent
- Illustrate how it can be measured
- Show how it impacts MOSFET choice for ZVS topologies

- Part numbers mentioned:
  - UCC24612 SR driver
  - UCC27712 600-V half-bridge driver
- Reference designs mentioned:
  - TI high-efficiency active-clamp Flyback EVM (under development)
- Relevant End Equipments:
  - High-density adapters
  - High-efficiency PSUs

Introduction

- Industry trend → high efficiency & small size adapters & PSUs
  - Standard 65-W adapter → 8 W/in^3
  - Zolt 70-W → 14 W/in^3
  - Finsix Dart → 17 W/in^3
- Higher power density
  - Higher frequency → smaller magnetics
  - Small size → less surface area to dissipate heat → need higher efficiency with less dissipation
- Need soft-switching or zero-voltage-switching (ZVS) topologies to enable high Fsw
- ZVS – eliminate switching loss
  - Allows higher Fsw → smaller magnetics (still limited by HF core loss, AC resistance)
  - Allows larger switching devices with lower conduction loss – no capacitive losses, right?

f_{sw}=65kHz

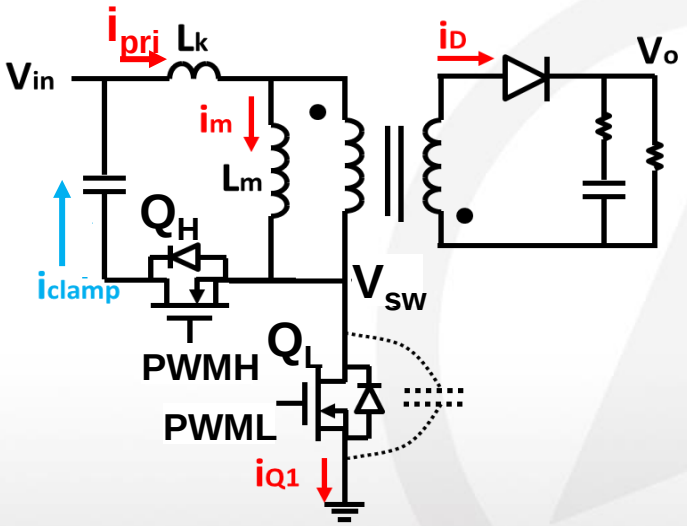
RM8 ~7300 mm^3

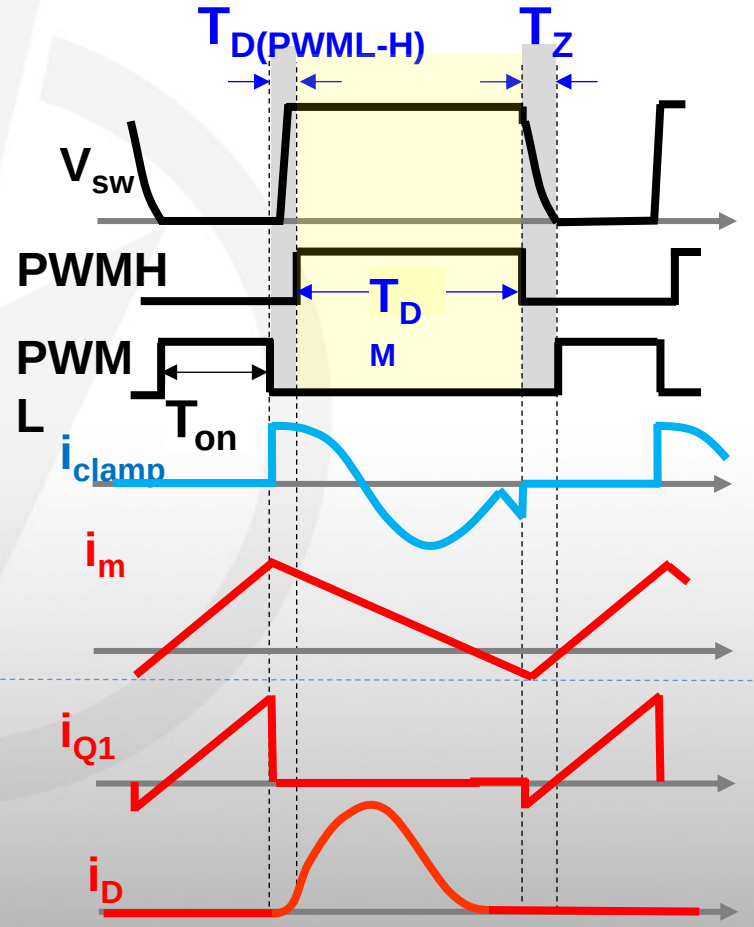
f_{sw}=200k~400kHz

EE16 ~3500 mm^3

Example ZVS topology – Active-Clamp Flyback

- QR Flyback only achieves partial ZVS
- Add active-clamp switch to achieve full ZVS
- Also recycle transformer leakage inductance energy





ZVS criteria: $\frac{1}{2} L_m i_{m(-)}^{\ 2} \geq \frac{1}{2} C_{sw} V_{sw}^{\ 2}$

Question #1: Where does ZVS start to become necessary & cost-effective for your designs and applications?

A. Above what power level?
   - *100 W, 200 W, 500 W?*

B. Above what switching frequency?
   - *200 kHz, 500 kHz, 1 MHz?*

C. Above what bus voltage level?
   - *100 V, 200 V, 400 V?*

D. Don’t know, don’t use ZVS topologies?

Zero-voltage-switching (ZVS) trade-offs

- ZVS – eliminate switching loss
  - Allows higher Fsw → smaller magnetics
  - Push Fsw higher – how high can or should you go?
  - Magnetics still limited by HF core loss, AC resistance loss
  - Allows larger switching devices with lower conduction loss
  - No capacitive losses, right?
  - Can push the capacitance way up, right?
- Not quite!

Superjunction high-voltage MOSFET

- Brief history:
  - Superjunction concept patents date from 1978-1990s
  - First commercialized 1998/9 by Infineon (CoolMOS) , 2000 by ST (MDMesh)
  - Breaks the theoretical Si limit of Rds(on) at high voltage
  - Uses vertical pillars of P/N to for more uniform field distribution
  - Allows much higher N-doping level (10x to 100x) vs std. MOSFET
  - Gives higher breakdown (uniform field) at very low Rds(on) (N-doping)
- Many Superjunction vendors:
  - Infineon/IR, ST, Toshiba, AOS, Fairchild/On, Vishay, Fuji, Rohm, NXP, EPC, Fujitsu, & others
- Non-linear Coss vs VDS
  - More pronounced with newer gen lower Rds(on), smaller feature size

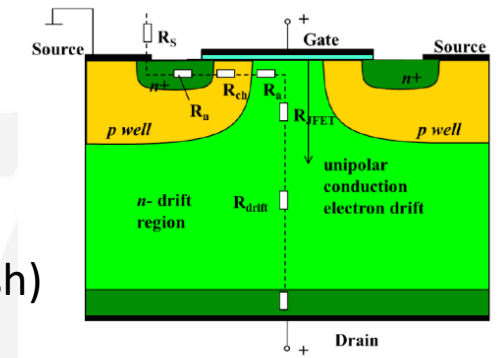


Fig. 1. Planar power MOSFET structure and the schematic representation of the resistance components of different regions in the on-state.

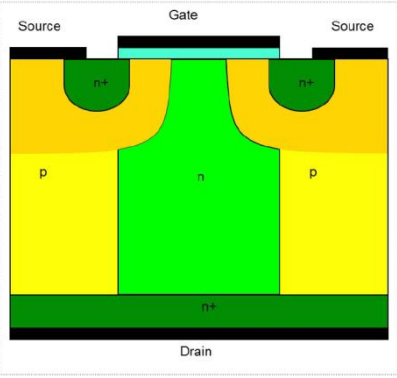


Fig. 8. CoolMOS structure using a planar gate [8].

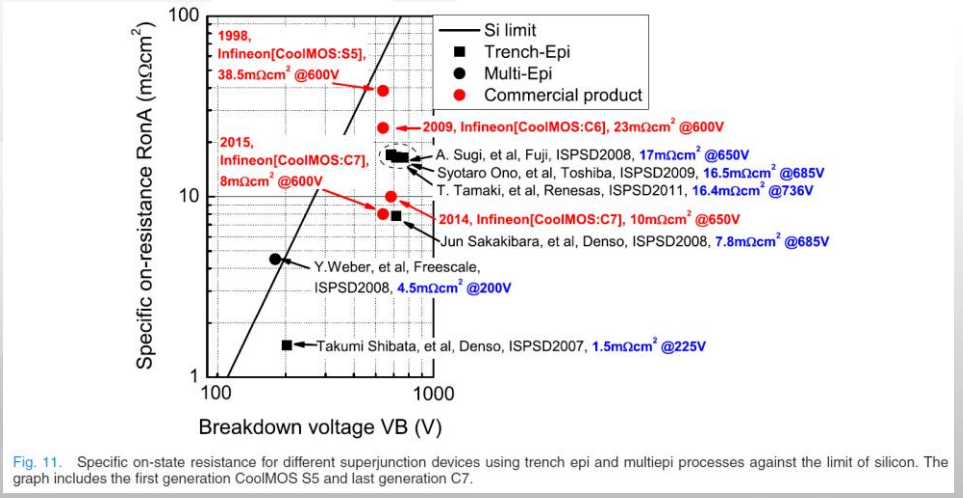


Fig. 11. Specific on-state resistance for different superjunction devices using trench epi and multiepi processes against the limit of silicon. The graph includes the first generation CoolMOS S5 and last generation C7.

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Question #2: Which type & generation Superjunction FETs do you use or prefer for your designs?

A. Older rugged series, like Infineon C3/CP?

B. Newer but still mature, like Infineon C6/P6/E6 series?

C. Newest gen leading-edge types, like Infineon C7/P7/G7?

D. Don’t use SJ at all – prefer standard rugged MOSFETs?

Eoss loss – background

- What is Eoss?
  - Energy-related loss due to charge stored in Coss
  - Depends on the bus voltage & device
- Eoss completely dissipated in hard-switching topologies
- Eoss partly recovered in quasi-resonant topologies
- ZVS topologies ideally avoid all Eoss loss
  - Can switch at very high frequency
  - Lower Eoss ⇒ less circulating energy to achieve ZVS
- Big variation in Eoss loss for different devices
  - New generations continually achieve lower Eoss
  - Curves show latest gen C7/P7/G7 close to WBG
- However MOSFET Coss charge and discharge has hysteresis

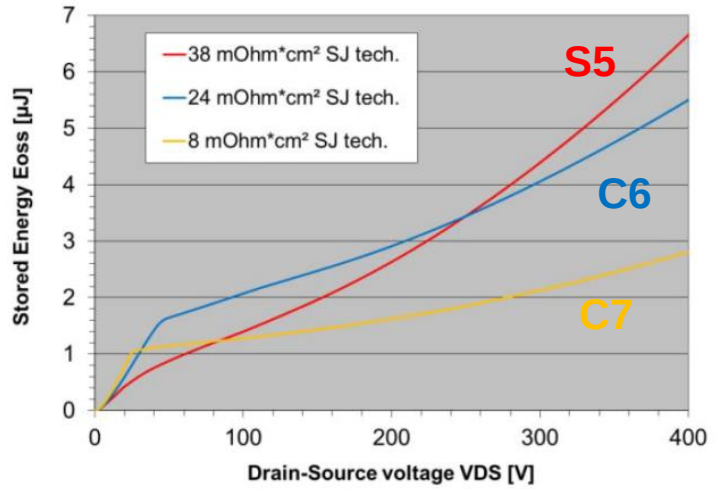

Fig. 13. Energy stored in the output capacitance of three subsequent generations of superjunction devices.

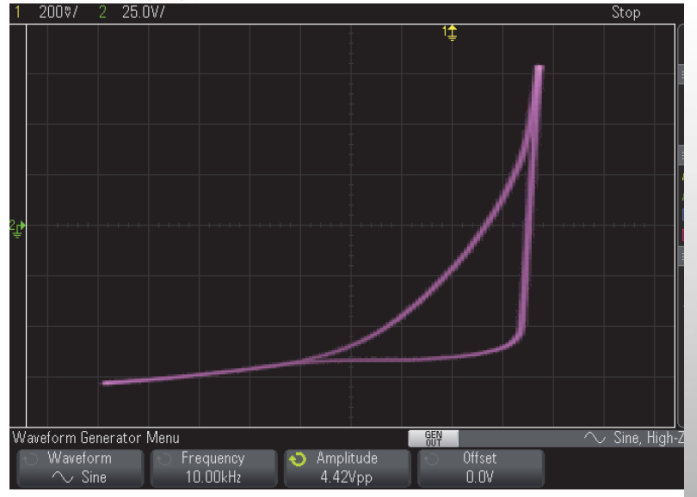

Fig. 1. Oscilloscope capture for Device A being n

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Coss hysteresis loss – the discovery

- Phenomenon first reported APEC 2014 by Enphase*
- Measured Coss to help choose best devices for HF ZVS
- Observed asymmetric charge/discharge waveforms
- Significant temperature rise for expected lossless charge & discharge of Coss
- Waveforms & losses did not match models & simulation
- Big variation in Coss loss for different devices A-E
- Proposed new ZVS Figure of Merit

Table 2. Characteristics of the superjunction MOSFETs measured.

Device	V_{DSS} at 25°C (V)	R_{DSON} max at 25°C (Ω)	C_{iss} at V_{DS}=0 (nF)	E_{stored}*† (μJ)	$E_{dissipated}$*‡ (μJ)	Area Specific On-Resistance typ at 25°C (mΩ cm²)
Device A	650	0.148	2.0	1.47	4.050	19
Device B	600	0.160	2.1	2.75	0.5664	27
Device C	600	0.178	2.0	2.46	0.242	26
Device D	600	0.158	3.3	4.06	0.140	30
Device E	600	0.160	1.9	2.67	0.079	33

*V_{GS}=0, V_{DS}=200V. †Calculated from small-signal C_{oss} versus V_{DS}. ‡Measured energy dissipation of C_{oss} per ZVS cycle.

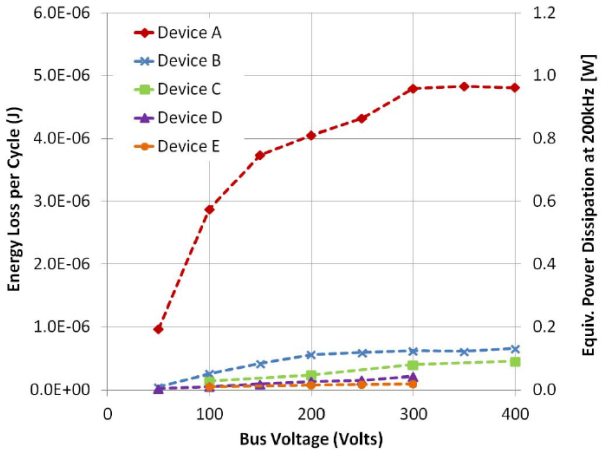


Figure 4. Measured C_{oss} related energy loss (per device) versus bus voltage of state-of-the-art MOSFETs from multiple vendors.

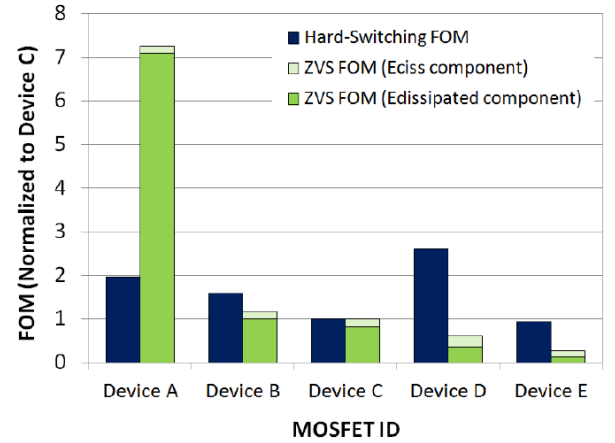


Figure 9. Comparison of normalized hard-switched and ZVS figures of merit with V_{GS}=10V and V_{DS}=300V for the MOSFETs tested where ZVS FOM [Eciss component] = R_{DSON} × E_{Ciss} and ZVS FOM [Edissipated component] = R_{DSON} × $E_{dissipated}$. The FOMs have been normalized to device C which has FOM_{ZVS} = 100 nJ Ω and FOM_{HS} = 1.51 nC Ω.

All images reproduced with permission from "Coss Related Energy Loss in Power MOSFETs Used in Zero-Voltage-Switched Applications", J. B. Fedison, M. Fornage, M. J. Harrison, D. R. Zimmanck, Enphase Energy Inc., APEC 2014, © IEEE
** Authors now with ST*

Coss hysteresis loss – other published results

- What causes hysteresis in Coss charge/discharge? Why are some devices better?
- Jaume Roig & Filip Bauwens proposed cause due to “stranded charges”, much worse in MEMI (multi-implant multiepitaxy) technology vs. TFEG (trench-filling epitaxial growth)
  - *“Origin of Anomalous Coss Hysteresis in Resonant Converters With Superjunction FETs”, Jaume Roig, Filip Bauwens, OnSemiconductor Power Technology Centre, IEEE Transactions on Electron Devices, Vol. 62, No. 9, September 2015*
- Possibly explains why different devices show grossly varying hysteresis loss?
- How can hysteresis loss be measured? Fedison et al (Enphase) used Sawyer-Tower method (detailed in the paper) for same FETS A-E:
  - *“Coss Hysteresis in Advanced Superjunction MOSFETs”, J. B. Fedison, M. J. Harrison, Enphase Energy Inc., APEC 2016*

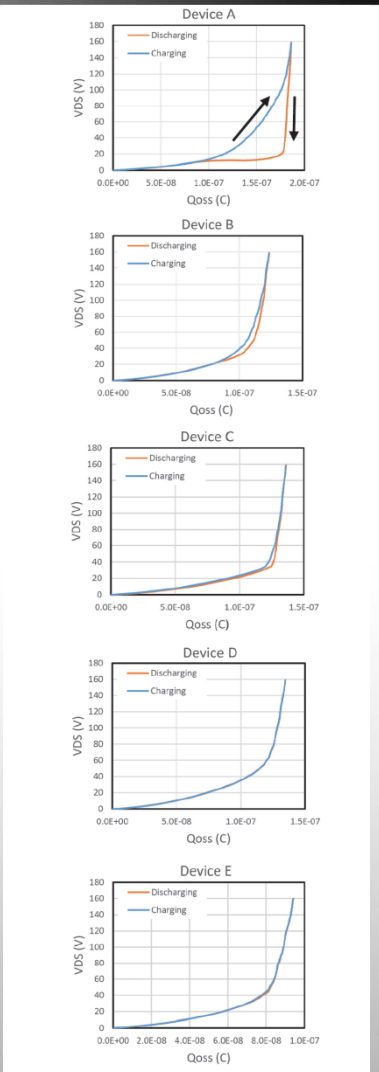
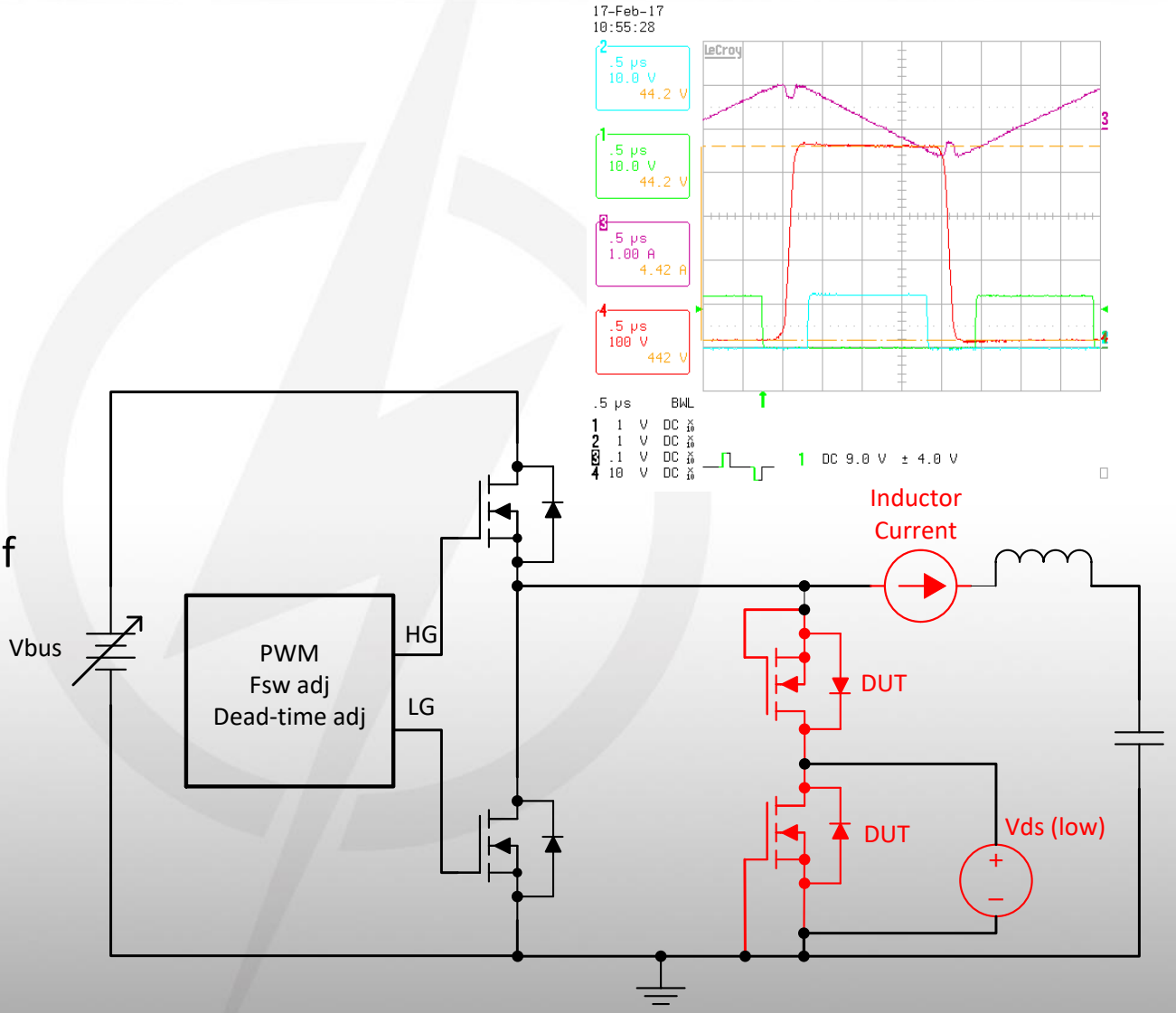


Fig 3. V_{DS} versus Q_{OSS} curves measured with the Sawyer-Tower circuit for devices A – E. Sweep frequency = 10kHz and peak-to-peak voltage = 160V.

TI investigation of Coss loss – test circuit

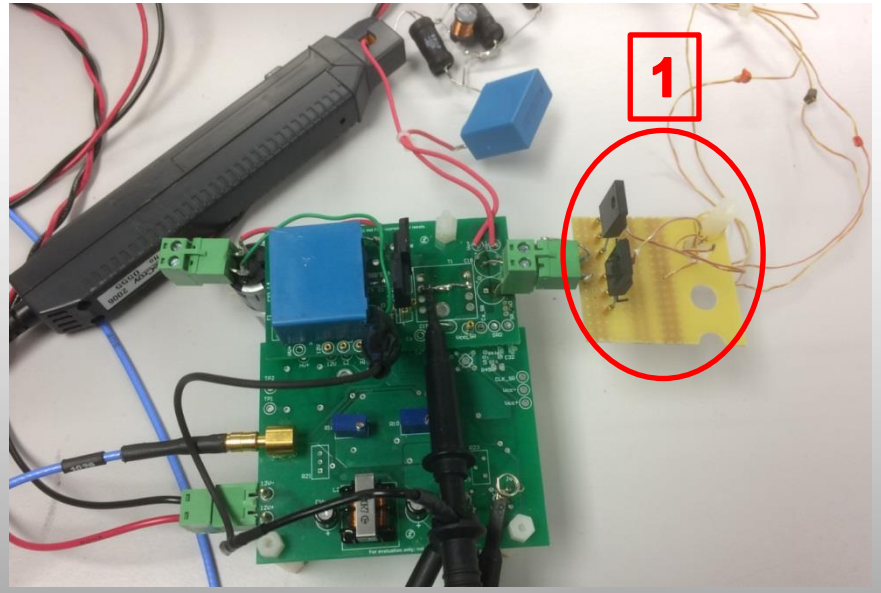
- Connect 2 identical DUTs back-to back in series
  - Back-to-back body diodes ⇒ no diode conduction
  - G-S short => FET off ⇒ no channel conduction
- Connect to driving high-freq high-voltage square-wave
  - Driving square-wave generated by half-bridge circuit
- Observe Vds of low-side DUT & inductor current
- Measure low-side DUT temperature rise to assess level of Coss hysteresis loss.
- Measure low-side DUT temperature rise ΔT
- Calibrate result
  - Same environmental setup (same thermal conditions)
  - Current I though body diode Vf to get same ΔT
  - $P_{diss} = I * V_f$
  - $E_{oss(hyst)} = P_{diss} / F_{sw}$

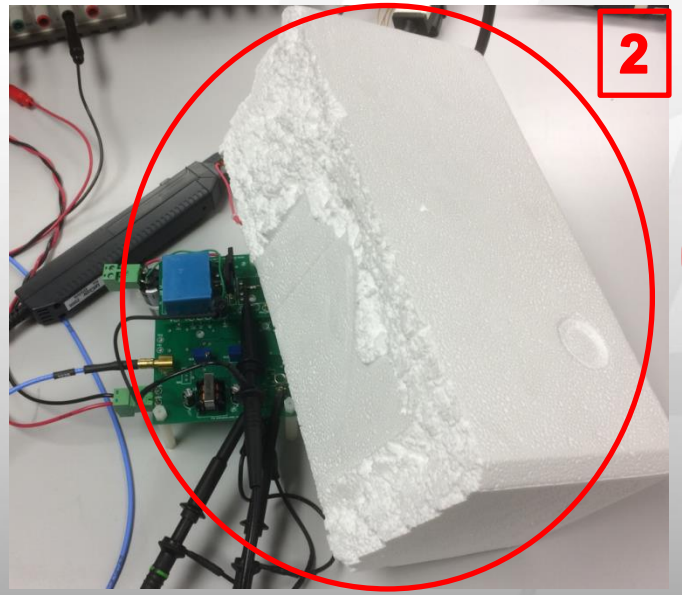


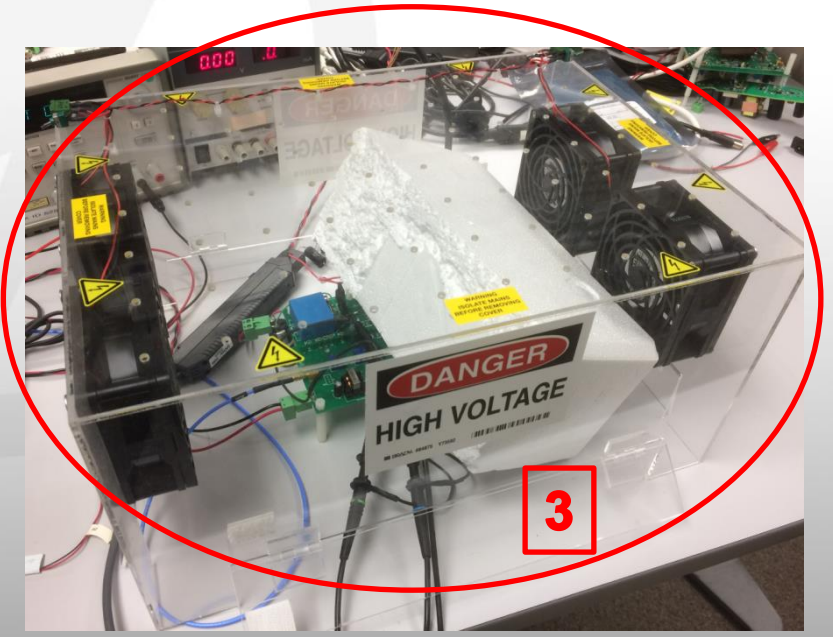
TI investigation of Coss loss – test setup

1. DUTs socketed with thermocouples glued to plastic body (not metal tab)
2. Styrofoam box to isolate DUTs from external HB FETs & inductor
3. Plastic safety enclosure over entire setup to block ambient air-conditioning airflow

Four K-type thermocouples measured – #1 Low DUT, #2 High DUT, #3 Ambient inside styrofoam, #4 DUT PCB







Devices tested – Infineon CoolMOS 600-V, 650-V & 700-V rated

- Note that Coss hysteresis loss is observed for ALL SJ MOSFETs – regardless of manufacturer
  - Actual loss varies, depending on internal design specifics
- Results summarised here – all Infineon
  - ***Not intended to single out Infineon, just take one manufacturers broad portfolio as an example***
  - ***To show comparative performance across families for a single manufacturer***
  - CoolMOS 700-V:
    - P7 – IPA70R360P7, IPA70R600P7, IPS70R900P7, IPS70R1K4P7
  - CoolMOS 650-V:
    - C7 – IPP65R225C7, IPA65R190C7, IPP65R125C7, IPP65R045C7
    - G7 – IPT65R195G7
  - CoolMOS 600-V:
    - C3 – SPP20N60C3
    - C6 – IPP60R190C6, IPP60R380C6, IPP60R600C6, IPP60R950C6
    - C7 – IPP60R180C7
    - G7 – IPT60R150G7

Key test results – C6 series

DUT	Vds	Series	Rdson	Eoss @ 450 V (uJ)	Eoss hyst (uJ)	Eoss Hyst %
SPP20N60C3XKSA1	600	C3	190	8.7	0.833	9.6%
IPP60R190C6	600	C6	190	5.9	0.636	10.8%
IPP60R380C6	600	C6	380	3.2	0.298	9.3%
IPP60R600C6	600	C6	600	2.1	0.288	13.7%
IPP60R950C6	600	C6	950	1.5	0.138	9.2%

- Good Eoss reduction (-33%) vs old C3/CP generations
- 600-V C6 family shows low hysteresis loss <10%
- Good choice for ZVS compared to older gen devices
- E.g. – 0.636 uJ @ 500 kHz = 0.32 W – not negligible! Significant temp rise
- E.g. – 50 W @ 93% eff –> extra 0.32 W loss –> ~0.55% eff drop

Key test results – C7 series

DUT	Vds	Series	Rdson	Eoss @ 450 V (uJ)	Eoss hyst (uJ)	Eoss Hyst %
IPP65R225C7	650	C7	225	2.6	1.478	56.8%
IPA65R190C7	650	C7	190	3.1	1.390	44.8%
IPP65R125C7	650	C7	125	4.7	1.766	37.6%
IPP65R045C7	650	C7	45	13	4.656	35.8%
IPP60R180C7	600	C7	180	3	0.264	8.8%

- Significant Eoss reduction vs older C6 generation
- 600-V C7 shows low hysteresis loss <9%, but also lower Eoss to begin with
  - 600-V C6 vs C7 – 0.636 uJ vs 0.264 uJ – 60% reduction
- 650-V C7 shows significantly higher hysteresis loss
  - Compare 180/190 mR 600/650-V devices – 8.8% vs 45%!

Key test results – P7 series

DUT	Vds	Series	Rdson	Eoss @ 450 V (uJ)	Eoss hyst (uJ)	Eoss Hyst %
IPA70R360P7	700	P7	360	2	0.603	30.1%
IPA70R600P7	700	P7	600	1.23	0.374	30.4%
IPS70R900P7	700	P7	900	0.97	0.235	24.2%
IPS70R1K4P7	700	P7	1400	0.64	0.196	30.6%

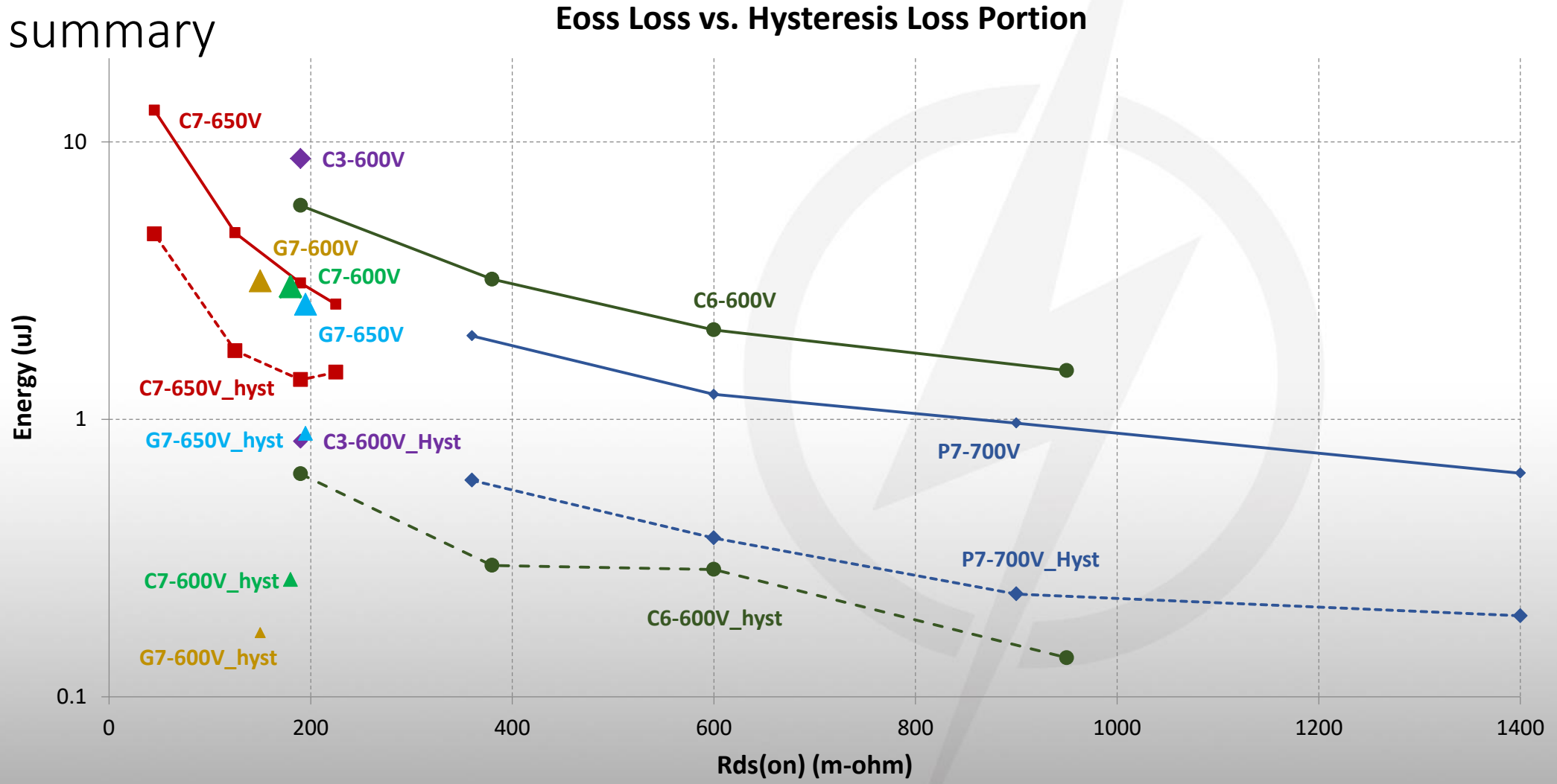
- Comparable Eoss values vs C7 650-V generation
- Achieves same Eoss at higher VDS 700 V
- 700-V P7 shows reduced higher hysteresis loss vs 650-V C7
  - Compare 225-mR 650-V C7 (57%) vs 360-mR 700-V P7 (30%)

Key test results – G7 series

DUT	Vds	Series	Rdson	Eoss @ 450 V (uJ)	Eoss hyst (uJ)	Eoss Hyst %
IPT60R150G7	600	G7	150	3.15	0.170	5.4%
IPT65R195G7	650	G7	195	2.6	0.889	34.2%

- Initially marketed as “P7 Gold”, later converted to G7
- Best-in-class Eoss (lower than C6/C7/P7)
- Comparable Eoss – 600-V G7 vs 600-V C7, but at lower Rds(on) (-17%)
- Comparable Eoss – 650-V G7 vs 650-V C7, but at lower Rds(on) (-14%)
- Again – observe a penalty at higher voltage – 650-V vs 600-V 34% vs 5%

Results summary



Conclusions & key take-aways

- Coss hysteresis is REAL and can be very apparent in ZVS topologies
- MOSFET datasheets do not include Coss hysteresis loss data; it cannot be predicted from other data
- Industry must encourage MOSFET vendors to test for and publish this data – and to reduce the loss!
- Different MOSFET generations are better suited to various hard-switched, QR & ZVS topologies
- Newer generation devices are improving – lower Rds(on), lower Eoss & lower hysteresis loss
- Specific observation – Coss Hysteresis Loss vs VDS Rating:
  - *Similar Rds(on), similar Eoss curves – observe higher loss for 650-V vs 600-V rated device*
  - *Depends on internal design and process, cannot be related to VDS rating alone*
- Advantage of Active-Clamp Flyback (ACF) ZVS topology –
  - *"Clean" waveforms allow use of 600-V MOSFETs with lowest Eoss and lowest hysteresis loss*
  - *EVM (under development) using 600-V FETs, UCC27712 HB driver, UCC24612 SR driver*