

LTpowerCAD Design Tool 101



Power Supply Loop Design/Optimization in the Lab







- Manually adjust R and C values. Check loop or load transient.
- Accurate, but time-consuming.
- ► How to support remote customers?



Complete Power Design Flow with LT Tools ...



ANALOG

AHEAD OF WHAT'S POSSIBLE"





Paper Design Is Difficult and Time Consuming ...

- Define supply specifications
- Decide topology
- ► Search for an IC (time ↑↑)
- Calculate power components (time \\ , suboptimal)
- Select components: L, C, FET (time \\ , suboptimal)
- Estimate efficiency/loss (difficult, inaccurate)
- Guess/simulate loop compensation (difficult, inaccurate)
- Draft schematics

⊗ Time consuming, difficult, suboptimal ...

⊗ Requires good power supply knowledge and skills







LTpowerCAD Design in 5 Simple Steps! Fast and Easy







- ► Free download at <u>analog.com/LTpowerCAD</u>
- Runs on Windows PC

Note for ADI users only: Install the program by RUN Elevated on an ADI PC.



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LTpowerCAD Main Window







Design Step 1: Enter Spec, Search a Part



	EVICE	S BLE ^M		Copyright 2014	CAD Design 4, Analog Devices Inc.	Tool V2.5.2 All rights reserved	I.	2 Se	arc
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Step 2: Power Stage Design (fs, L, C, etc.)







Step 2: Power Stage Smart Warnings







Warning levels are set by apps engineers for different products.

Automatic warnings guide to proper values



Step 3: Efficiency Optimization





Real-Time Estimations for Optimum $\eta\%$



Step 4: Loop and Transient Design





Real-Time Loop and Transient Optimization



Step 5: Design Summary, BOM, Size



.oss Est	imate & Break Down	Lo	oop Comp. & Loa	ad Transient	Power Desig	n Summary						
	9, 9, 5) S		Print Summa	iry Report		Sum	mar	y R	epo	rt		
	LTC3833 Su	ipply [Design Su	mmary								
	Project Info:	Ref Des	ign 12Vin to 1	1V/20A, 10/2	2014, H.Z.		Desig	an Specifi	cations			
	Steady State :						-					
	Rail #	Vin Min.	Vin Nom.	Vin Max.	Fsw	Vo	ΔVo rip. p-p	ΔVo rip.%	Io Max	∆iLp-p	ΔiL%	iLpk
orformanco	1	10.8 V	12 V	13.2 V	399 kHz	1 V	7.82 mV	0.4 %	20 A	9.19 A	45.9 %	24.59 A
enumance	Efficiency and l	.oop :										
	Rail # Vo		Iomax	Eff.@Iomax	PLoss@Iomax	Loop BW	Loop PM	Step Low	Step High	Step Slew	ΔVo@Step	∆Vo@Step %
Summary	1 11		20 A	91.99 %	1.741 W	79.43 kHz	79.26 deg	0 A	10 A	10 A/µs	22.1 mV	+/-2.2 %
<u> </u>	Recommendatio	ons and V	Narnings :									
	wessage						_	6				
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		Malua -	Overtite	Description	n Mfr Name	MG Devit #		Dia dararian	1 (14/()	11/	U N
	U1	value	Quantity	IC	IINFAR TECH	ITC3833		ekg. (Imperial)	L(mm)	w(mm)	H(MM)	User Note
	101	0.25uH	1	IND	COLCRAFT	MVR1251T-251			11.5	9.75	5.1	
	Cinh1	180uE	1	CAP	PANASONIC	165VP180MX			10.3	10.3	79	
BOM	Cincl Cinc2	100pi	2	CAP	MURATA	GRM22ER61CA	76KE15	ro •	2.0	25	17	
	Cabl Cabl Cabl	220.JE	2	CAP	SANVO		/UKEIJ	1210 •	7.2	4.2	1.0	
	Cost Cost	100. F	2	CAP	TDK	C2225V5P0140	754	D2E •	2.2	25	1.0	
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olution Size	Power Component	ts Area (Exc	ludes ICs)	541.5 mm 0.839 in^2	^2	Part # 1		Part # 2	ength			
	* Power Componen	ts Area (Inc	ludes ICs)	561.5 mm 0.87 in^2	^2 2	t dia		Width				



(Optional) Step 6: Export to LTspice Simulation





* Key LTpowerCAD design tool values are exported to LTspice

LTspice Simulation for Detailed Waveforms



Design Shortcut: Leveraging Existing Solutions



a e e e 🗉 Sa(0 ,	M. Ø 🛄 🛄 🗖	OL _								
LTC3833 - Fast Accurate Step-Down	DC/DC C	ontroller wit	th Differential Output	Sensing			Project I	Name:				
Vin(norm) 12 V VIN	CinC	Solutions Libra	ry					Date.				8
		Built-In Solu	tions									_
Total CIN RMS 6.614 A Part # 255VPF180M	TT I	Part Name	Solution Name			(V)	Vin [nom] (V) Vin [max] (V) Rail Voltage(s) (V)	Output Current(s) (A)	Description	
Total CIN Ploss 0.151 W C Nom 180 µF	- c	LTC3833	Datasheet P36				12	14	Vout1 = 5.5V	Iout1 = 4A	Fsw=2MHz Design	*
ESR 16 mΩ		LTC3833	DC1516A-A				12	24	Vout1 = 1.5V	Iout1 = 15A	1.5V/15A DCR Sense	
# Cap 2	#	LTC3833	DC1516A-B				12	24	Vout1 = 1.5V	Iout1 = 15A	1.5V/15A with Rsense	
VOUT	111	LTC3833	DC1640A-A				12	24	Vout1 = 1.5V	Iout1 = 20A	1.5V/20A DCR Sense	
Feedback	01	LTC3833	Ref Design 5-12Vin to 10A	1V 500kHz d	ual 3x3 FET DCI	R	12	14	Vout1 = 1V	Iout1 = 10A	DCR Sensing. Reference Design Only.	
Sug. Rt1 30.1 kΩ Rt1 Cff1		LTC3833	Ref Design 5-12Vin to 10A	1V 500kHz d	ual 3x3 FET Rse	n	12	14	Vout1 = 1V	Iout1 = 10A	Rsense Sensing. Reference Design Only.	·
		-User's Soluti	ons									
Vosns+		Part Name	Solution Name	Vin [min] (V)	Vin [nom] (V)	Vin [ma	ax] (V) Rail	Voltage(s) (V)	Output Currents(s) (A)	Description	File Name	
Rb1 Cfit1		LTC3833	DC1640A-A Demo Board	4.5	12	24	Vou	t1 = 1.5V	Iout1 = 20A	Inductor DCR Sense	LTC3833 DC1640A-A Demo Board.ltpc	
Sug. Rb1 20 kΩ		LTC3833	DC1640A-B Demo Board	4.5	12	24	Vout	t1 = 1.5V	Iout1 = 20A	Rsense	LTC3833 DC1640A-B Demo Board.ltpc	
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I Cthp1												
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Duty & Ton Compensation					New So	lution N	ame :					
Vout1 Duty 12.5 % Cth1 470 pF Ton1 @ Vin Max 210 ns Rth1 16.5 kΩ	-				New Celes							
Change Change	to DCR Sensin				New Solut	ion Des	inption :					
Solution library de	ome	hoa	rds data	shee	ot cire	cui	ts	tion		Overwrite Selecte	ad Solution	
obration instary at		Boa	ae, autu						•	over white beleet	a solution	
reference designs									1			
Tererence designs								xit	J			

- ► Users can add/build their solutions, too.
- Quick start point of a new design!





LTpowerCAD Bench Verification Report (on a Standard Demo Board)





Other Tools in LTpowerCAD







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Webpage: analog.com/LTpowerCAD





► Free download

- Quick-start guide
- Articles and videos





Advanced Features ...

Design Curves (for Wide V_{IN} Range)





- Check the design in the full V_{IN} range.
- Check the worst case.



Power Stage Design: Component Libraries





Show Suggested Parts eases component selections



Component Library (Power MOSFET Example)



0 LT	powerCAD II V2.5.4 - LTC3833 D	DC1640A-B.ltpc										×				
File	Help															
1	Power Stage Design	Loss Estimate & Break Down	k Load Transient Power De	ign Summary												
Output Rail # 1	Design Specs Vin min: 4.5 Vin nom: 12 Vin max: 24 Sw. Freq: 298 Vout: 3.2 Iout: 10 Ta: 25 °C	MOSFETs Control MOSFET Vendor: Infineon Part: BSC0504NS Vdss: 30 V # Fets: 1 Qg: 6 nC Qgd: 1.4 nC	For CCM Mode Only Rail #1 (3 98	.32V) Efficiency	y & Power Le	D55	Inductor AC I	Loss Entered by Use	er Power Loss Br	eakdown (Fu	ll Load)	1				X
	Inductor Inductor : XEL6	Rdson: 3.85 mΩ Qgs: 1.9 nC Rg: 1.2 Ω Vmiller: 2.7 V	96	Show All Parts Built-In Parts	Show Suggest	ed Parts	Vin	12 (V) #	Parallel Fets 1	pcs. (for M	IOSFET Loss Calcula	tion) Updat	te Search	Show Only AEC	•Q Parts Clear S	earch Entries
	L: 2.2 uH DCR: 6.1 mΩ	valoae: 0.34 V vth: 1.6 V PLoss: 0.293 W/Fet Coss: 250 pF θja: °C/W ΔTja: °C	92-	Vendor Clear	Name Clea	Est. Loss(W)	Vdss(V)	Vgs1(V)	 Rds1(mΩ) Clear 	Qg1(nC)	Vgs2(V)	Rds2(m)	Qg2(nC)	Qgd(nC) Clear	Qgs(nC) Clear	Coss(p
	θwa: 17.1 °C/W	Sync MOSFET	00	Infineon	BSC0504NSI	0.204	30	4.5	4	5.2	10	3	11	1.4	1.9	250 🔺
	Select	Vendor : Toshiba	00	Infineon	BSZ0506NS	0.208	30	4.5	4.4	5.2	10	3.5	11	1.4	1.9	220
	Inductor Loss	Part : TPHR6503P	86-	Infineon	BSC0503NSI	0.209	30	4.5	3	7.1	10	2.3	15	1.8	2.5	330
	Tw : 25 °C	Vdss : 30 V # Fets : 1 pcs	84	Infineon	BSC0502NSI	0.223	30	4.5	2.4	9	10	1.9	19	2.3	3.1	420
	DCR @ Tw : 6.1 mΩ	Qg: 60.4 nC Qgd: 16 nC	82	Infineon	BSZ0503NSI	0.223	30	4.5	3.5	7.1	10	2.8	15	1.8	2.5	330
	DCR Loss : 0.62 W	Rdson : 0.57 mΩ Qgs : 24 nC	80-	Infineon	BSZ0502NSI	0.239	30	4.5	2.9	9	10	2.4	19	2.3	3.1	420
	Total Loss : 112 W	Rg : 0.6 Ω Vmiller : 3 V	70	Infineon	BSC0501NSI	0.252	30	4.5	2	11.4	10	1.5	23	2.9	3.9	530
	10tal Loss . 1.12 W	Vdiode : 0.82 V Vth : 1.6 V	8	Infineon	BSZ0501NSI	0.256	30	4.5	2.1	11.4	10	1.7	23	2.9	3.9	540
		PLoss: 0.129 W/Fet Coss: 2720 pF θja: °C/W ΔTja: °C	5, 76	Infineon	BSC052N03LS	0.261	30	4.5	5.8 III	5.9	10	4.3	12	1.9	2.2	300 ×
	Q _T	Estimate	5 70	User Parts:												
			70	test	test part 1	0.522	30	4.5	12.2	7.5	10	8.1	17	2	3.9	370 🗘
		Vin 12 V Update	10						m							•
		✓ Freeze Plot	68-	Add A New User	Part:			1	1		1					
		External Bias	66-	Vendor	Name	Vdss(V)	Vgs1(V)	Rds1(mΩ)	Qg1(nC)	Vgs2(V)	Rds2(mΩ)	Qg2(nC)	Qgd(nC)	Qgs(nC)	Coss(pF)	Rg(Ω)
		EXTVCC : V LTC3833 Gate Drv. = 5.3V	64	-												-
	FET Vmiller	Rail Total Power Loss @ Full Load	62-	٠	·	·		<u> </u>	•	<u>^</u>		·) (
	1	Pin : 35,45 W	60						A	dd Part To Library						
				Vendor Links			ISHAY.	(İnfineon	ne	e <mark>x</mark> pe	ria 🕯	RENES		FOSHII eading Innov	BA ation >>>

Show Suggested Parts—quick efficiency optimization







AHEAD OF WHAT'S POSSIBLE^M

MLCC: significant capacitance loss at V_{BIAS}

► How to design it in LTpowerCAD?

MLCC Auto Derating vs. DC Bias





Component Estimation Settings										
LINEAR TECHNOLOGY										
MLCCs MOSFETs Inductors Limits (FAE Only)										
Estimate Actual Capacitance at DC Bias :										
OK Exit										





Input EMI Filter Design (Only for Differential Mode, Conducted EMI)





Released for buck and boost converters



Input EMI Filter Design Curves



EMI Noise vs. Standard



Filter Insertion Gain (with Damping)



Filter/Supply Impedance (with Damping)





Auto Loop Compensation









LTpowerPlanner[®] Design Tool Brief Introduction

BY HENRY ZHANG AND TIM KOZONO APPLICATIONS ENGINEERING POWER PRODUCTS



A System Board Example



- A modern electronic system usually has many power supplies and loads.
- A power tree drawing is needed.





A Power Management System Example



- A system designer needs to plan and development the entire power management system.
- System optimization: total efficiency, loss, size, cost, etc.



A system-level design and optimization tool is needed



LTpowerPlanner[®] Design Tool



A System-Level Power Planning Tool:

- Create a system power tree diagram.
- Estimate total system power, efficiency, and size.
- Optional links to LTpowerCAD and LTspice Designs.

- Available in the LTpowerCAD package.
- LTpowerCAD free download: <u>analog.com/LTpowerCAD</u>.
- Windows PC based.



Why Use the LTpowerPlanner[®] Tool?



- Draw system power tree diagram
- ► Calculate total system power, efficiency, and solution size
- Document system architecture and design solutions
- Compare different system solutions for optimum solution
- Present intuitive system solutions



LTpowerPlanner[®] Tool: Getting Started





"System Design" in the LTpowerCAD package.



Step 1: Drawing a System Power Tree





Place input source, converter, and load components.

Draw power wire connections (from left to right)



Step 2: Updating Parameters (For Input Source, Converters, and Loads)







Total Efficiency = 90.22% Total Size = 3Units^2

Calculate total input power, output power, loss, efficiency, and size (based on user's entries of generic component parameters).





Step 3: Run Calculation





2V 8A

P=16W

Comparing Different Architectures





A quick power tree comparison for optimum design



A Communications System Power Tree Example



- Multichannel converters.
- Resistive component:
 R, L, FET, etc.
- Colored nets/loads to represent power-up/-down sequence.





LTpowerPlanner[®] Component Visual Options







FPGA Reference Designs on analog.com



Many existing FPGA/processor reference power trees.

ANALOG Q Search AHEAD OF WHAT'S POSSIBLE' EDUCATION **APPLICATIONS** COMMUNITY SUPPORT MY HISTORY PRODUCTS DESIGN CENTER Design Center > Reference Designs > Circuit Collections > Altera Arria 10 FPGA Development Kit **Altera Arria 10 FPGA Development** Kit **Reference Materials** Overview



Solution Power Tree Example Library



Some existing FPGA/processor reference power trees.





(Optional) Links to LTpowerCAD and LTspice





Leverage LTpowerCAD and LTspice tools to design each supply.





LTpowerPlanner tool helps you design a system with:

- Easy steps
- Intuitive GUI interface
- ► Short time
- Optimum system power solution





LTPOWERCAD MAKES DESIGN QUICK AND EASY

Questions and Suggestions?

Email : LTpowerCAD@analog.com (formerly LTpowerCAD@linear.com)

Free Download at analog.com/LTpowerCAD

