

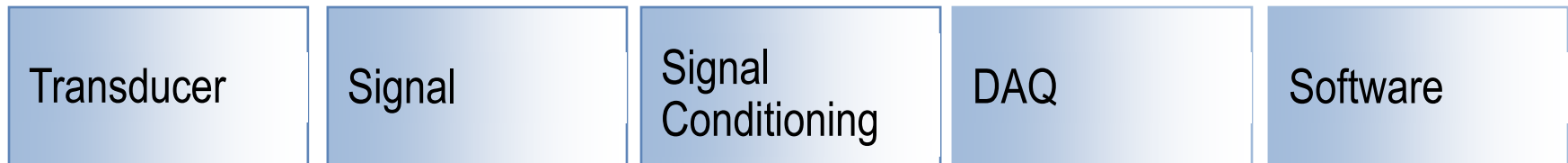
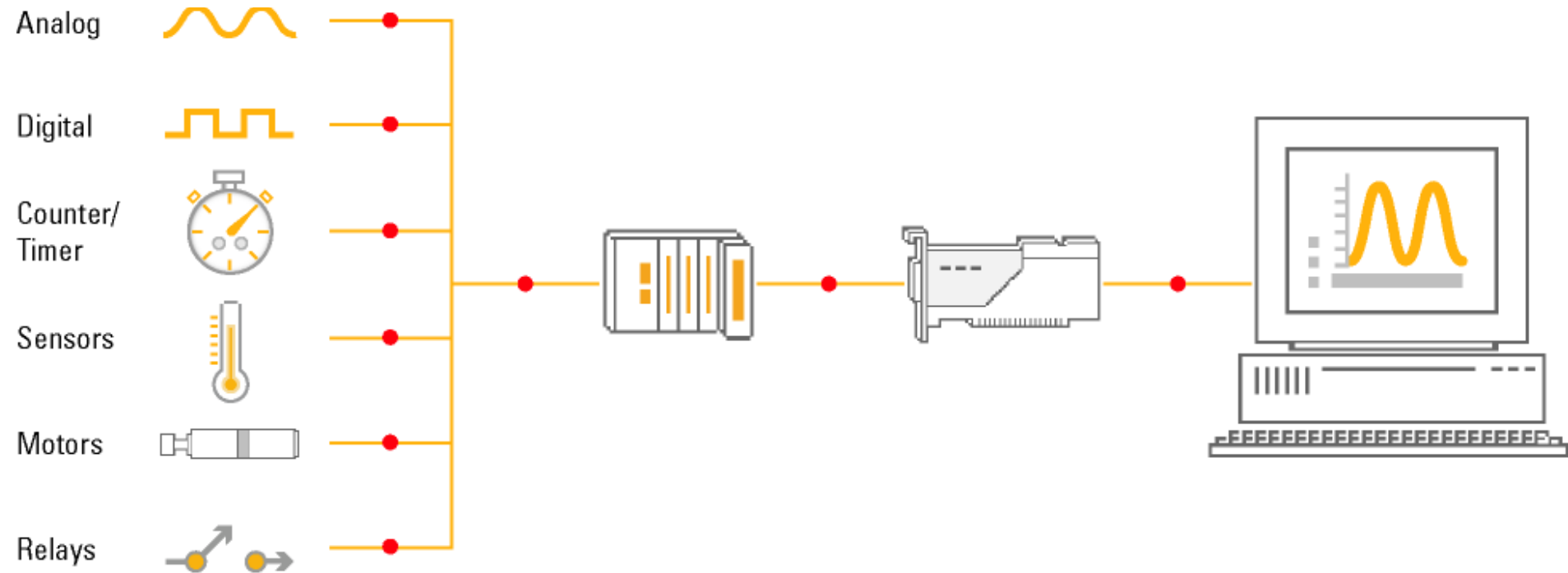
Utilizing the Latest Technologies in Data Acquisition



Agenda

- Computer Based DAQ Fundamentals
- Utilizing New Technologies

PC-Based Data Acquisition (DAQ)



PC-Based Data Acquisition (DAQ)



Gas Turbine Engines



NASA James Webb Space Telescope



HIL Simulation for Hybrid Cars



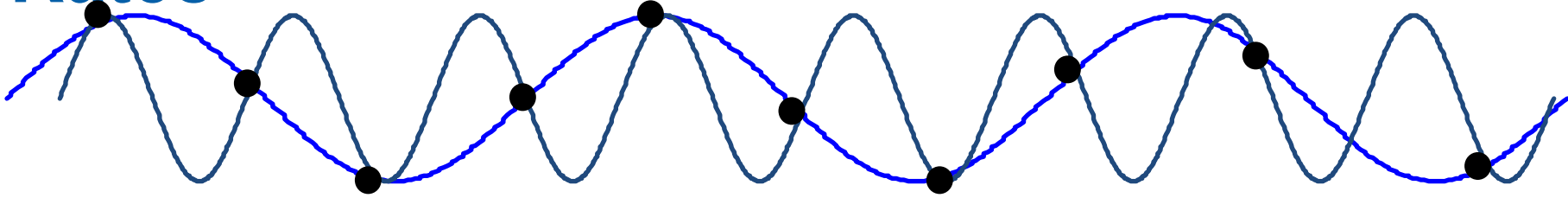
Bridge Health Monitoring in India

Measuring Analog Input Signals

Factors to consider:

- Sampling rate
- Resolution
- Range and amplification
- Noise and filtering

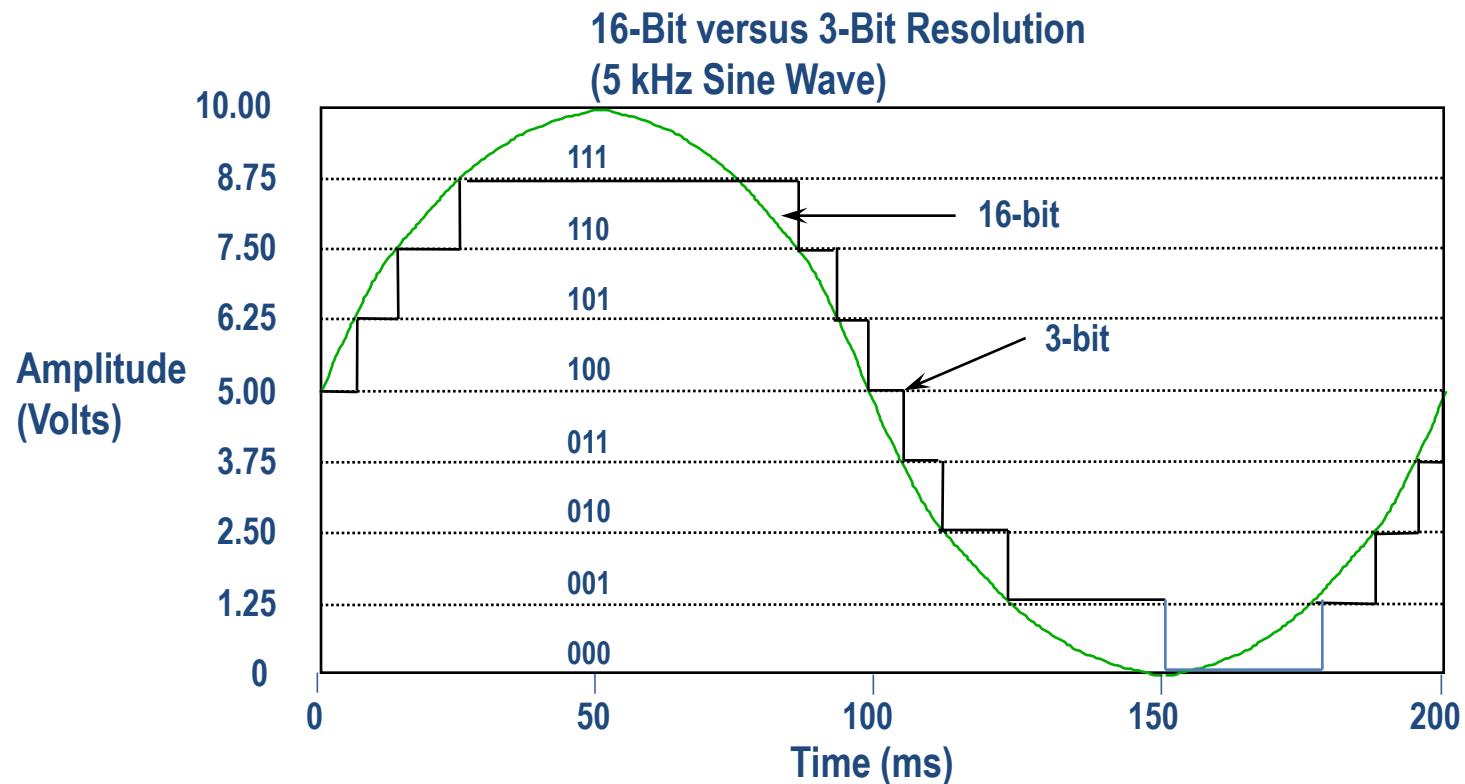
Analog I/O: Sampling Rates and Update Rates



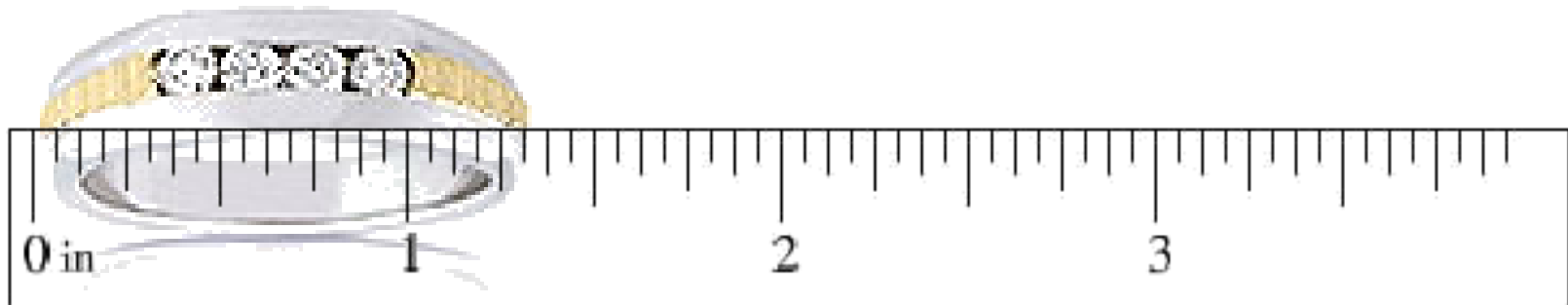
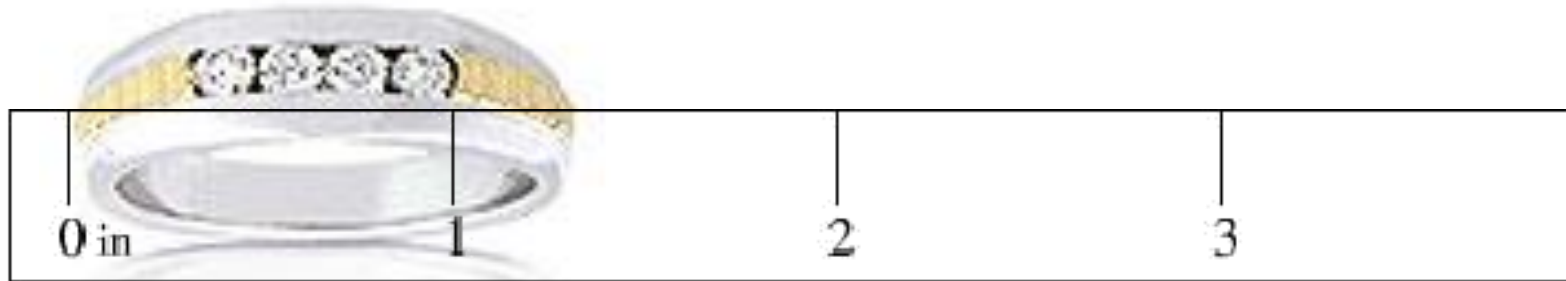
- Undersampling may result in the misrepresentation of the measured signal (aliasing).
- After a signal is aliased, it is impossible to reconstruct the original signal.
- Sample at least twice as fast as the highest frequency signal being measured.

Resolution

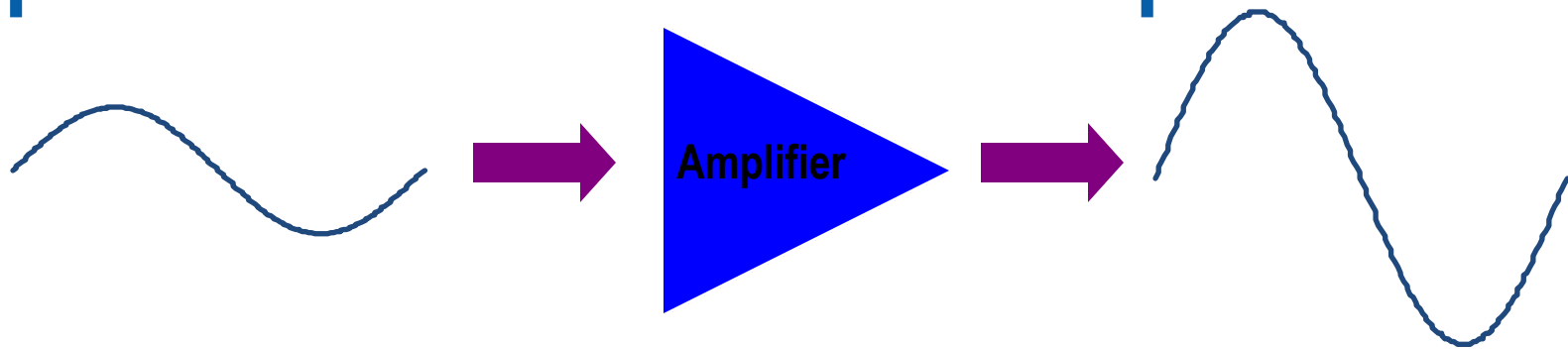
- Number of bits analog-to-digital converter (ADC) uses to represent a signal
- Higher resolution—Detect smaller voltage changes



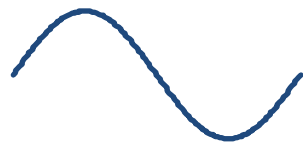
16-Bit versus 12-Bit Measurements



Optimize Resolution with Amplification



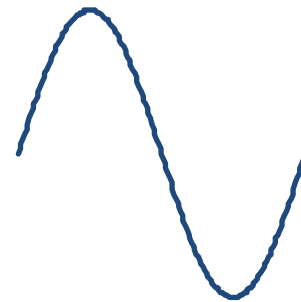
Optimizes Resolution over the Range of the Measurement



10 mV
signal

16-bit
Digitizer

32 levels
of resolution

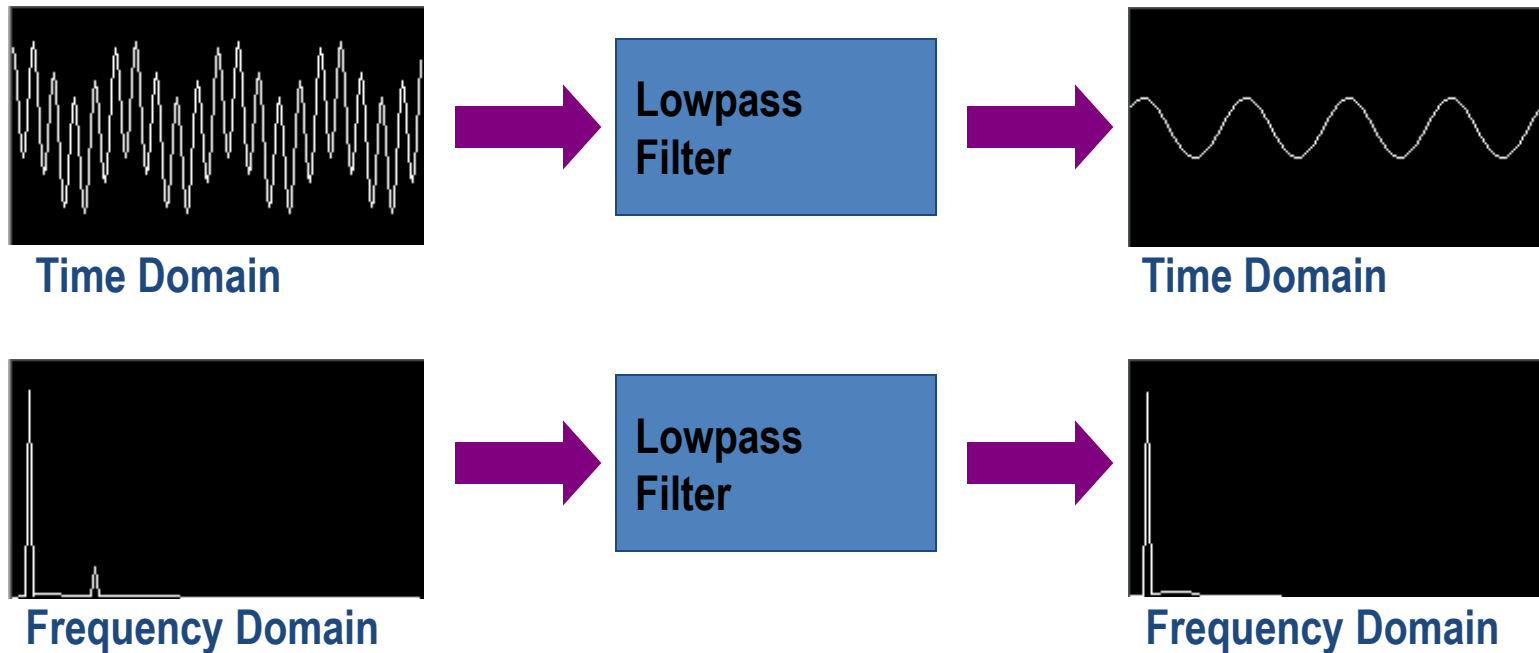


10 V
signal

16-bit
Digitizer

65,536 levels
of resolution

Use Lowpass Filters to Remove Noise

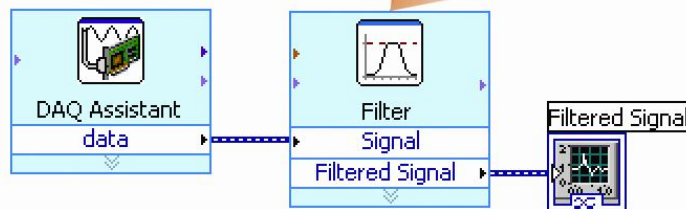
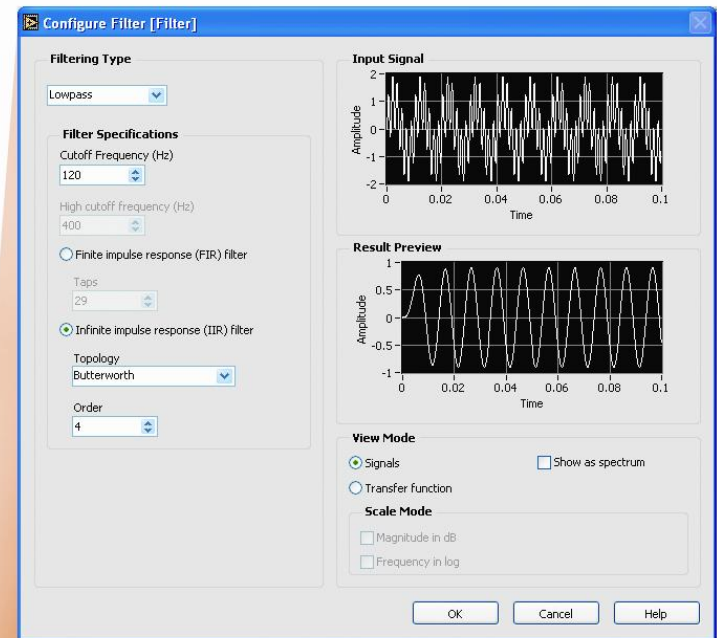


- Removes noise
- Blocks unwanted frequencies
- Prevents aliasing

Improve Filtering Flexibility with Digital Filters

Software (algorithmic) filters

- Change filter topology
- Change filter type (lowpass and so on)
- Change cutoff frequency
- Change filter order (number of poles)



Use a Combination of Analog and Digital Filters

- Analog filters prevent signal aliasing
- Circuit components dictate the type and frequency of the filter
- Digital filters complement analog filters by providing infinite “tunability”
- Digital filters consume processor time but they can be used post-acquisition

Signal Conditioning Provides Amplification and Filtering

Front-End Signal Conditioning

SCC



SCXI



Integrated Signal Conditioning



PXI Instruments



SC Series



FieldPoint



cDAQ

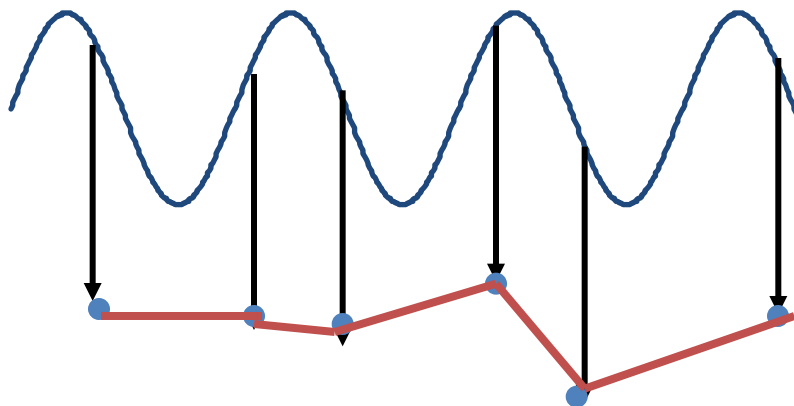
Signal Conditioning Inputs

- Low-level voltage signals (0–100 mV)
- High voltage signals (10–1,000 V)
- Sensors
 - Thermocouples
 - RTDs
 - Strain Gauges
 - Pressure Sensors
 - Accelerometers
 - Load Cells
 - LVDTs/ RVDTs
 - Resolvers



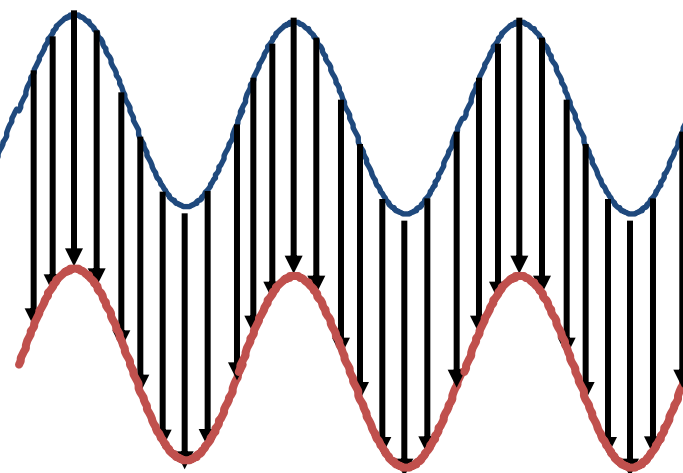
Hardware versus Software Timing

20 kHz Signal



**1 kS/s to 20 kS/s
varying by point**

**Arbitrary sampling rates,
point-by-point data**

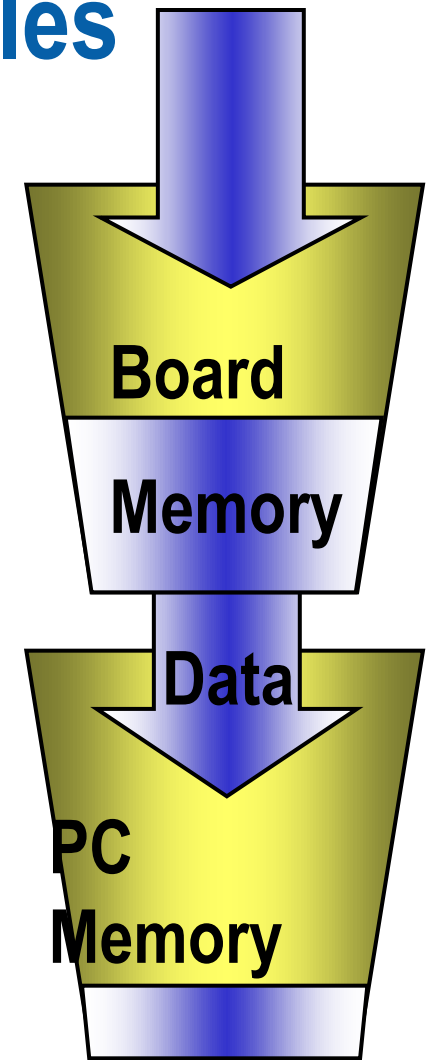


**0 to 200 kS/s
50 ns timing accuracy**

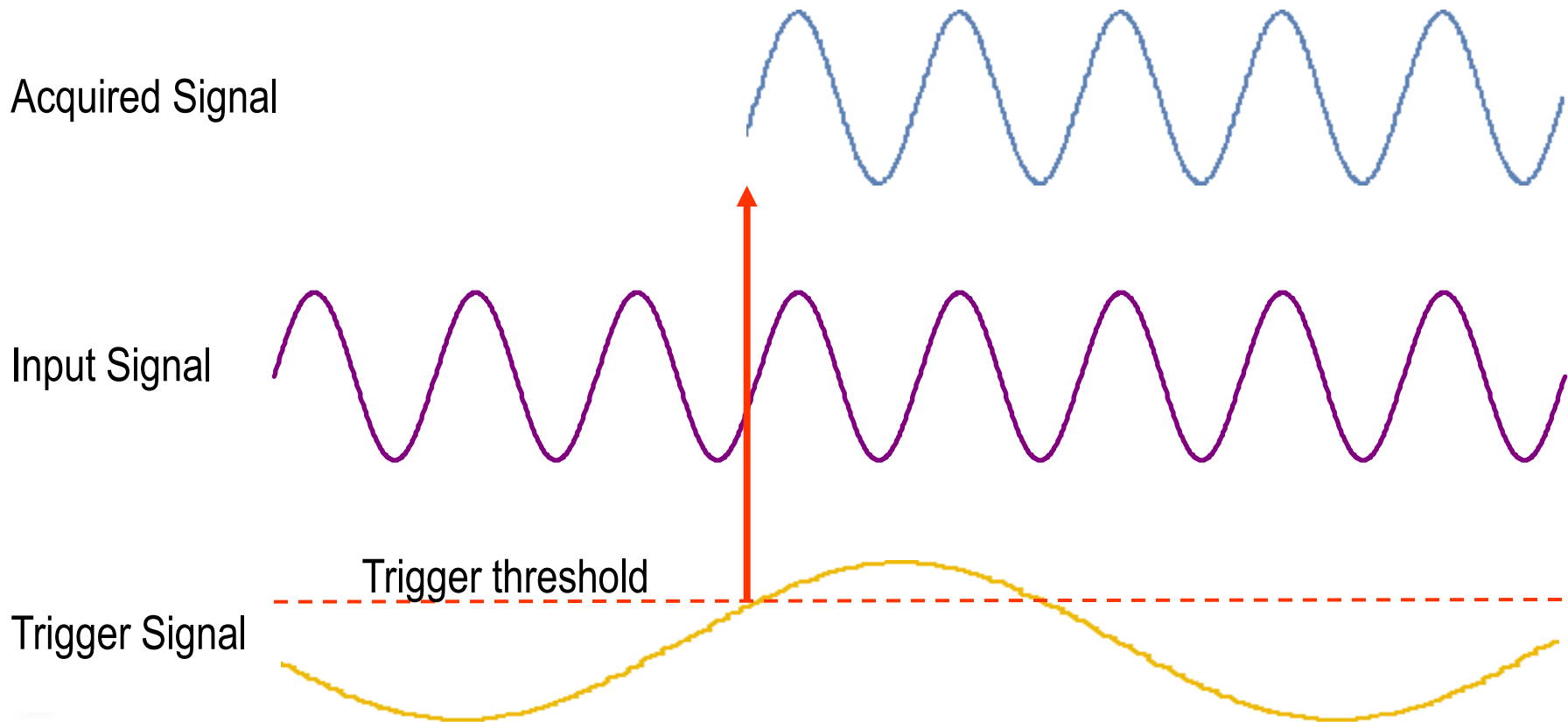
**Clocked sampling rate,
buffered data**

Using a Buffer to Acquire Samples

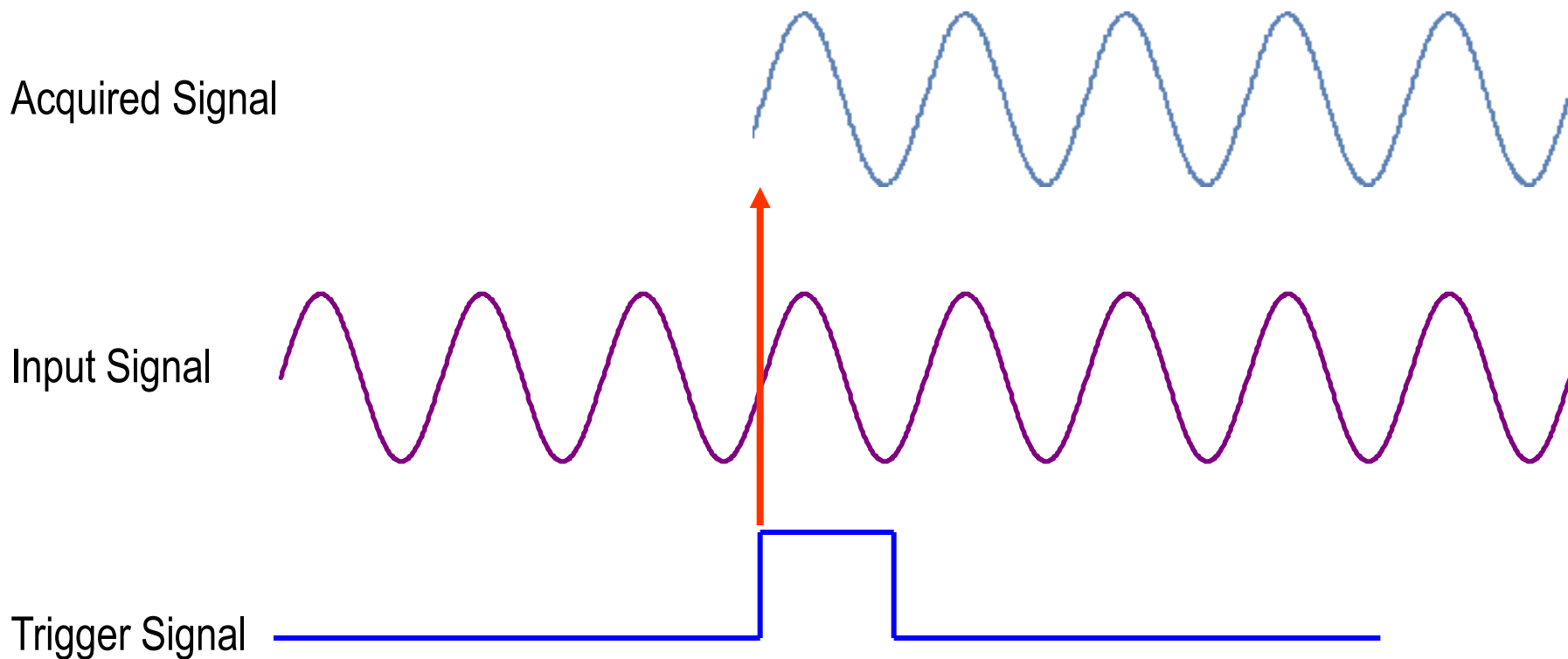
- Use in conjunction with hardware timing
- Continuous or finite length



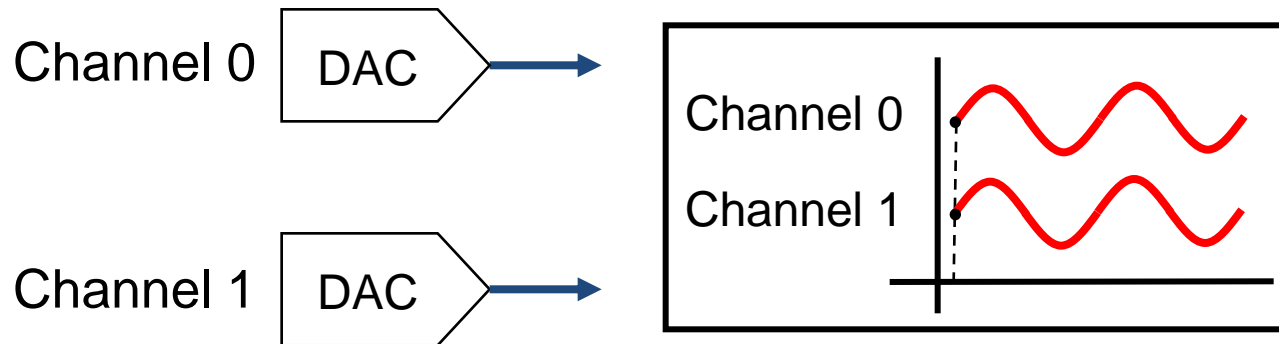
Analog Triggering



Digital Triggering



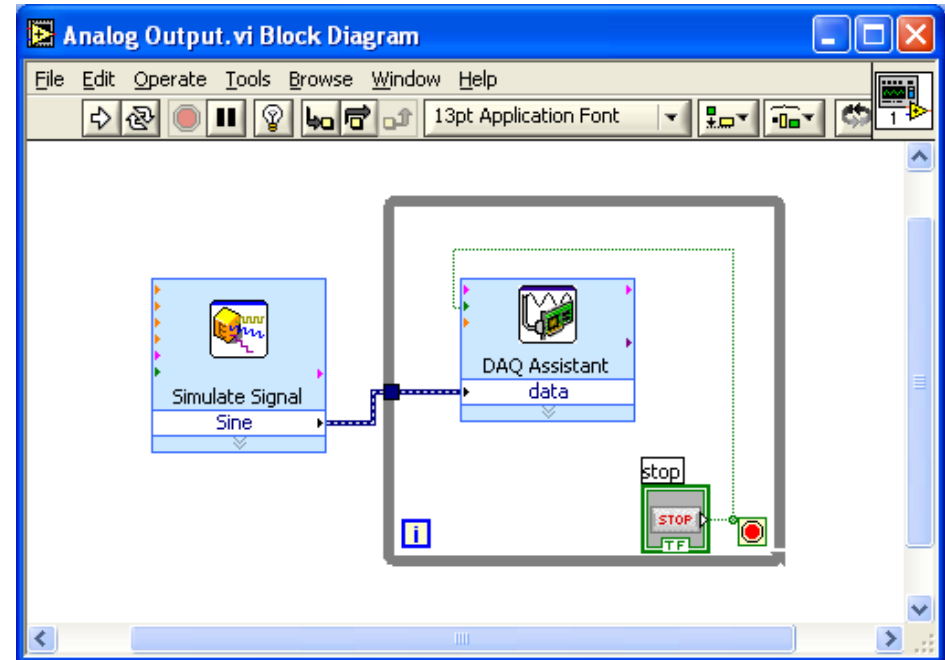
Analog Output



- Most Multifunction DAQ devices have a digital-to-analog converter (DAC) for each of their analog output channels
- DACs are updated simultaneously with the AO Sample Clock

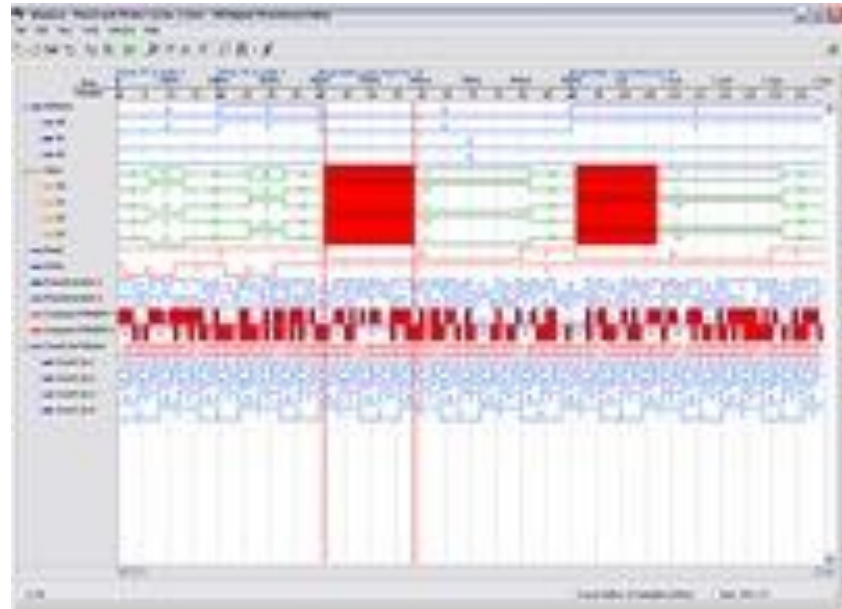
Waveform Generation

- Hardware time (clocked) buffered output
- Each channel can output independently timed waveforms
- Multiple AO operations can occur in parallel



Digital I/O

- DIO with Multifunction DAQ Devices
 - Static (software-timed) DIO
 - Eight or 32 lines
 - Add SCXI or SCC for isolation
- High Speed DIO
 - Dedicated digital devices
 - Up to 100 MHz clock rates
 - Up to 64 Mbits/ch onboard memory
 - Programmable voltage levels (–2.0 to 5.5 V)
- Industrial DIO
 - Up to 60 V ranges
 - Built-in bank or channel-channel isolation



Utilizing the Latest Technologies in DAQ



New Bus Technologies



Digital Isolators and Their Impact on Measurement Performance



Advanced Data Acquisition Techniques with Onboard FPGAs



Timing and Synchronization Technologies for Challenging Applications

Utilizing the Latest Technologies in DAQ



New Bus Technologies



Digital Isolators and Their Impact on Measurement Performance



Advanced Data Acquisition Techniques with Onboard FPGAs



Timing and Synchronization Technologies for Challenging Applications

The Convenience of USB

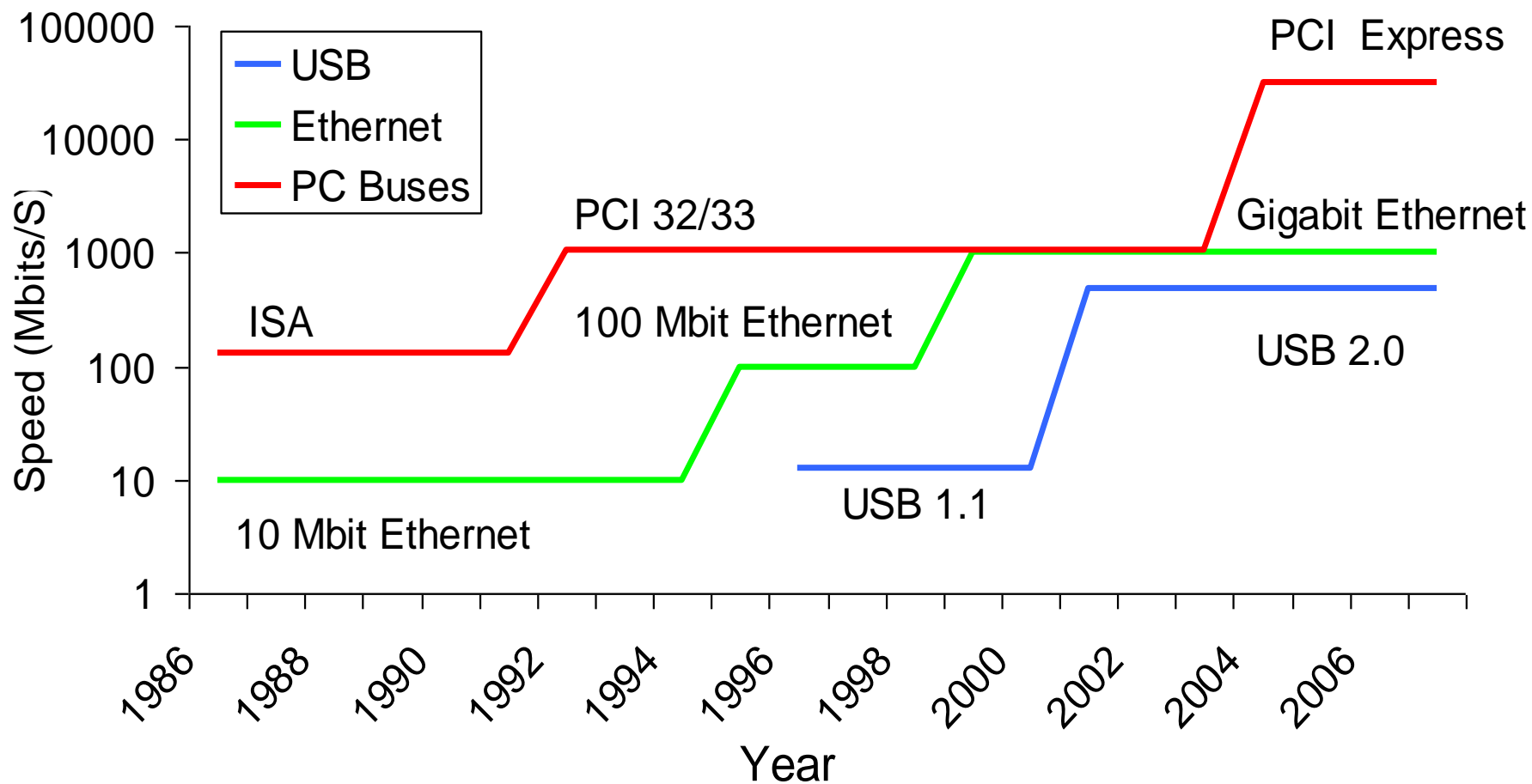
- **Simplicity**
 - Plug and play
- **Wide Adoption**
 - 2.1 billion USB devices by 2009¹
 - 4 USB ports per PC²



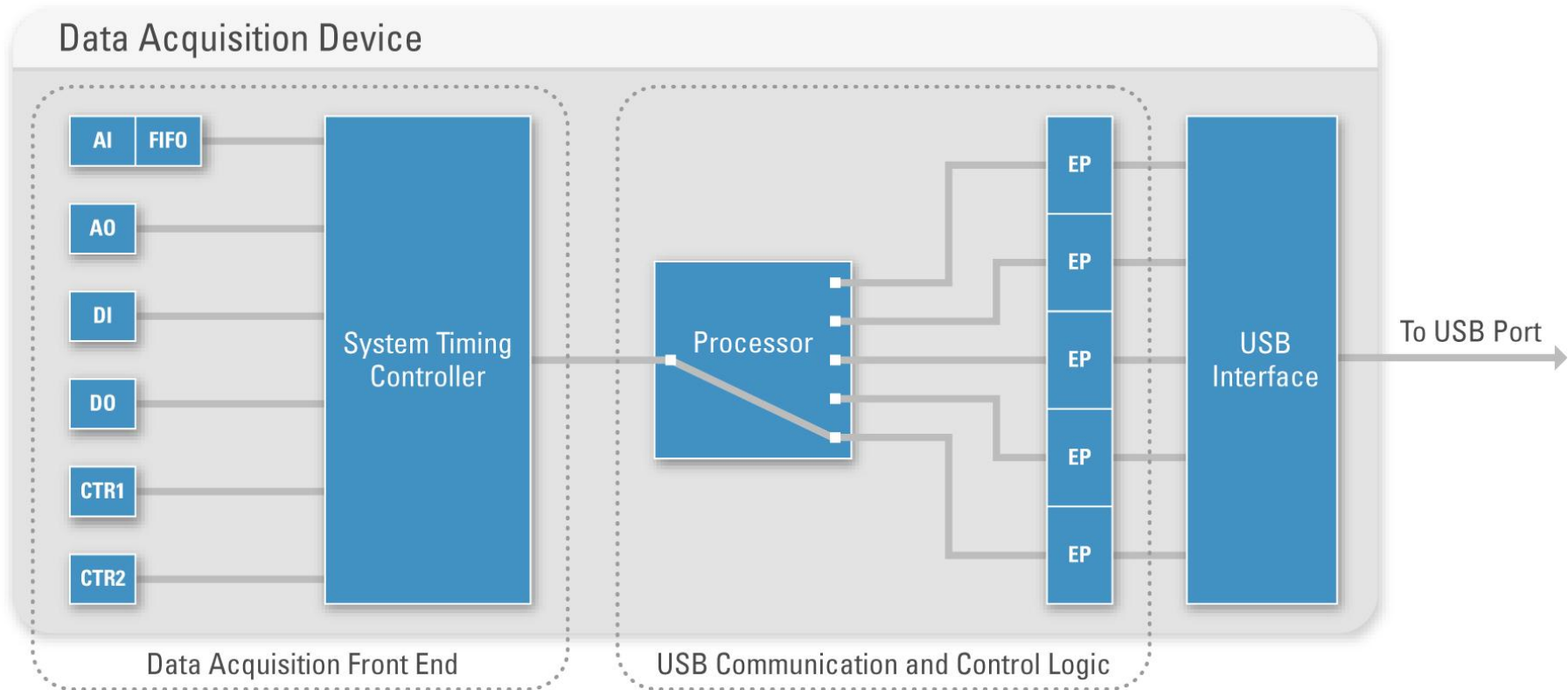
¹ Electronics.ca Research Network, Feb 2005

² PC Magazine.com, Dec 2005

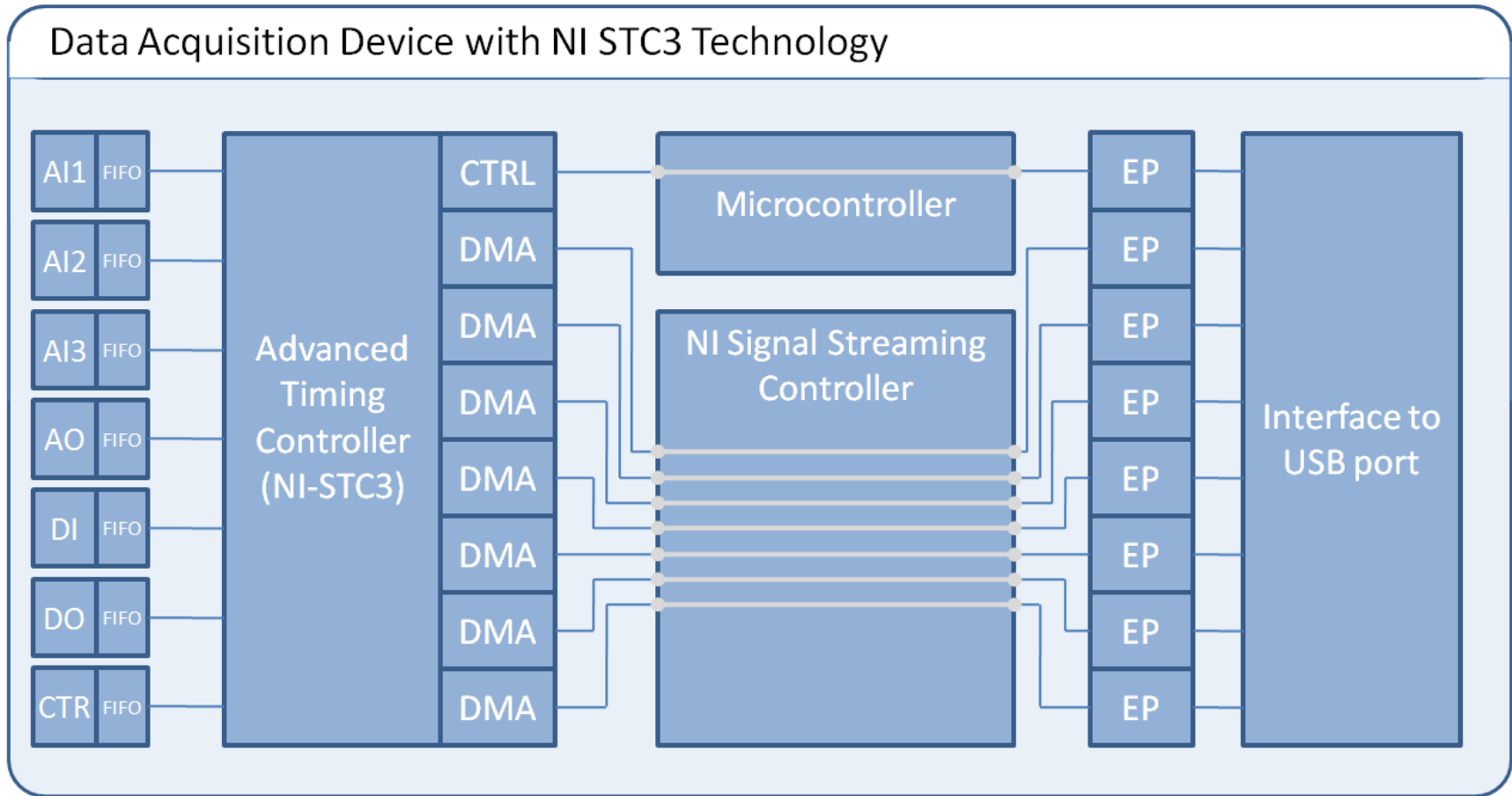
USB Evolution



Traditional USB DAQ Transfer Architecture



NI Signal Streaming Technology



Message Based Communication

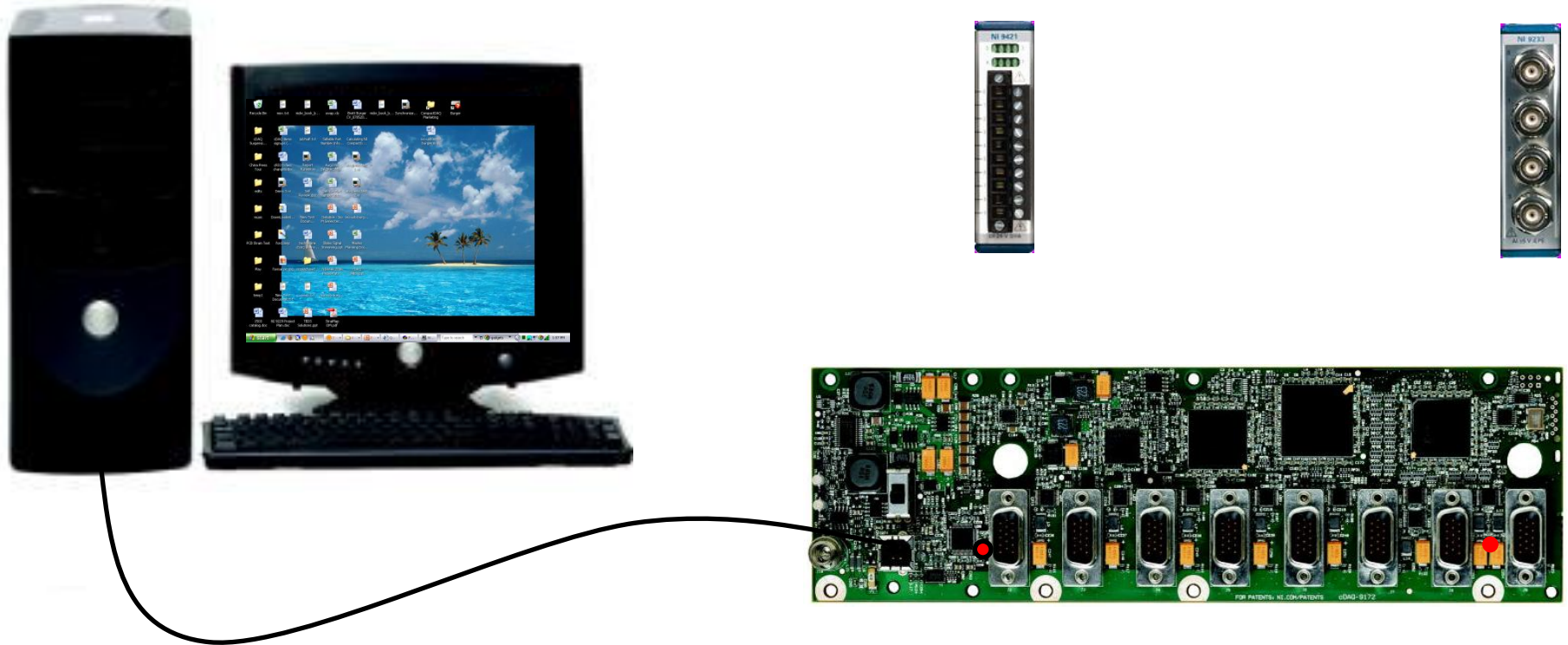
```
stc->AI_Mode_1.set_AI_CONVERT_Source_Polarity
stc->AI_Mode_1.set_AI_CONVERT_Source_Select
stc->AI_Mode_1.set_AI_SI_Source_Polarity
stc->AI_Mode_1.set_AI_SI_Source_Select
stc->AI_Mode_1.set_AI_Start_Stop
stc->AI_Mode_1.set_AI_Trigger_Once
stc->AI_Mode_1.set_AI_Trigger_Once
stc->AI_Mode_2.set_AI_SC_Initial_Load_Source
stc->AI_Mode_2.set_AI_SC_Reload_Mode
stc->AI_Mode_3.set_AI_Delayed_START1
stc->AI_Mode_3.set_AI_Delayed_START2
stc->AI_Mode_3.set_AI_External_Gate_Mode
stc->AI_Mode_3.set_AI_External_Gate_Polarity
stc->AI_Mode_3.set_AI_External_Gate_Select
stc->AI_Mode_3.set_AI_SI2_Source_Select
stc->AI_Personal.set_AI_EXTMUX_CLK_Pulse_Width
stc->AI_SC_Load_A.set
stc->AI_SC_Load_B.set
stc->AI_START_STOP_Select.set_AI_START_Edge
stc->AI_START_STOP_Select.set_AI_START_Polarity
stc->AI_START_STOP_Select.set_AI_START_Select
stc->AI_START_STOP_Select.set_AI_START_Sync
stc->AI_START_STOP_Select.set_AI_STOP_Edge
stc->AI_START_STOP_Select.set_AI_STOP_Polarity
stc->AI_START_STOP_Select.set_AI_STOP_Select
stc->AI_START_STOP_Select.set_AI_STOP_Sync
stc->AI_Trigger_Select.set_AI_START1_Edge
stc->AI_Trigger_Select.set_AI_START1_Polarity
stc->AI_Trigger_Select.set_AI_START1_Select
stc->AI_Trigger_Select.set_AI_START1_Sync
stc->AI_Trigger_Select.set_AI_START2_Edge
stc->AI_Trigger_Select.set_AI_START2_Polarity
stc->AI_Trigger_Select.set_AI_START2_Select
stc->AI_Trigger_Select.set_AI_START2_Sync
```



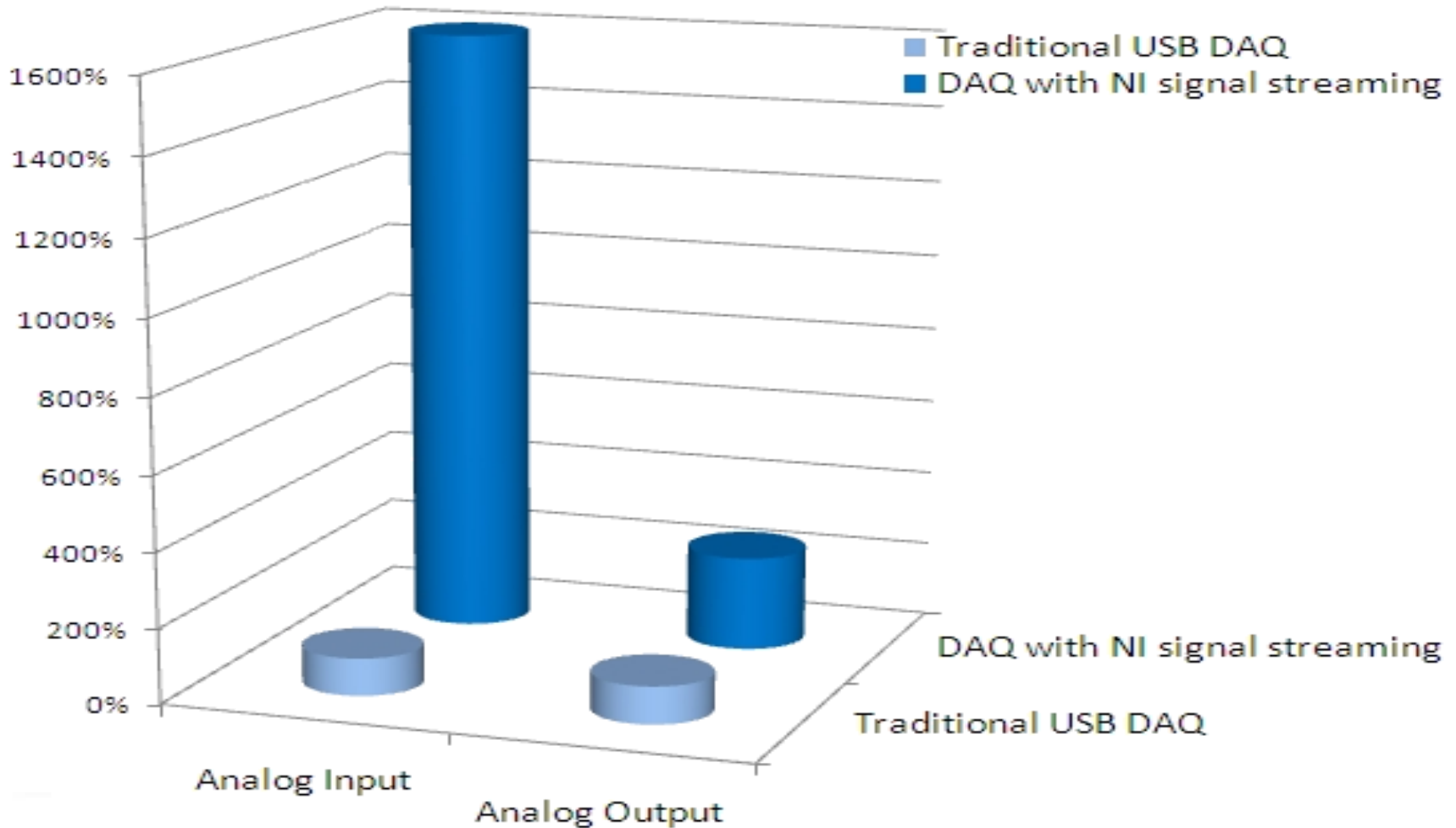
acquire.commit

Increased Device Intelligence

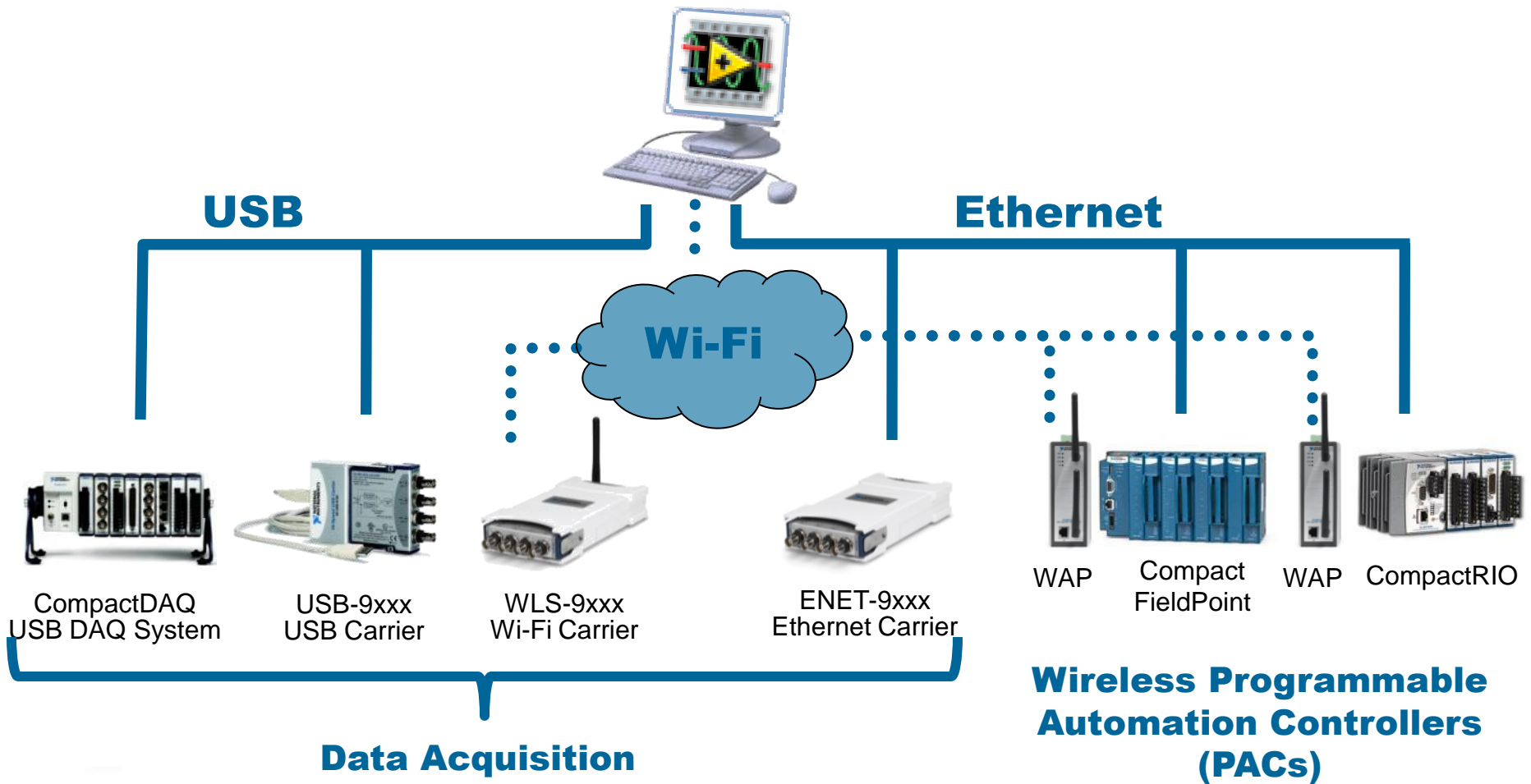
- Device contains element of driver



NI Signal Streaming Performance Improvement



Wireless: The Next Bus for Data Acquisition



NI Wi-Fi Data Acquisition

- NI-DAQmx driver software
- 10/100 Base-T/X Ethernet
- IEEE 802.11b/g radio
 - Easy to use
 - Secure (IEEE 802.11i)
 - High bandwidth
 - Established infrastructure



Wi-Fi: The Basics

Version	Released	Frequency	Max Rate	Range
802.11	1997	2.4 GHz	2 Mb/s	~30 m
802.11b	1999	2.4 GHz	11 Mb/s	30 m
802.11a	1999	5 GHz	54 Mb/s	10 m
802.11g	2003	2.4 GHz	54 Mb/s	30 m
802.11n	2009?	2.4 GHz	~540 Mb/s	~50 m

- 2.4GHz is an unlicensed band
 - You're competing with cordless phones, Wi-Fi hotspots, and microwaves
- 802.11b/g defines 11 channels to reduce interference

Wi-Fi Security

- Three levels of Wi-Fi security
 - WEP (not good)
 - WPA (better)
 - WPA2 (best, synonymous with IEEE 802.11i)
- The best wireless security has two key components
 - **Encryption** = data protection
 - **Authentication** = access control

Encryption

- TKIP = Temporal Key Integrity Protocol (WPA)
- AES = Advanced Encryption Standard (WPA2)
 - NIST-endorsed standard for government agencies
 - FIPS-approved (FIPS 197)

Key size (bits)	Number of alternative keys	Time required at 1 decryption/us	Time required at 10 ⁶ decryptions/us
32	$2^{32} = 4.3 \times 10^9$	35.8 minutes	2.15 milliseconds
56	$2^{56} = 7.2 \times 10^{16}$	1,142 years	10 hours
128	$2^{128} = 3.4 \times 10^{38}$	5.4×10^{24} years	5.4×10^{18} years

Time required for exhaustive key search (brute force attack)

<http://csrc.nist.gov/publications/fips/fips197/fips-197.pdf>

Authentication

- Three players in 802.11i authentication
 - Supplicant = client trying to access network (Wi-Fi DAQ)
 - Authenticator = WAP hardwired to secured network
 - Authentication Server = verifies identity of client



Supplicant



Authenticator



Authentication
Sever

Native x1 PCI Express Interface

- Dedicated bandwidth of up to 250 MB/s in each direction
- 8 DMA channels
- Software optimizations for low latency and single-point control applications



Utilizing the Latest Technologies in DAQ



New Bus Technologies



Digital Isolators and Their Impact on Measurement Performance



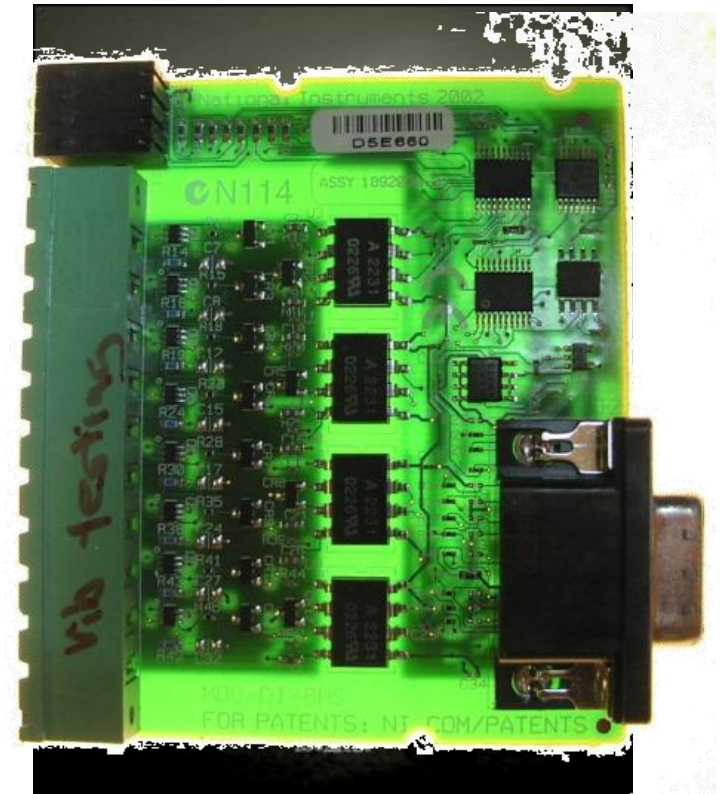
Advanced Data Acquisition Techniques with Onboard FPGAs



Timing and Synchronization Technologies for Challenging Applications

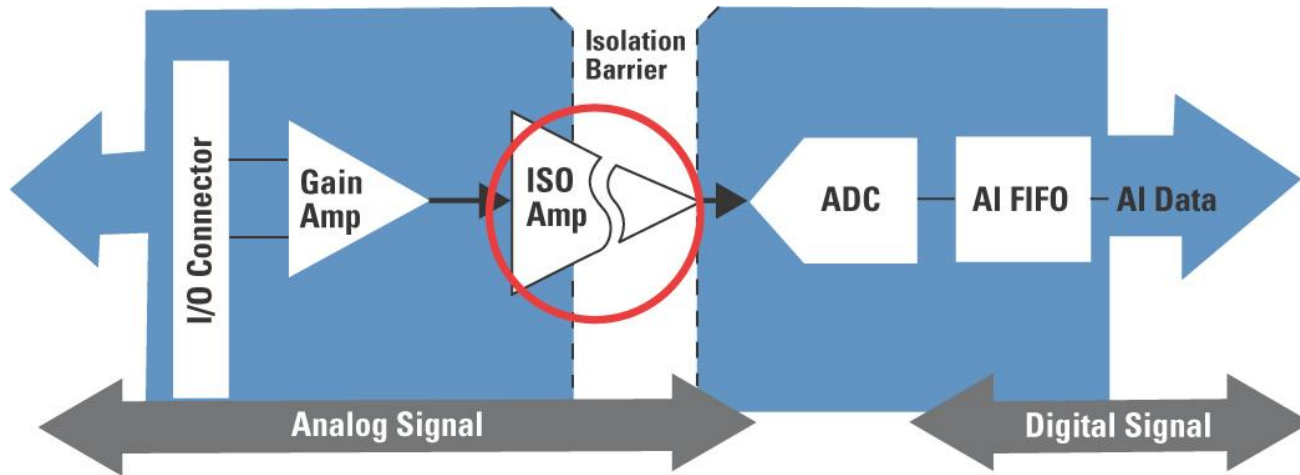
What is Isolation?

- No direct electrical connection between two or more circuits
- Floating from any other reference potential
- Separated from undesired influence of another circuit
- A.K.A. Not “Touching”

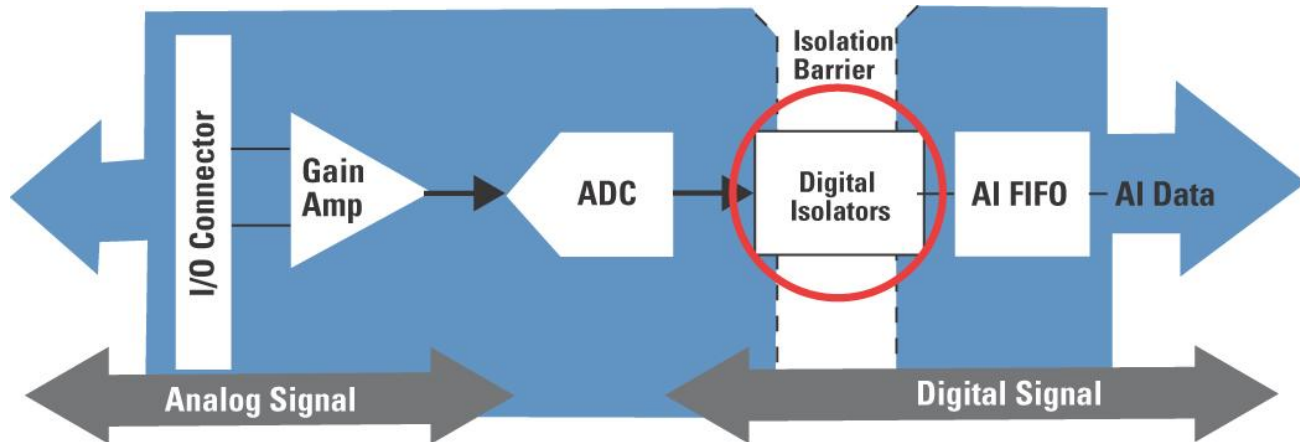


Types of Isolation

Analog Isolation

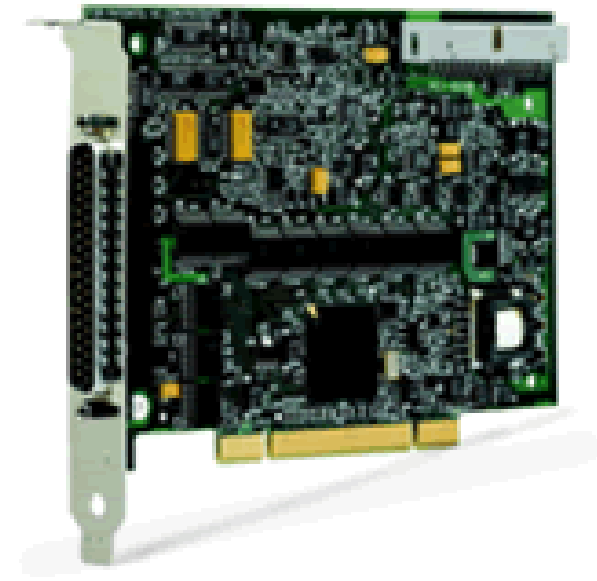


Digital Isolation



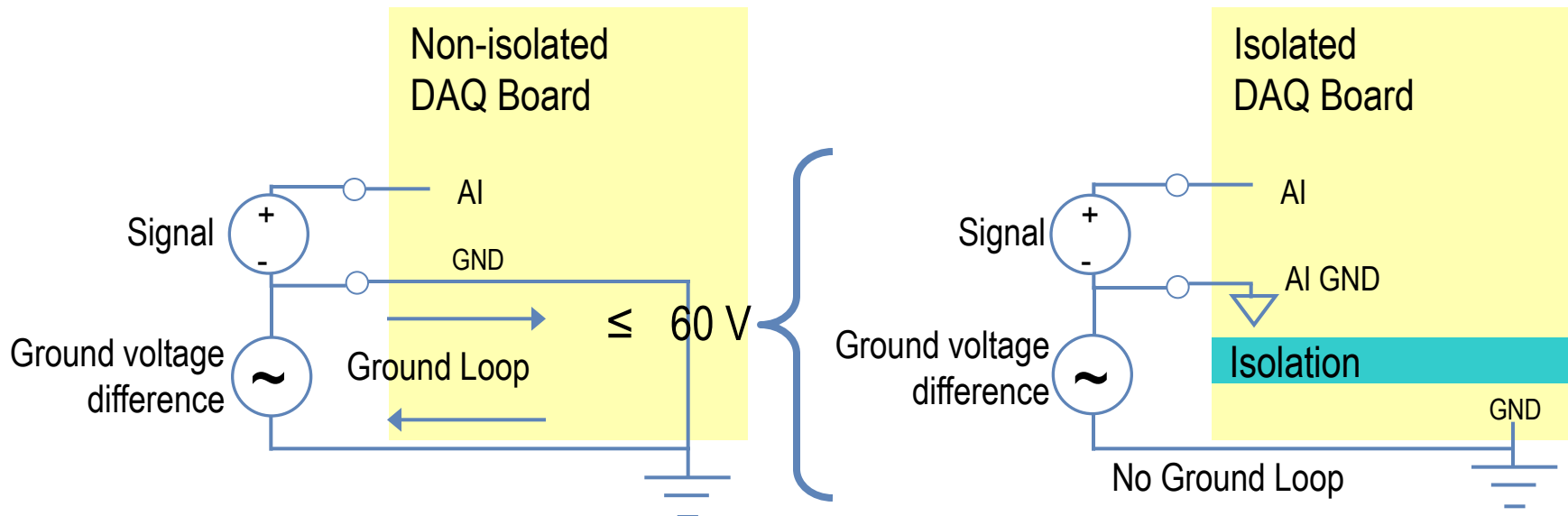
Benefits of Isolation

- Accuracy
 - Eliminates ground loops
 - Rejects common mode voltage
- Safety
 - Protection from voltage spikes
 - Tested and certified
- Simplicity
 - 0 to 20 mA I/O, 24 V DIO
 - No need for external conditioning



Accuracy: Eliminates Ground Loop

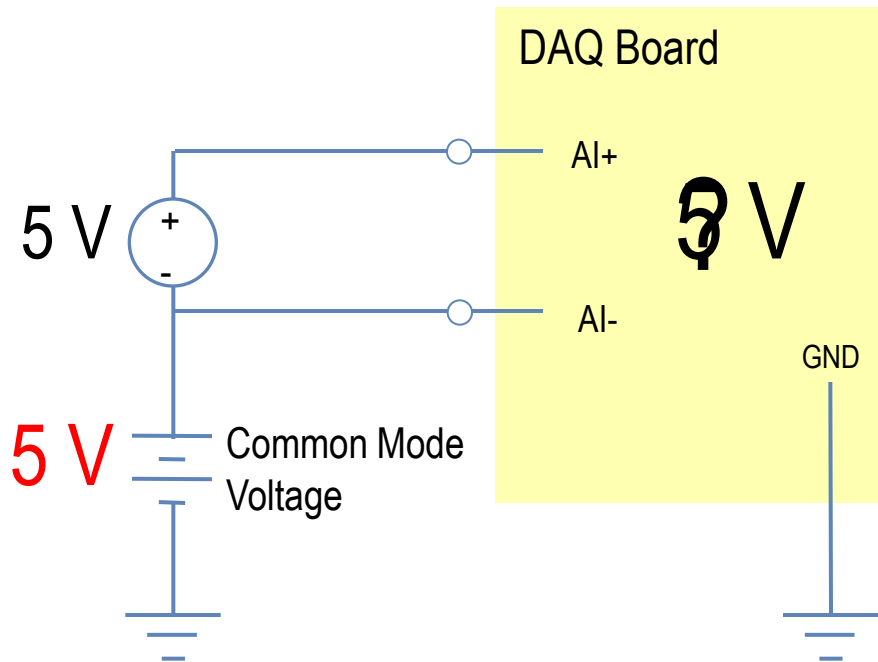
- Common problem with single ended measurements
- Cause - Difference in ground potentials
- Differential – only good for under +/- 10 VDC



Accuracy: Common Mode Voltage Rejection

- Voltage common to both the + and - channels

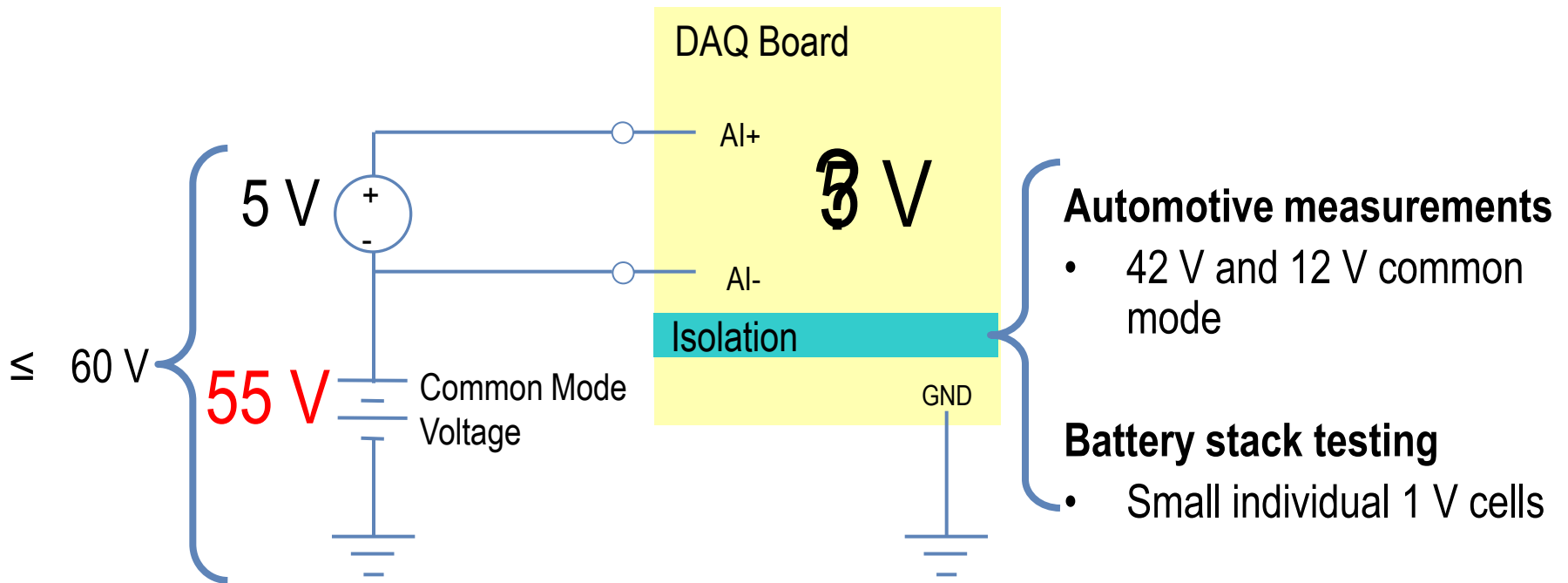
What will a non-isolated M Series board read?



Accuracy: Common Mode Voltage Rejection

- Voltage common to both the + and - channels

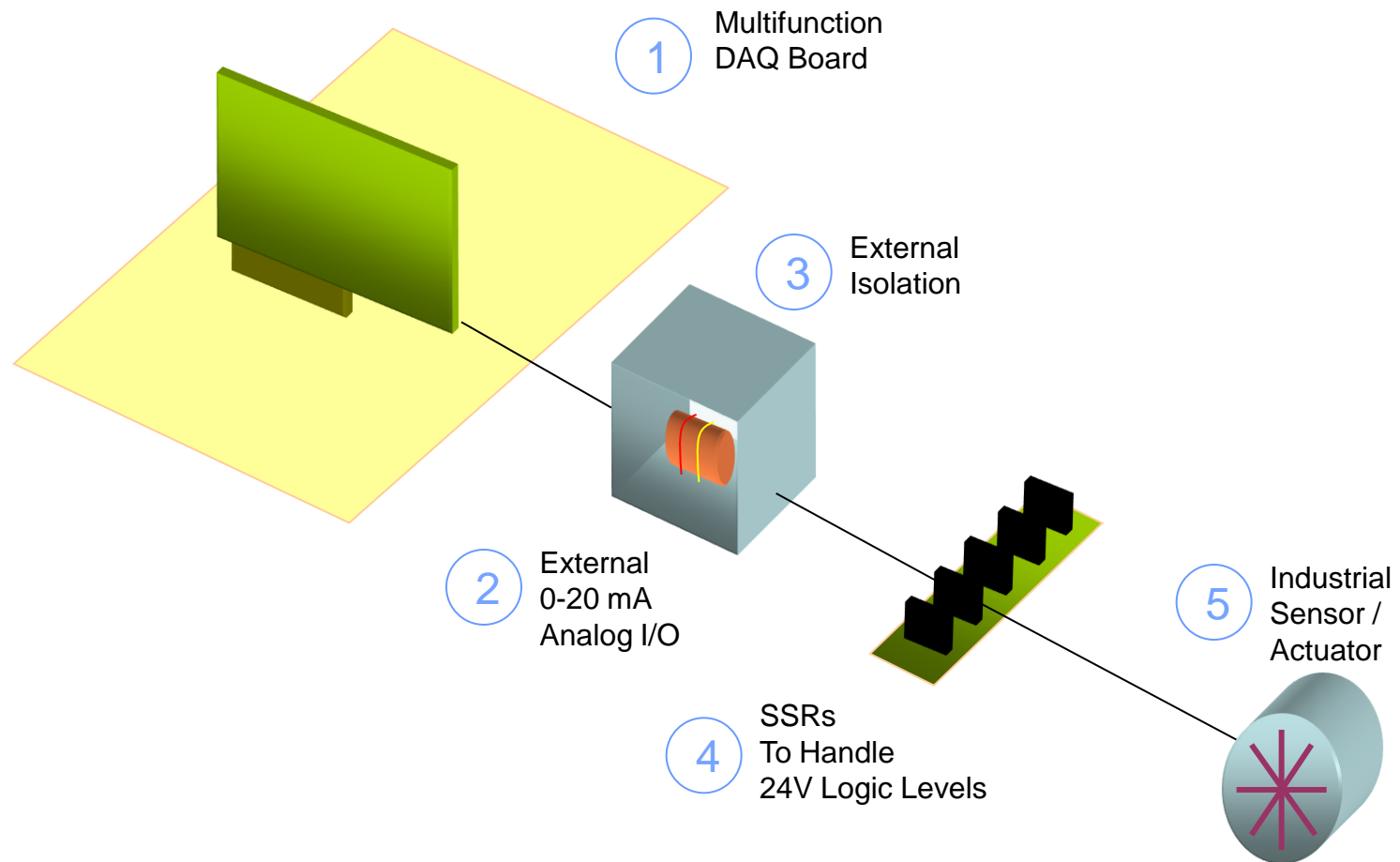
Isolated DAQs will reject the common mode voltage and we read 5 V



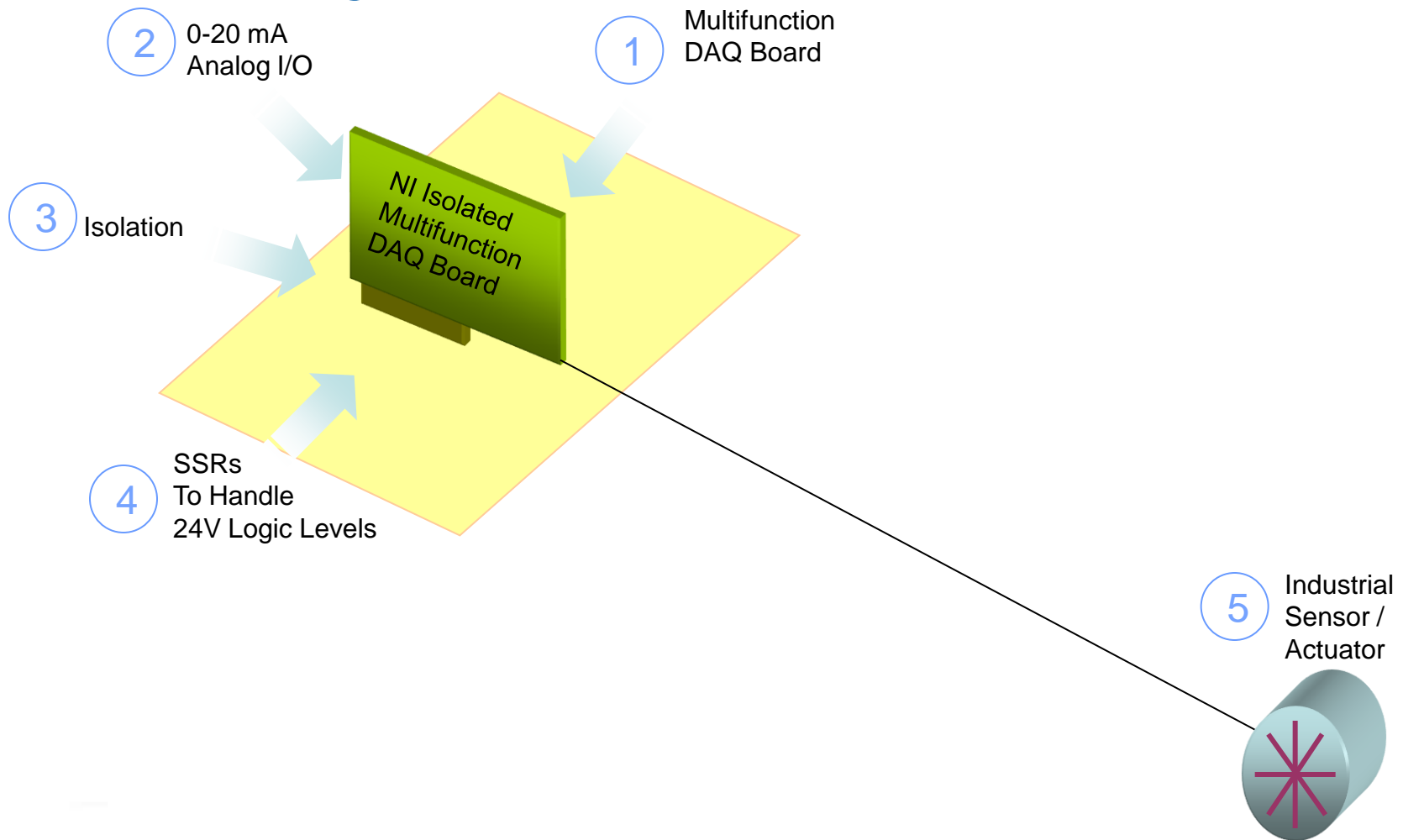
Signal + Common mode = ± 60 VDC

Signal = ± 10 V (same as the non-isolated M Series)

Simplicity



Simplicity



Safety from Hazardous Voltages

- Protection for user, data and equipment from transients
 - Isolated M and S Series: 1400 Vrms / 1950 VDC for up to 5 sec
- Applications
 - Factory floor, production lines, process control where high voltage and transient signals are common
 - Proximity to large motors or wall power lines
 - Medical equipment
 - University Labs



Utilizing the Latest Technologies in DAQ



New Bus Technologies



Digital Isolators and Their Impact on Measurement Performance



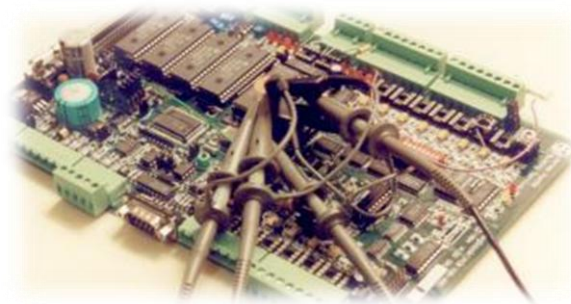
Advanced Data Acquisition Techniques with Onboard FPGAs



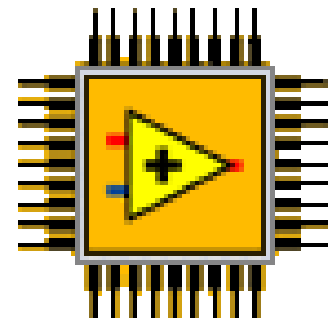
Timing and Synchronization Technologies for Challenging Applications

Applications Requiring Custom Hardware

- Custom data acquisition
- Digital communication protocols
- Decision making in hardware
- Control over 40 kHz
- Sensor level signal processing

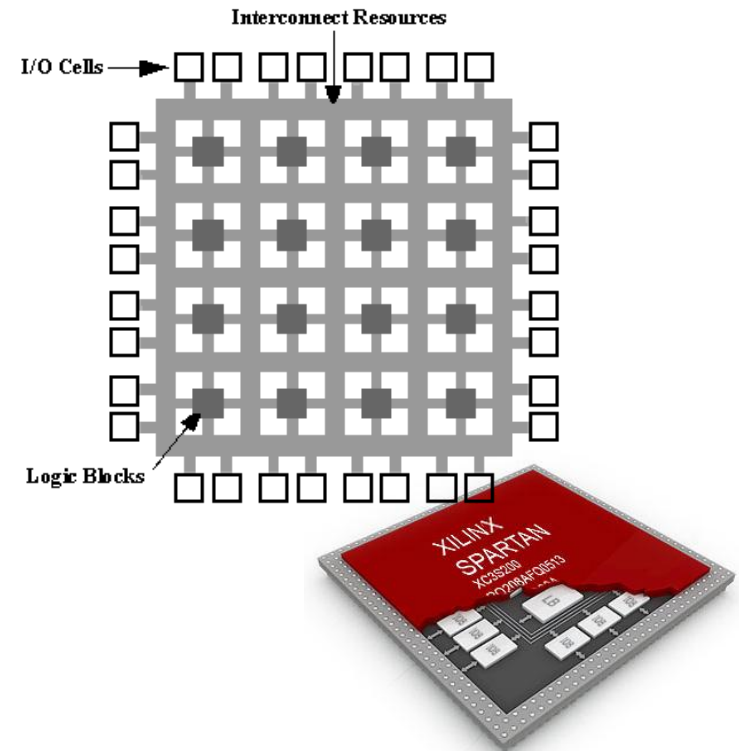


OR



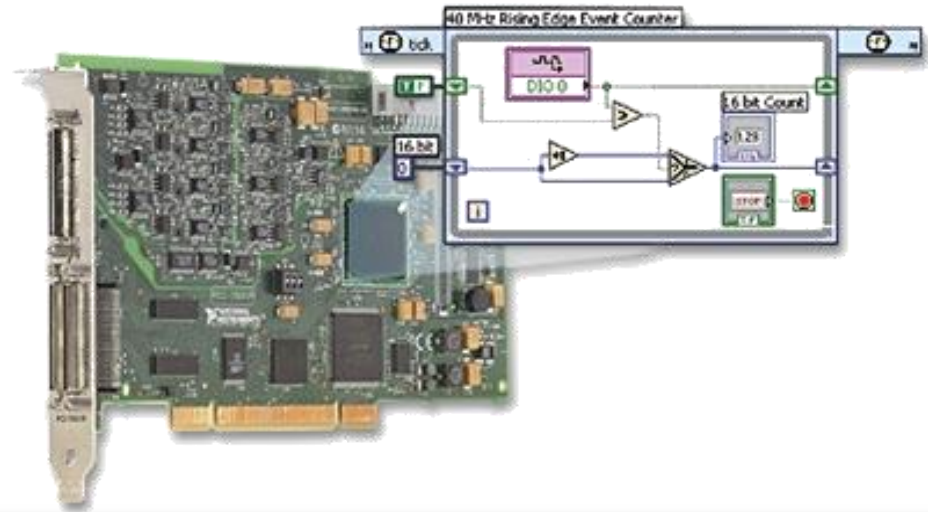
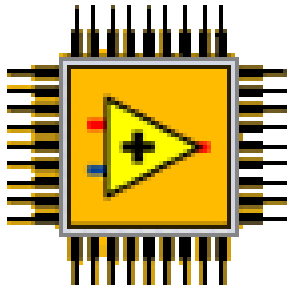
Benefits of FPGAs

- 👍 Massively parallel
- 👍 Reconfigurable
- 👍 Digital signal processing
- 👍 High-speed control
- 👍 Faster time to market
- 👎 Typically require digital design expertise

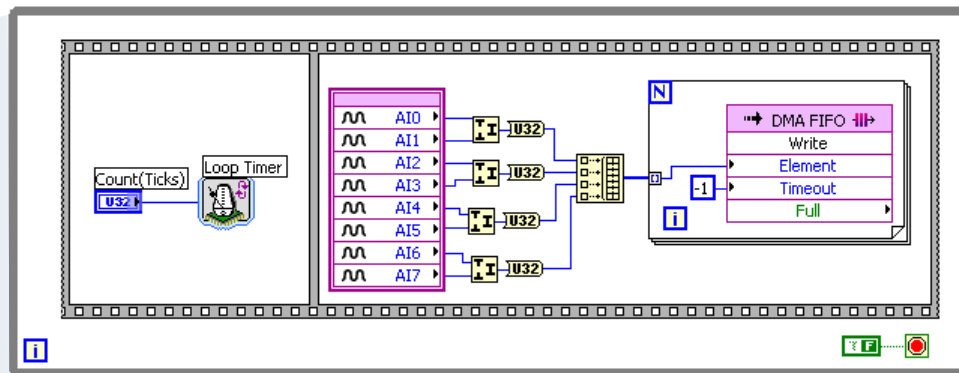
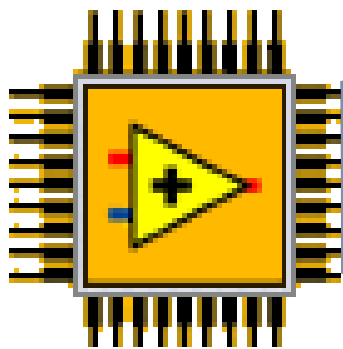
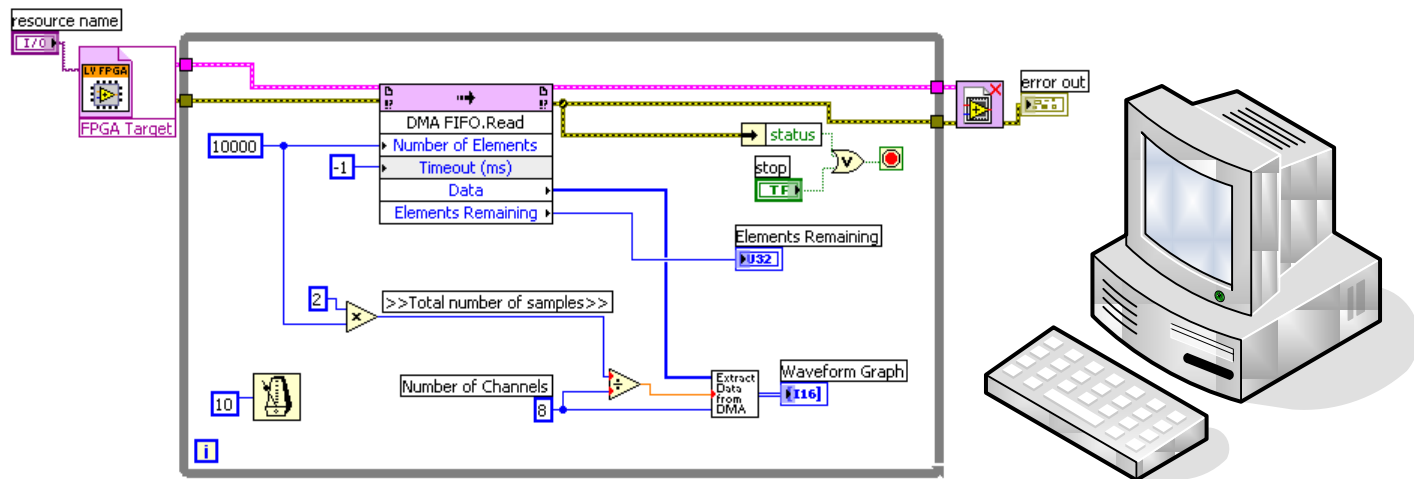


Reconfigurable Intelligent DAQ

- FPGA-based I/O timing
- User-defined onboard processing
- Hardware-timed speed and reliability

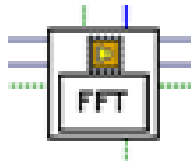


LabVIEW FPGA Module

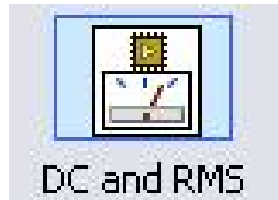


Intellectual Property (IP)

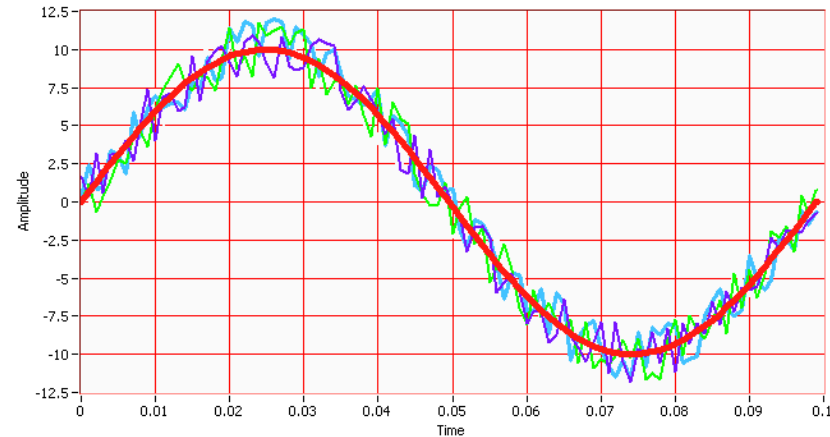
FFT



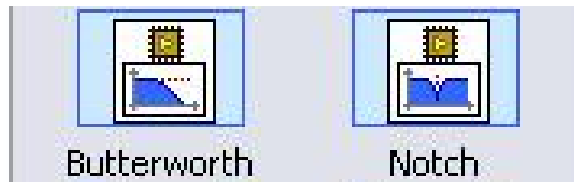
DC/RMS



Waveform Averaging

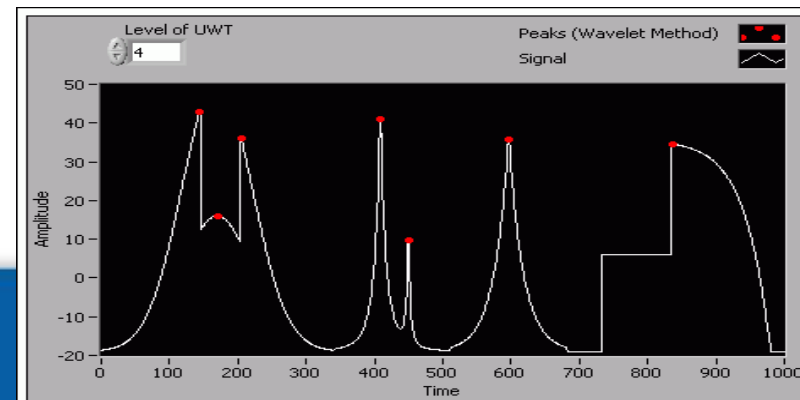


Digital filtering



Windowing

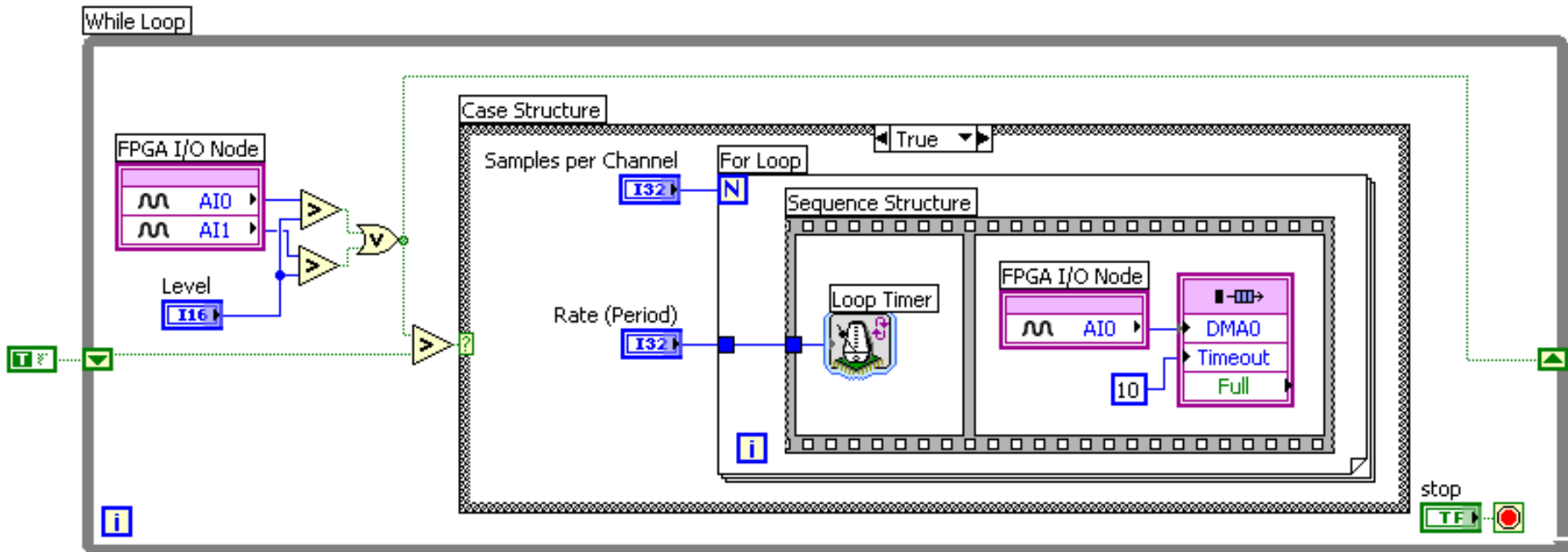
Resampling



Typical MIO DAQ vs. Intelligent DAQ

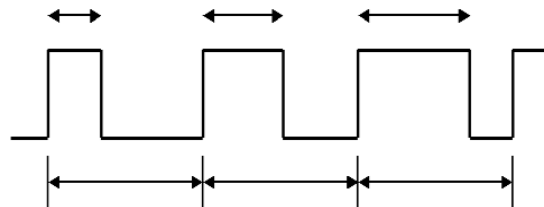
I/O Control	Fixed ASIC for timing and triggering	↔	Open FPGA for timing and triggering
Analog I/O	Multiplexed, shared sample clock	↔	Simultaneous or independent operation
Digital I/O	Up to 32 lines, Correlated DIO	↔	Up to 160 lines, hardware timed
Onboard Counters	2 general purpose counters	↔	Custom counters on any digital line

Custom Triggered Analog Input With Intelligent DAQ



Intelligent DAQ Applications

- Custom timing/triggering
- Ultra-high speed control
- Sensor simulation
- Hardware-in-the-loop test
- Specialized communication protocols

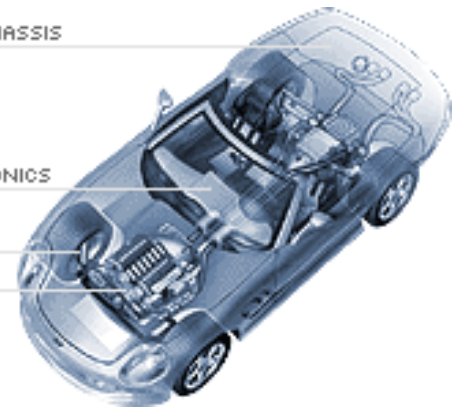


BODY AND CHASSIS

AUTO ELECTRONICS

SAFETY

POWER TRAIN



Utilizing the Latest Technologies in DAQ



New Bus Technologies



Digital Isolators and Their Impact on Measurement Performance



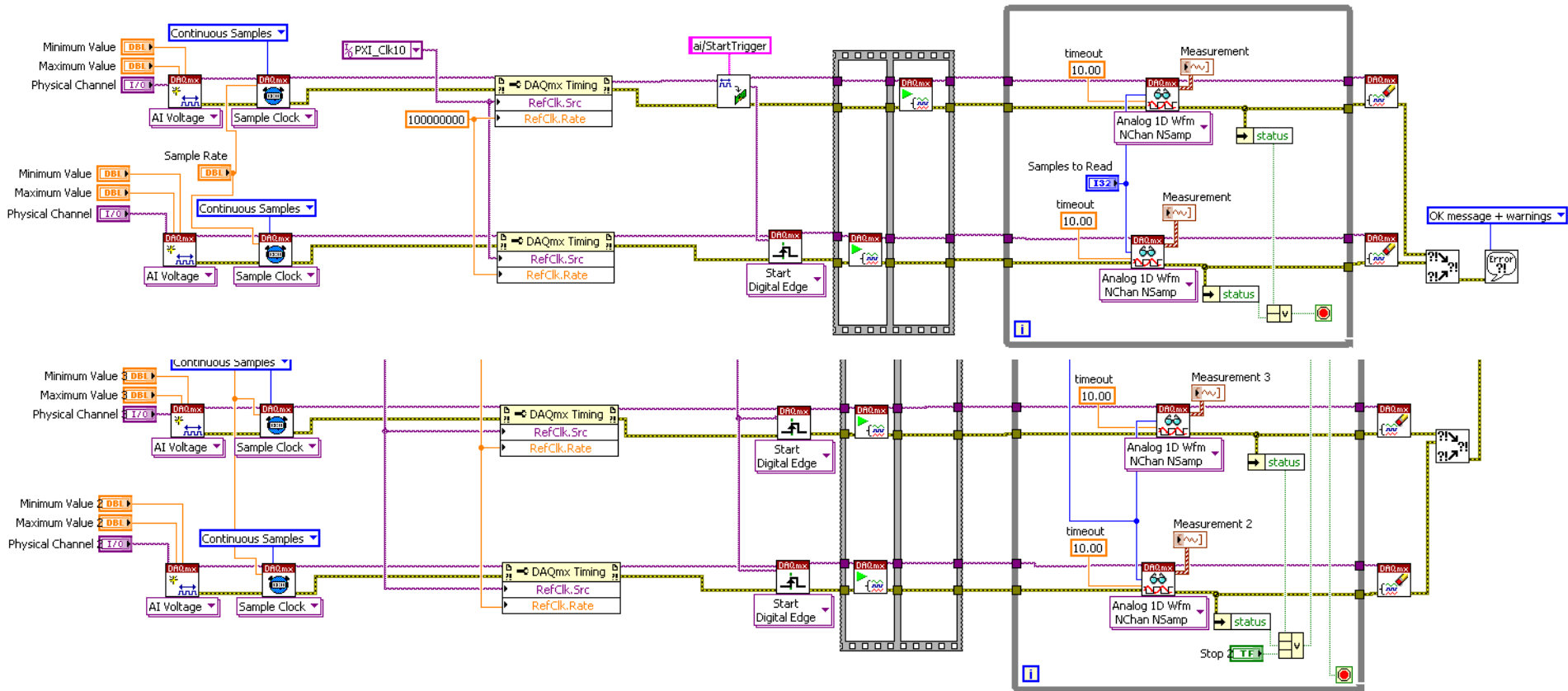
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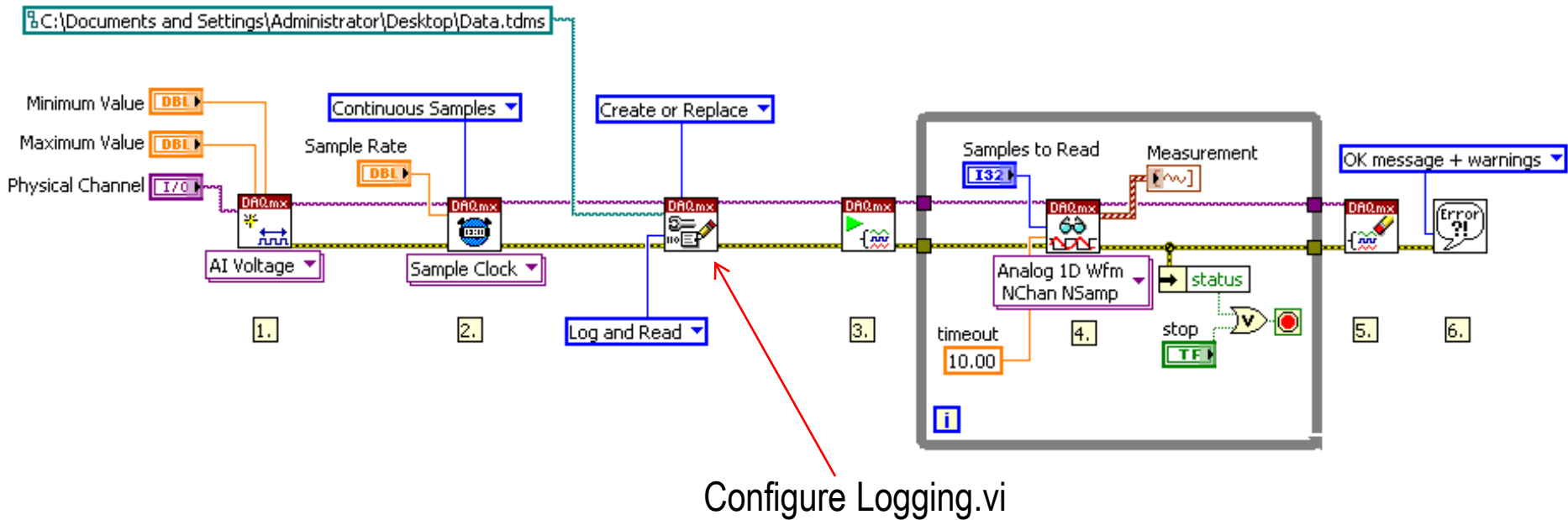
Timing and Synchronization Technologies for Challenging Applications

Synchronizing Multiple Devices

M Series



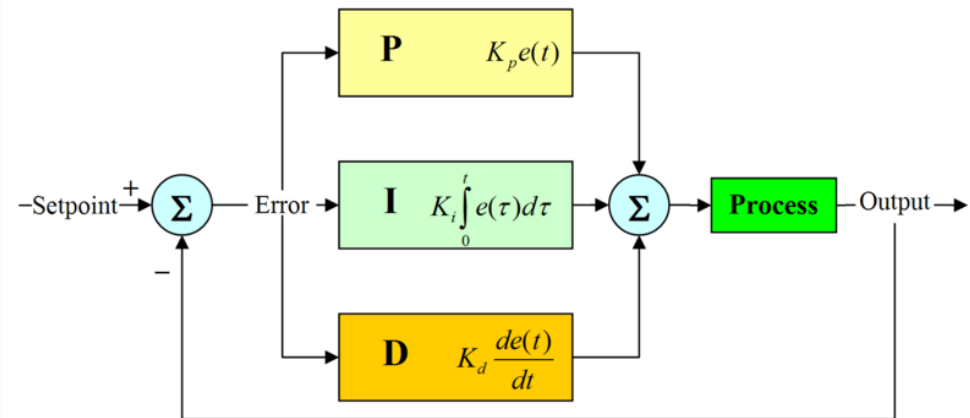
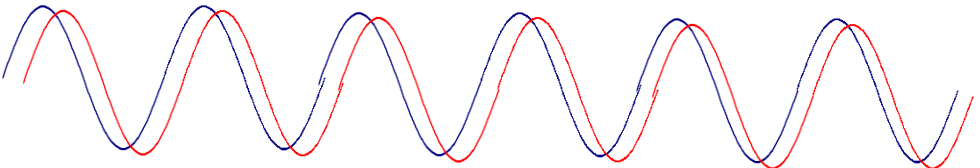
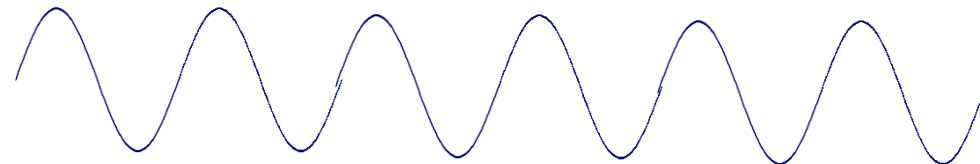
Multidevice Acquisition AND Logging



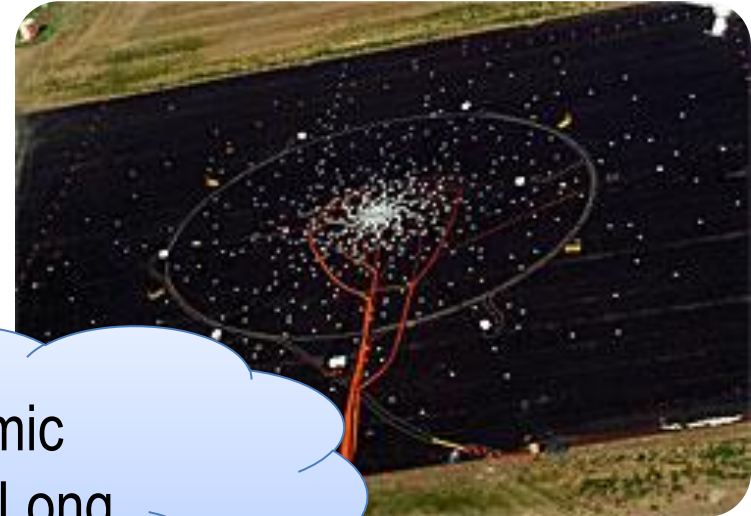
The **easiest AND fastest** way to log acquired data to disk

Importance of Timing in Test, Measurement and Control

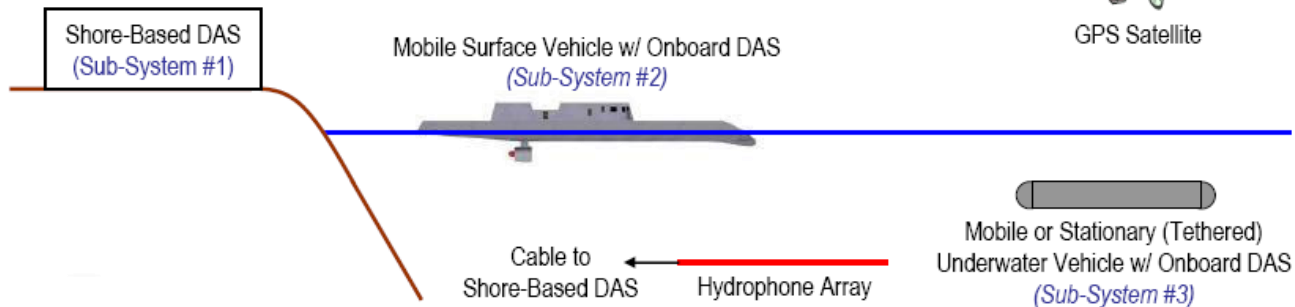
- Trending
 - Allows interpolation
 - Graph vs histogram
 - DMM vs Digitizer
- Correlation
 - Relating two events to one another
 - Phase
- Controllability
 - Timing of control loops
 - Determinism
- Simulation Capability
 - Timing is inherent to a simulation



The Challenge

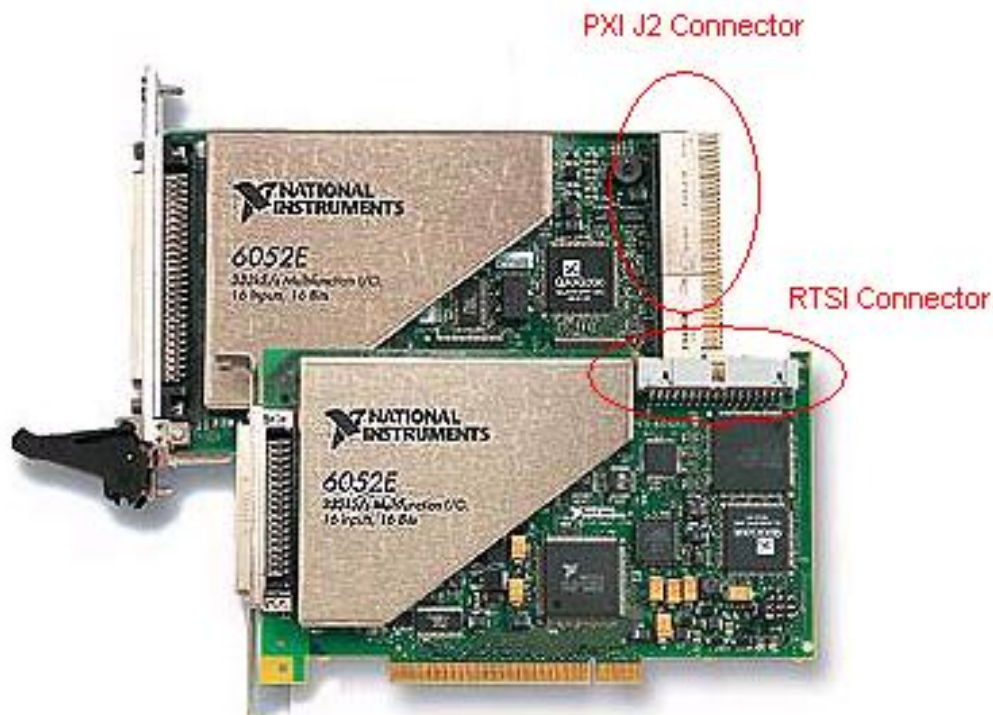


Synchronize Dynamic Measurements Over Long Distances



RTSI and the PXI Trigger Bus

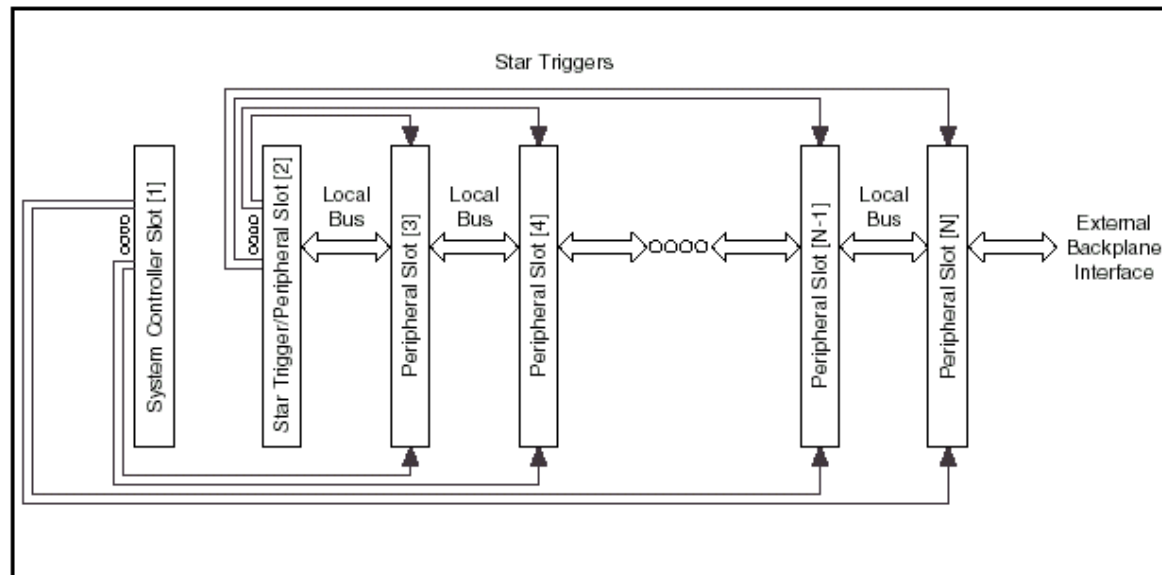
RTSI	PXI
RTSI 0	PXI_Trig0
RTSI 1	PXI_Trig1
RTSI 2	PXI_Trig2
RTSI 3	PXI_Trig3
RTSI 4	PXI_Trig4
RTSI 5	PXI_Trig5
RTSI 6	PXI_Star
RTSI Clock	PXI_Trig7



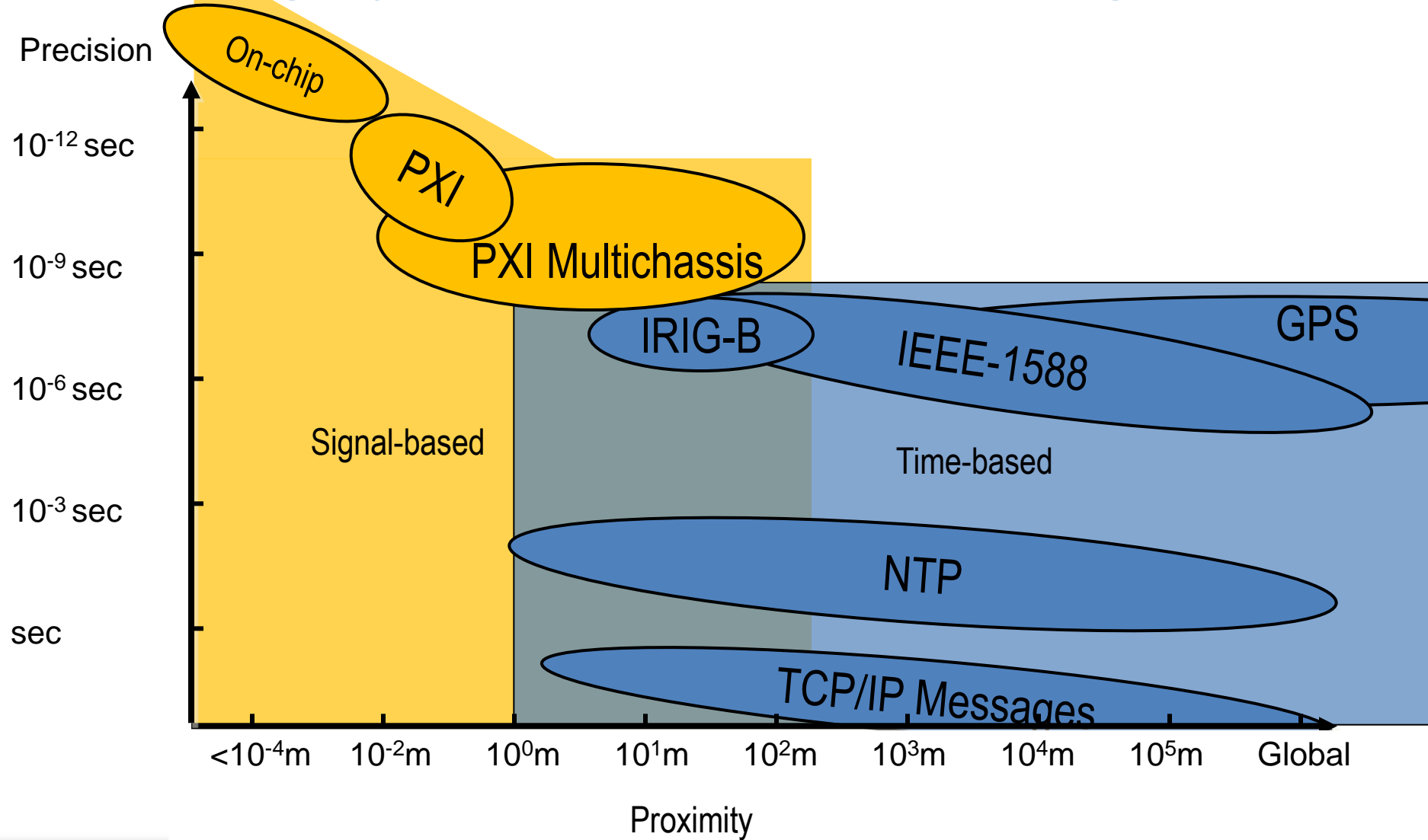
- Direct mapping of RTSI signals to PXI Backplane Connector (J2), no ribbon cable needed

Considerations for Distance and Delay

- Delay of a signal is proportional to the distance it has to travel
- Star triggers are designed so all trigger signals have the same delay (<1 ns, <150ps)

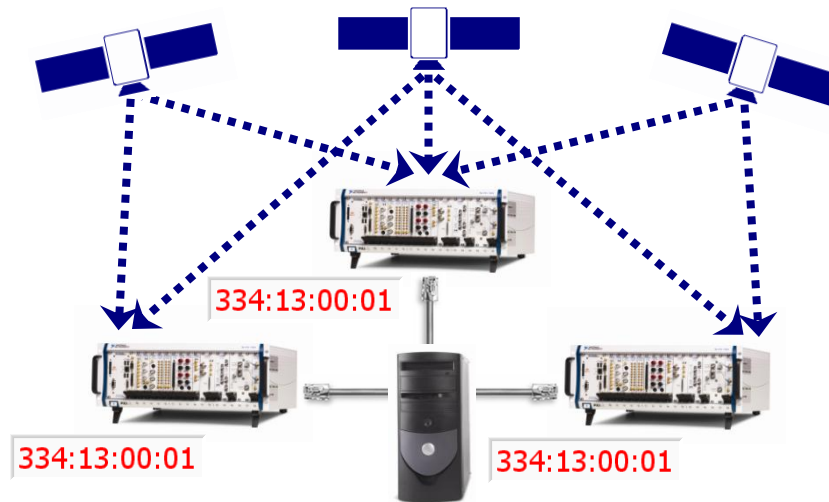


Comparing Synchronization Technologies



Global Positioning System (GPS)

- Satellite constellation completed in March 1994 ⁽¹⁾
- Globally-available
- Time synchronization between 10's and 100's of ns
- Can be used to calculate position within meters



(1) Source: Trimble <http://www.trimble.com/gps/howgps-positions.shtml#0>

IRIG

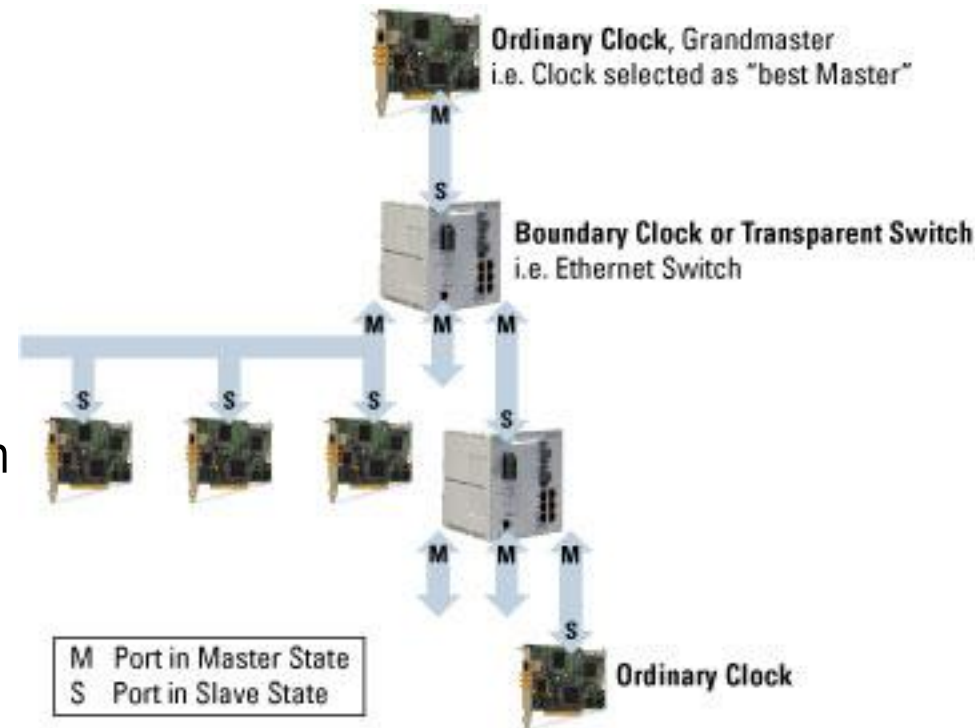
- Inter-Range Instrumentation Group time codes
- AM or DC method of encoding a time reference
- Encoding/Decoding precision in the 10's of ns

NTP

- Network Time Protocol
- Ethernet-based synchronization using standard NICs
- Provides synchronization in the ms

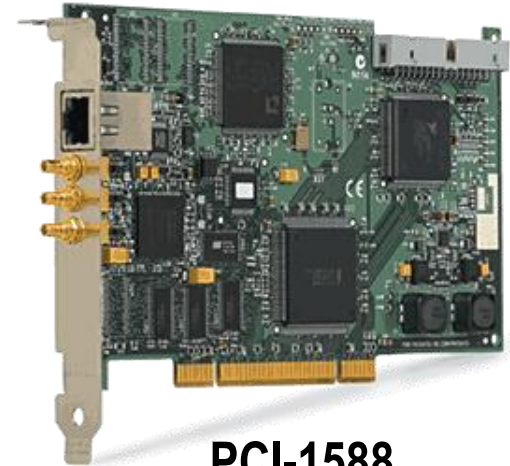
IEEE 1588 – Precision Time Protocol

- Used to synchronize distributed time
- Operates via message-based two-way time exchange (like NTP)
- Automatically configures network in to master/slave hierarchy
- Protocol does not specify implementation
- Synchronization characteristics & applications are highly implementation specific



Time-Based Synchronization Solutions

- IEEE1588 provides submicrosecond synchronization over Ethernet
- Universal PCI connector for operation in 5 V and 3.3 V slots
- Standard RJ-45 Ethernet plug and CAT 5 cabling
- IEEE 1588-2002 compatibility
- Auto-MDI capable for use with straight-through or crossover cables
- Ideal for distributed measurement and remote industrial control applications



PCI-1588



PXI-6682

Utilizing the Latest Technologies in DAQ



New Bus Technologies



Digital Isolators and Their Impact on Measurement Performance



Advanced Data Acquisition Techniques with Onboard FPGAs



Timing and Synchronization Technologies for Challenging Applications

