Optimizing and Analyzing Closed Loop Performance for Power Electronics

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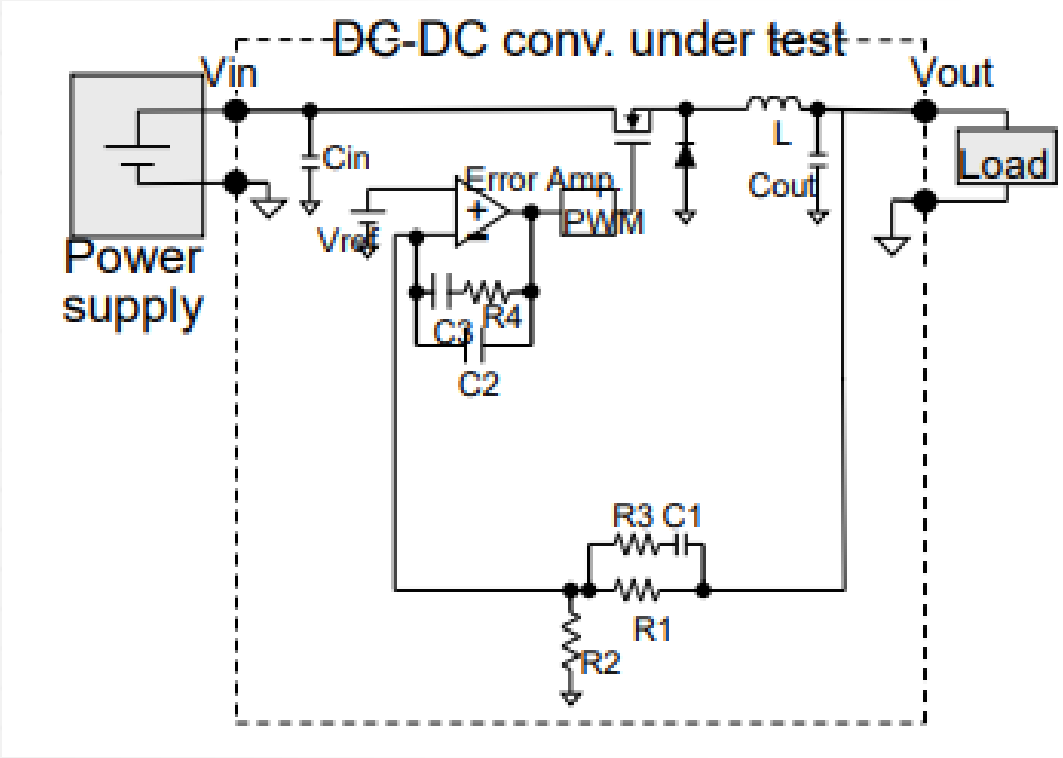
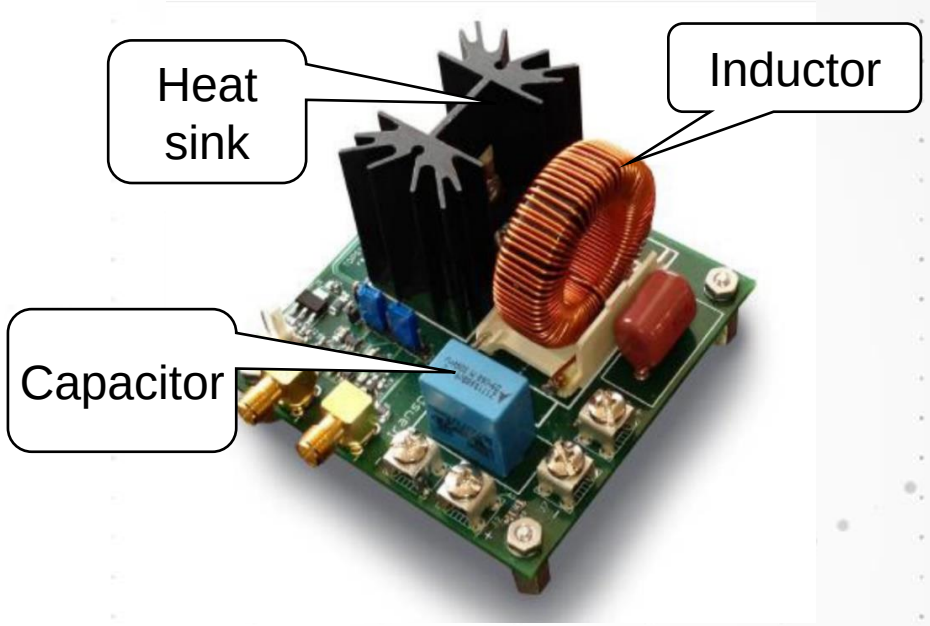
KEYSIGHT TECHNOLOGIES

Typical Switched Mode Power Supply



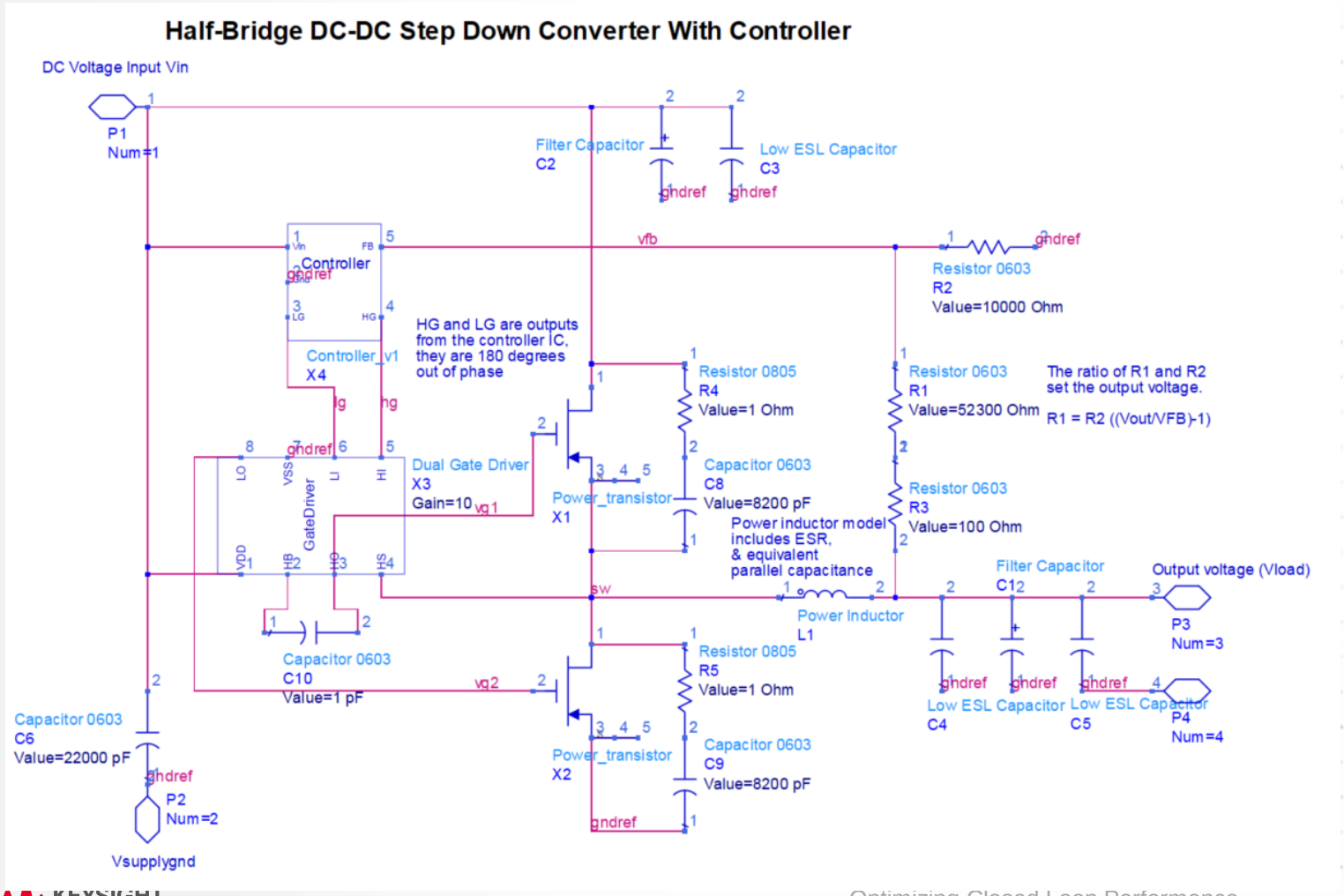


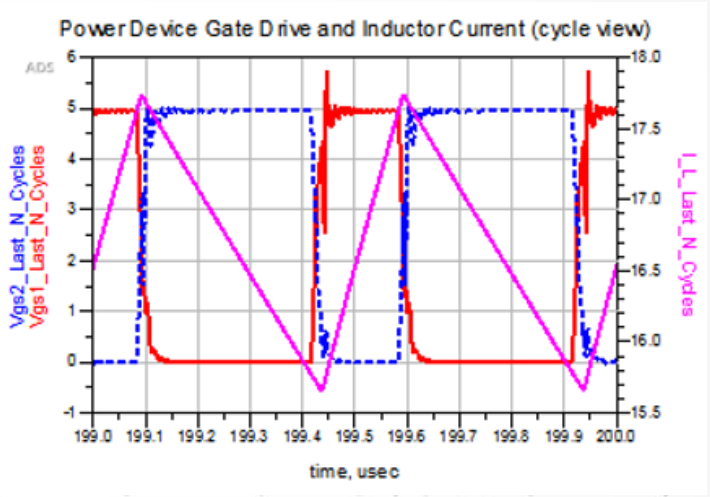
Traditional (cut-and-try) design methods don’t work for high di/dt

- $V_{spike} = L_{parasitic}$ di/dt
- Need to add a field solver to extract layout parasitics into an EM-based model

Typical Switched Mode Power Supply

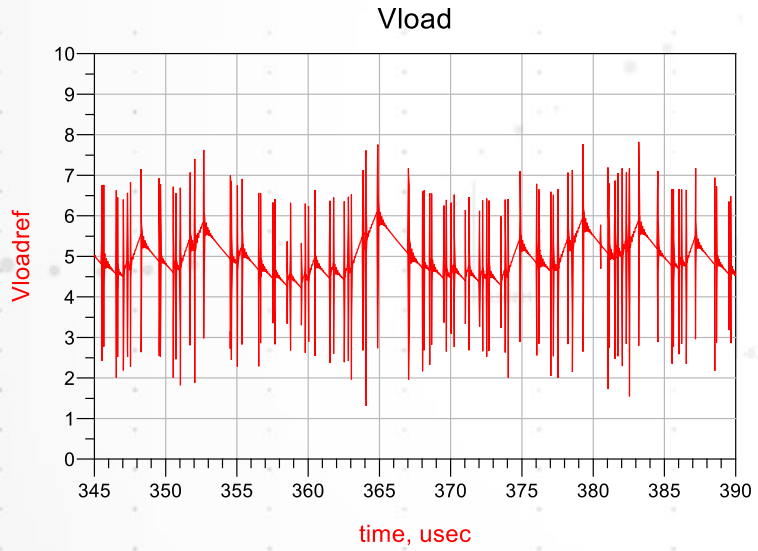
SiC or GaN Converter Designs switching at 0.5A/ns can lead to destructive failures. We need to analyze loop performance with an understanding of how parasitics effect stability.





Closed Loop Challenge

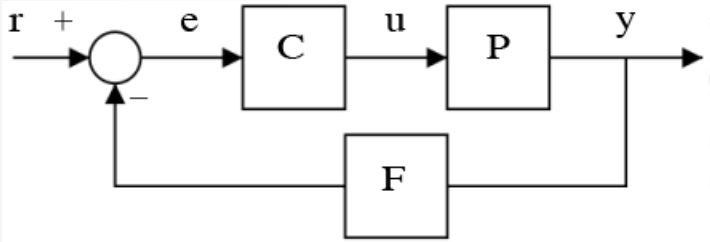
A lot of thought can go into designing a closed loop power system on paper, and a initial system design may seem solid. However, performance may not live up to expectations or worse yet the design is unusable, leaving the designer confused. Simple system simulations cannot guarantee performance.

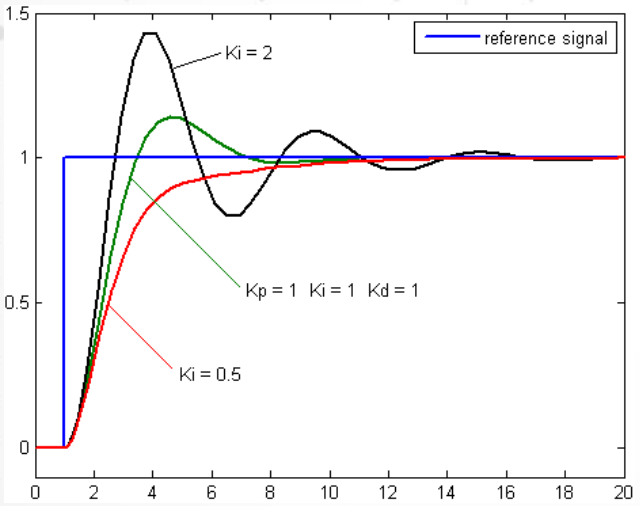


Fortunately, newer EDA tools can provide insights into issues allowing the designer to build their expertise and get designs right the first time.

What This Paper IS About

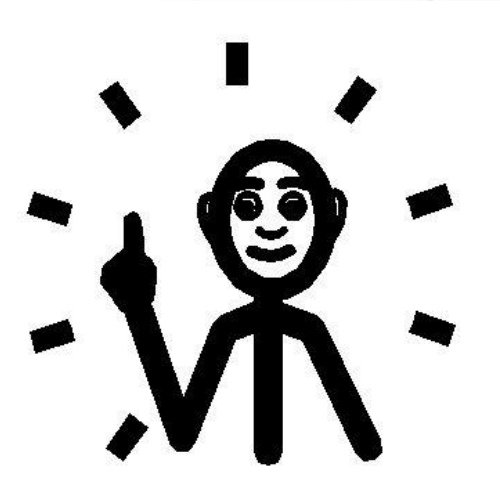
Out topic is NOT about traditional control loop system design! There are many papers and materials on this topic





Our topic is about:

1. Understanding mechanisms which cause designs to not work as intended
2. Learning new techniques which can provide insights into problems
3. Avoiding and correcting issues before fabrication through an improved workflow



Agenda

STABILITY ANALYSIS METHODOLOGIES

OPEN LOOP DESIGN ANALYSIS

CASE STUDY: CLOSED LOOP PERFORMANCE OPTIMIZATION

NISM – NON INVASIVE STABILITY MEASUREMENT

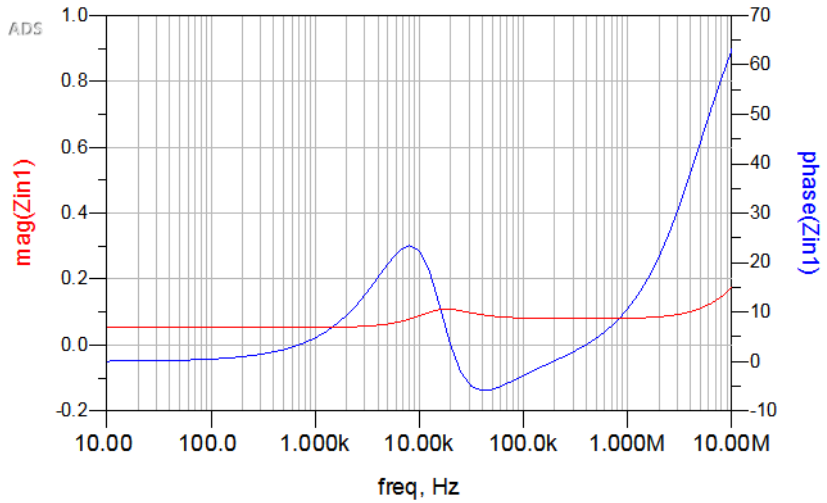
Stability Analysis Methodologies

RESTORING PERFORMANCE DESTROYED BY PHYSICAL IMPLEMENTATION

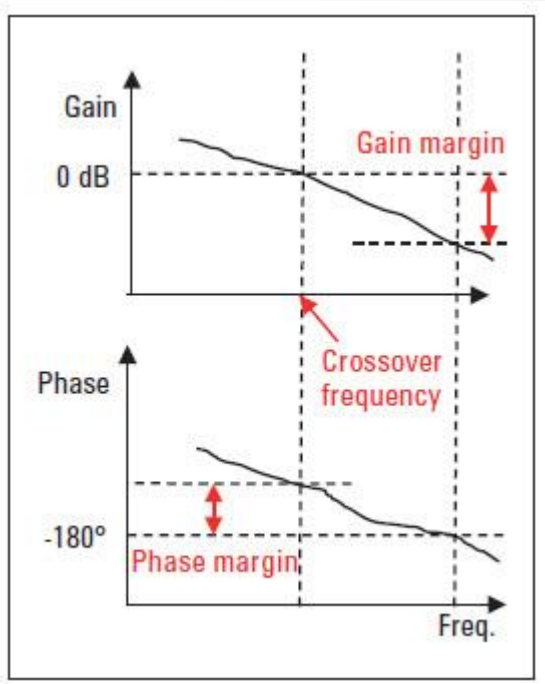
Closed Loop Stability Analysis

SOME ANALYSIS METHODS USED TODAY

- Bode Plot, perhaps the most famous
- Stepped load response, examining damping
- Output impedance analysis, avoiding resonances within the loop BW
- NISM – Non-invasive Stability Measurement



Gain margin = attenuation @ -180deg (-20dB or better)



Phase margin = phase @ 0 dB gain (60deg or better)

Reference:
"Characterizing and Selecting the VRM"
Steven Sandler
DesignCon 2017

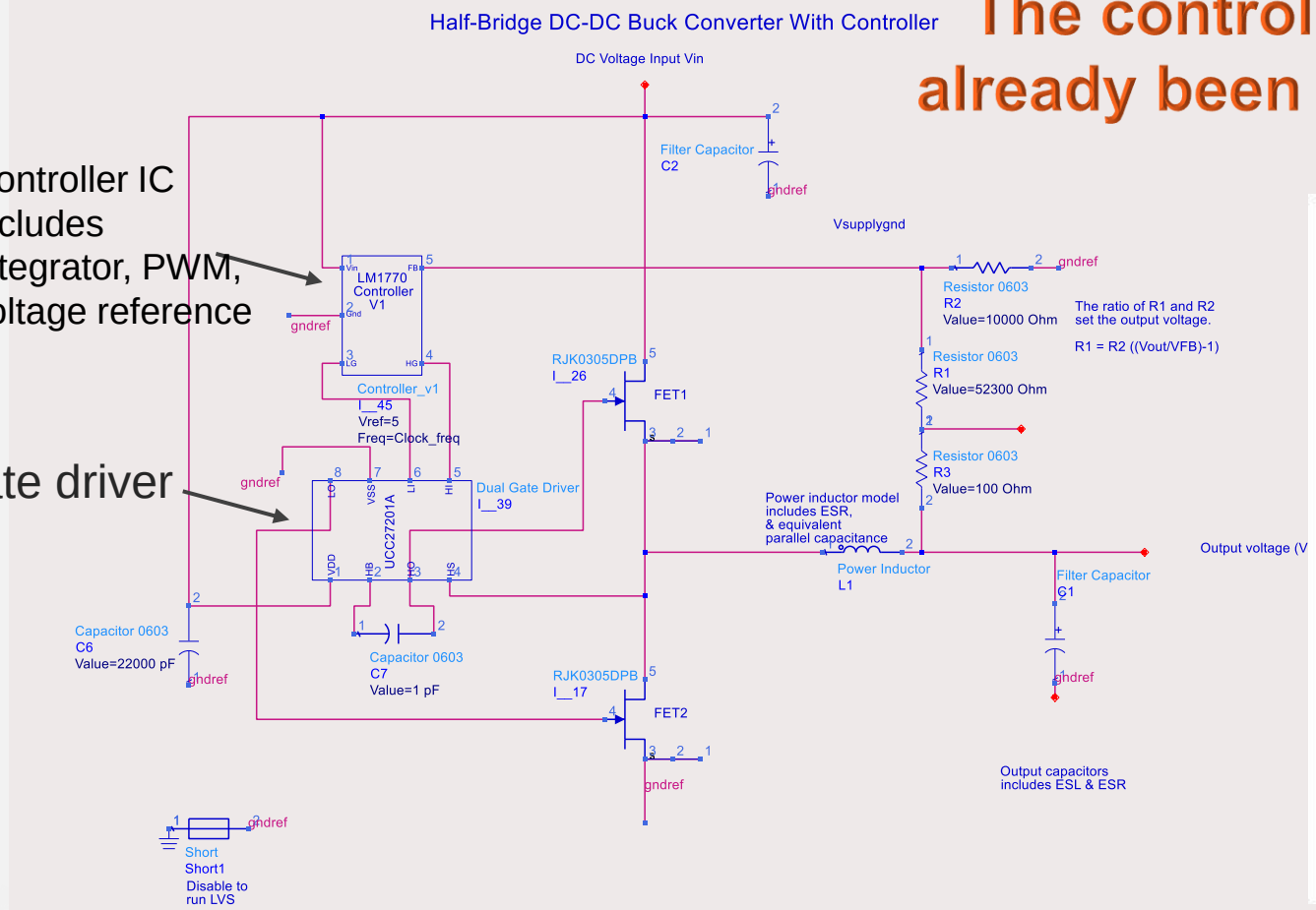
Consider:

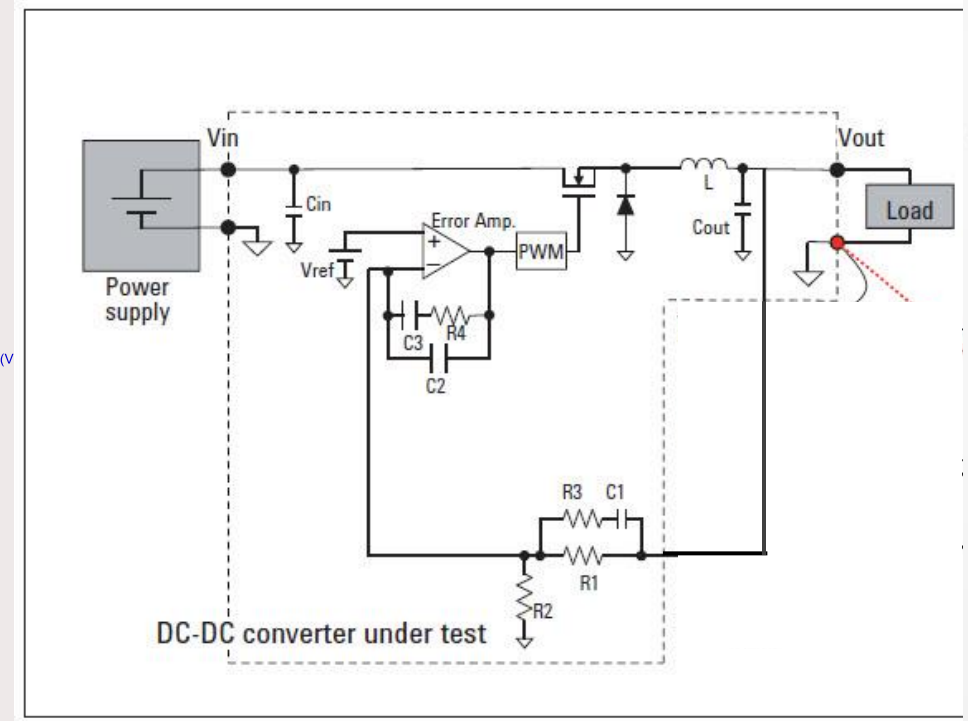
A CIRCUIT IMPLEMENTATION OF A SYSTEM

The control loop system has already been designed on paper

Controller IC includes integrator, PWM, voltage reference

Gate driver





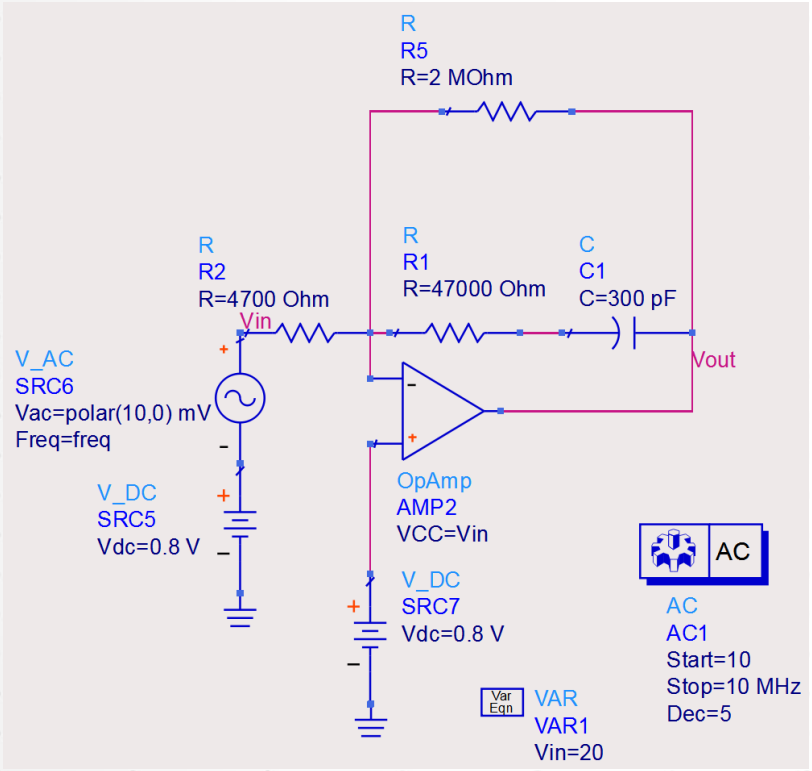
Open Loop Design Analysis

MULTI-STEP TECHNIQUES TO VERIFY THE DESIGN

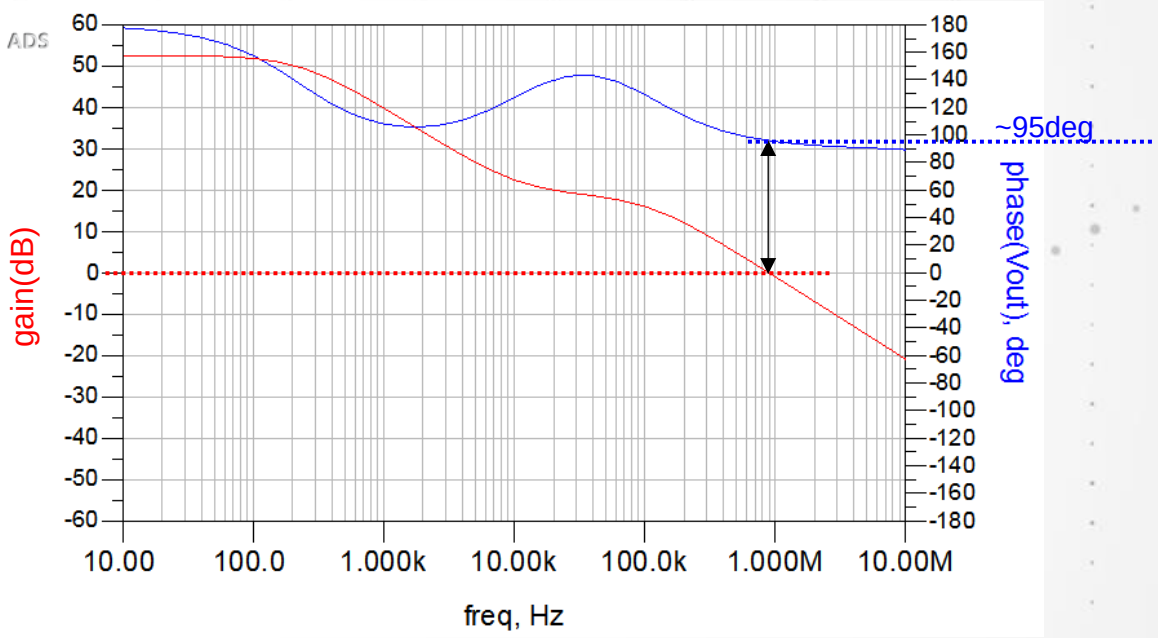
Control Loop Circuit Level Verification

STEP 1: ANALYZE THE LOOP FILTER

Verifying the loop filter



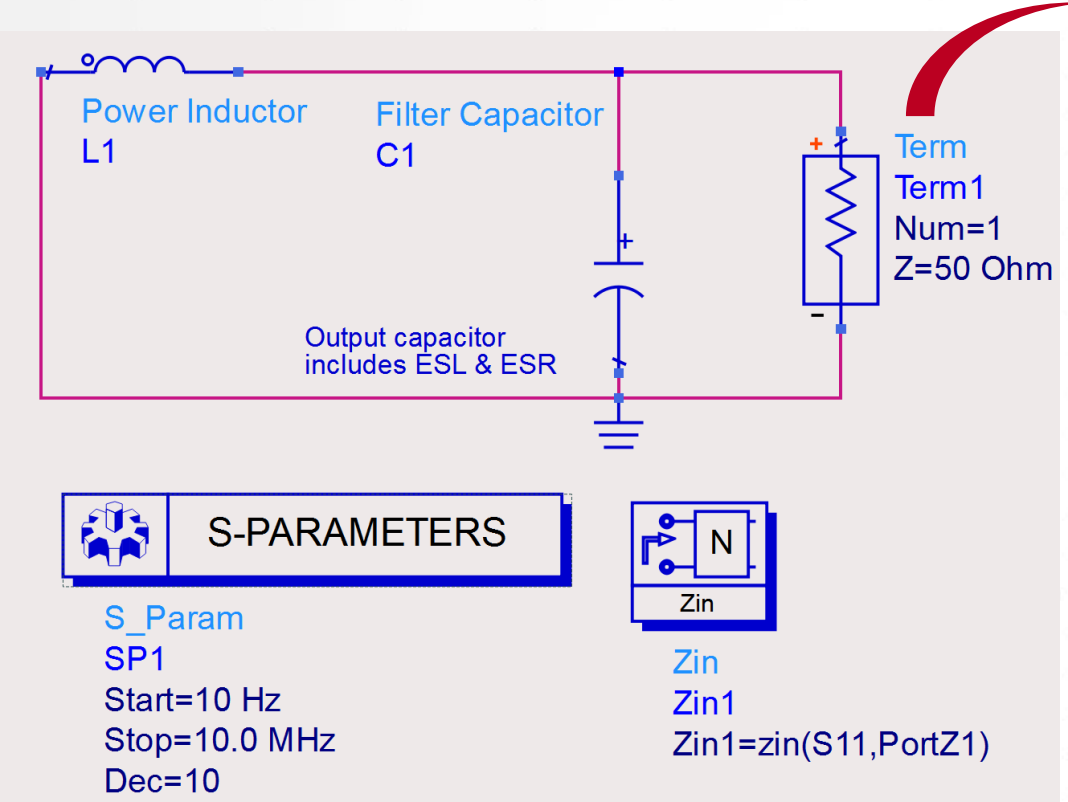
Bode Response Looks Good



A quick AC analysis check.
<1 second simulation in ADS

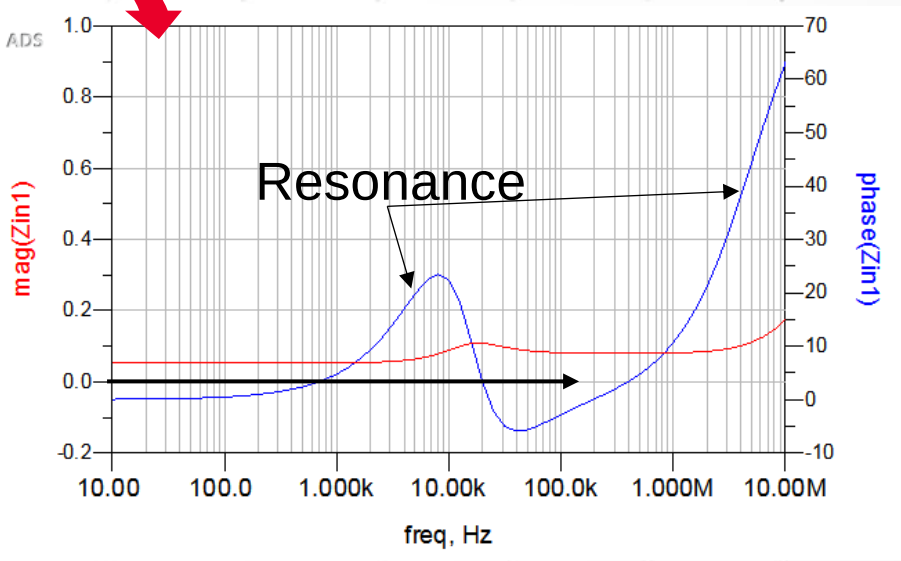
Examining the Converter Output Impedance

STEP 2: OPTIMIZE THE OUTPUT IMPEDANCE



An S-parameter analysis is fast and easy.
<1 second

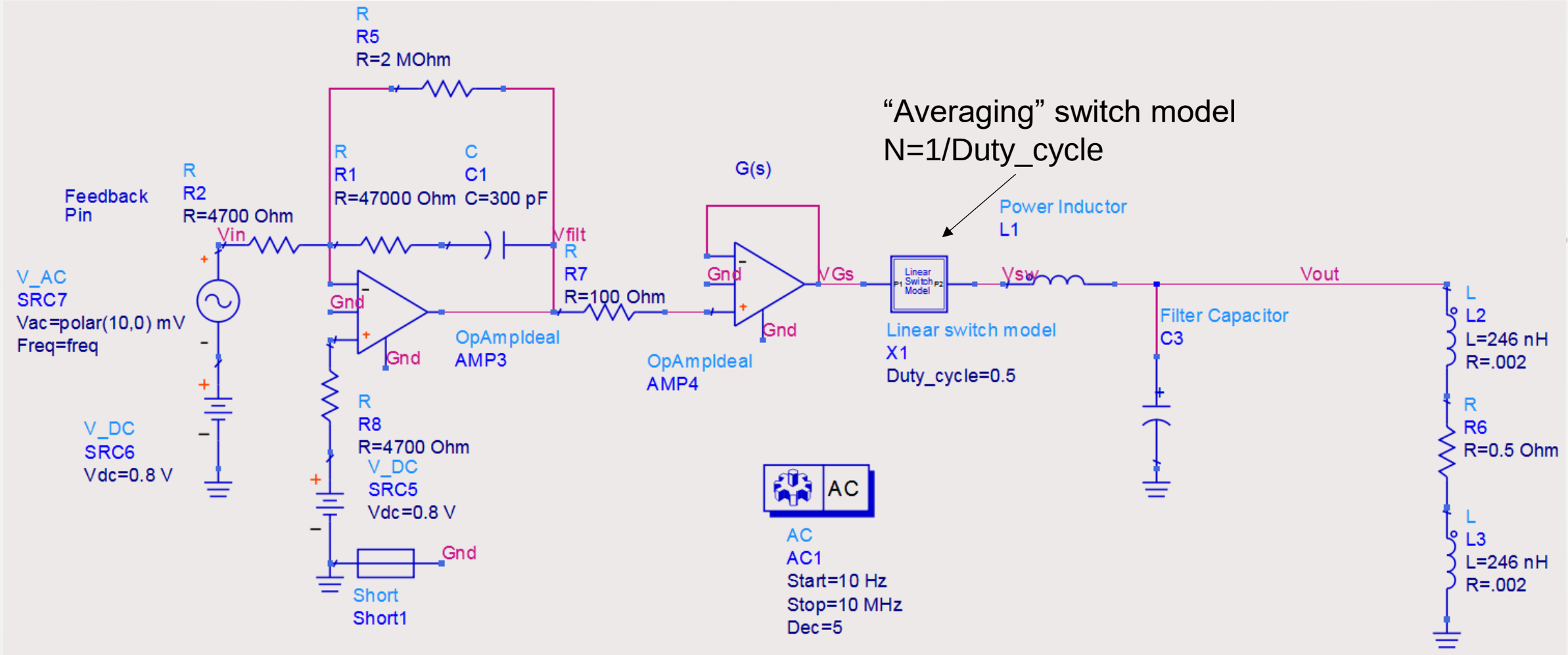
Magnitude and Phase



Ideally, the output impedance should be flat within the loop bandwidth (black)

Putting It All Together

STEP 3: FAST OPEN LOOP BODE PLOT ANALYSIS

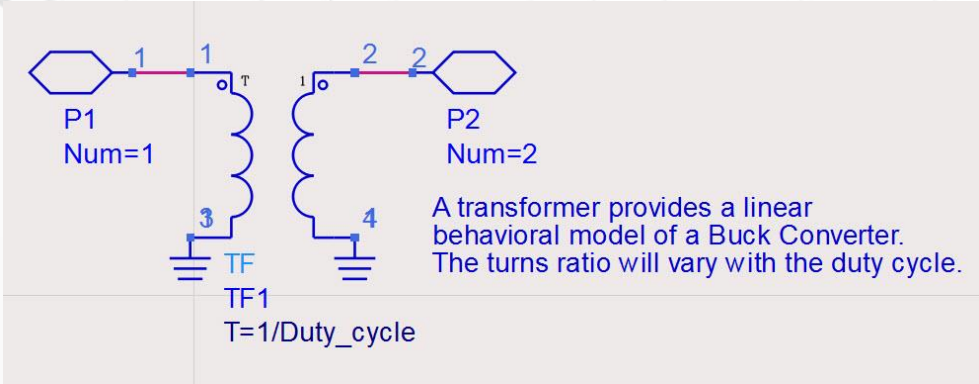


The “Averaging Model” for The Switching Circuit

LINEARIZATION OF NON-LINEAR CIRCUITS

- Mentioned in 1972 IEEE Power Processing and Electronics Specialists Conference. *“Low Frequency Characterization of Switched DC –DC converters.” G.W. Wester and R.D. Middlebrook*
- *Robert Erickson’s book “Fundamentals of Power Electronics.”*

A buck converter switch can be modeled as a transformer with a turns ratio of 1/duty cycle ~ 2 for a 50% duty cycle.

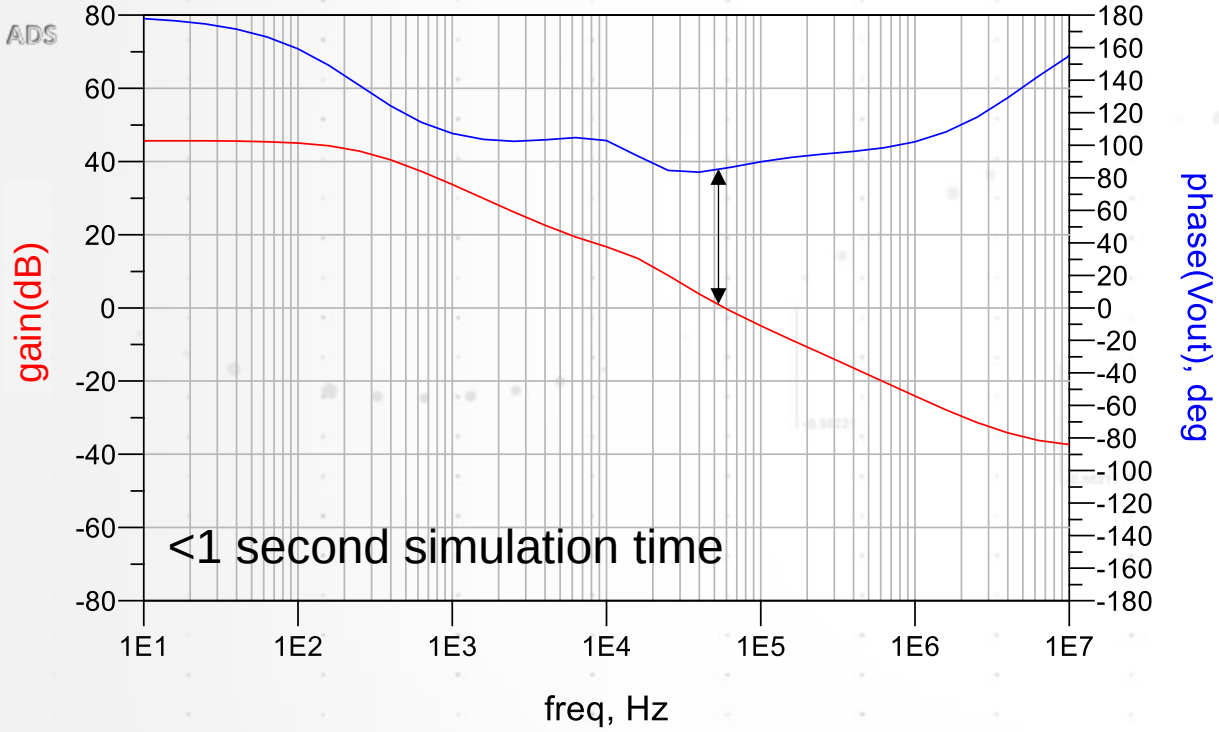


Linearization gives up some detail, but gives a reasonable initial look.

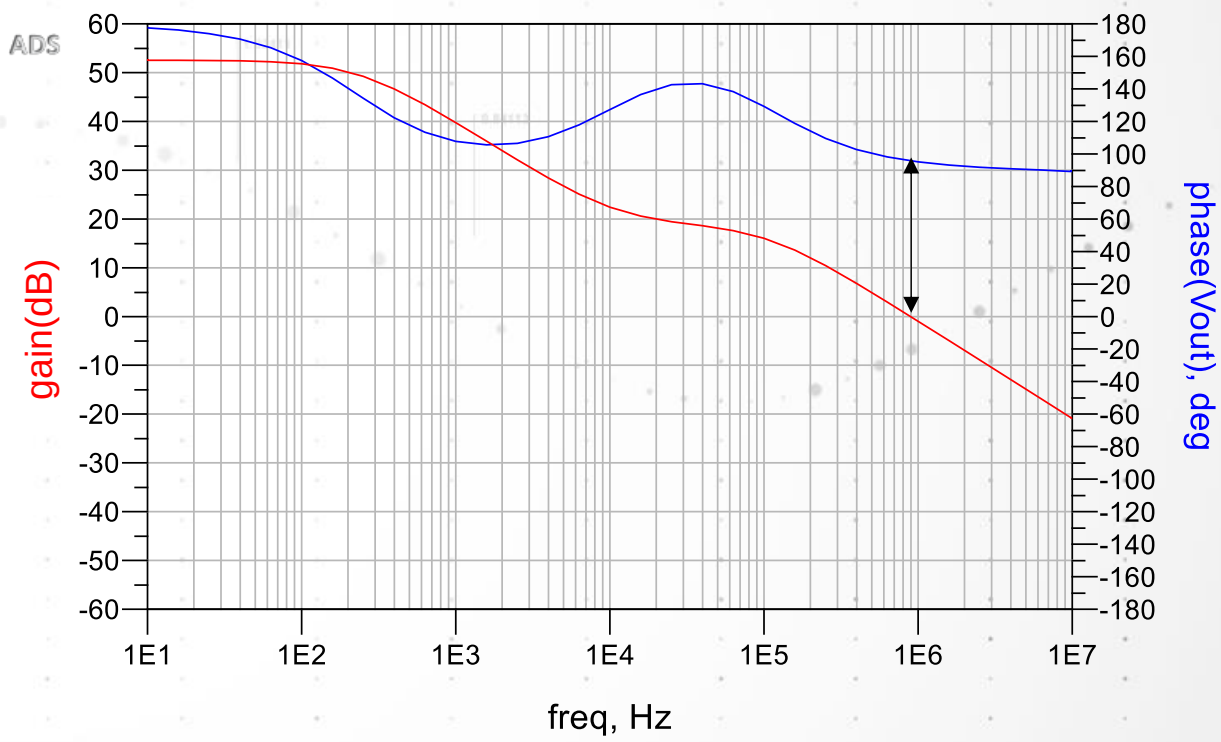
Open Loop Bode Plot Analysis

THIS LOOKS GOOD

Open Loop System Response



Loop Filter Alone



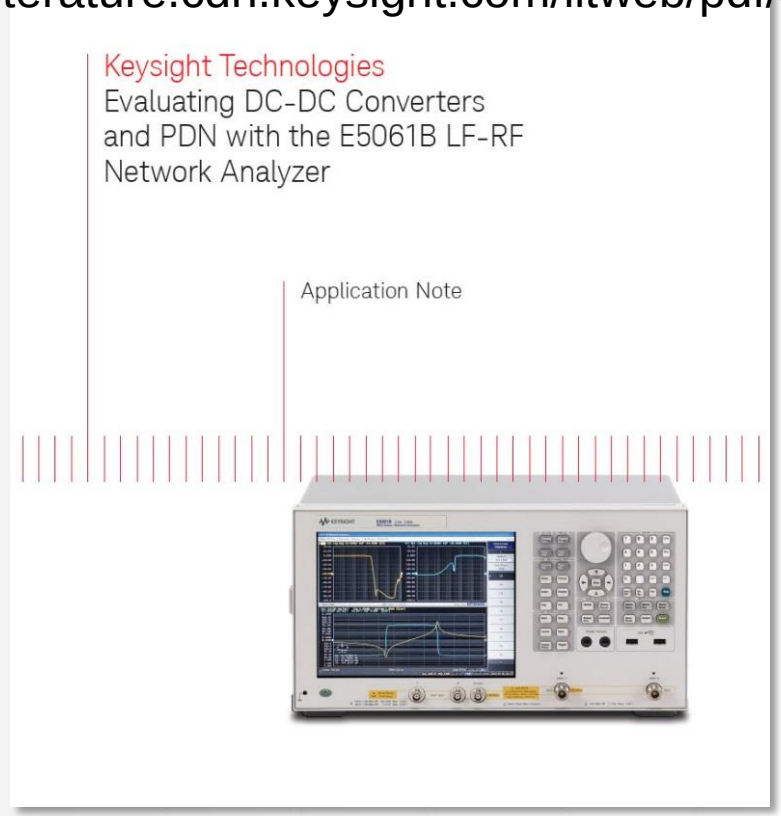
Case Study: Closed Loop Performance Optimization

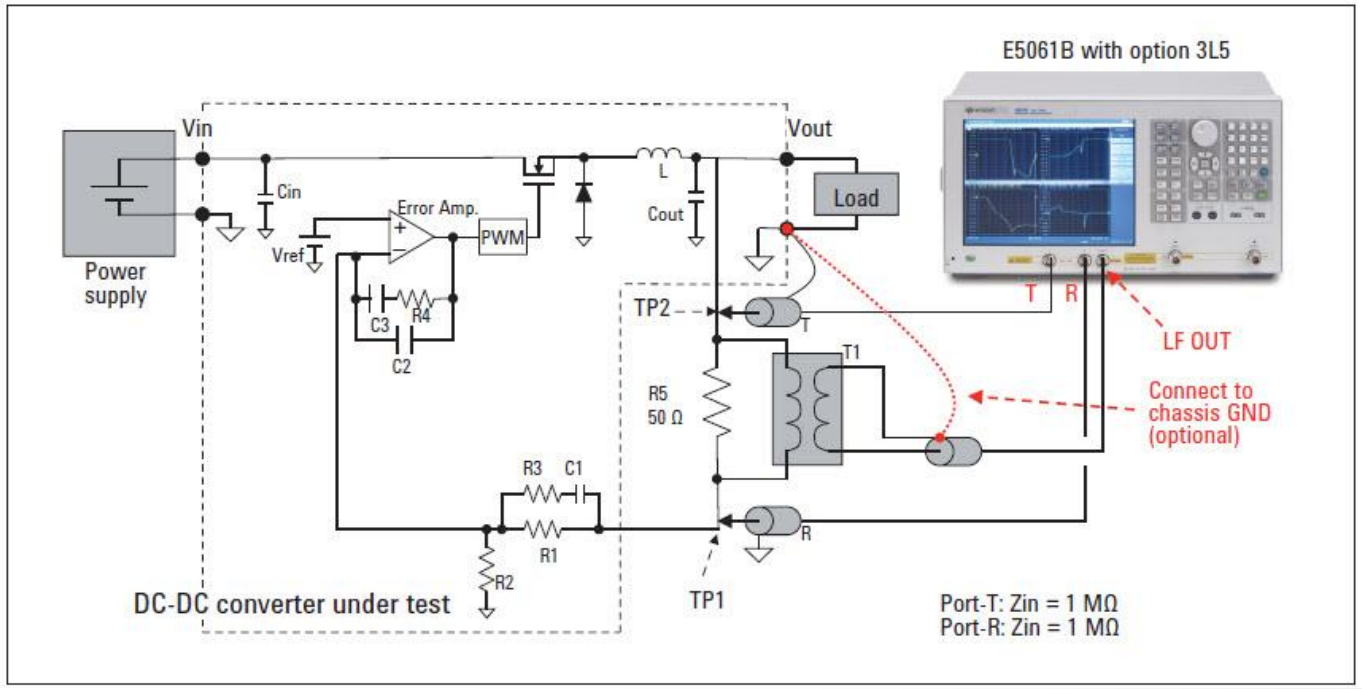
RESTORING PERFORMANCE DESTROYED BY PHYSICAL IMPLEMENTATION

Testing Closed Loop Converter Loops

INJECTION METHOD TESTS CLOSED LOOP PERFORMANCE

http://literature.cdn.keysight.com/litweb/pdf/5990-5902EN.pdf





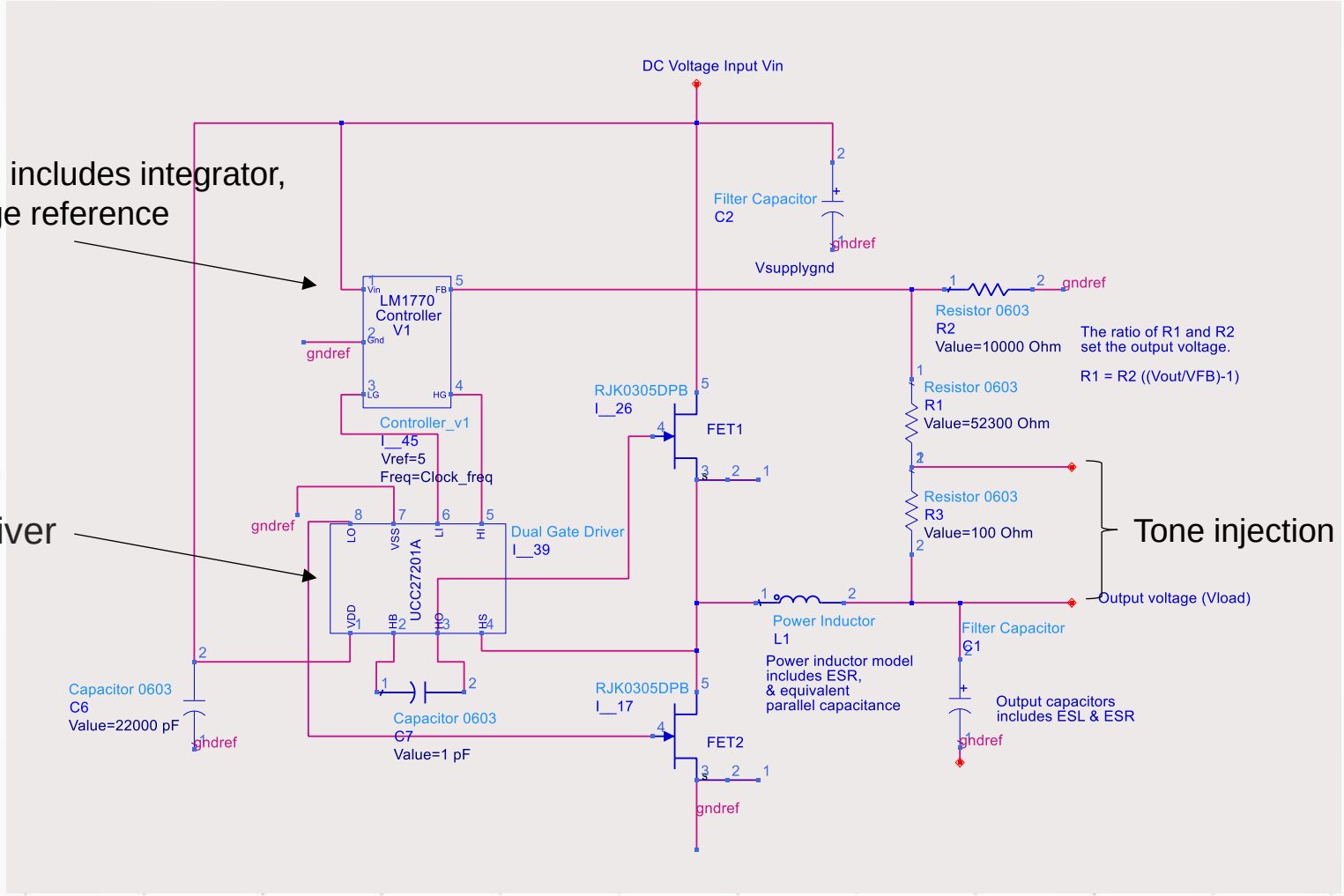
- Using the same methodology in simulation and test provides consistency in the design validation process.
- Captures the non-linear and parasitic effects which impact loop performance in a closed loop condition.

Closed Loop Bode Analysis for Simulation

THIS WILL MODEL NON-LINEAR BEHAVIOR

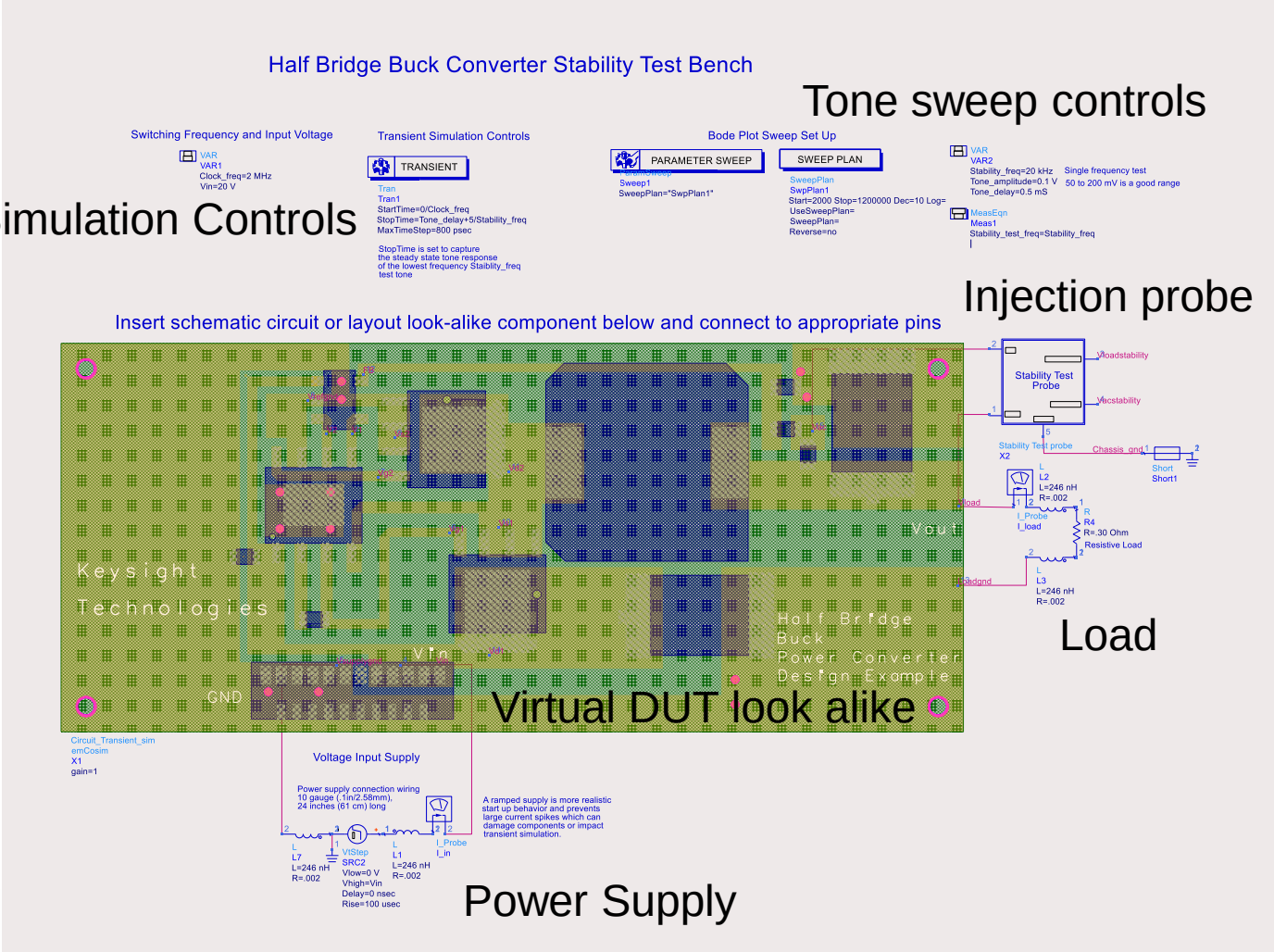
Controller IC includes integrator, PWM, voltage reference

Gate driver



Stability Analysis

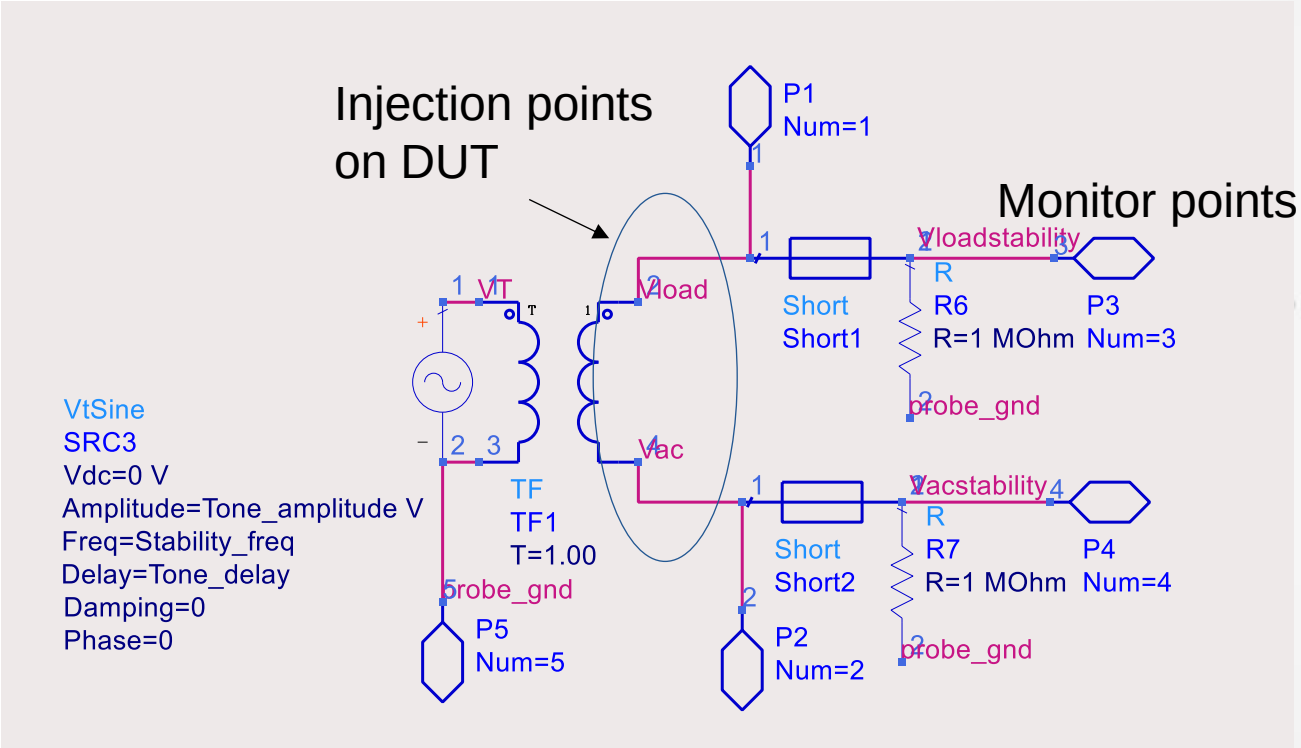
- The underlying circuit schematic is included in the virtual DUT symbol.
- This method allows the user to toggle between a schematic view and one that also contains the layout!



Note: the EM Co-simulation topic is covered in other Keysight Papers

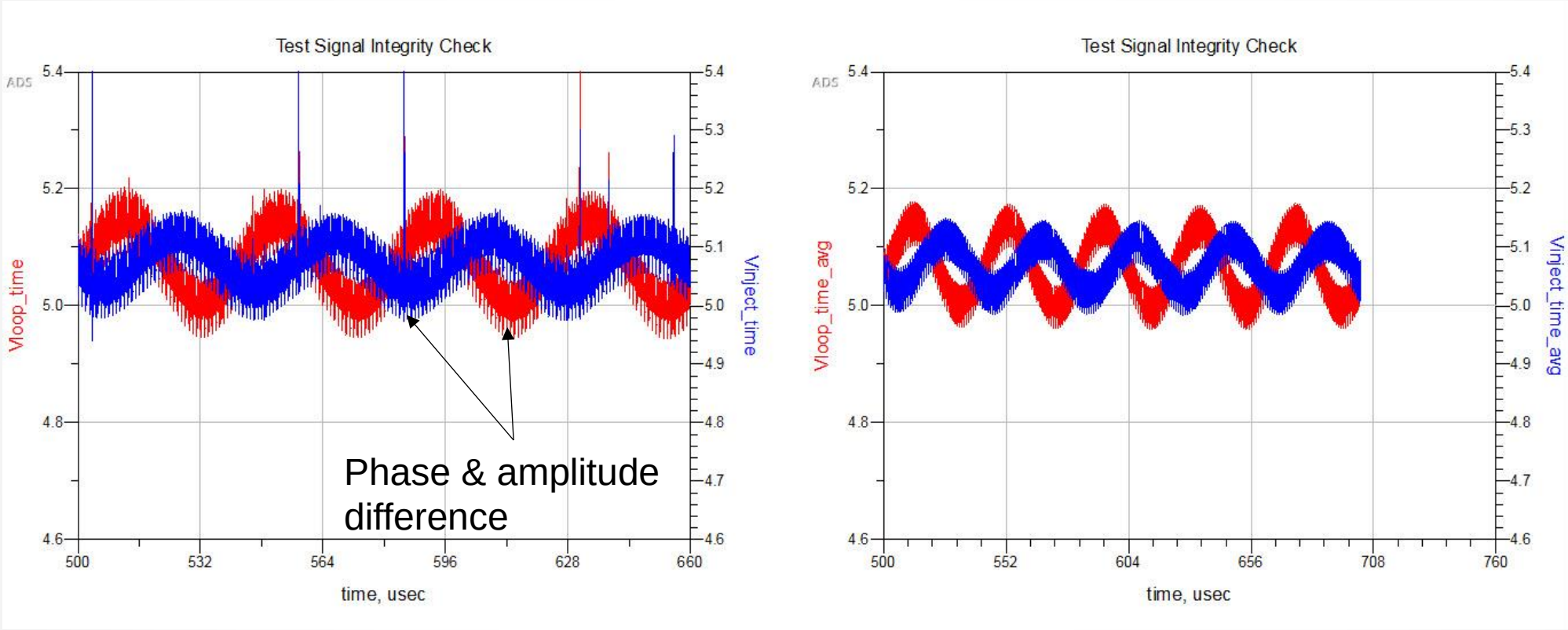
A Look At The Injection Probe

Because of the high loop gains, the injection tone should be between 50 and 200 mV to maintain linearity of the loop



Tone Analysis: Amplitude and Phase Relationships

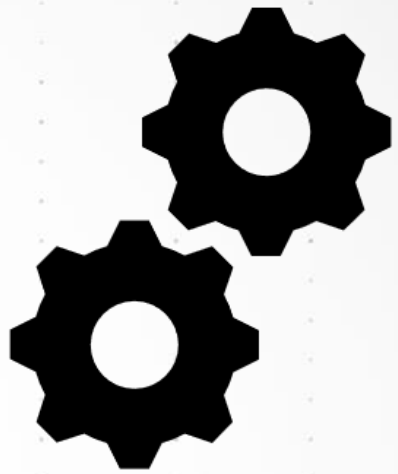
CONVERTER OUTPUT TONE VS INJECTION TONE



- The injected tone amplitude and phase is compared with the same tone present at the output of the power converter.
- The amplitudes and phases are compared to determine the loop gain and phase.
- The tone gain and phase relationships change with tone frequency.

Processing Tones

PROCESSING TONES IS DONE IN THE DATA DISPLAY



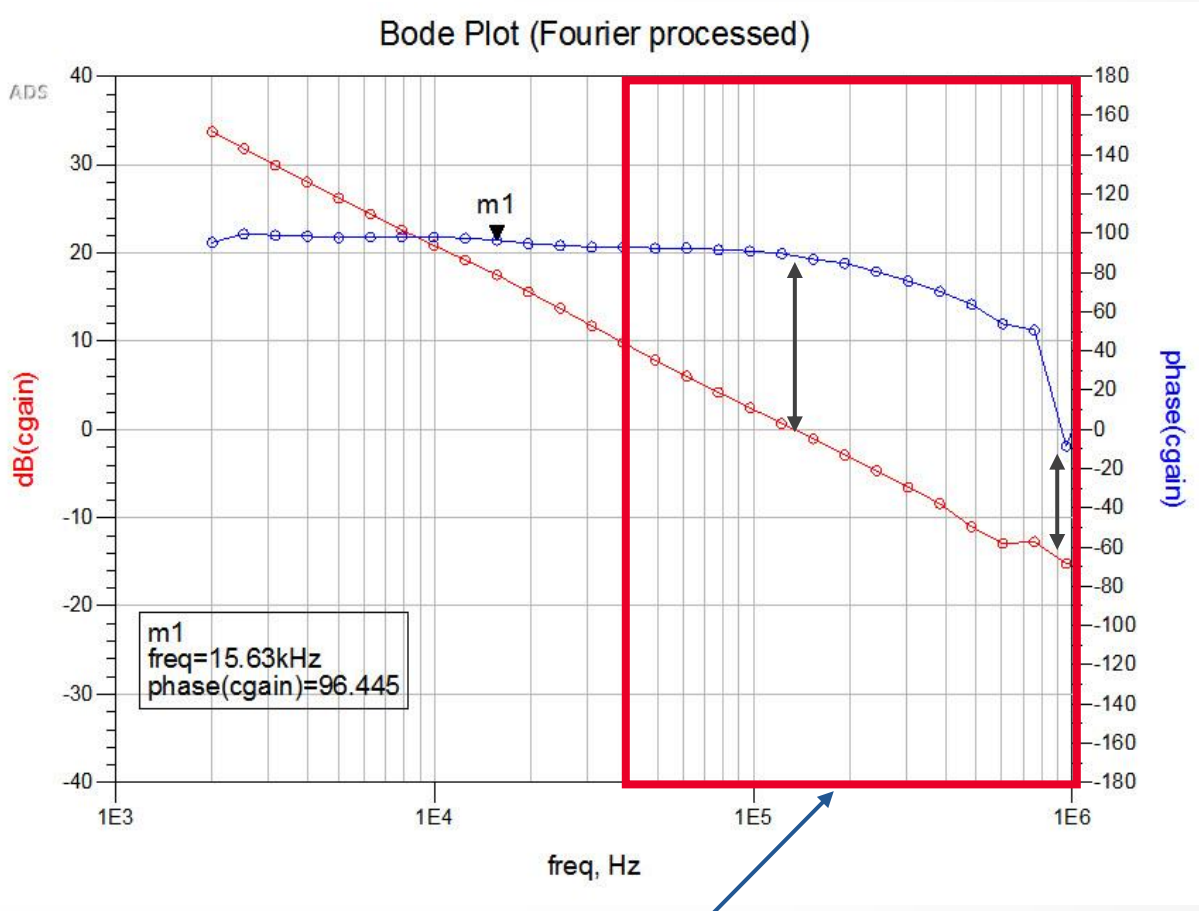
- At low injection tone frequencies, the tone present at the output of the converter will be large. The opposite is true at higher frequencies.
- Non-linearities and noise generated by the physical implementation will mask the injection tone. Fourier processing is done to pull the signal out of the noise and produce consistent results
- In the ADS analysis, the Fourier processing and tone frequency sweep are controlled through AEL expressions.

Schematic Simulation Results Look Good

NON-LINEARITIES HAVE ALTERED THE LOOP RESPONSE

Transient simulation sweeps were done to populate the graph but the length of each simulation varies with tone frequency.

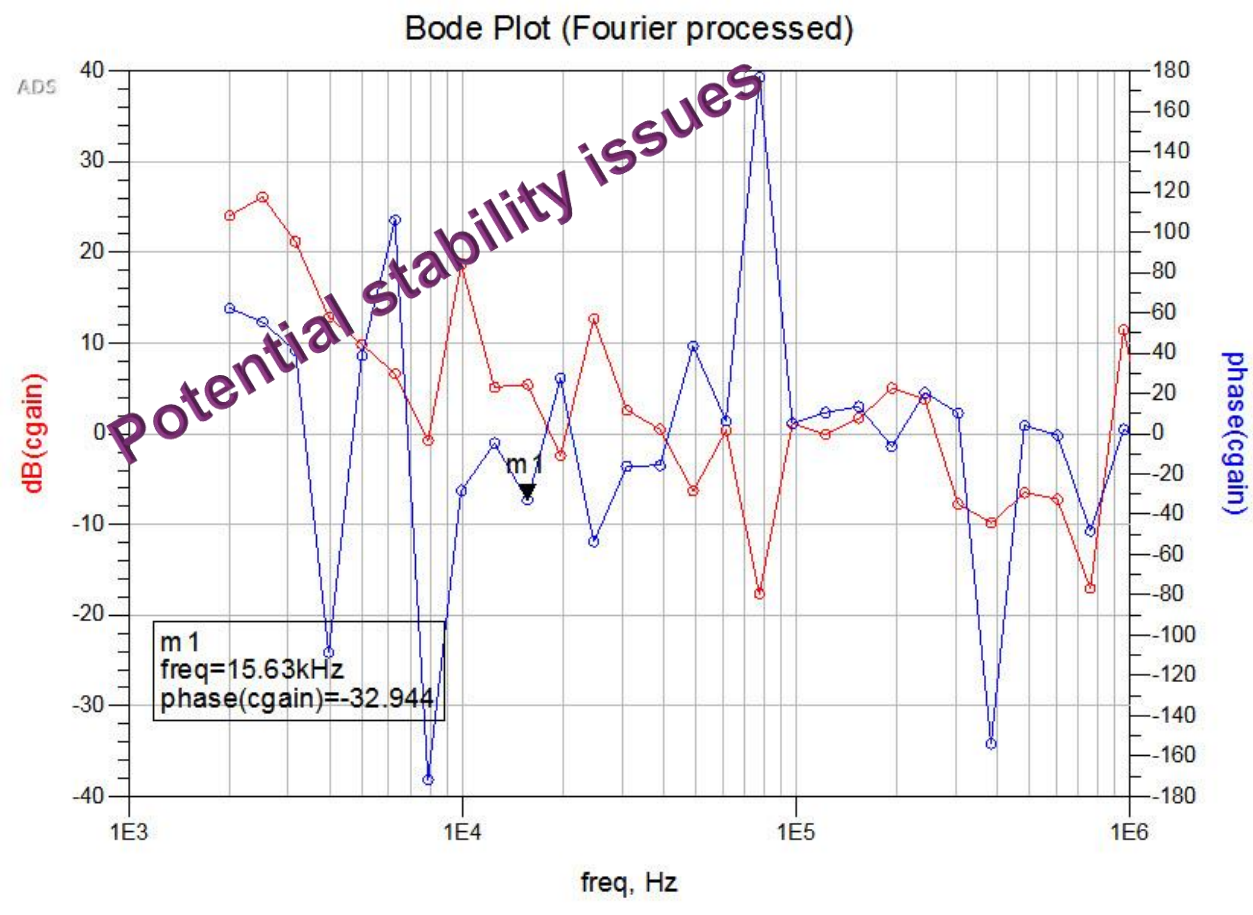
The simulation time can be shortened by only using injection tones in the red box.

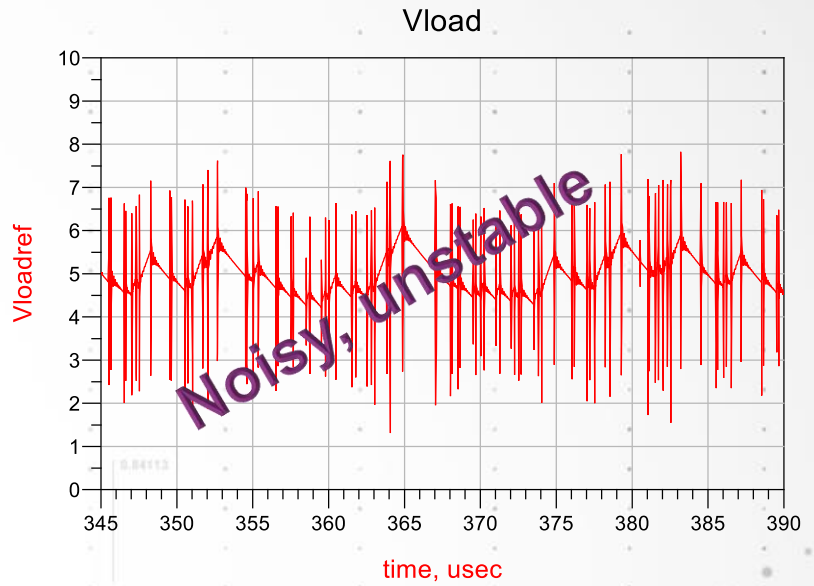


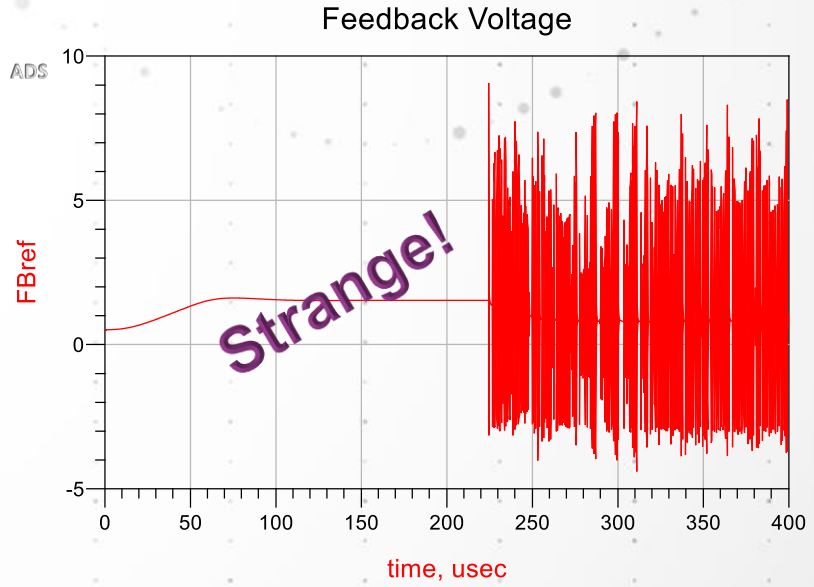
Most issues with gain and phase margin occur within the red box.

EM Co-simulation Results

THE LAYOUT IS ADDED. WHAT HAPPENED?







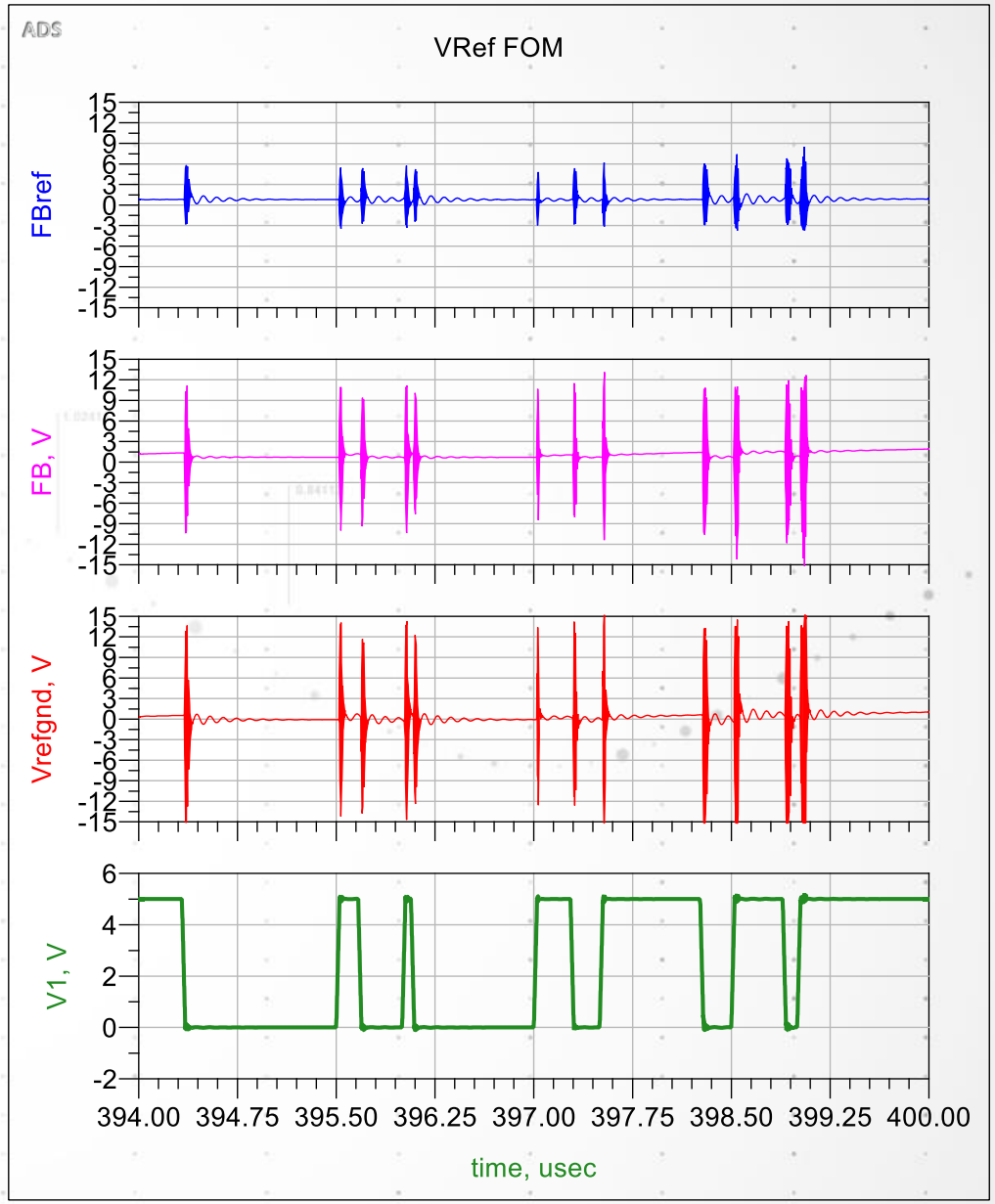
A closer examination of the load and feedback voltage gives clues, but is there more to this?

A Closer Examination

TROUBLESHOOTING THE FEEDBACK PATH

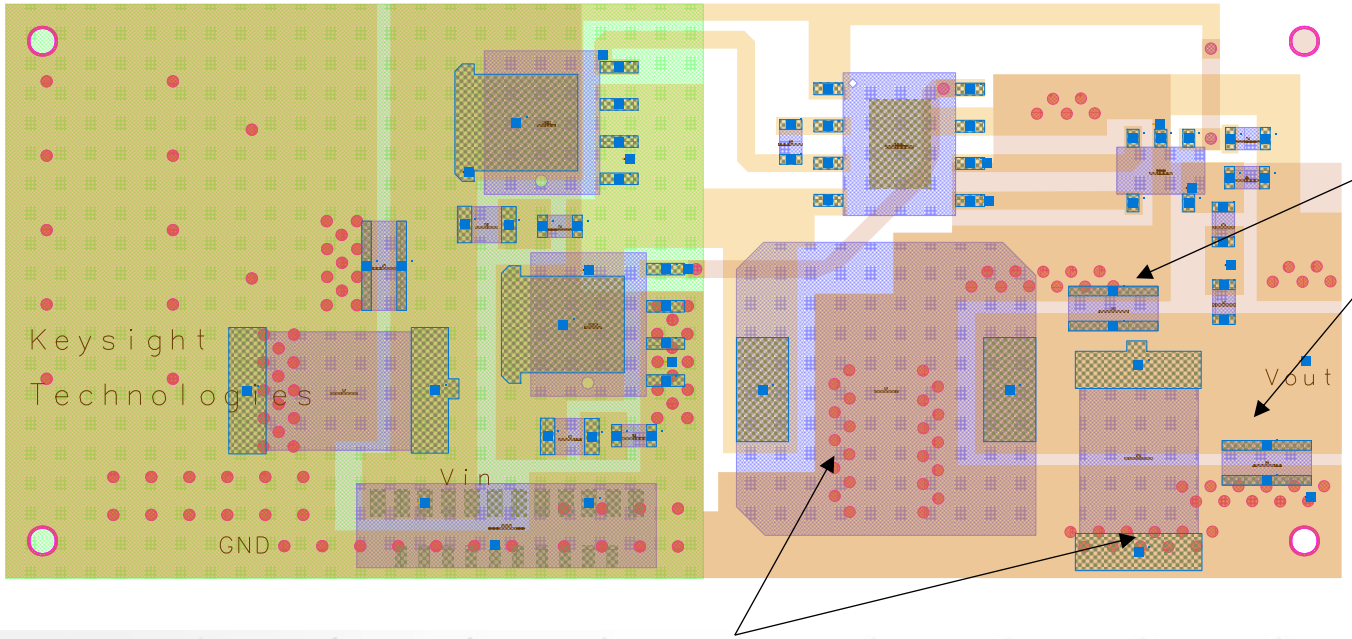
- Significant noise is generated near the ground pin of the voltage reference (Vrefgnd) which is also the controller ground.
- The feedback (FB) voltage also shows the noise.
- FBref is the feedback voltage relative to its local ground. It is what the controller IC sees.
- V1 is the output of the PWM showing misfires. The pulses should be uniform in the steady state condition.

The grounds should be improved.



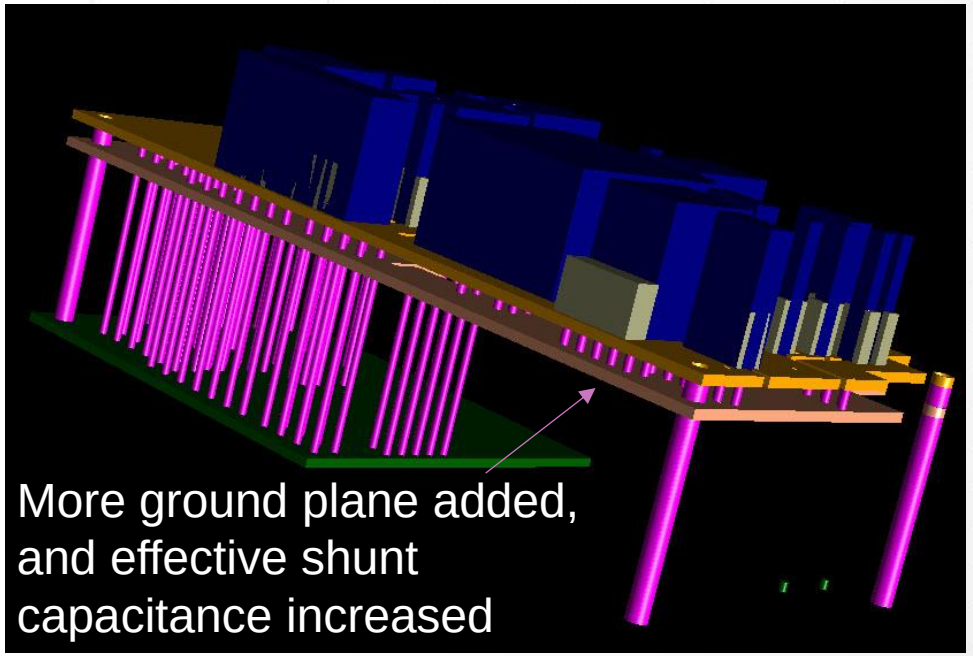
Updating the Layout: Layout #2

SHORTER CURRENT LOOPS AMONG OTHER IMPROVEMENTS



Low ESL capacitors

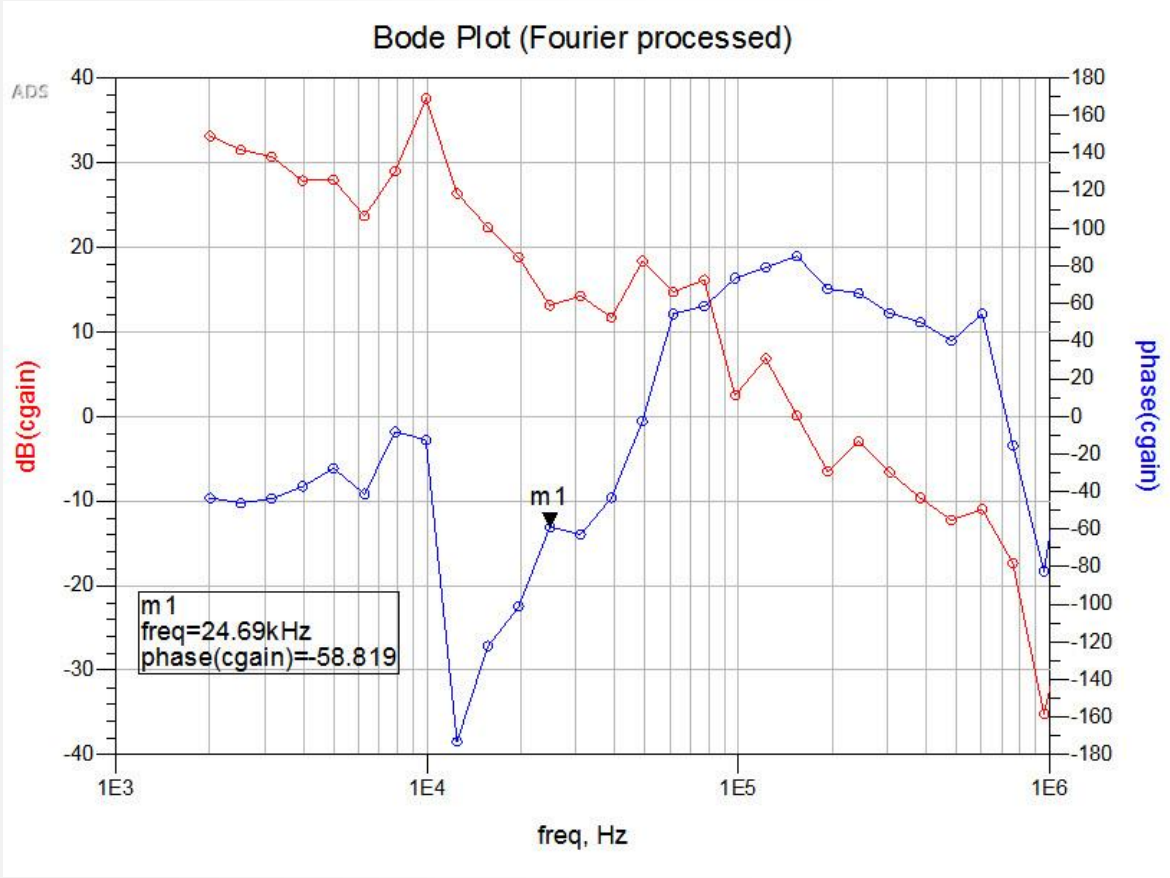
More vias



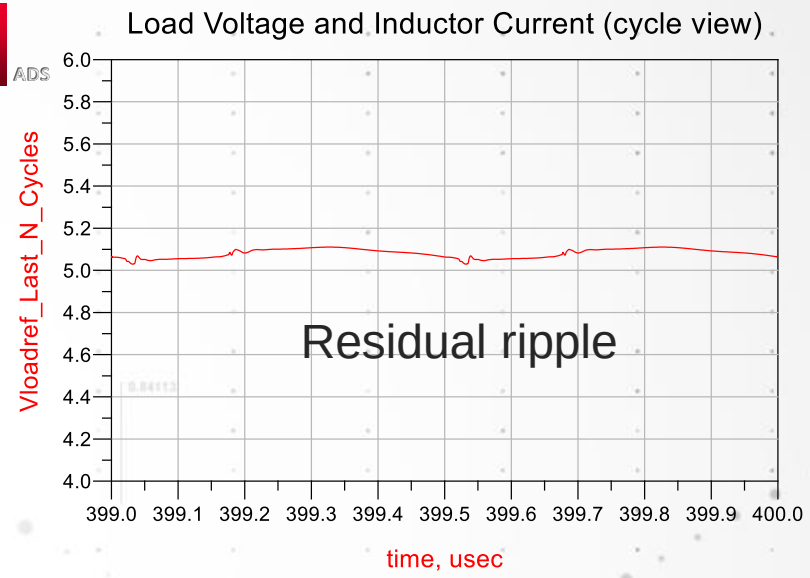
A virtual board spin is faster, costs much less, and provides valuable insights into designs

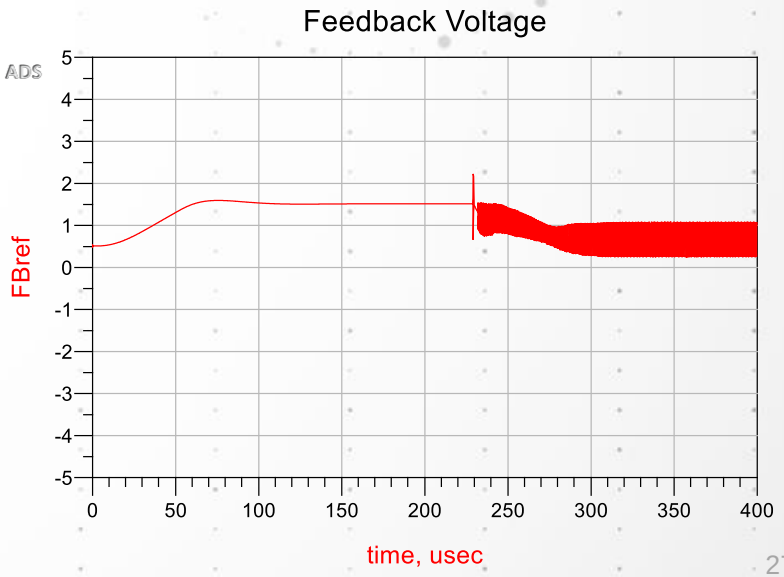
Results from Layout #2

CLEANER RESULTS BUT THERE ARE STILL ISSUES



Gain and phase margin results are good, technically…





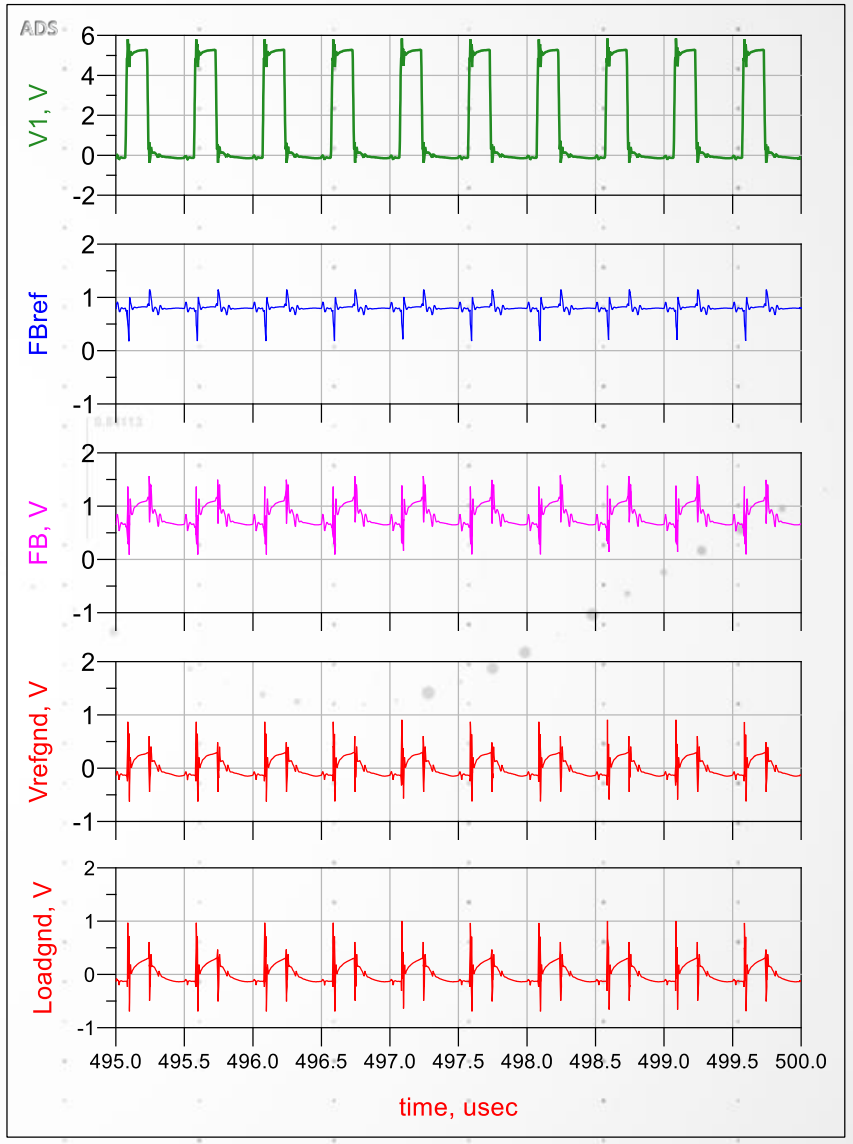
A Closer Examination

HOW ARE THE GROUNDS?

- Noise in the FB path (FBref) is significantly reduced
- The PWM produces a more uniform pulse train

Can we improve things further?

If the FBref noise is reduced to zero, there will be little impact on the gain and phase relationship within the controller IC.



Developing Additional Insights

DEVELOPING A FIGURE OF MERIT (FOM)

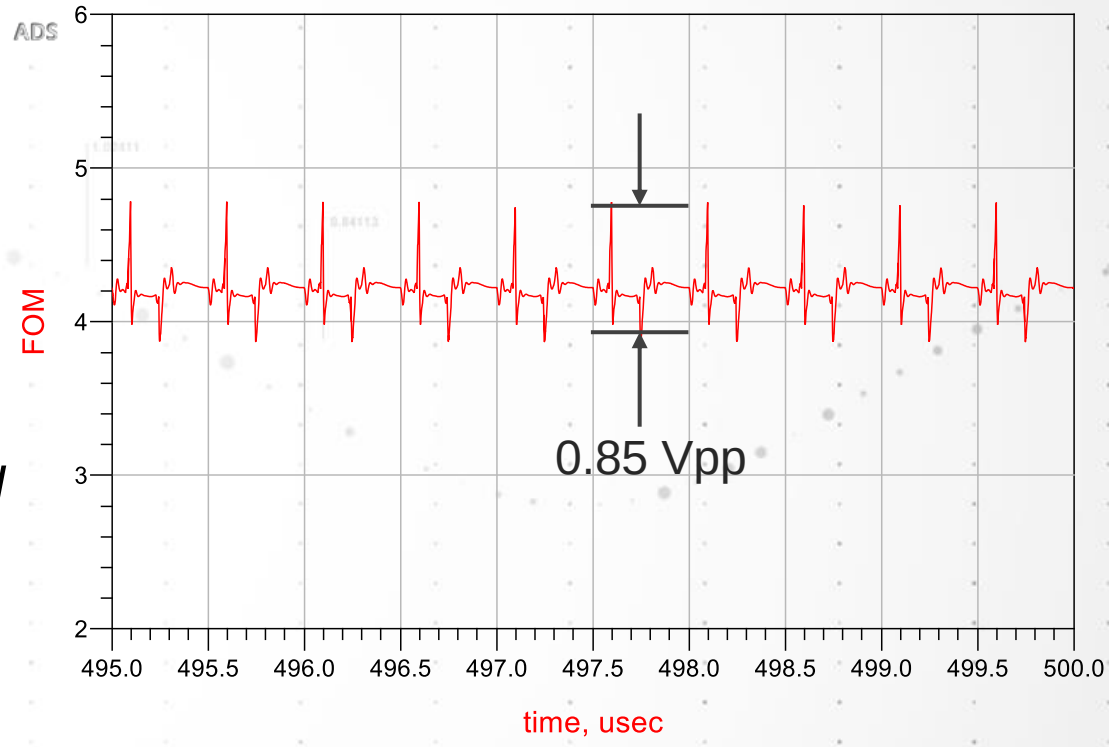
In a perfect world, the 5V output is scaled down to the 0.8V reference voltage, by scaling factor X (resistor divider).

Adding noise…

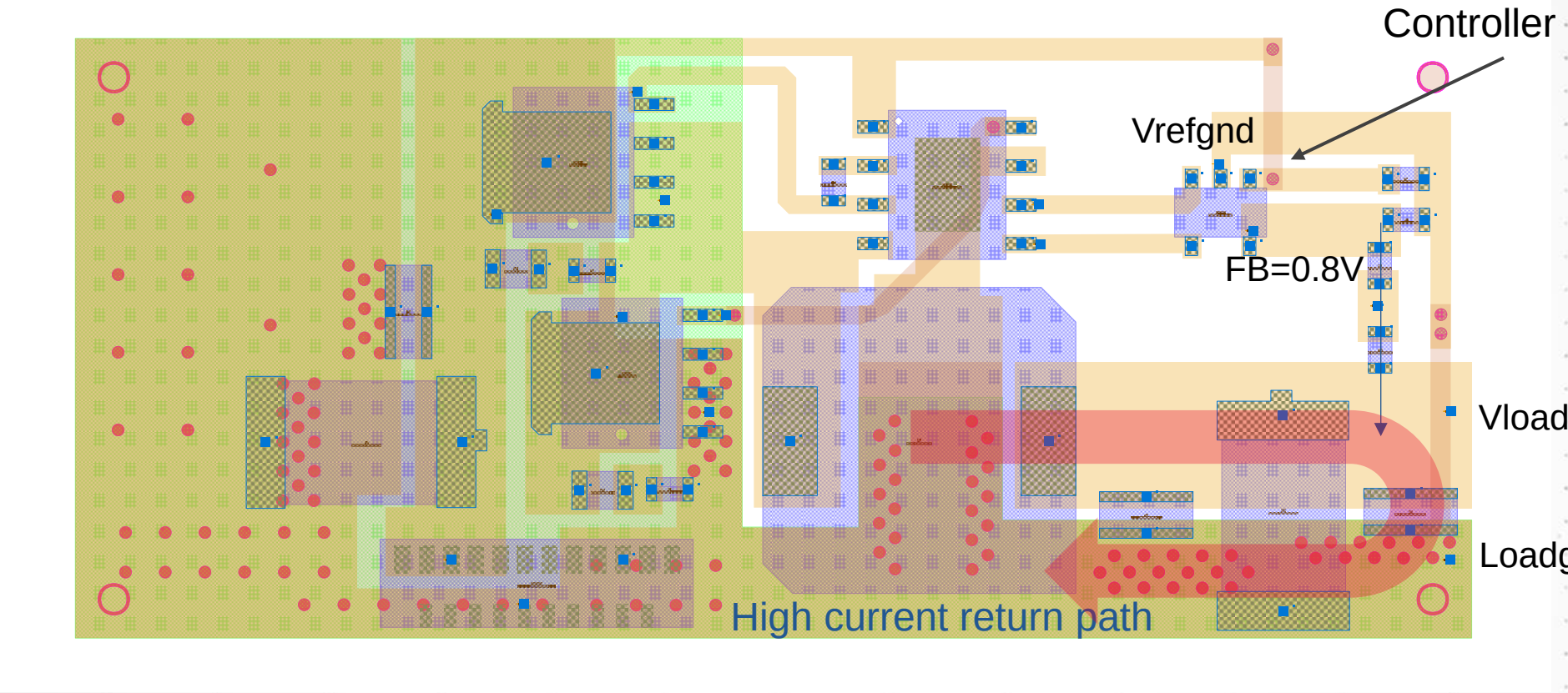
(5V + noiseA) – Loadgnd = X (0.8V + noiseB) – Vrefgnd

We need noiseA=noiseB and Loadgnd=Vrefgnd for a noiseless feedback voltage.

The figure of merit plot shown here represents this relationship.



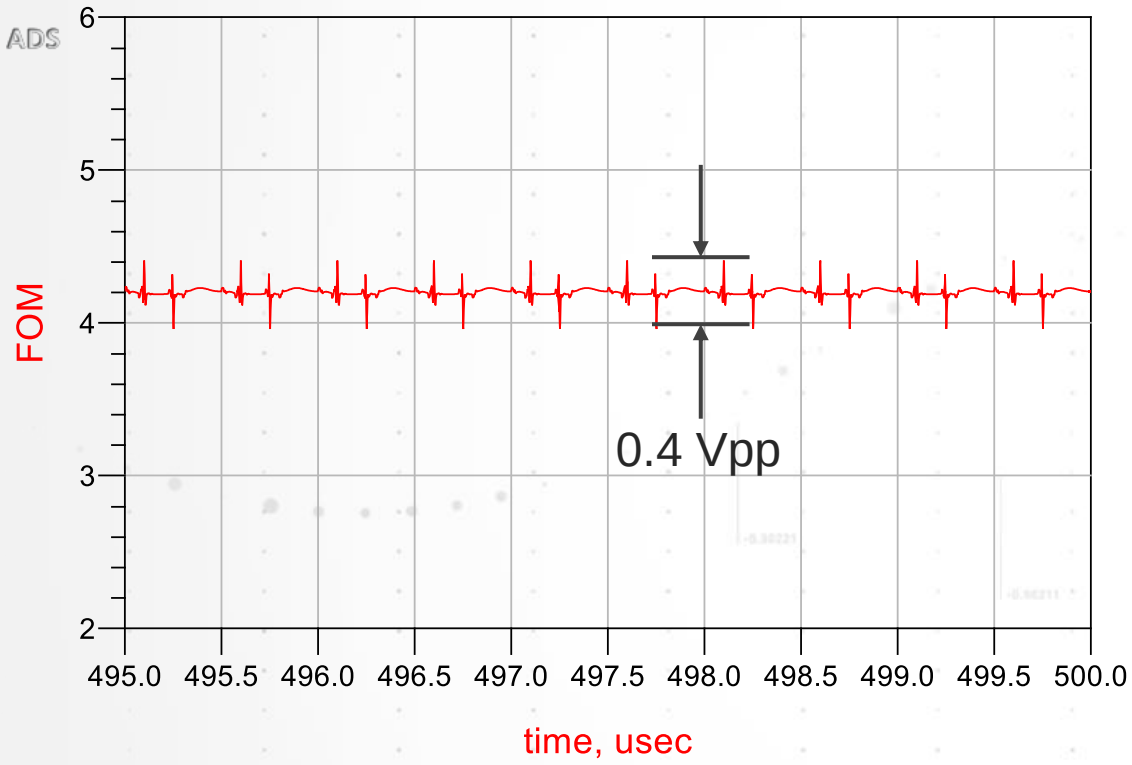
One More virtual Board Spin…Layout #3



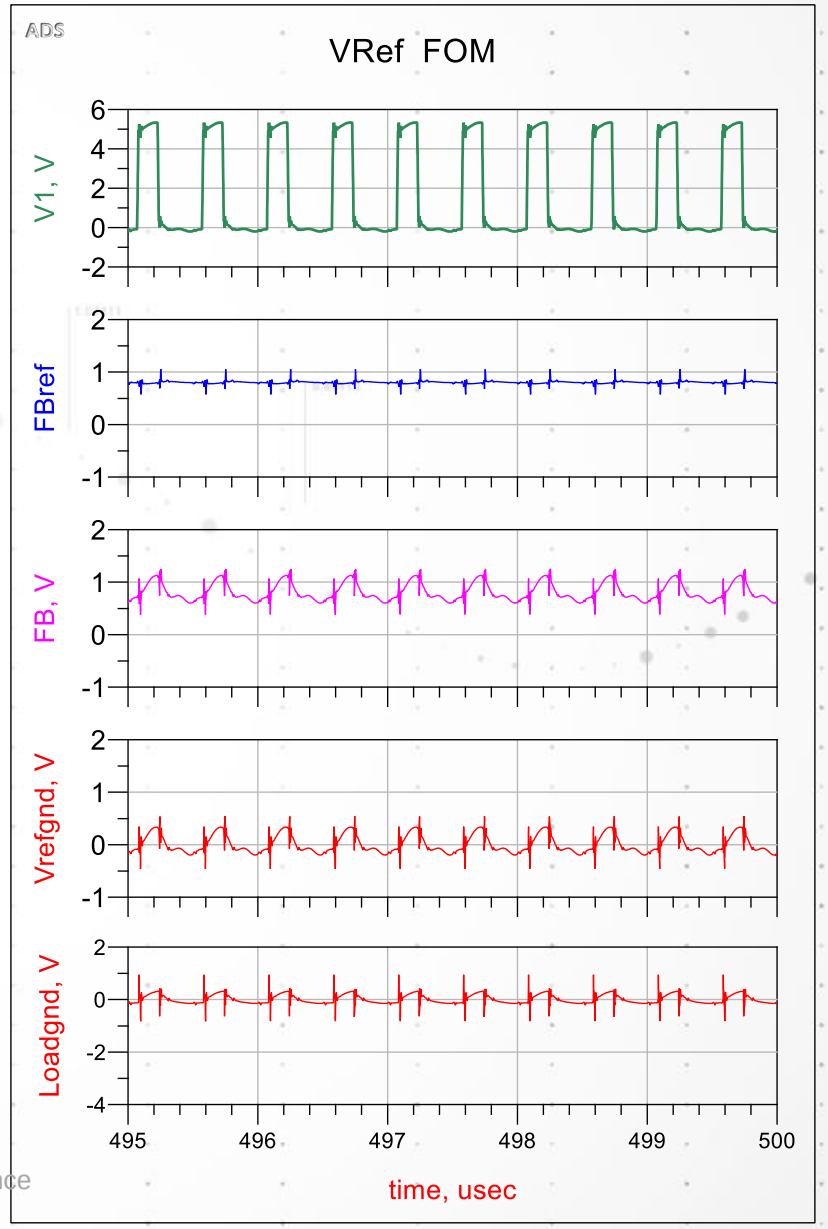
1. High current path coupling to the FB loop is reduced so noiseA ~noiseB
2. The controller ground is tied tightly to the load ground. Little other non-feedback current flows thru the connection so that Loadgnd ~ Vrefgnd
3. To accomplish 1 & 2, grounding is actually reduced!

Simulated Results Show Improvement

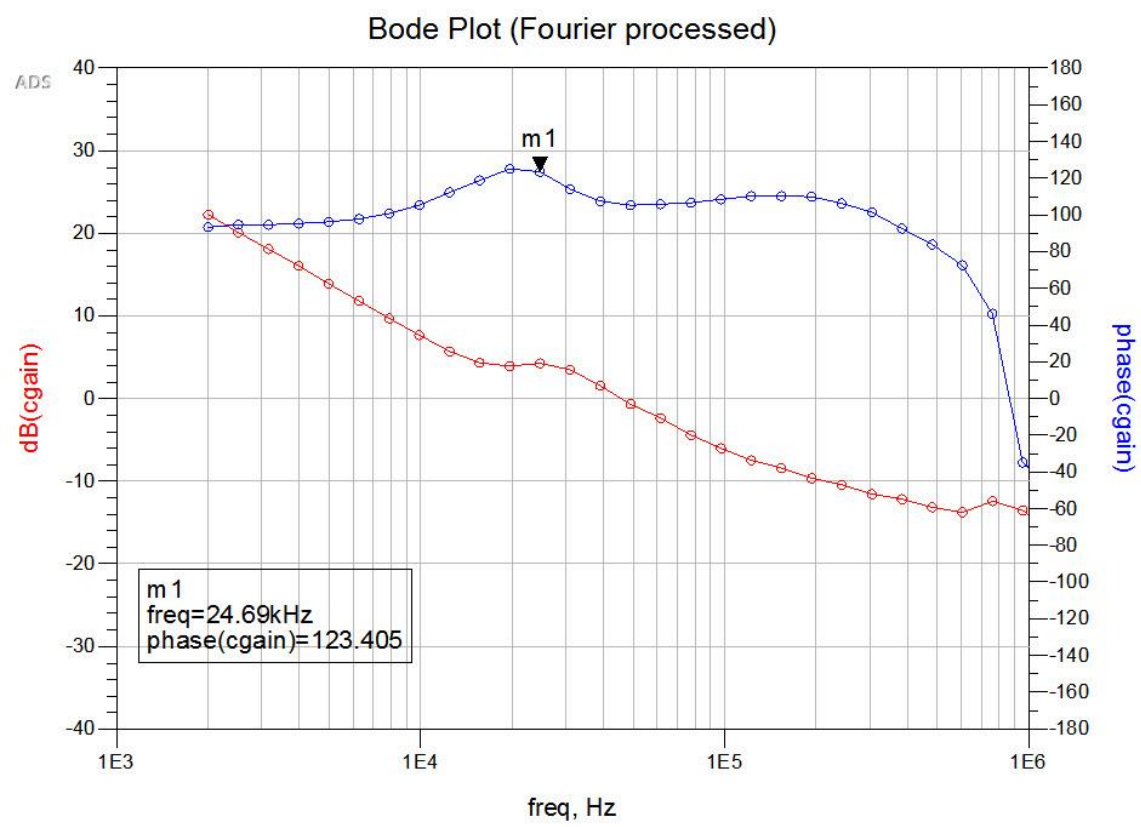
THE FOM AND FB VOLTAGE IS BETTER



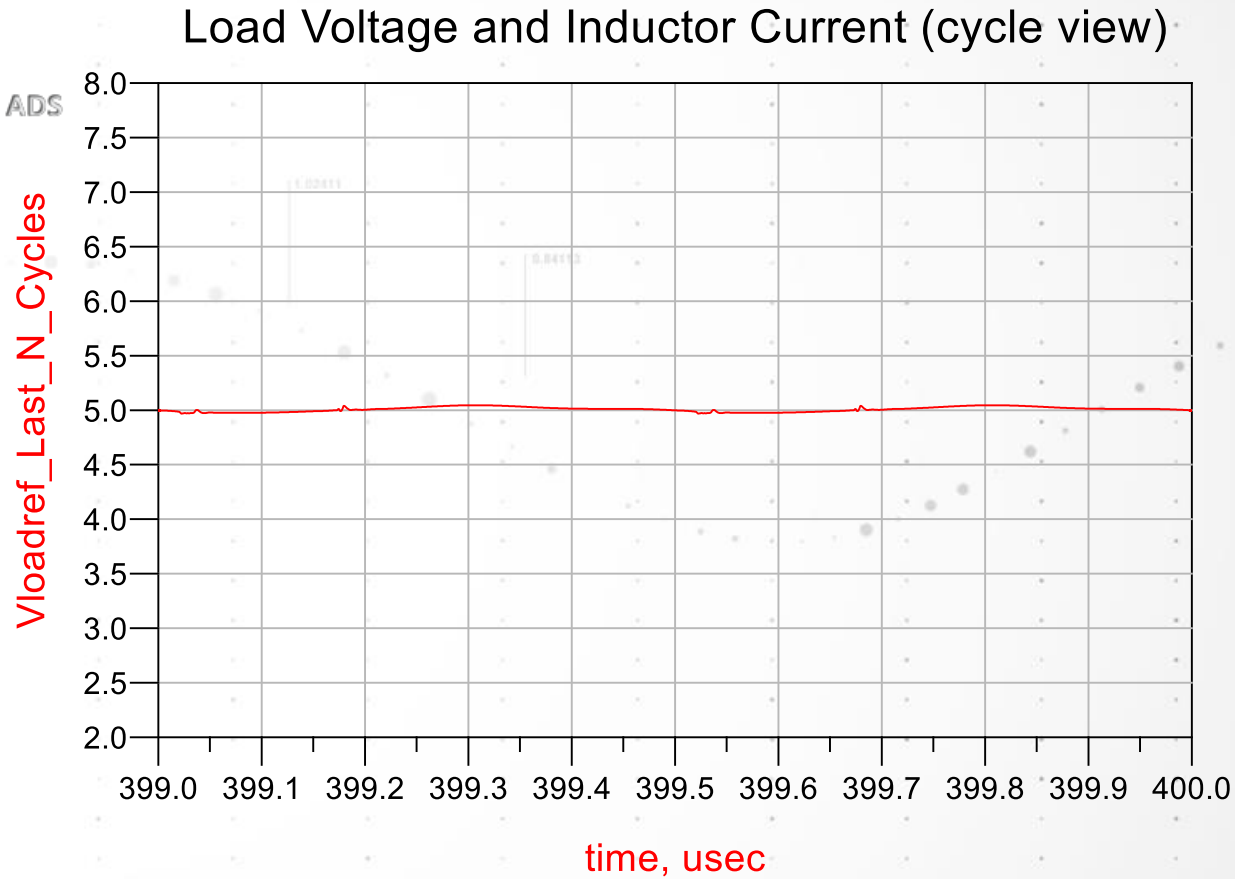
Using the FOM simulation, we do not have to re-run the Bode Plot verification simulation until we get the FOM where we need it to be and the pulse widths are uniform.



Results Now Are Satisfactory



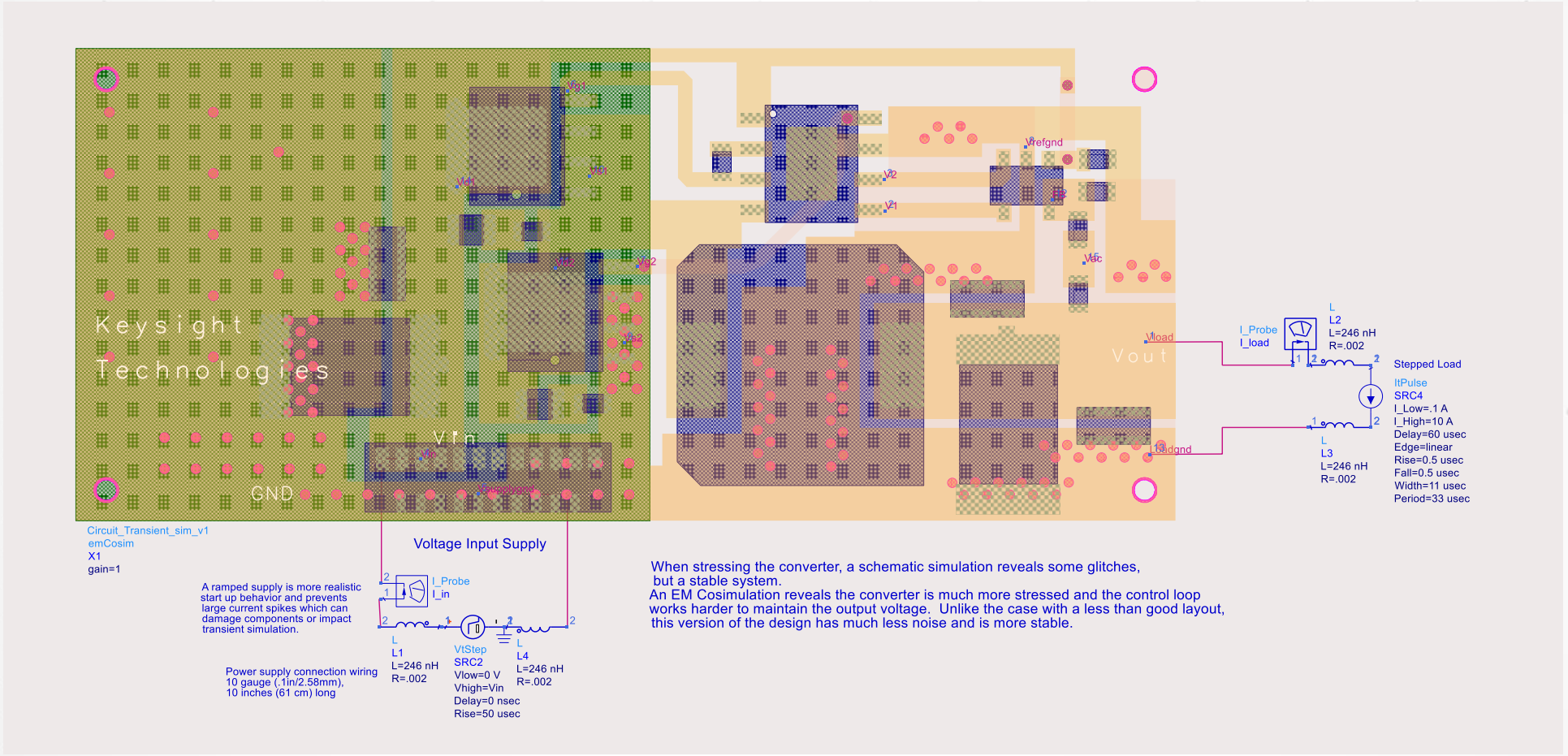
Bode response is much closer to schematic simulation



The output of the SMPS is “clean”

One More Verification

DYNAMIC LOAD RESPONSE

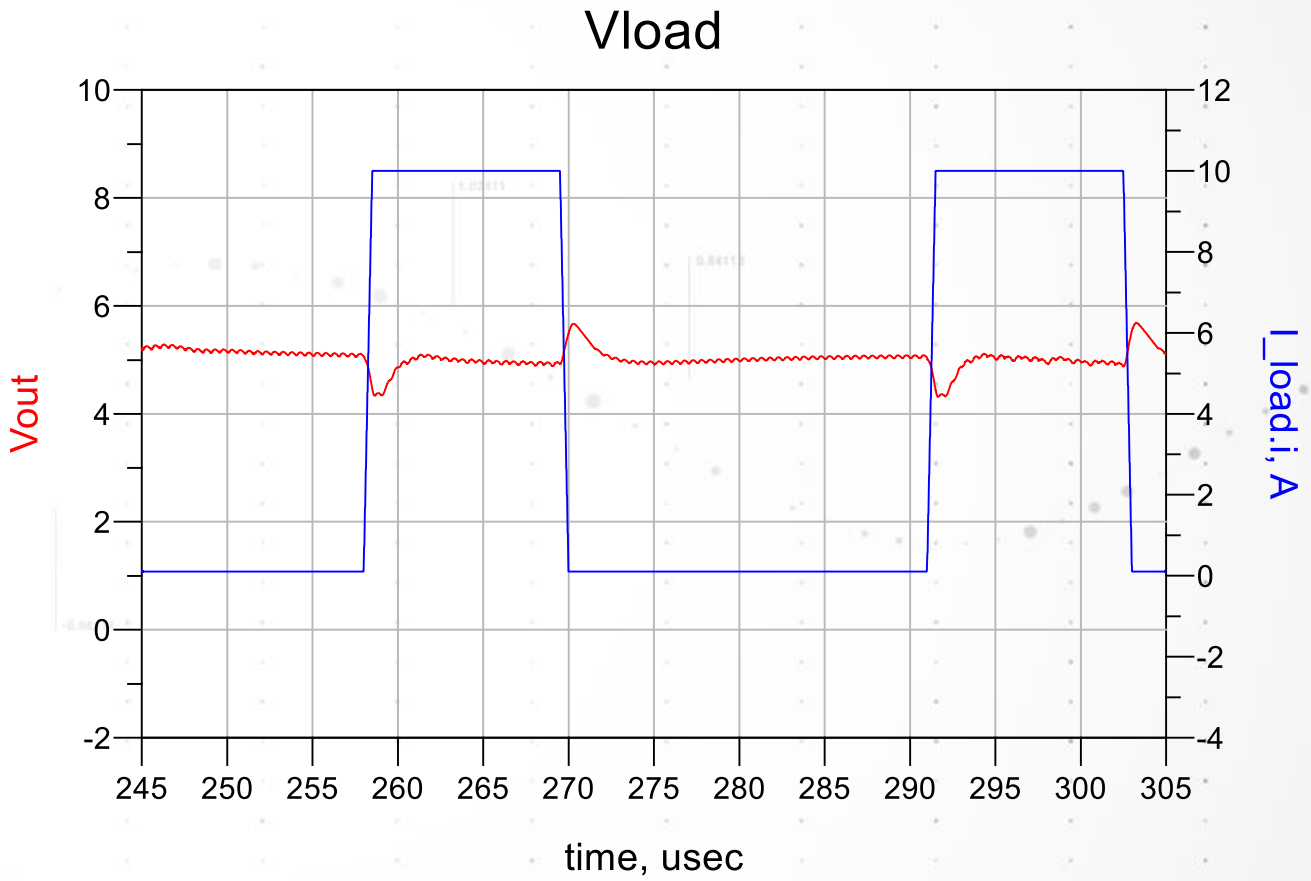


- Test stability under dynamic conditions (varying load)
- This is a quick and easy test

Dynamic Load Response

THE TRANSIENT RESPONSE IS ACCEPTABLE

- Acceptable overshoot
- No ringing or oscillations



NISM – NON INVASIVE STABILITY MEASUREMENT

KILLING THE BODE PLOT – STEVE SANDLER (PICOTEST) – DESIGNCON2016

NISM – Non Invasive Stability Method

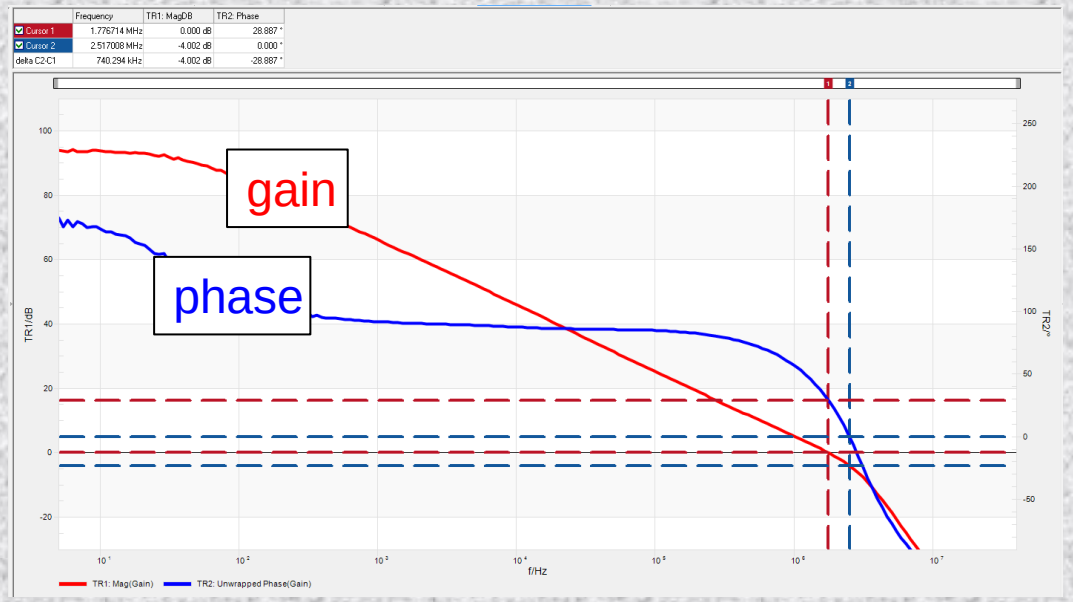
THE BODE PLOT'S DAYS ARE NUMBERED

R.I.P.

The worlds most popular stability assessment test

Rest in Peace

1947-201?



The first problem is that the Bode plot is a *POOR* indicator of *RELATIVE* stability.

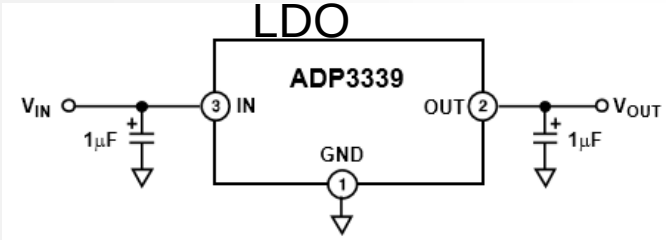
Another problem is that the measurement requires us to inject a signal into the loop. Many devices simply don't provide access to the loop.

NISM – Non Invasive Stability Method

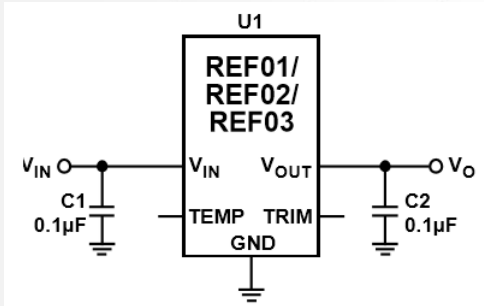
WHY ARE BODE PLOTS BECOMING IRRELEVANT

Poor or No Control Loop Access

3.3V/1.5A LDO

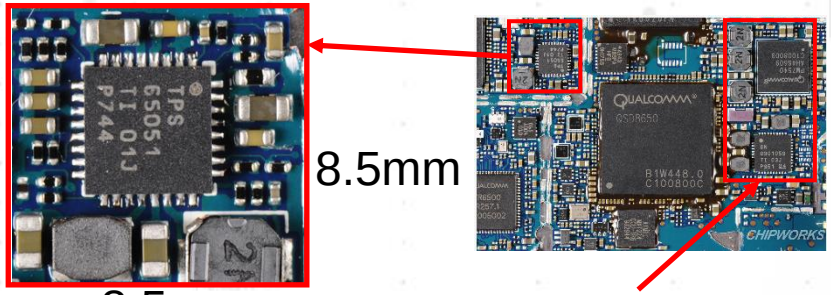


Fixed regulators/references don't allow access to the control loop



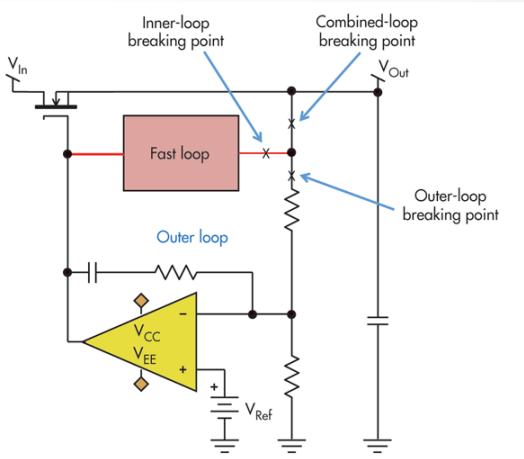
In other cases, we might not have physical space to inject into the loop or their might be a large number of power supplies

6 output power supply



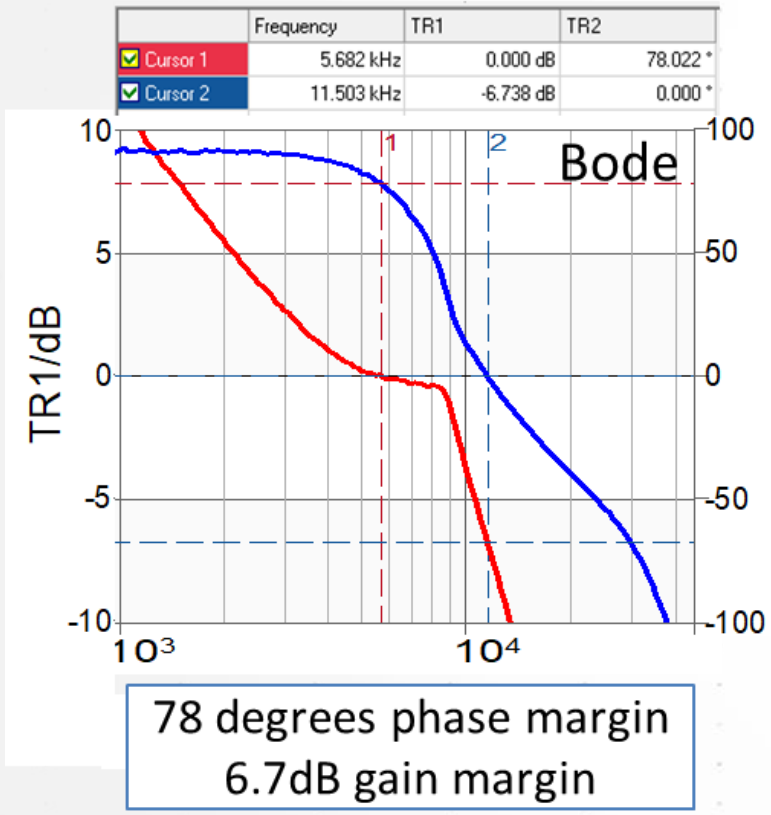
Or we might not want to gain access because it requires cutting a trace or a wire

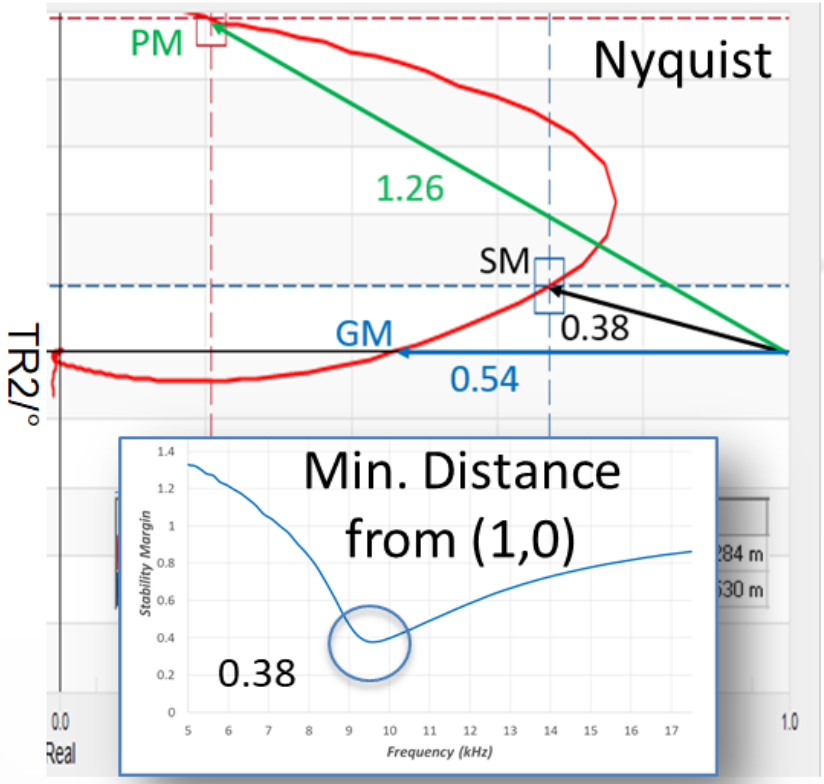
Multiple or Digital Control Loops



NISM – Non Invasive Stability Method

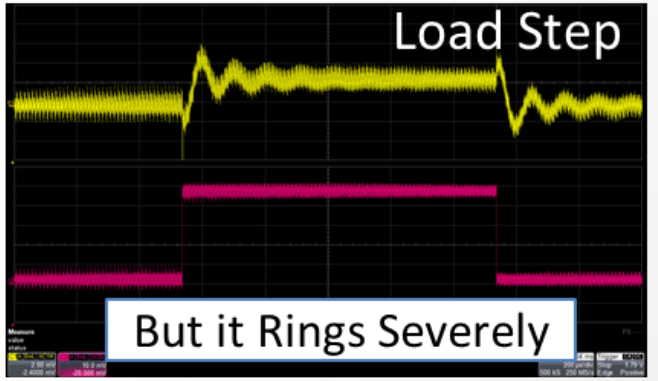
A DC-DC CONVERTER EXAMPLE





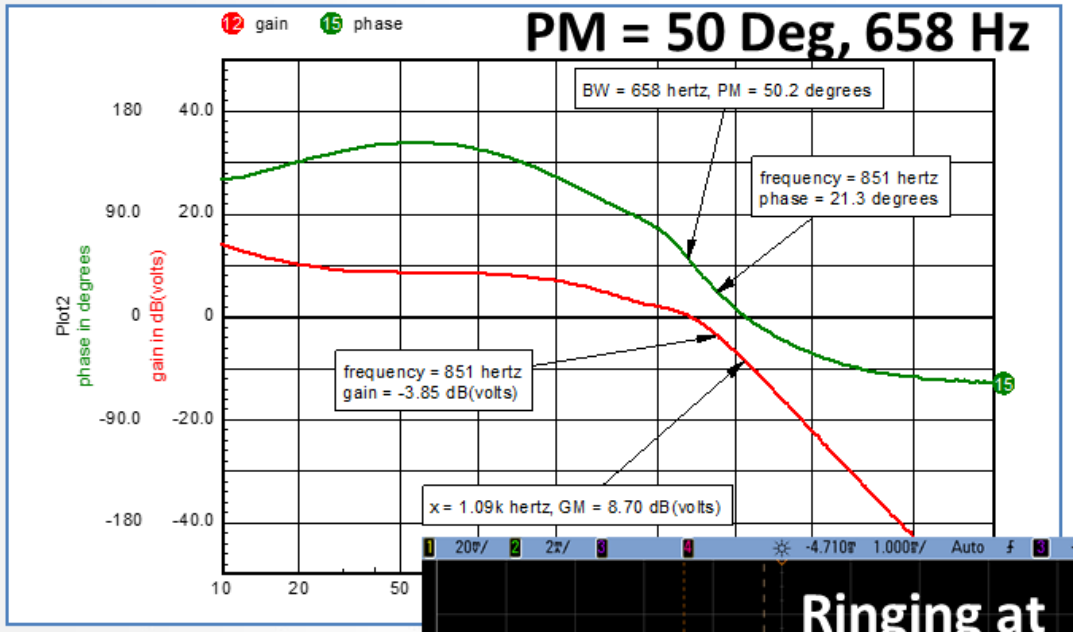
What's Interesting

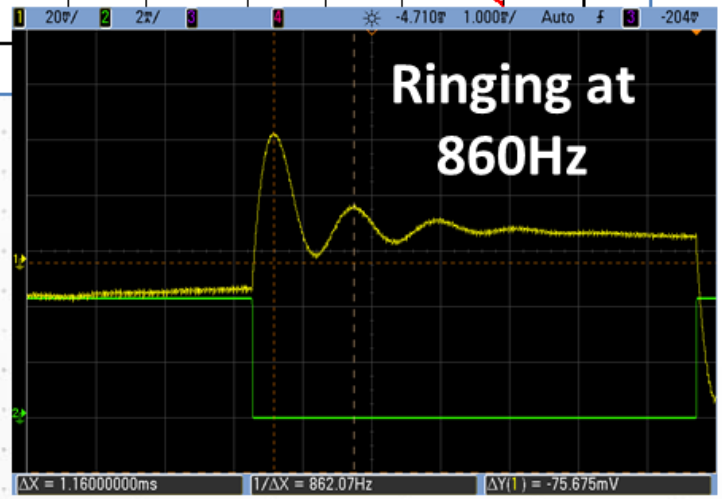
- Bode & Nyquist - same data
- Bode didn't indicate stability
- Scope Owners: load step ringing may or may not indicate a stability issue
- Must use a Closed Loop Test → Nyquist, Impedance, etc.



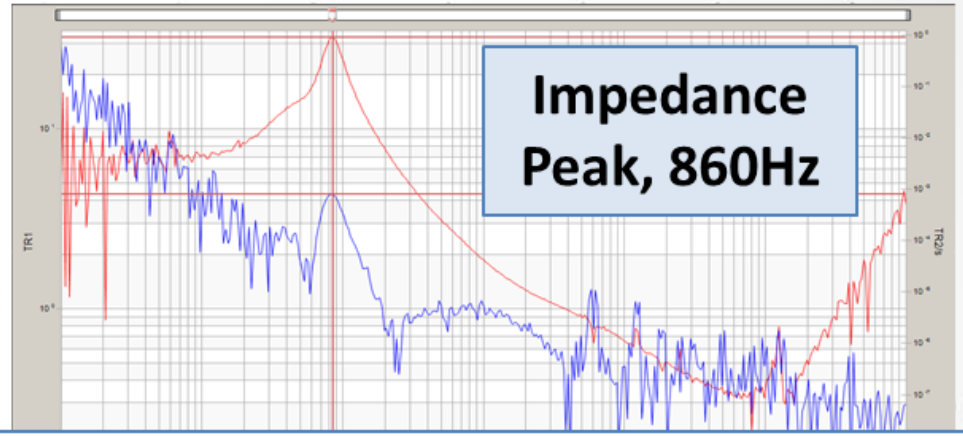
NISM – Non Invasive Stability Method

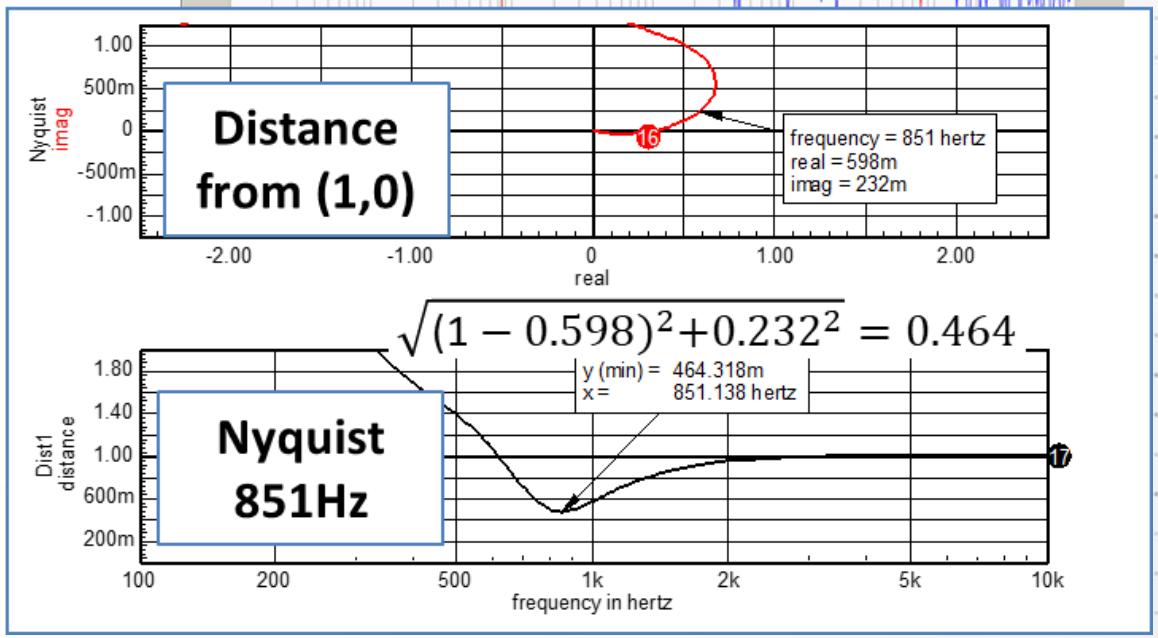
OUTPUT IMPEDANCE IS AS GOOD AS NYQUIST





Flyback Converter

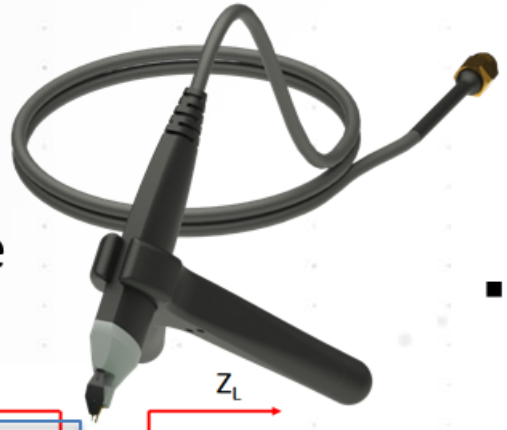


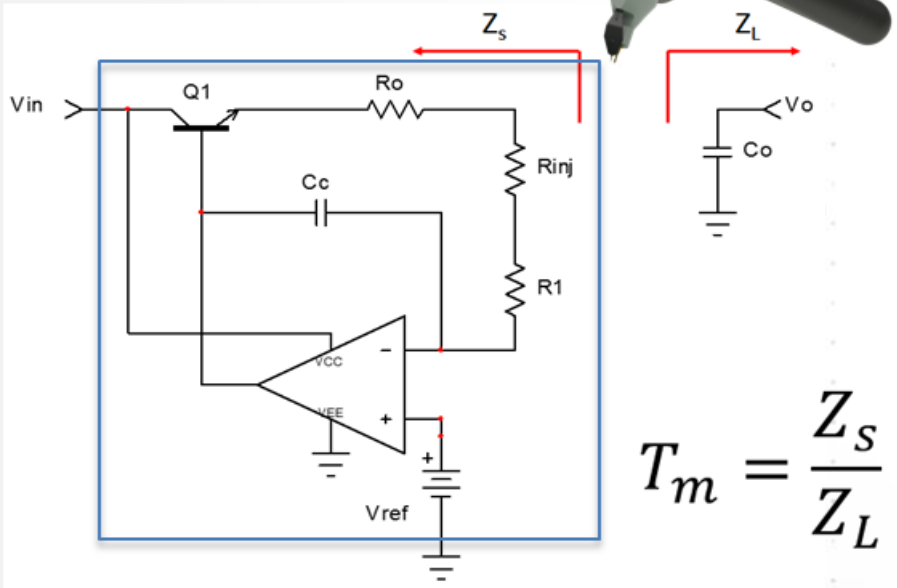


NISM – Non Invasive Stability Method

HOW TO MEASURE NISM

Yes. You can measure phase margin from a single measurement





$$T_m = \frac{Z_s}{Z_L}$$

- From 1 Impedance Measurement - 3 data points
  - Impedance Magnitude, Phase, and Group Delay
- The NISM software extracts data from output impedance and the 'Q' via group delay and allows the Z_S and Z_L to be mathematically determined so they can be converted to Stability Margin
- Phase margin is determined by setting |Tm| = 1 and solving for phase

NISM – Non Invasive Stability Method

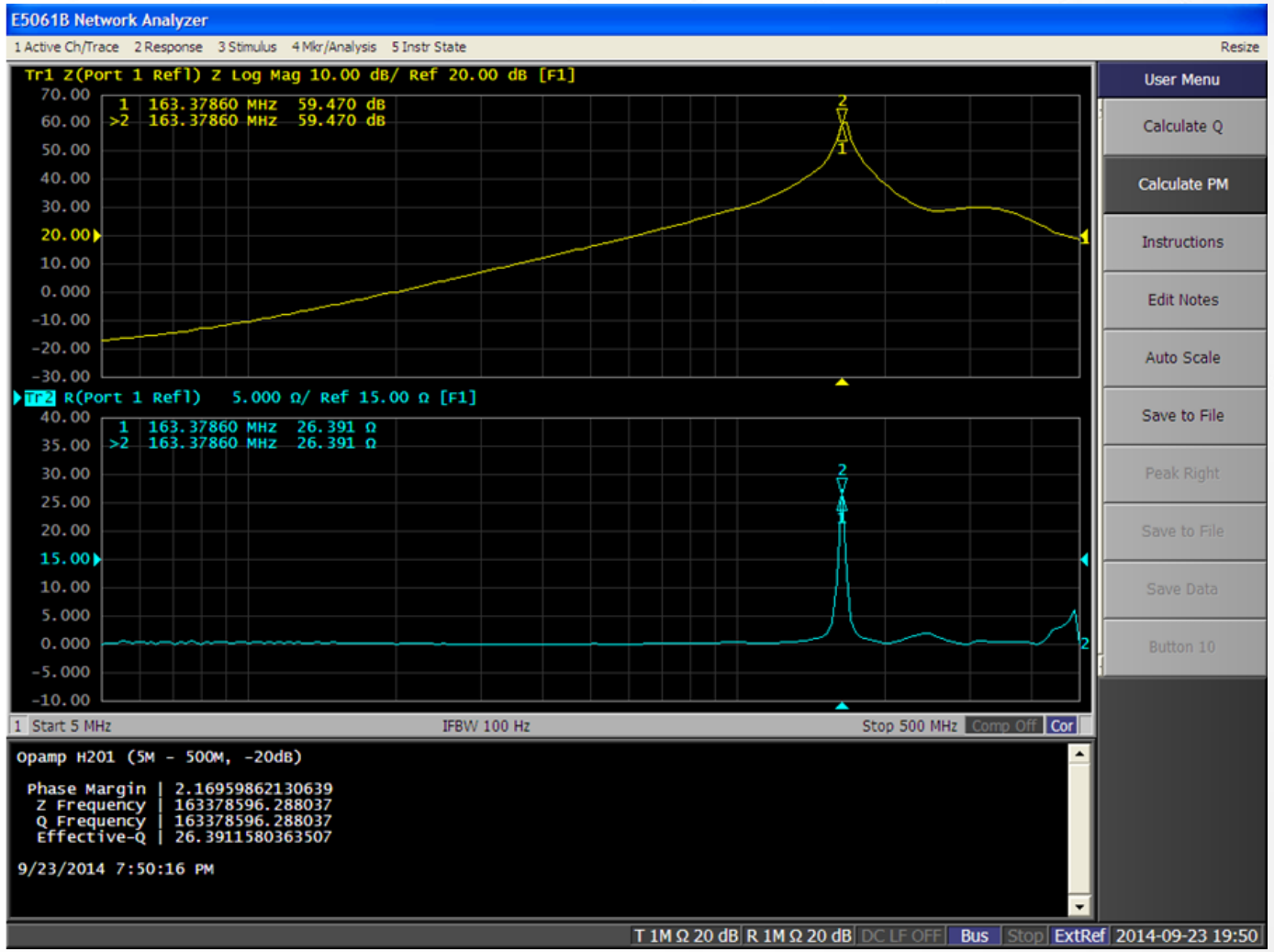
HOW TO MEASURE NISM

- Step 1: Measure Impedance
- Step 2: Set Cursors

Practically speaking, output impedance is measured with a suitable probe in a 1 or 2 port configuration

The software converts the impedance to group delay and Q

The user positions waveform cursors on the impedance and Q waveforms and the conversion to phase margin is read out on the instrument's screen



Conclusions

- On-paper designs – no longer sufficient.
- Noise from switching and layout parasitics – leads to problems.
- Techniques shown enable insight and better performance
- NISM shows a practical method for assessing stability without tone injection

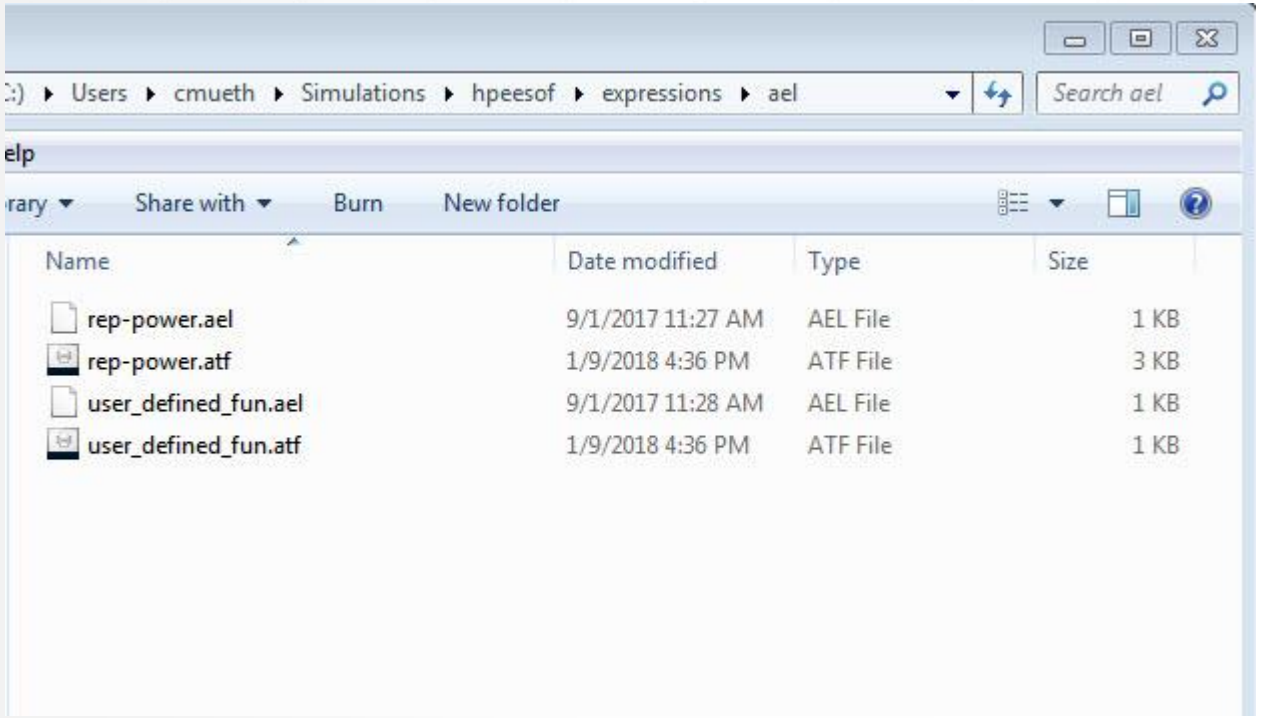

KEYSIGHT
TECHNOLOGIES

Appendix

Processing Tone

AEL EXPRESSION FOR POST PROCESSING

Location of AEL files



AEL expression call within the data display

```
Eqn Vinject=Vacstability-Loadgnd
Eqn Vloop=Vloadstability-Loadgnd
```

Includes local ground reference

```
Eqn cgain=rep_cgain(Vinject, Vloop, 500u, 1, 5)
```

Analyze cycles with 500 uSec simualtion tone delay,
one cycle post processing delay, 5 cycles of analysis