Power Electronics Device & System Development based on Real-Time Simulation and Testing

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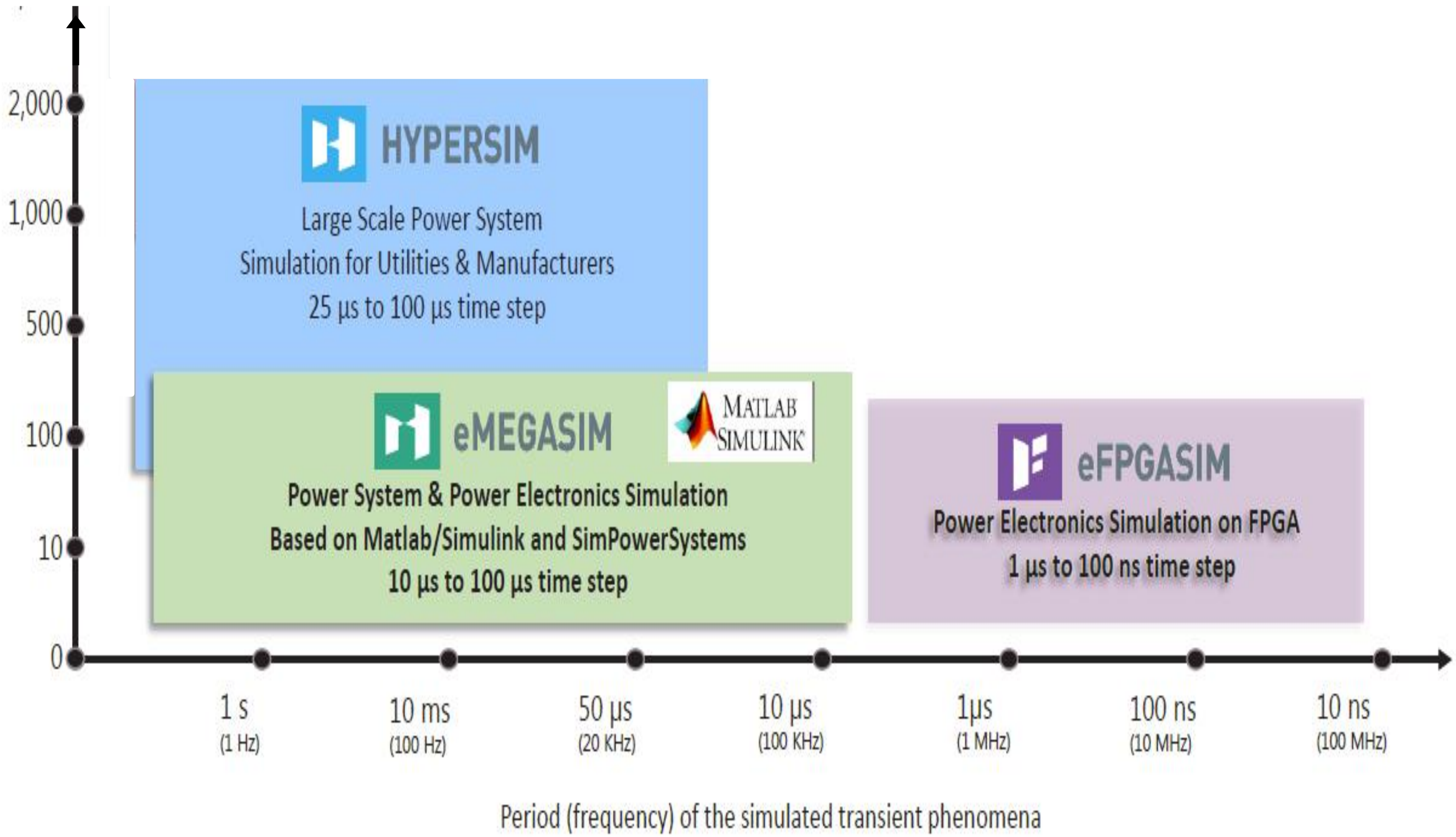
Content

- Real Time Systems and Application
- Microgrid system and control development based on Pure Real-Time Simulation
- PV Controller Hardware-in-the-Loop Simulation and Testing
- Power Hardware-in-the-Loop Simulation and Testing

RT Simulators in DERSIL

- OP5600 Platform
  - 12-core CPU
  - 64 Analog & 64 Digital IO
  - Voltage/Current Interface
- Server Platform
  - 32-Core CPU
  - OP 5706 with FPGA Board
  - 32 Analog & 64 Digital IO

Modeling for RT Simulation



(From Opal-RT)

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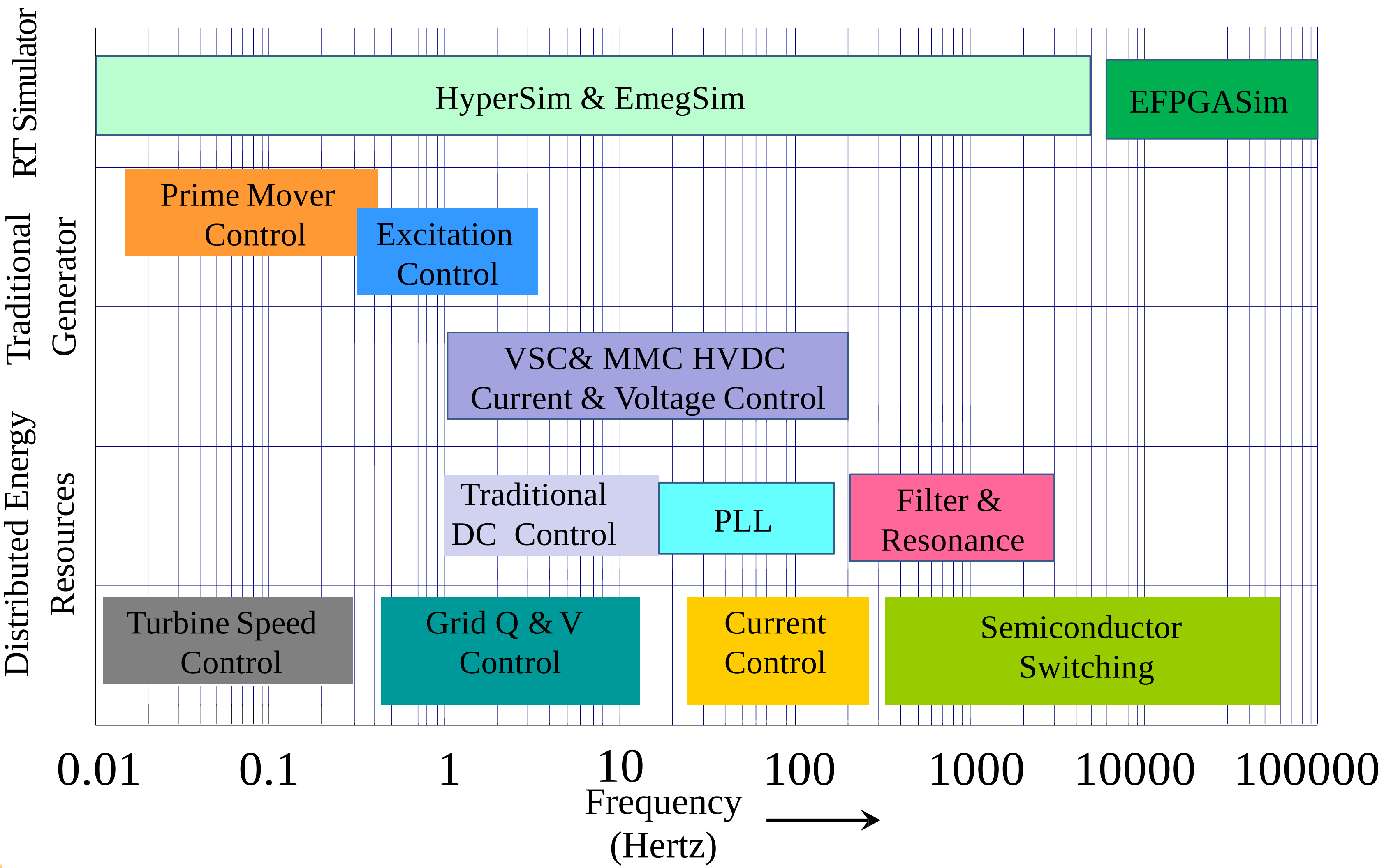
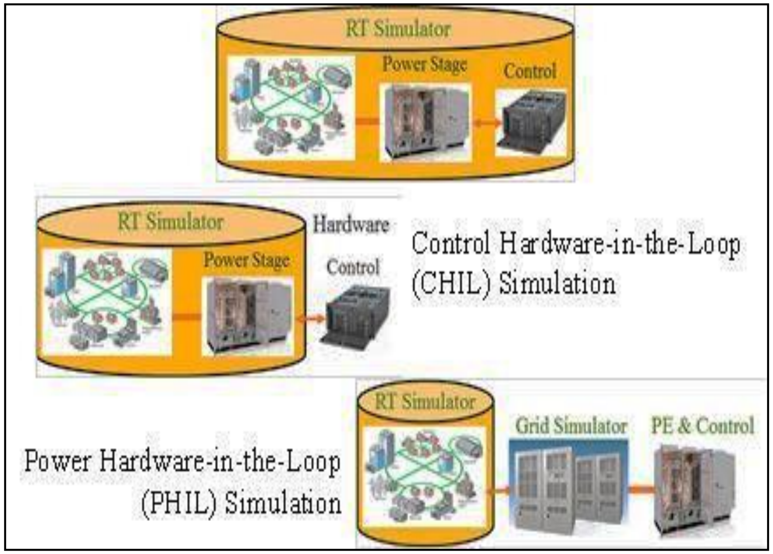
Application of RT Simulation



From Real Time to HIL

- Pure RT Simulation
  - Up to 4000 Nodes at 50 μs Time Step
- Controller HIL
  - Down to 200 ns Time Step Based on FPGA
- Power HIL
  - Up to 45kW



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RT & Faster Than RT Simulation

- Minimum Time-Step & Complexity or Size of the System
- Shortcomings
  - Vulnerable to Instability from Non-Linear Events
  - Restricted Accuracy due to Fixed Time-Step
- Advantages
  - Strong Calculation Capability
  - Interconnection with Hardware

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Application of RT Simulator

- Pure RT or Faster then RT Simulation
  - Deterministic or Statistic Analysis
  - Rapid Control Prototyping
- Controller Hardware-in-the-loop Simulation & Testing
  - Verify Real Controller
- Power Hardware-in-the-loop Simulation & Test
  - Verify System & Hardware

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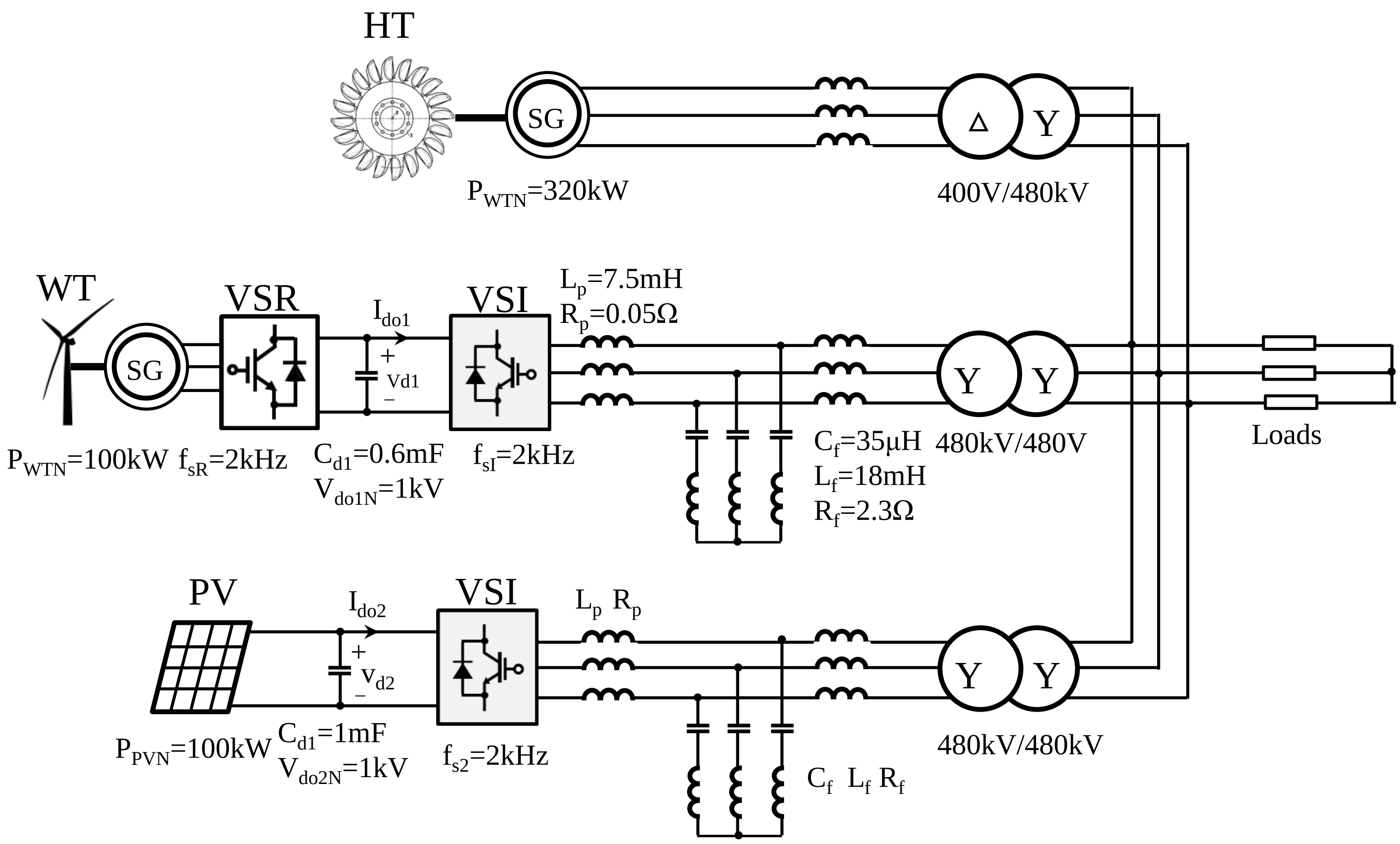
Hydro- Microgrid Configuration



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System Operation Modes

- Master-Slave Cooperative Control
  - Voltage & Frequency is Regulated by Hydro Turbine
    - PV & WT work in MPPT mode
- Full Droop Control
  - Voltage & Frequency Control is dominant by Hydro-Turbine
    - PV & WT work in Droop Power Control

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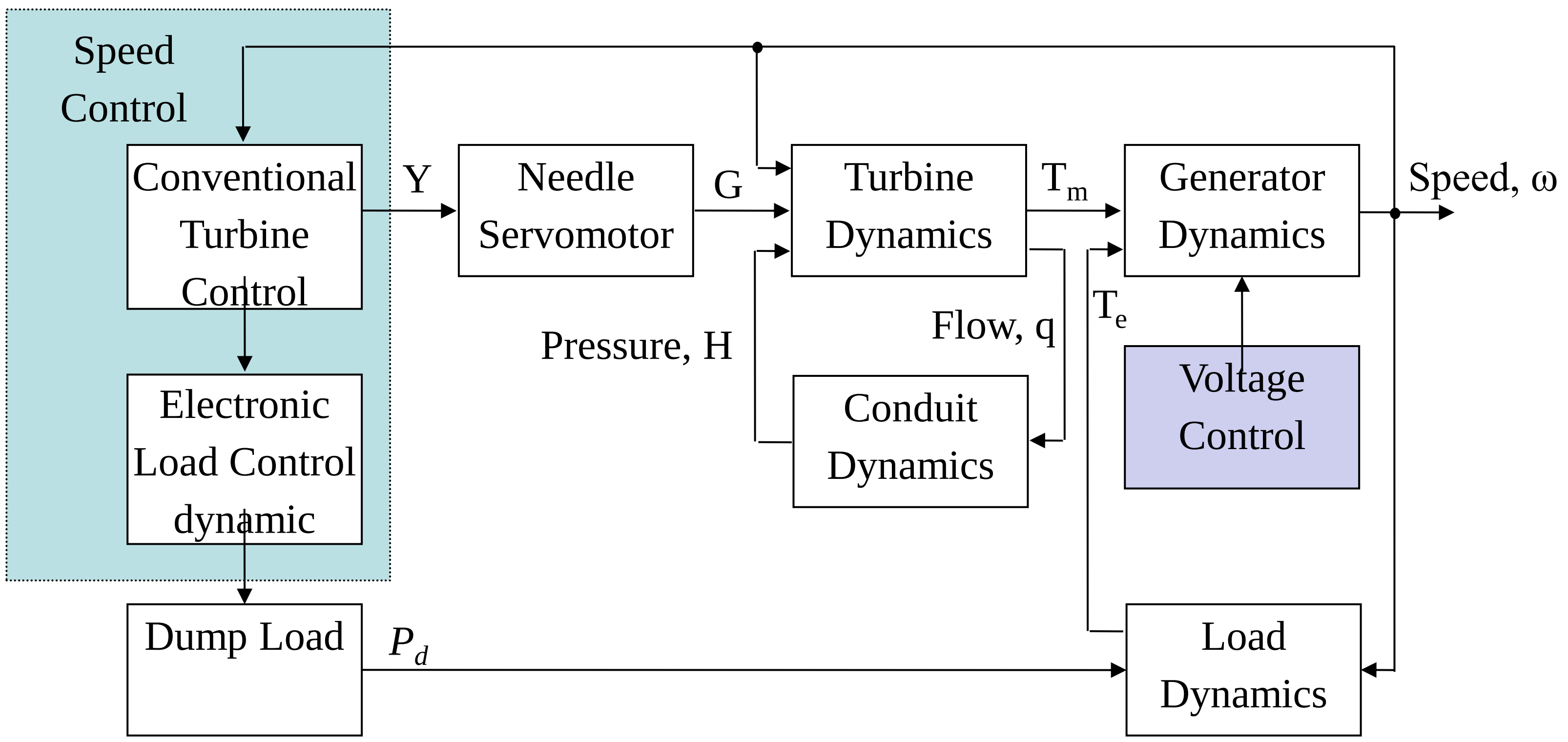
Hydro Turbine Function Diagram



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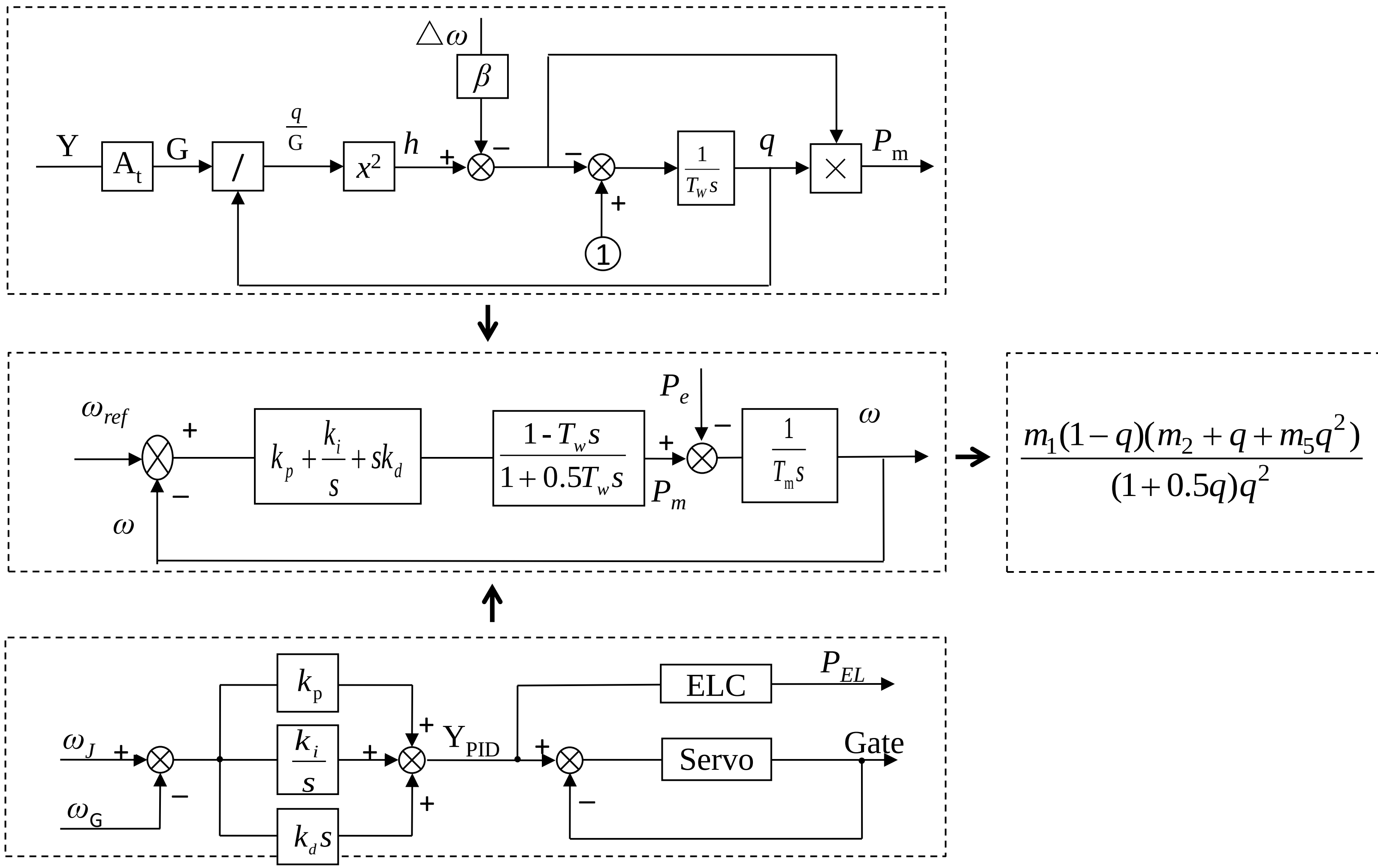
Hydro Turbine Transfer Function



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Hydro Turbine Operation & Control

- PID Controller
  - Stability & Routh-Hurwitz Criterion
    - Root Loci Analysis
    - Transient Analysis
    - Bandwidth Frequency and Relative Stability
  - Dynamic Response: Overshoot, Response Time
- EL Controller
  - Response for Dynamic Operation
  - Corporate with the PID Controller
    - Cutoff Frequency

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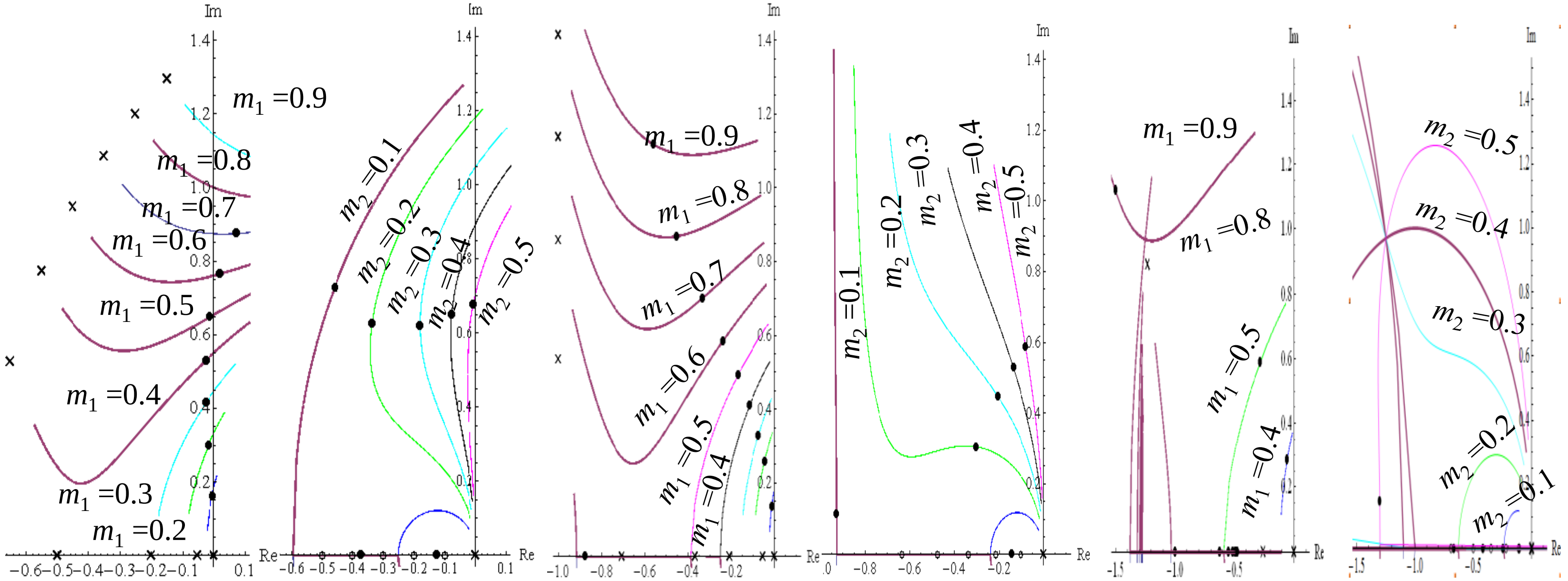
Root Loci for HT Stability

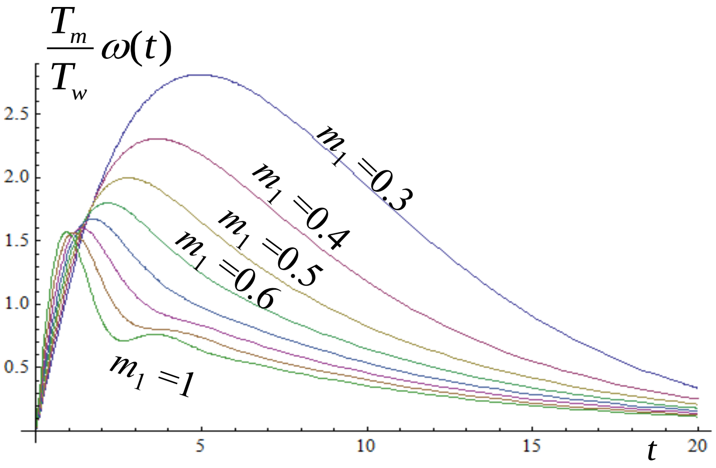
- Reasonable Range: $0<m_1<0.9$, $0.1<m_2<0.5$, $m_5>0$



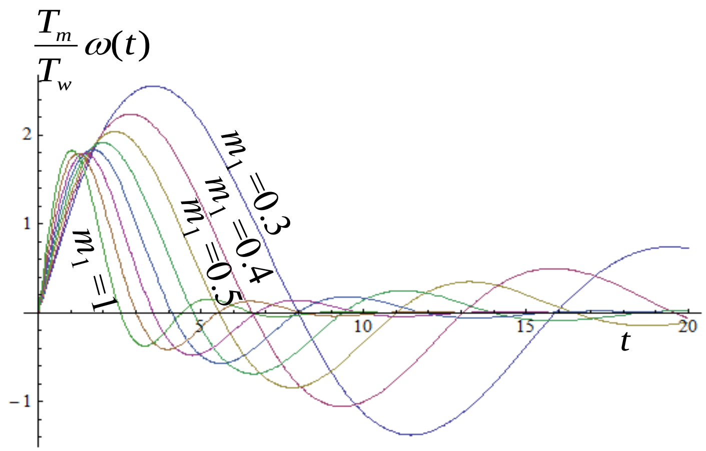
increasing m_2 increasing m_1 increasing m_2 increasing m_1 increasing m_2 Increasing m_1

m_5=0 m_5=1/3 m_5=0.4

Transient & Relative Stability



m_2=0.2, m_5=1/3



m_2=0.4 m_5=1/3

Design Parameters (m_1,m_2,m_5)	**Phase Margin**	**Gain Margin**
(0.8, 0.3, 1/3)	22º	5dB@100Hz
(0.8, 0.1,0.5)	35º	2dB@100Hz
(0.8, 0.2, 0.5)	35º	2dB@100Hz
(0.8, 0.3, 0.5)	30º	1.2dB@100Hz

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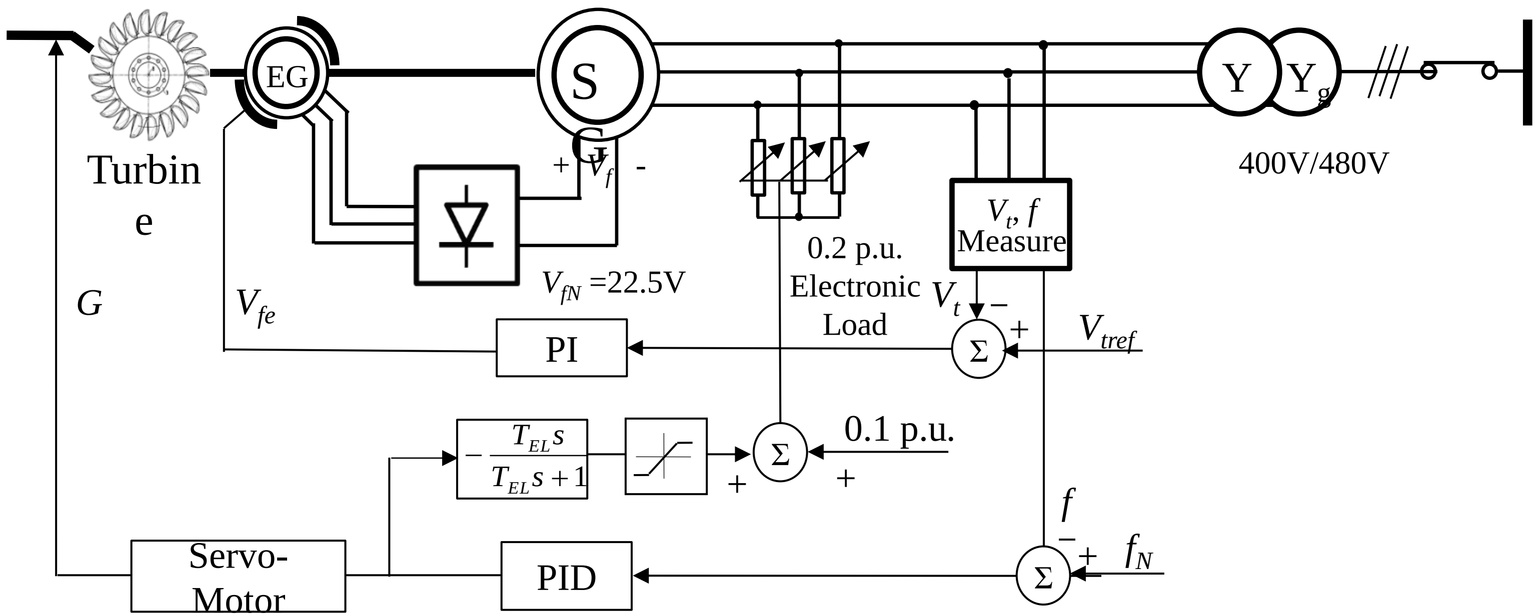
Hydro Turbine Subsystem Control



Turbine & Generator	Value	Unit
Turbine Rated Power.	350	kW
Generator Power	320	kW
Exciter Rated Power	8	kW

Control Design	Parameters
PID Controller (kp, ki, kd)	5.03, 2.79, 1.35
PI Controller (kp,ki)	10, 8
EL Controller (T_{EL})	1.6

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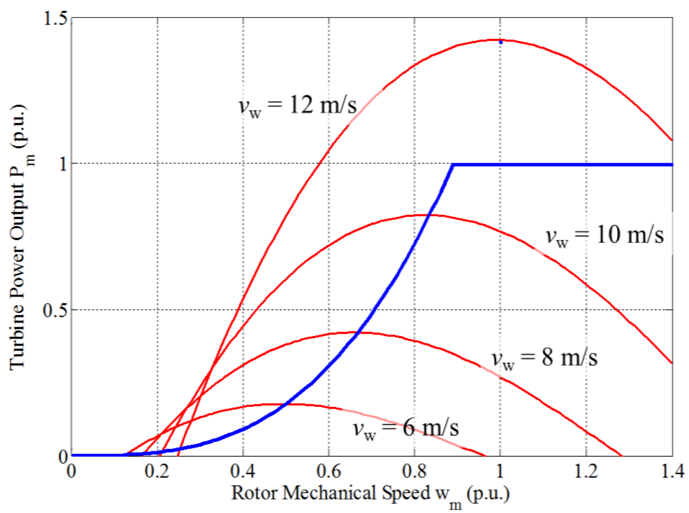
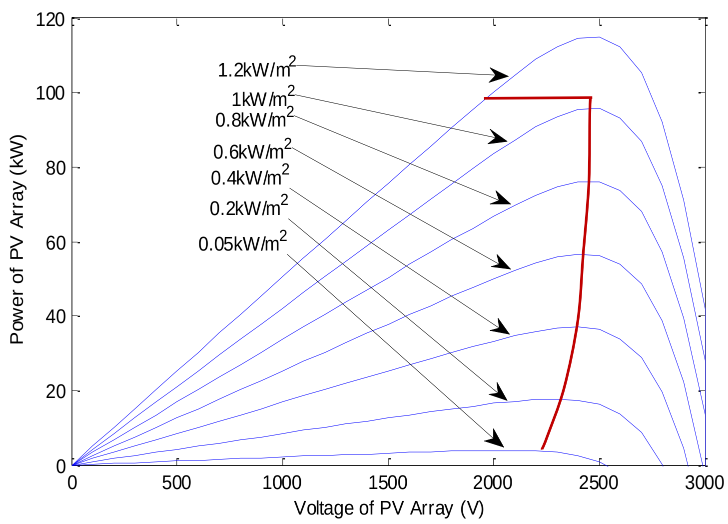
Wind Turbine & PV MPPT

- Wind Turbine

$$P_{mech} = \frac{\rho}{2} A_r V_w^3 C_p(\lambda, \theta_{pitch}) = k_{WT1} V_w^3 C_p\left(\frac{k\omega_r}{V_w}, \theta_{pitch}\right)$$

- PV





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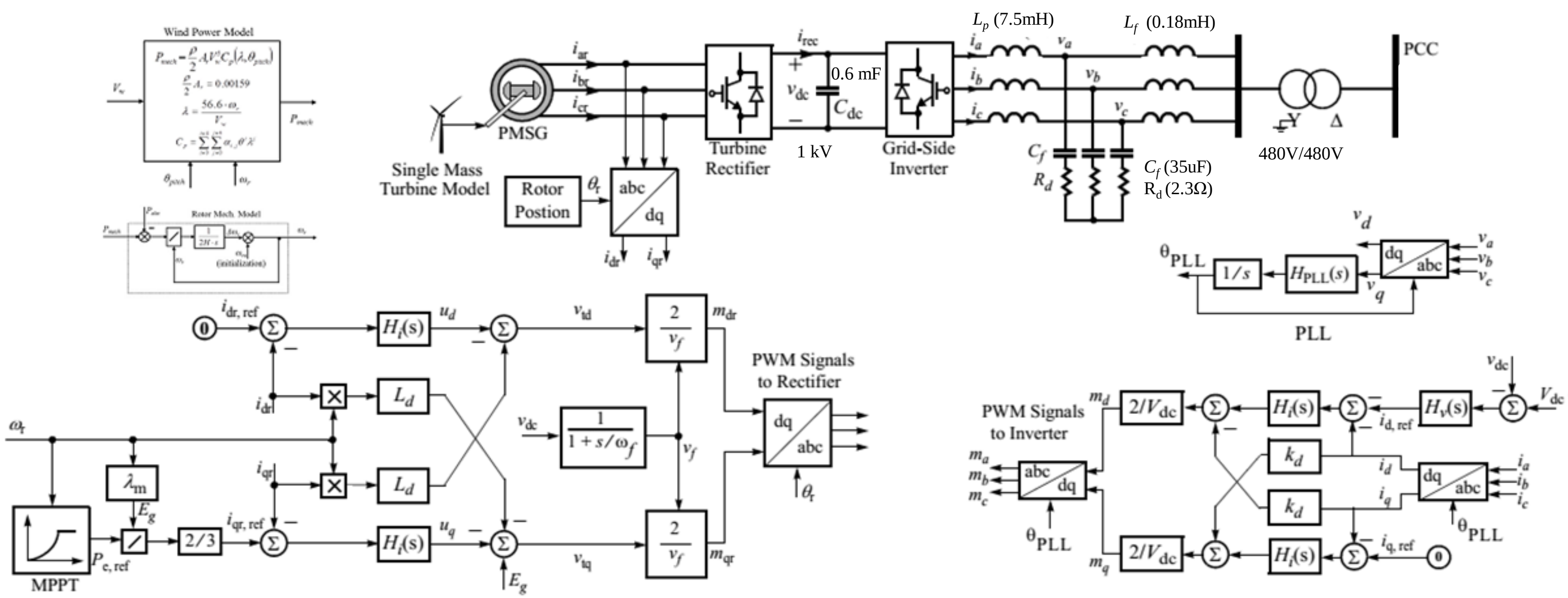
Wind Turbine Subsystem



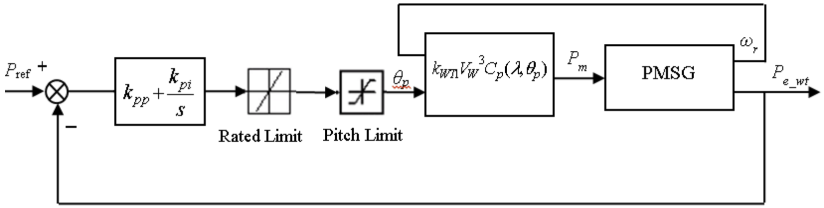
PMSG Parameters	Value	Unit
Rated Volt.	1.25	kV
Poles	96	-
r_s (0.02 p.u.)	0.57	Ω
L_m (0.2 p.u.)	1.2	mH

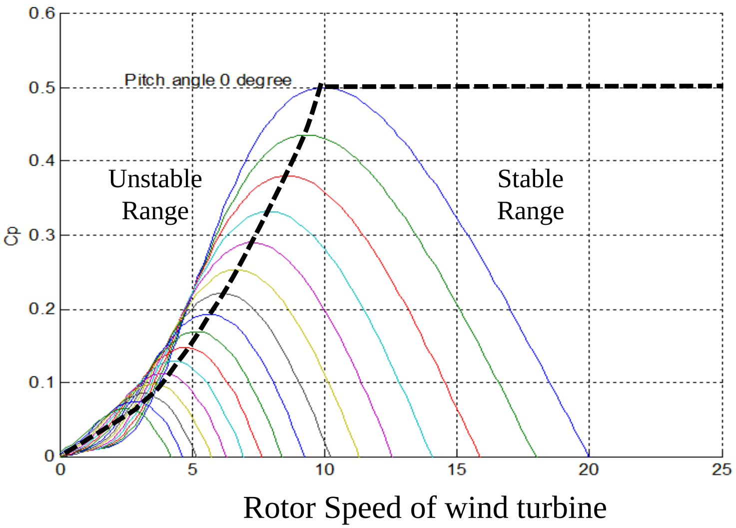
Control Design	Bandwidth (Hz)
Turbine Rectifier Current Control	200
Grid-Side Inverter PLL	30
Grid-Side Inverter Current Control	200
Grid-Side Inverter DC-Bus Voltage Control	20

Control and Stability

- Power Control
  - Pitch angle Regulation
  - Rotor Speed Coordination for Stable Operation

$$\omega_{rCpm} < \omega_r < \omega_{r\max}$$





$$\begin{cases} P_{e\_wt} = P_{e\min},\ \theta_p \text{ is increased till } P_{ref} = P_{e\min} \text{ or } \theta_p = \theta_{p\max} & \text{if } P_{ref} < P_{e\min} \\ P_{e\_wt} = P_{ref},\ \omega_r \text{ changes till } P_m = P_{e\_wt} & \text{if } P_{e\min} \le P_{ref} \le P_{e\max} \\ P_{e\_wt} = P_{e\max},\ \theta_p \text{ is reduced till } P_{ref} = P_{e\max} \text{ or } \theta_p = 0 & \text{if } P_{ref} > P_{e\max} \end{cases}$$

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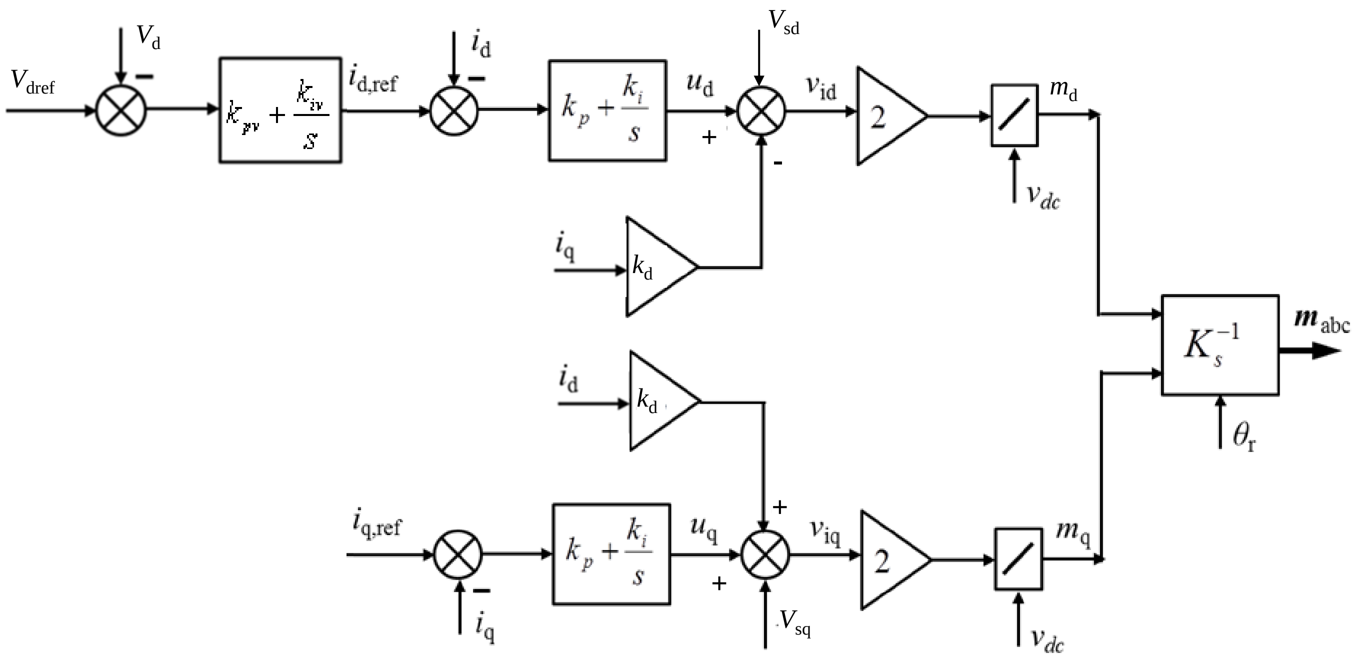
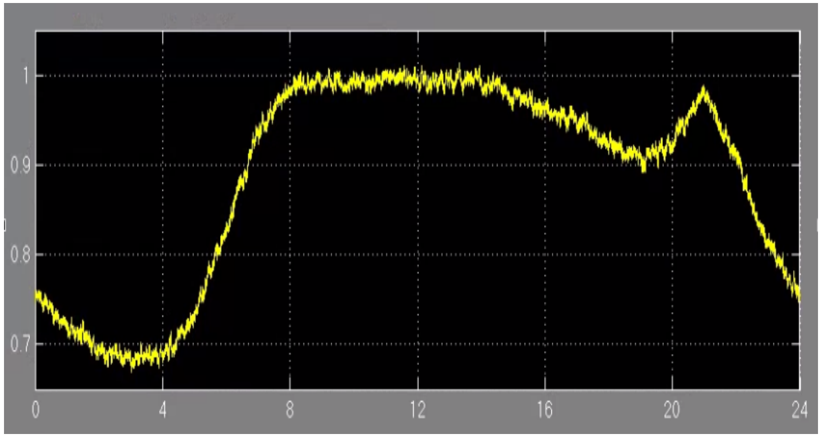
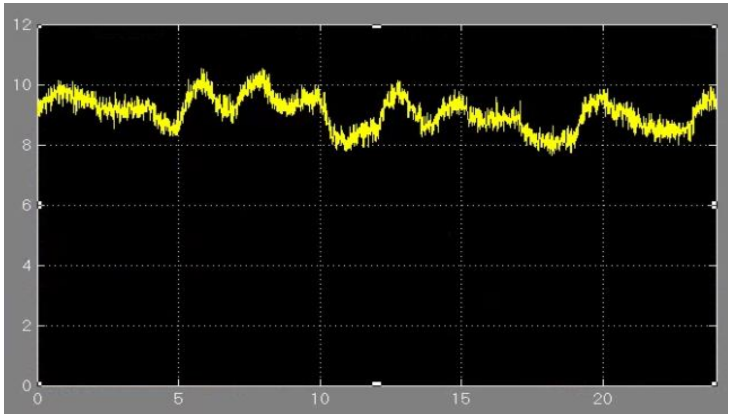
PV VSC Inverter Control



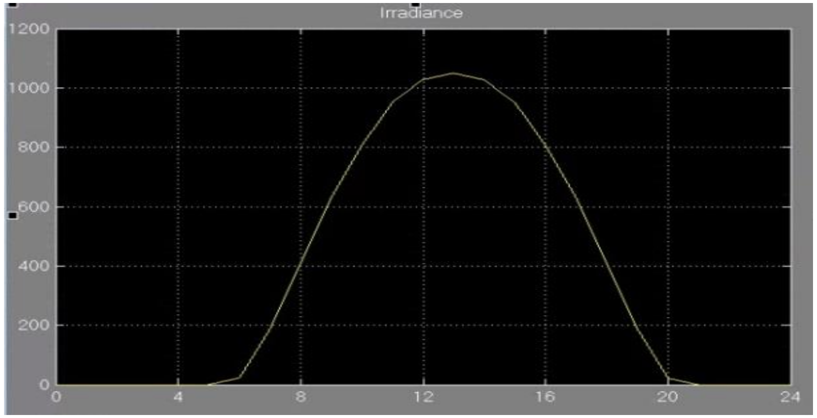
Source & Load Profiles



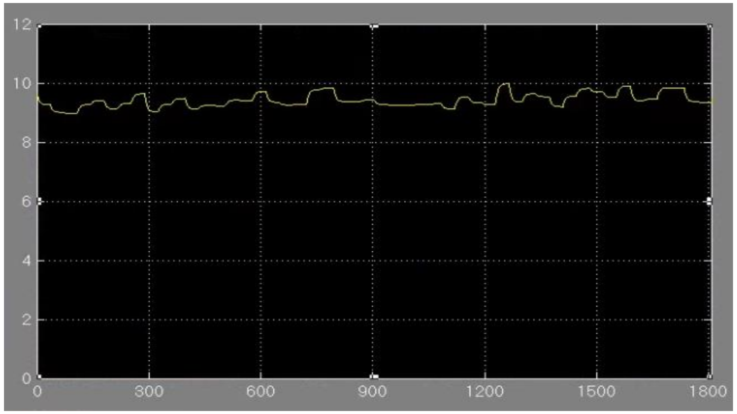
Daily load profile



Wind speed (h)



Irradiance of clear day



Wind speed (s)

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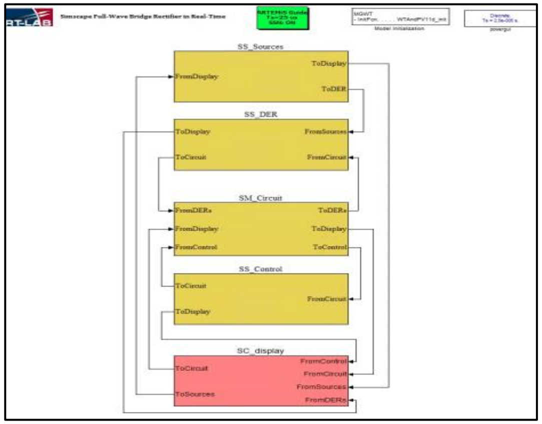
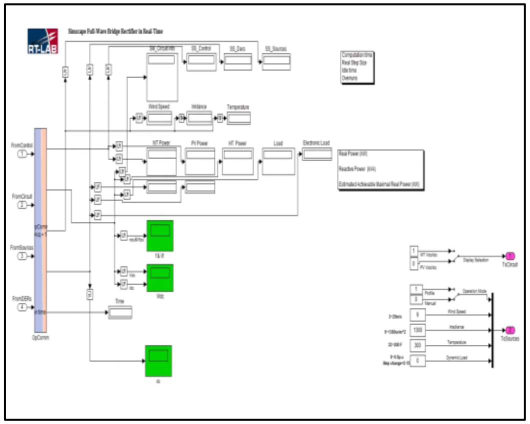
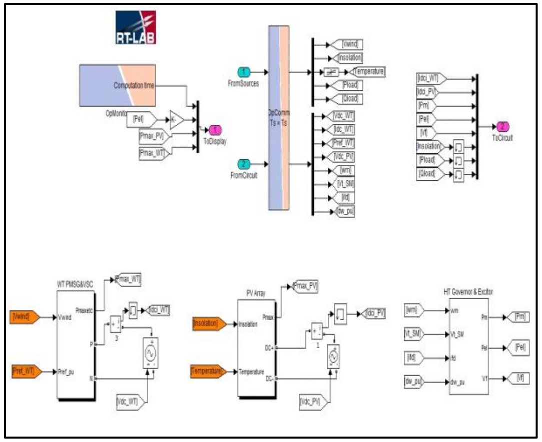
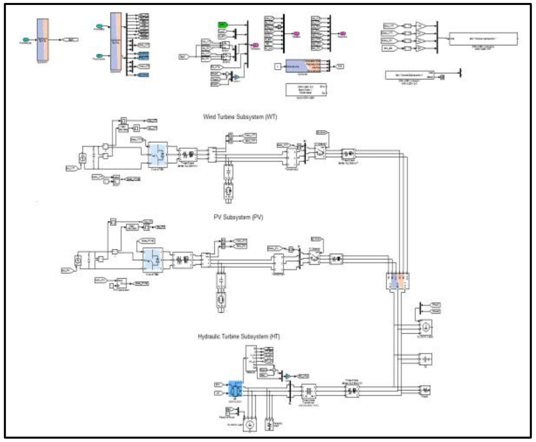
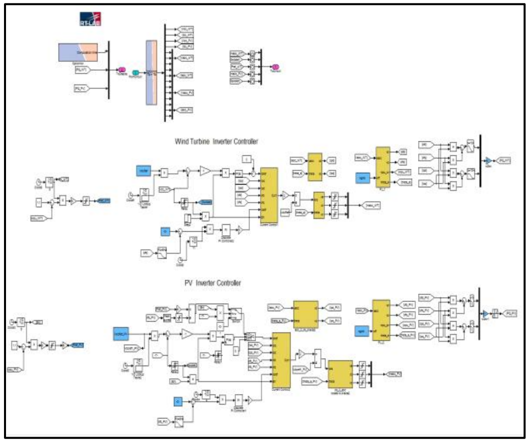
System Modeling



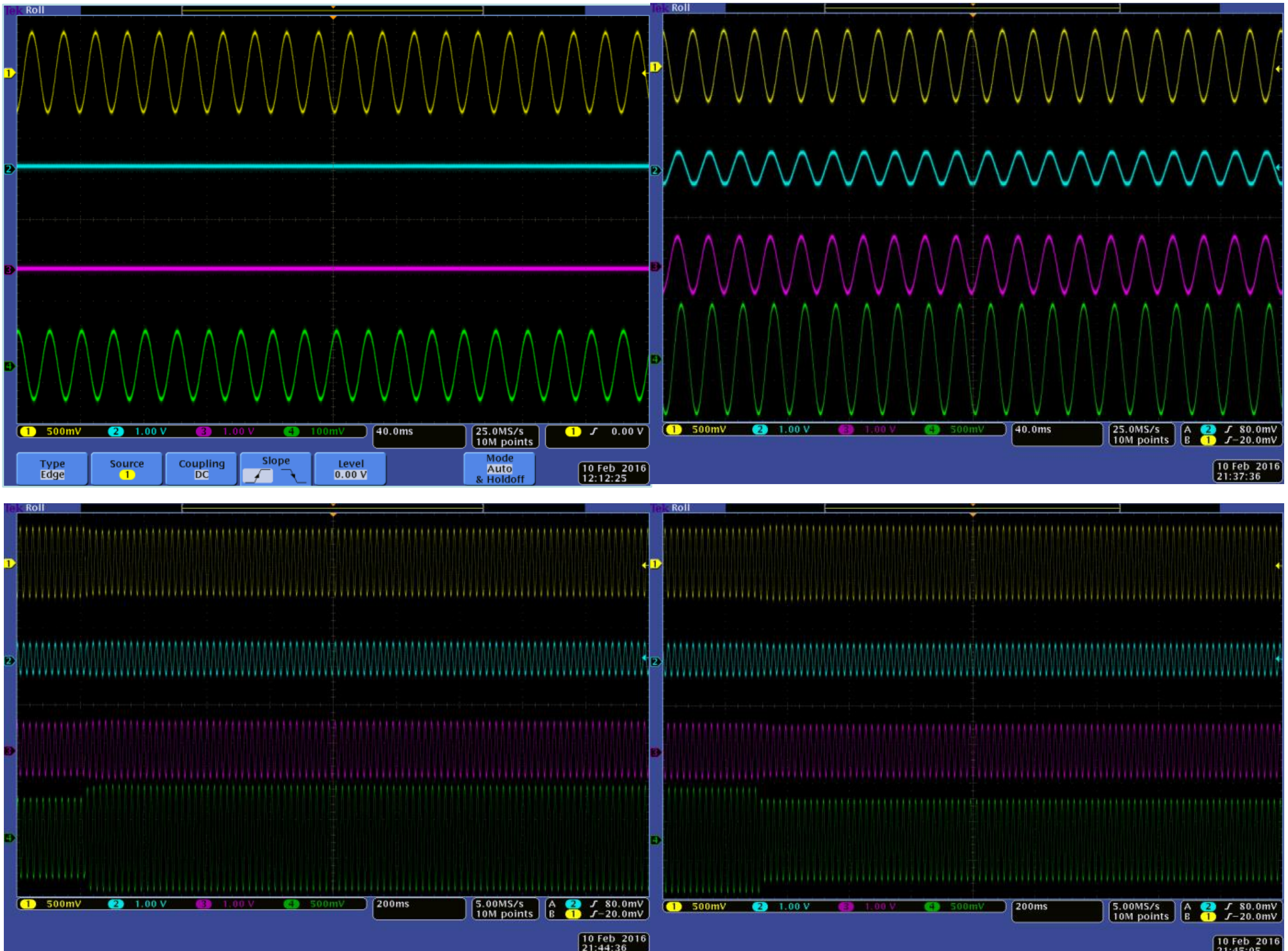








Master-Slave Mode Simulation



- Steady Operation
  - 0.06pu
  - 0.70pu
- Operation dynamics
  - Load Step Increase & Decrease

PCC Voltage (800V/V)

WT Current (200A/V)

PV Current (200A/V)

HT Current (800A/V)

with step increasing load

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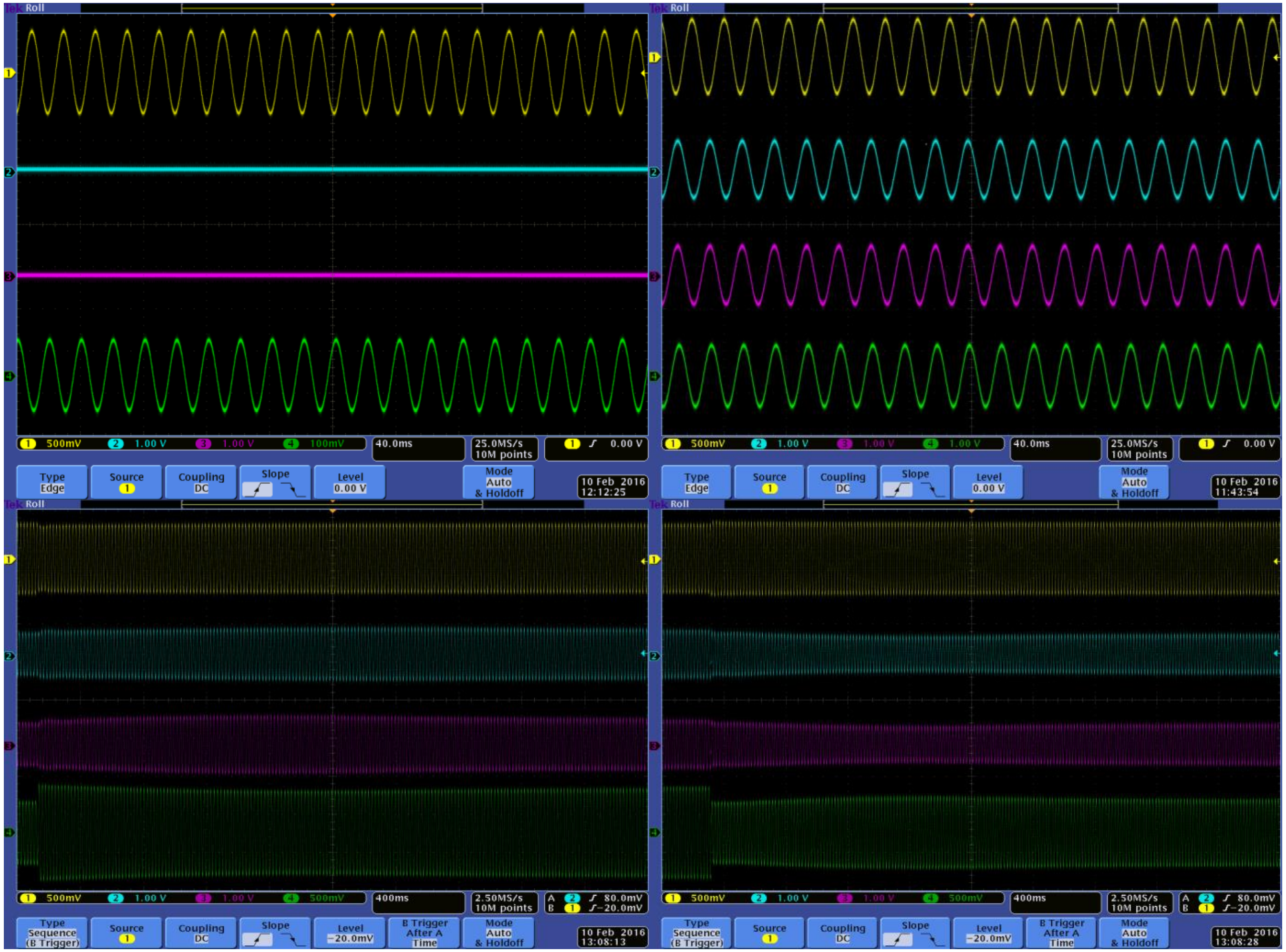
Full Droop Control Mode



- Steady Operation
  - 0.06pu
  - 0.80pu
- Operation dynamics
  - Load Step Increase & Decrease (0.15 pu)

PCC Voltage (800V/V)

WT Current (200A/V)

PV Current (200A/V)

HT Current (800A/V)

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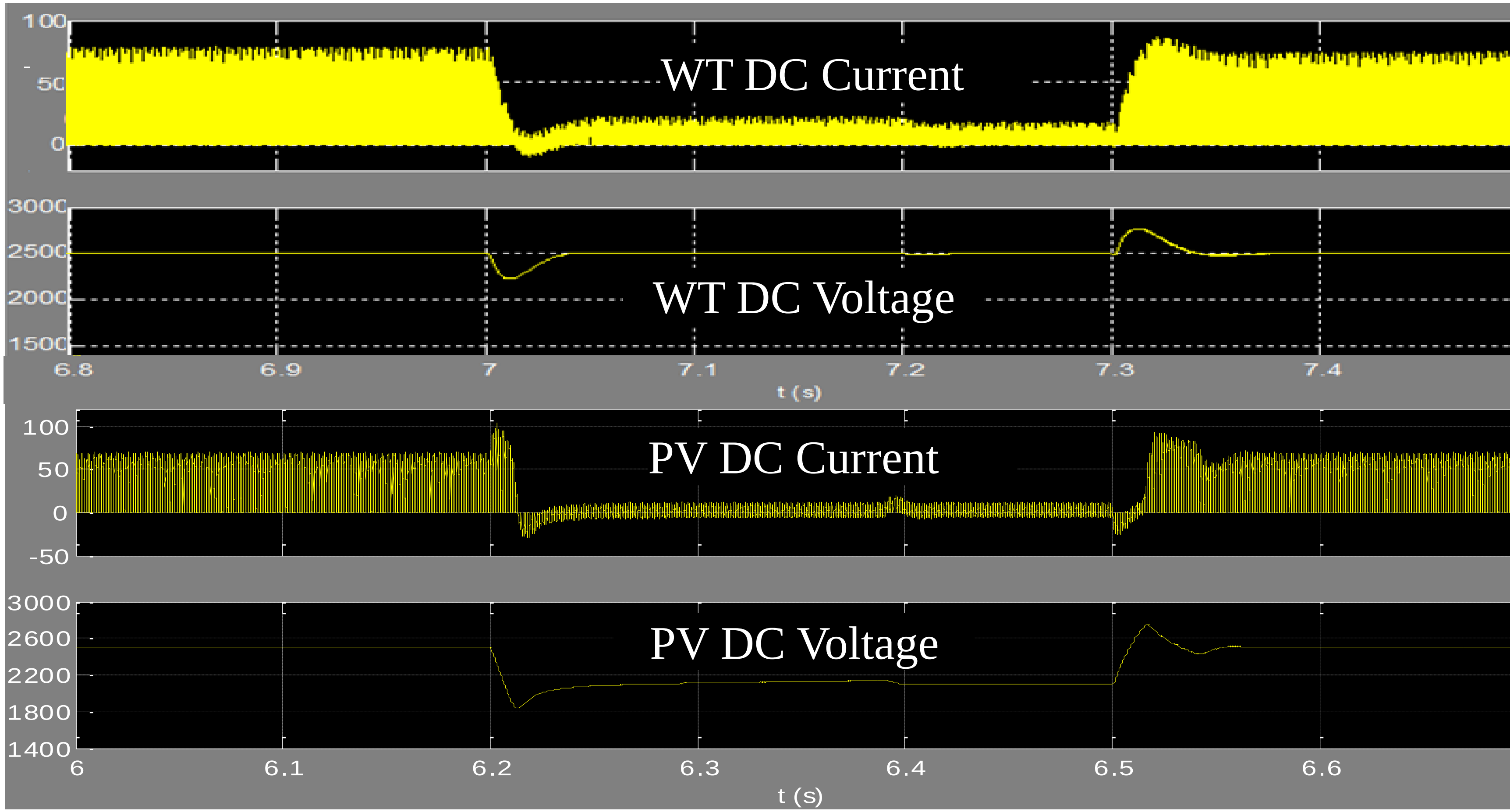
Dynamics on DC Side



WT: 100kW ↔ 10W, PV: 1kW/m^2 ↔ 50W/m^2

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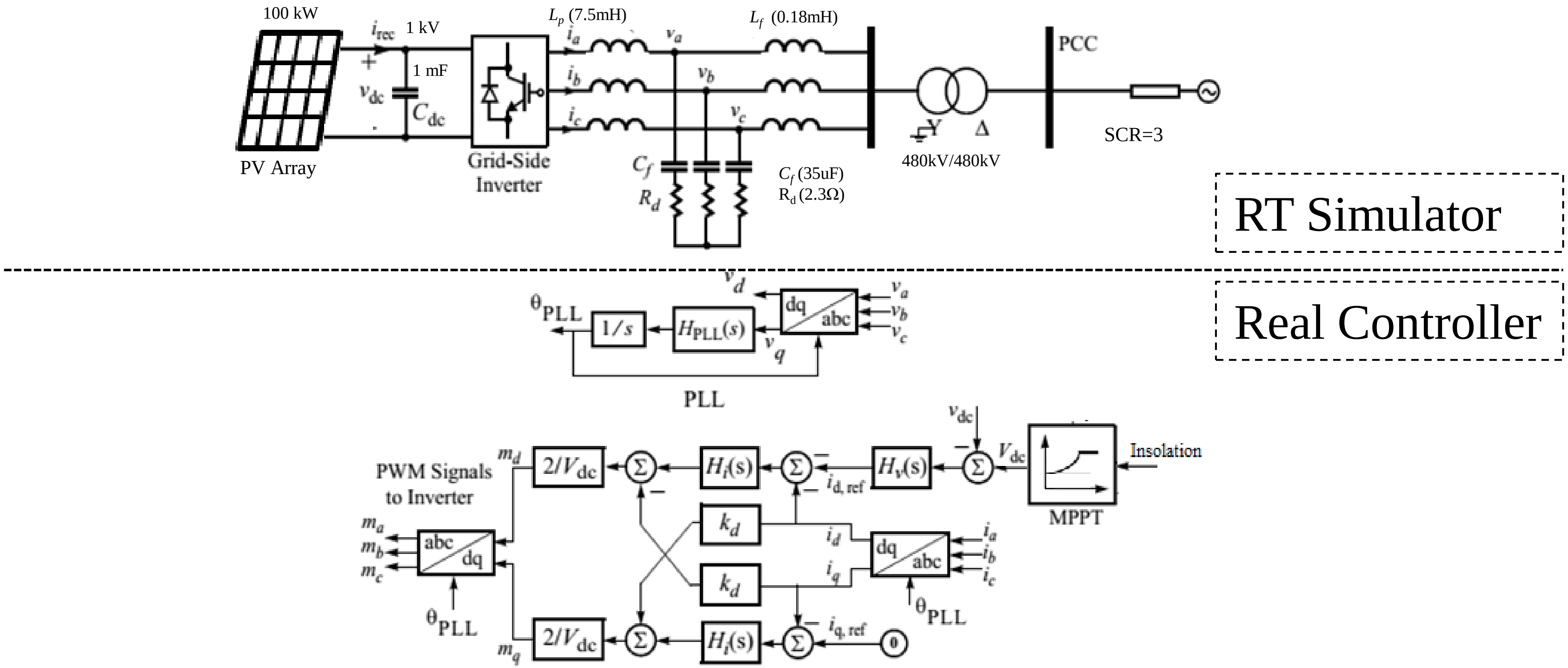
CHIL of PV Integration



PV Array Parameters	Value	Unit
Rated Volt.	1	kV
Rated Power	100	kW
Panel & Array	50, 100×5	Cells, Panels

Control Design	Bandwidth (Hz)
Grid-Side Inverter PLL	30
Grid-Side Inverter Current Control	200
Grid-Side Inverter DC-Bus Voltage Control	20

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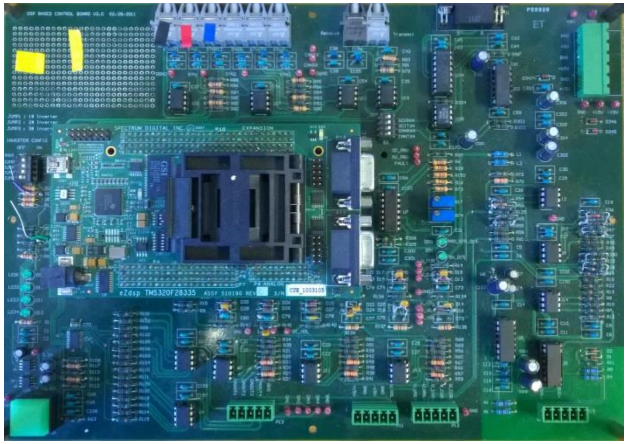
DSP Controller Hardware

- Based on TI TMS320f28335
  - 150MHz Operating Speed
  - 16 Channels ADC & Four 16 Bit DAC
  - 512k Flash & 256k SRAM
- I/O Interface
  - Six AC & One DC Sampling
  - Eight Optical Input/output
  - Switches/LEDs/Communication Ports



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DSP Controller Software

- Grid-tied Inverter Control
  - PLL Algorithm
  - Current PI Regulation
  - DC/AC voltage PI Regulation
- Synchronization with FPGA Board for co-Work on Complex Algorithm

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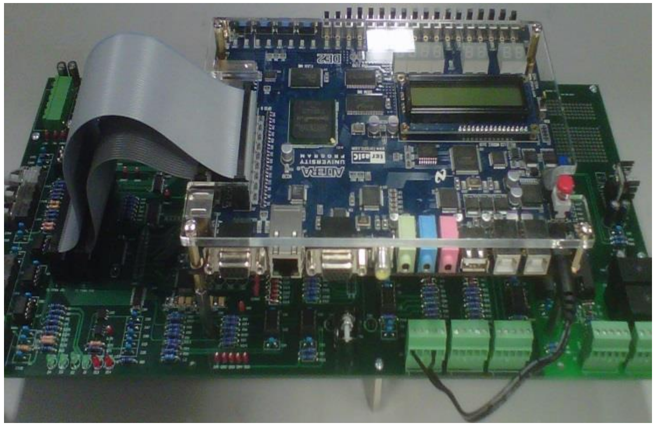
FPGA Controller Hardware

- Based on Cyclone II EP2C35
  - 50/27MHz Oscilator
  - Six 16-Bit ADC & Four 12 Bit DAC
  - 4M Flash, 512k SRAM & 8M SDRAM
- I/O Interface
  - Six AC & One DC Sampling
  - Six Optical Input/output
  - Switches/LEDs/Communication Ports



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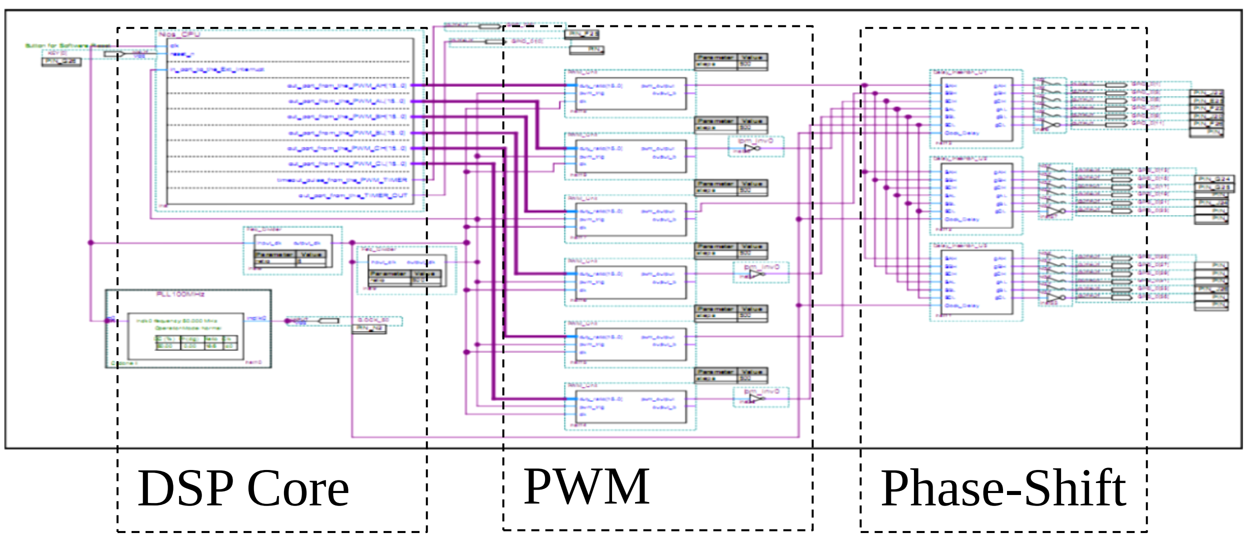
FPGA Controller Software

- Converter Control
  - PI Algorithm
  - PWM & Phase-Shift Insertion
- Synchronization with DSP Board for co-work



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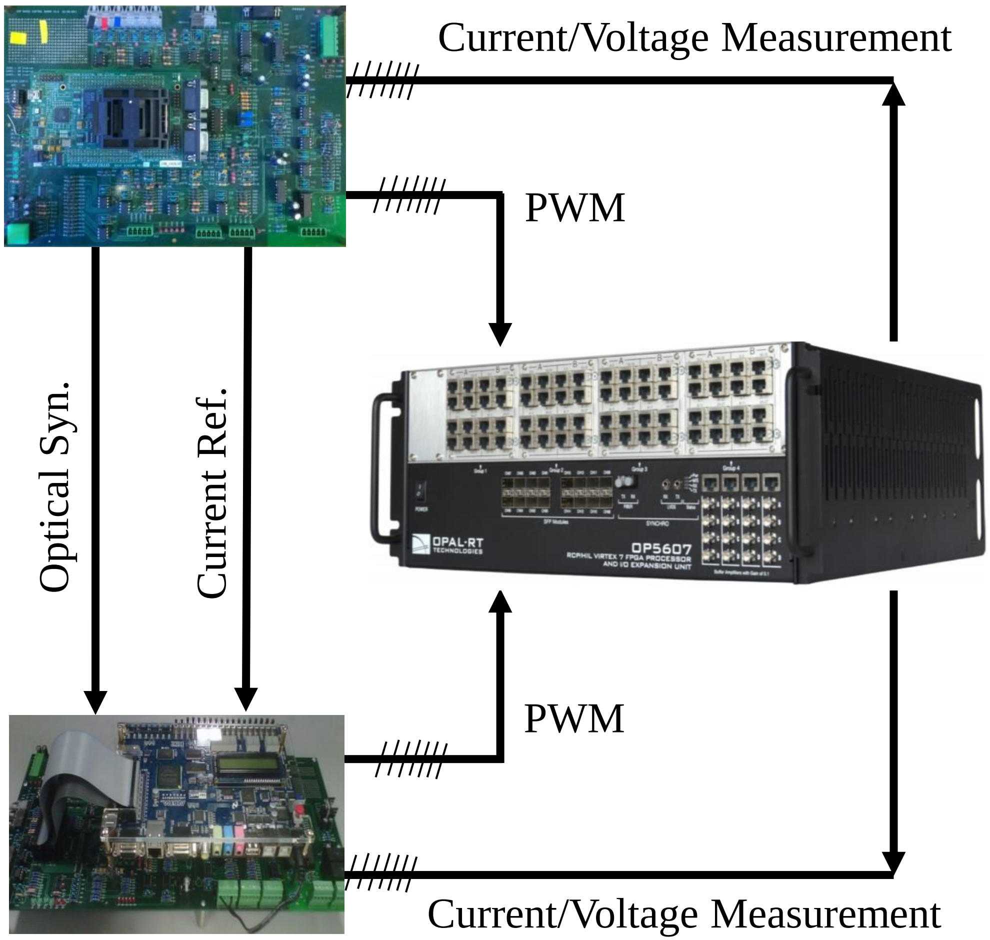
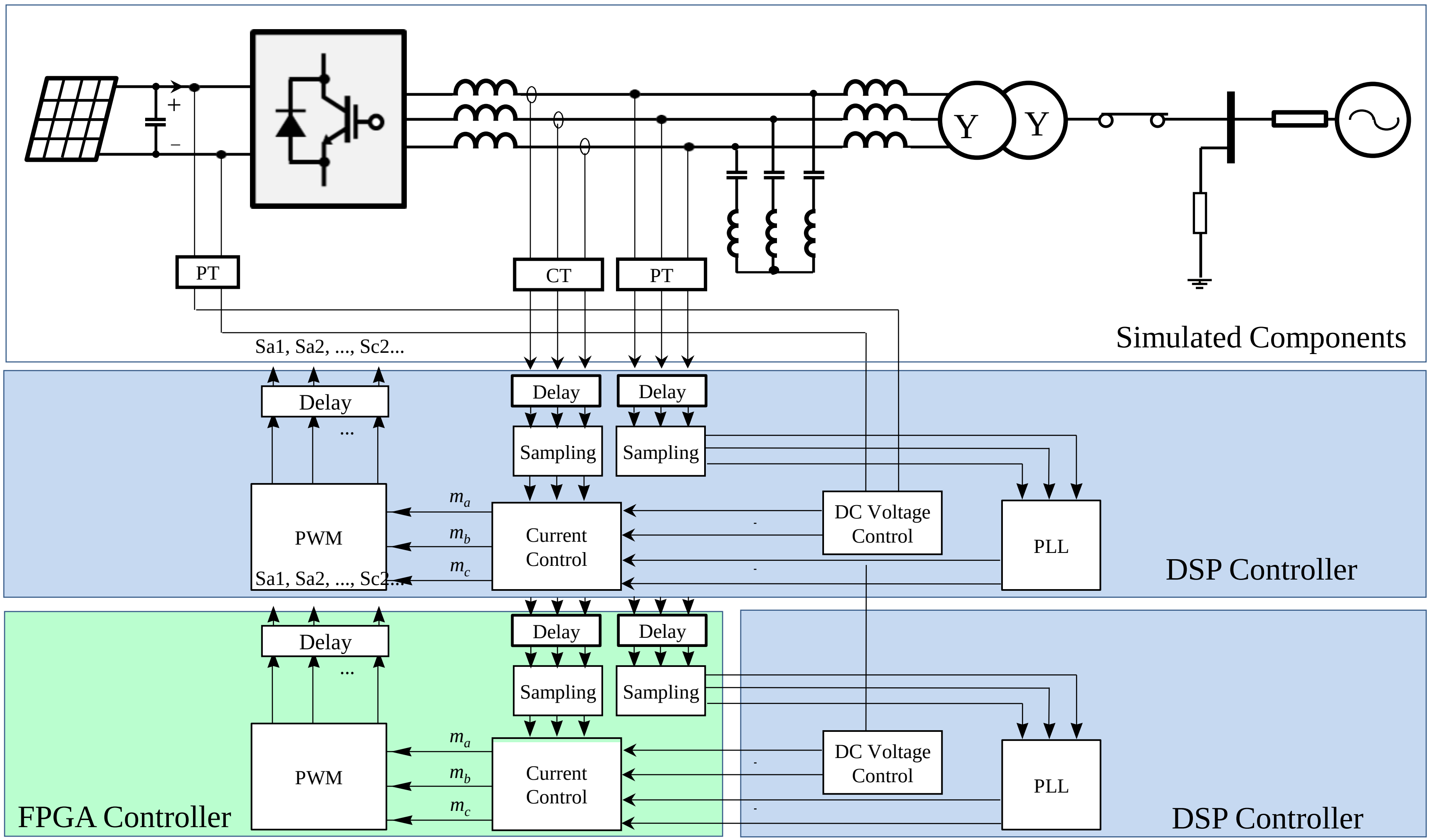
Setup of CHIL



Testing Modes of CHIL



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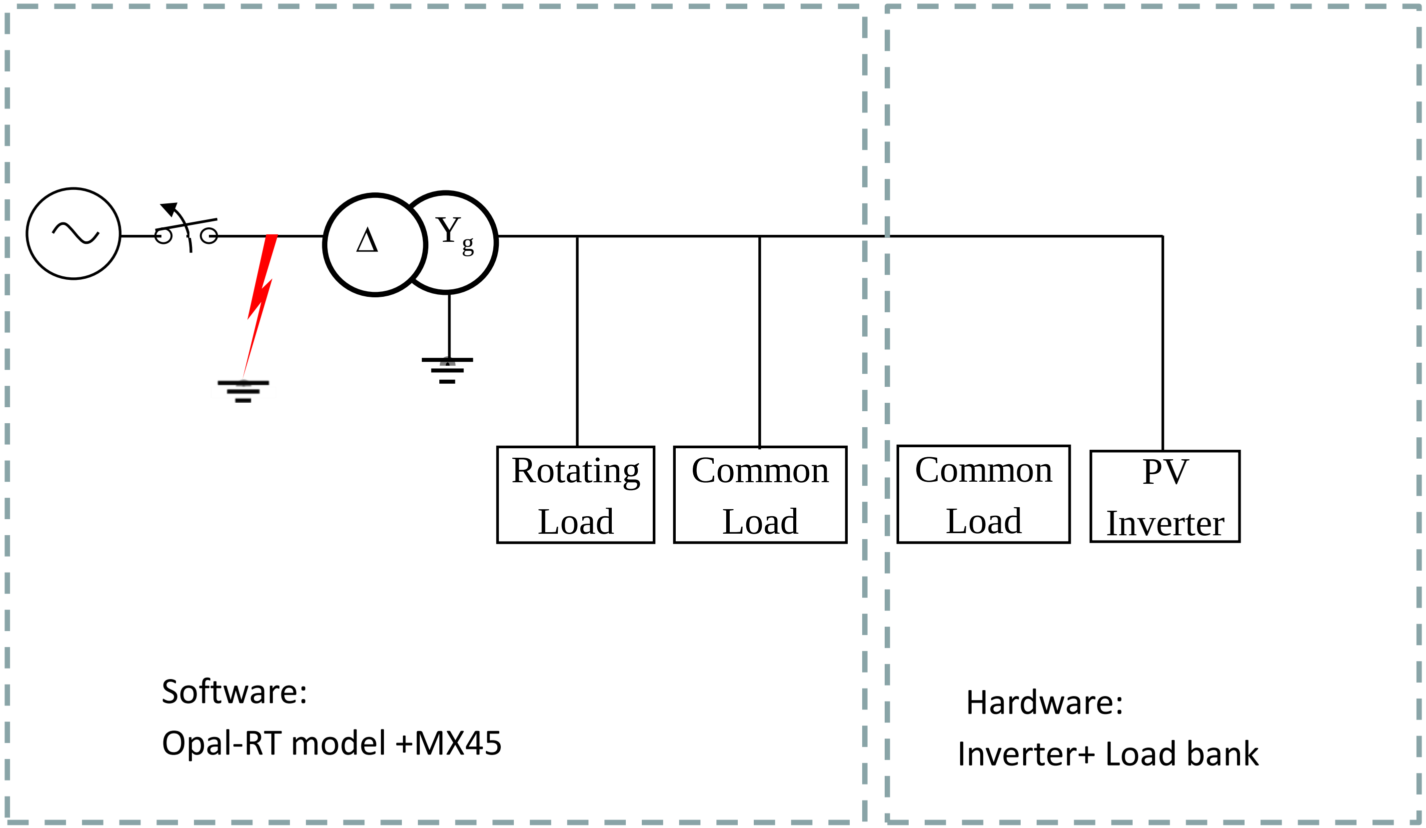
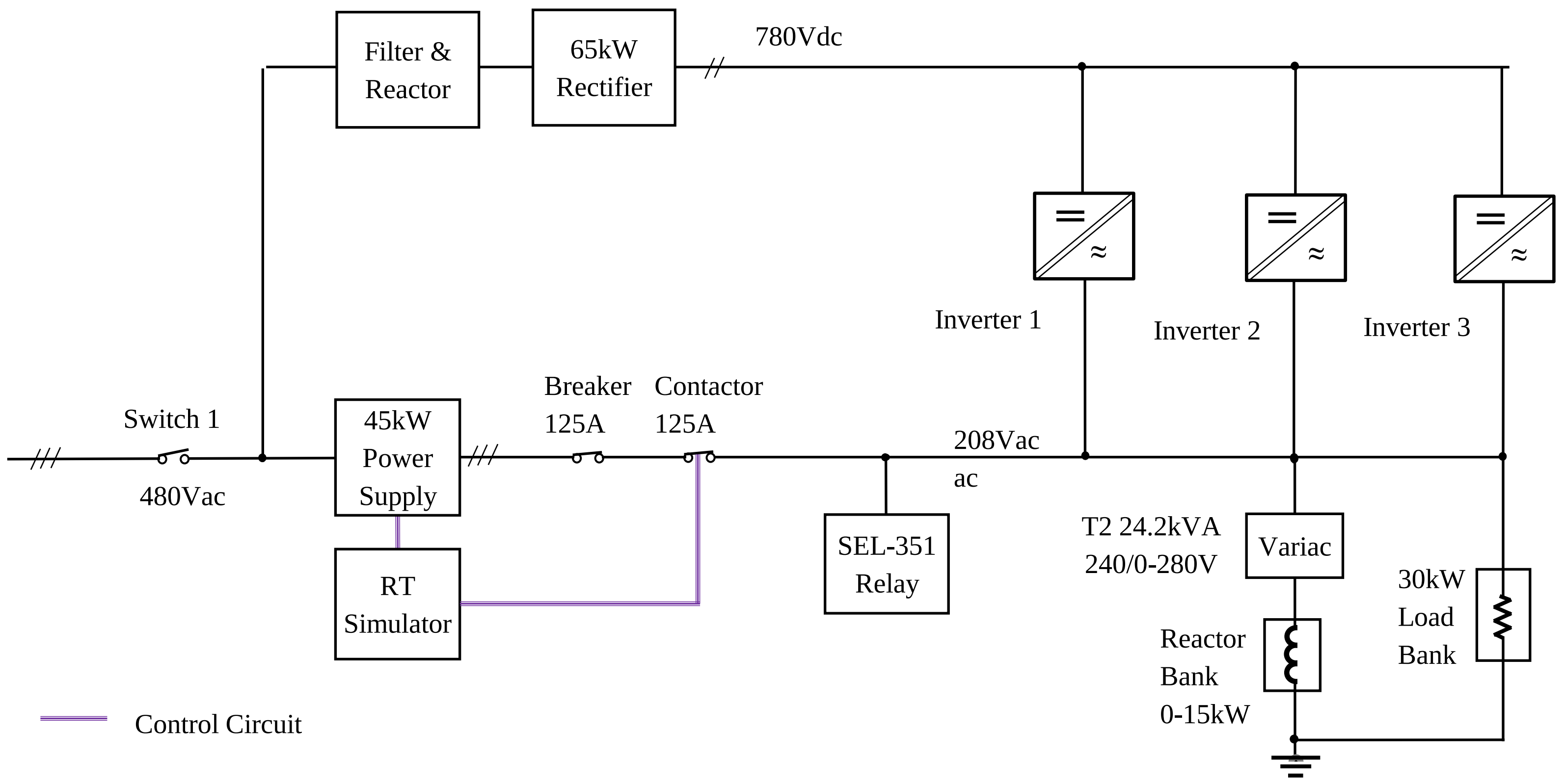
System Setup for GFOV Testing



Power HIL for Upcoming Project



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