Power Integrity and its Impact on Clock Jitter

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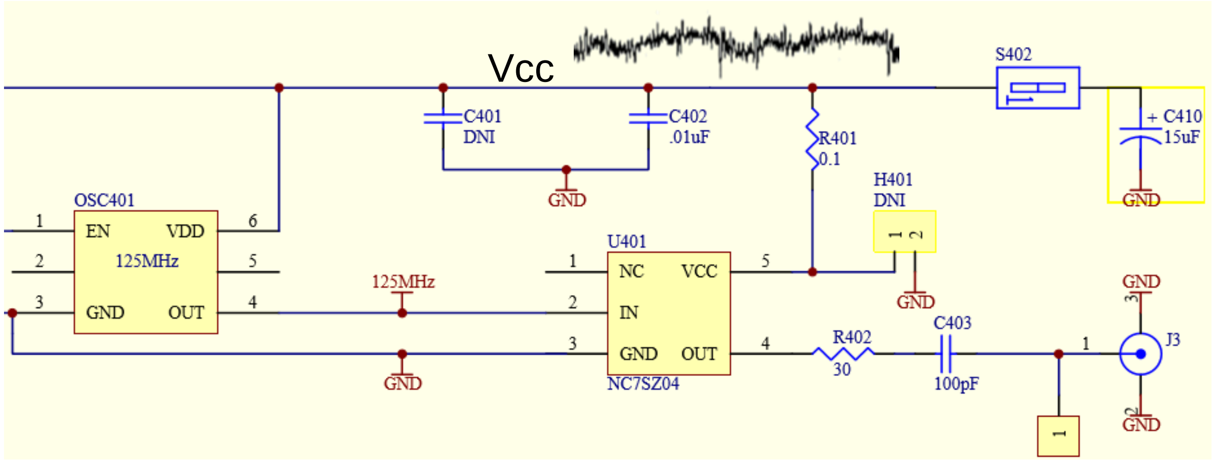
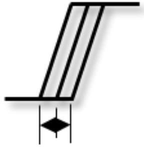
Agenda

- Introduction: power rail noise and conversion to jitter
- Sampling theory and its application to jitter measurement
- Jitter measurement using an oscilloscope (TIE and period)
- Analyzing jitter in the frequency domain
- Correlating power rail ripple voltage with timing jitter
- Measurement example

Power Integrity and Clock Jitter

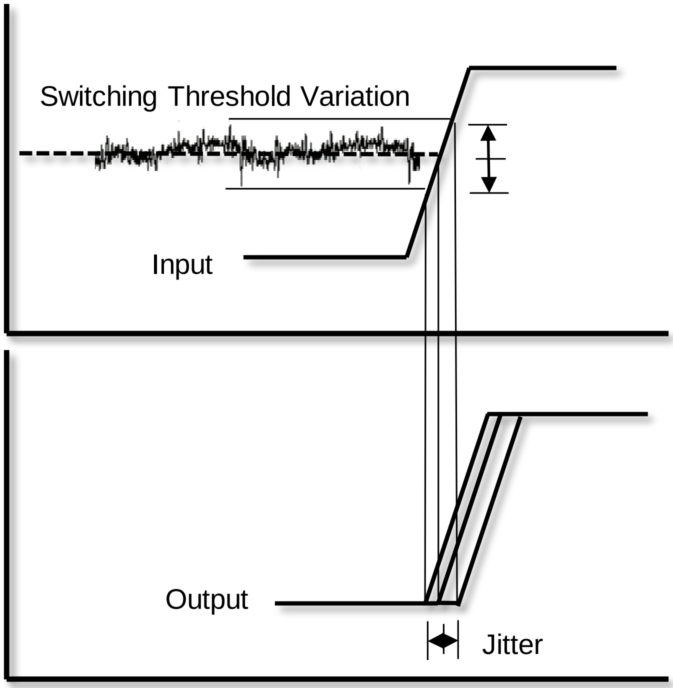


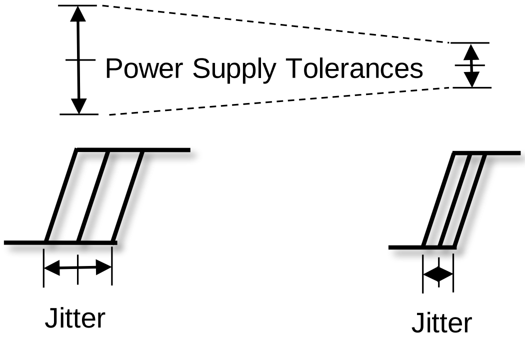


Power Integrity is a Leading Cause of System Jitter

Power supply noise causes clock/data jitter.

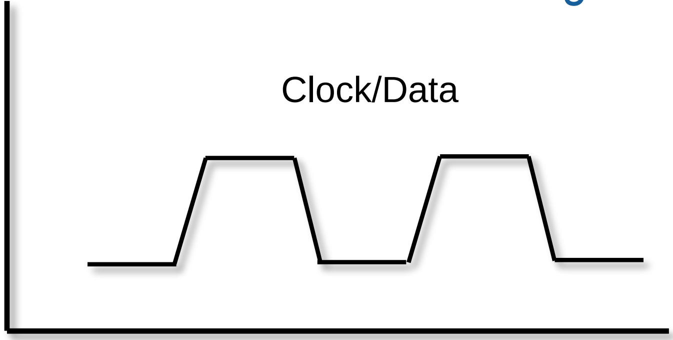
$$\frac{1\ mV\ RMS\ noise}{1\frac{V}{ns}\ slew\ rate} = 1\text{ ps RMS jitter}$$

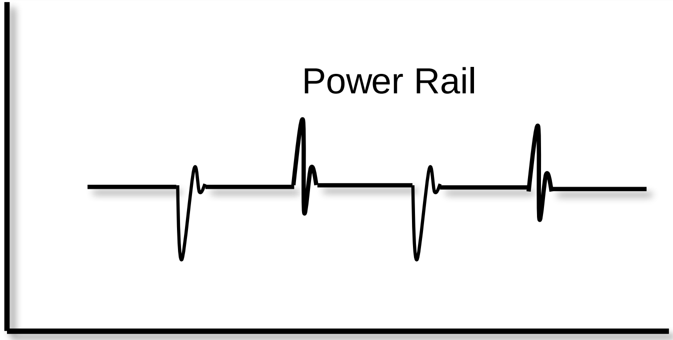


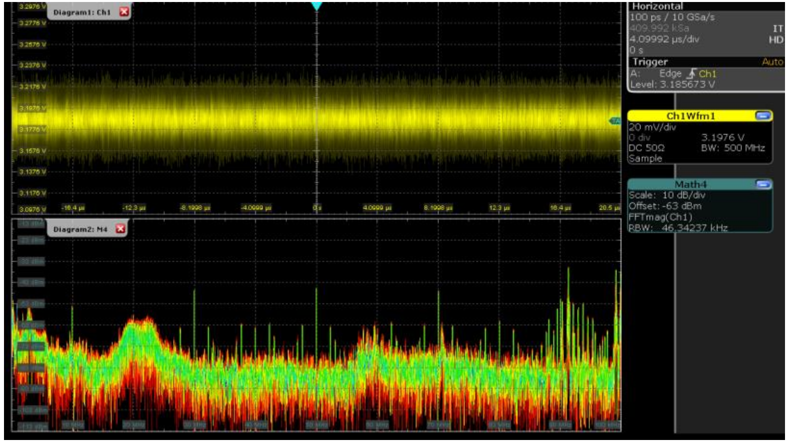


Power Integrity Measurements

Additional Challenge

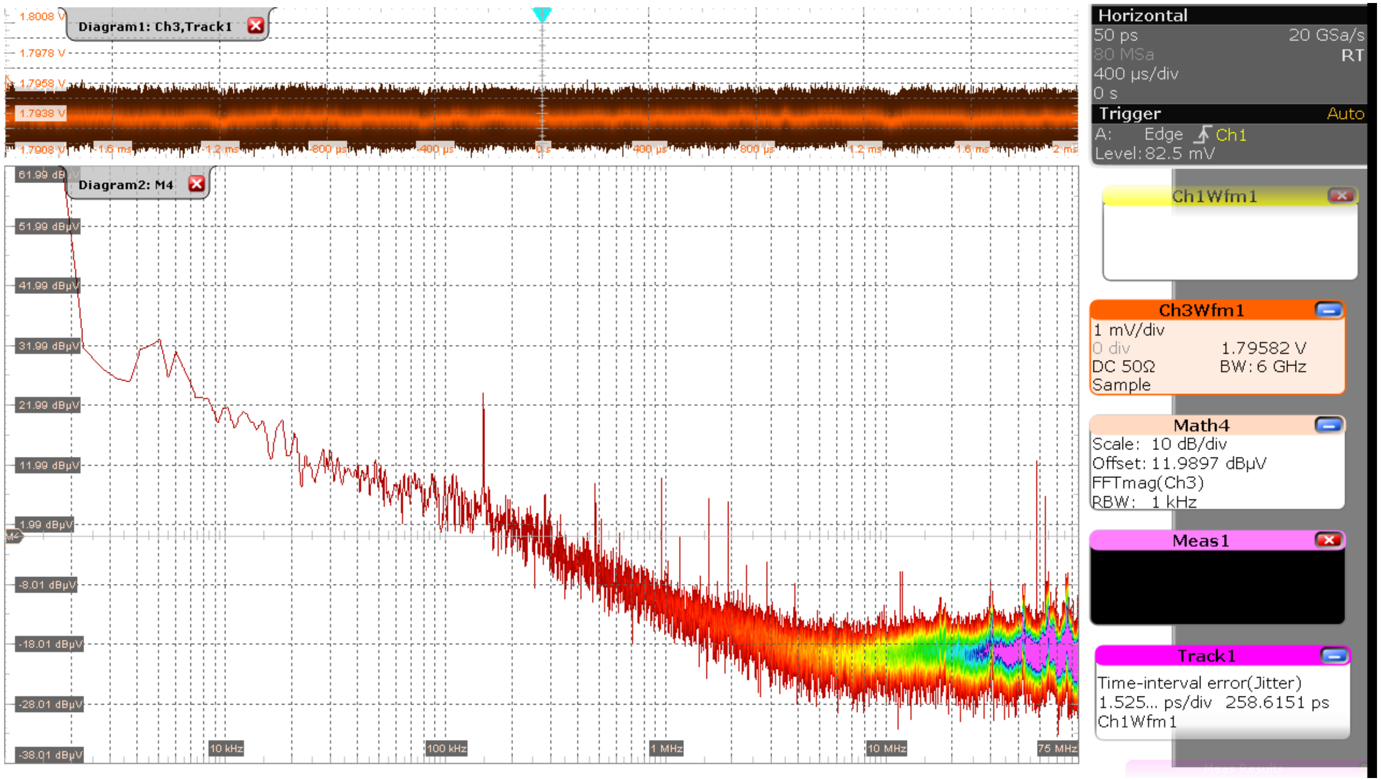






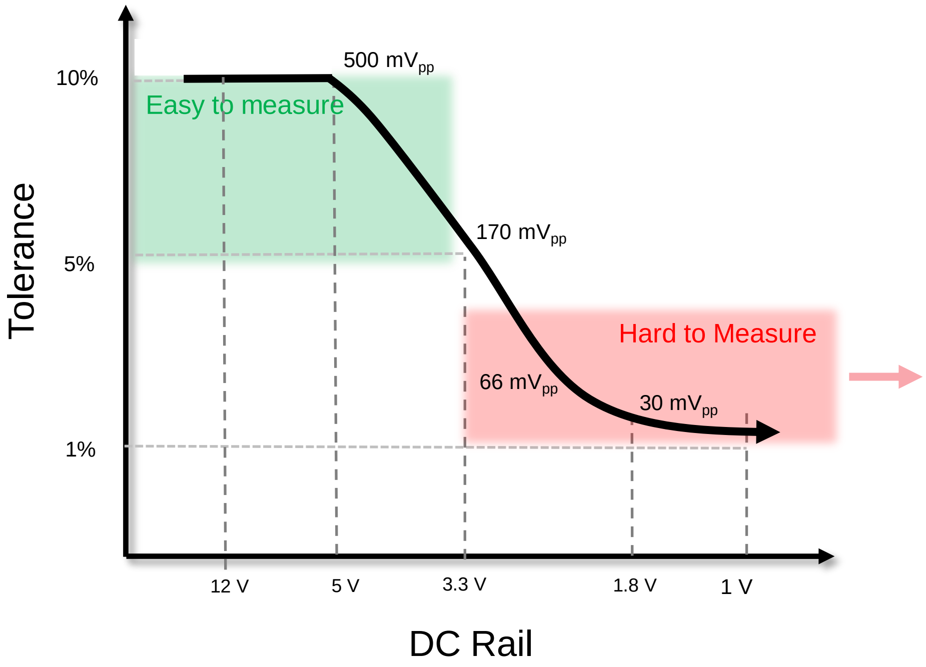
Power rails can carry other coupled sources

Spectrum Analysis of Ripple Voltage



Power Rail Measurement Challenges

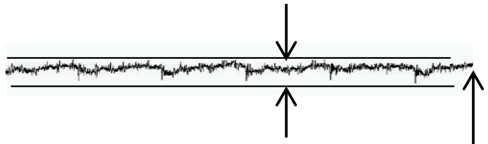
Lower rail voltages and smaller tolerances



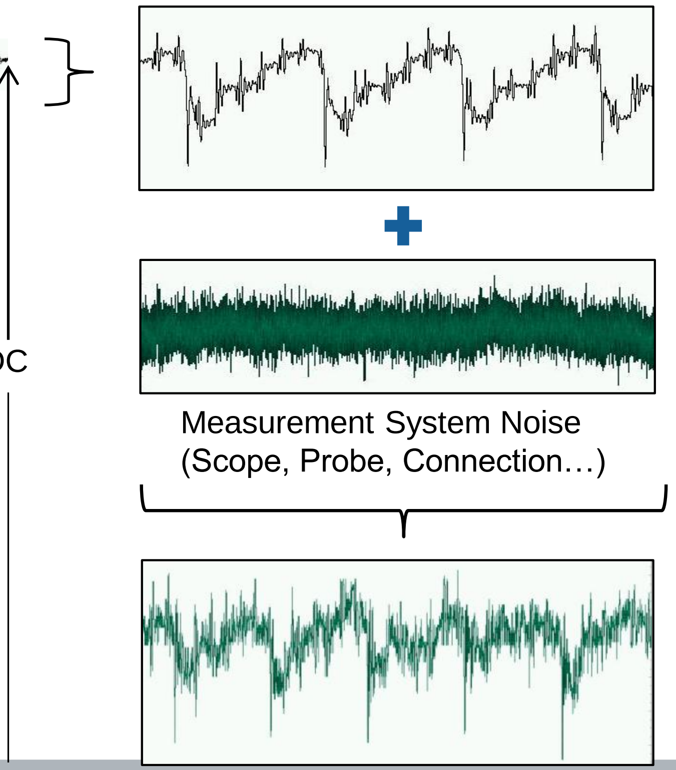
Examples

Rail Value	Tolerance	Need to measure
3.3 V	2%	66 mV$_{pp}$
1.8 V	3 %	30 mV$_{pp}$
1.2 V	2.5 %	30 mV$_{pp}$
1 V	3 %	30 mV$_{pp}$

Power Integrity Measurements: Primary Challenge



Challenge: Measure small ac signal on top of large dc signal



Issues to overcome:

1. Measurement system noise
2. Large DC Offset
3. Maintain high BW

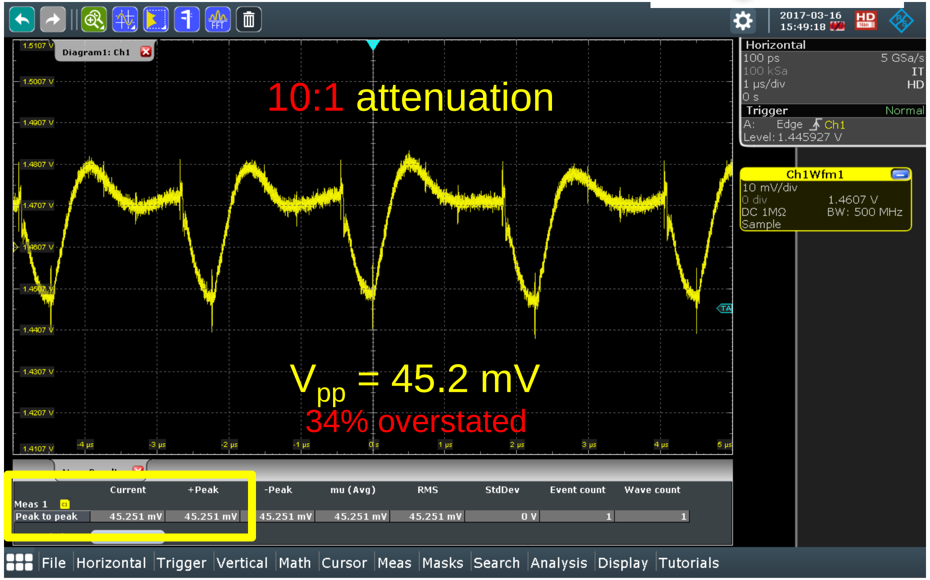
Power Rail Probes…specialty tool

Circular saw
Great for a bunch of stuff.
Can't cut door jambs.

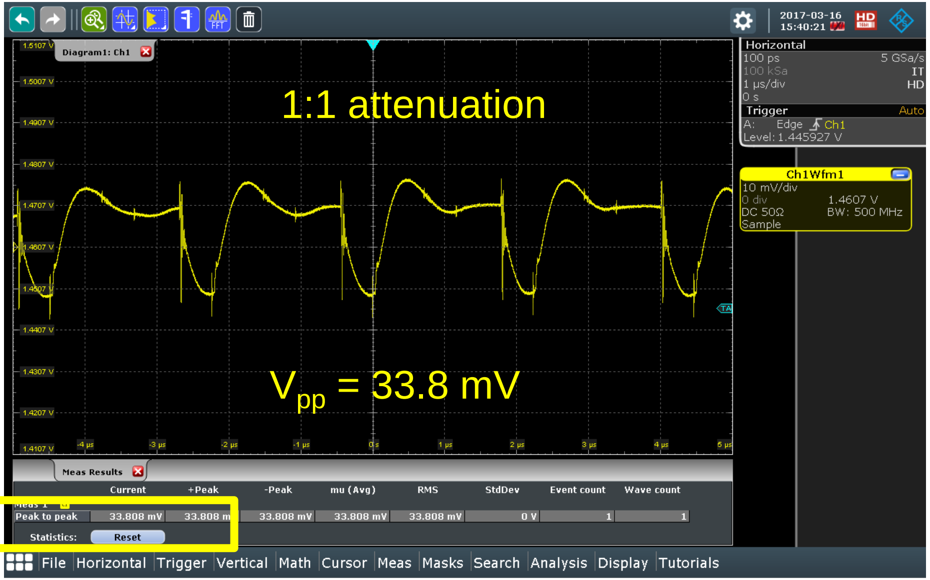
Jamb saw.
Does one task really well.
Not useful for anything else.

Measurement Accuracy: Noise Due to Probe Attenuation Ratio

10:1 (10 mV/div)



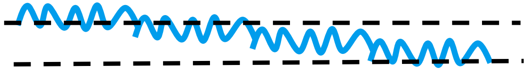
1:1 (10 mV/div)

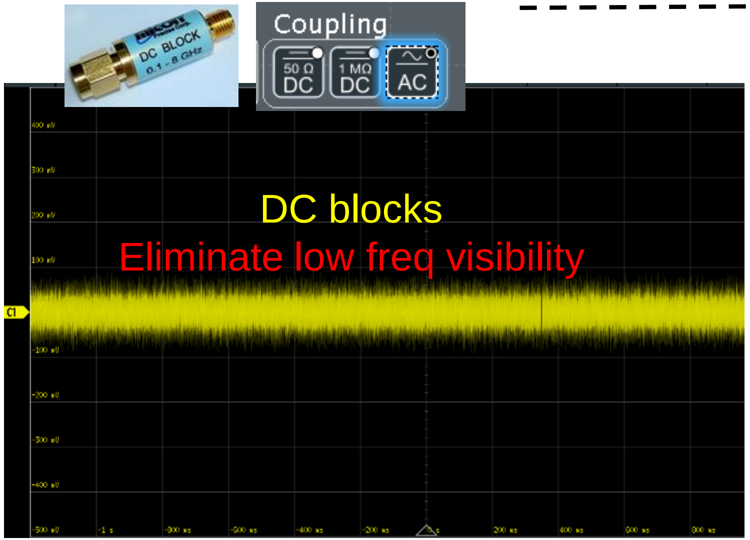


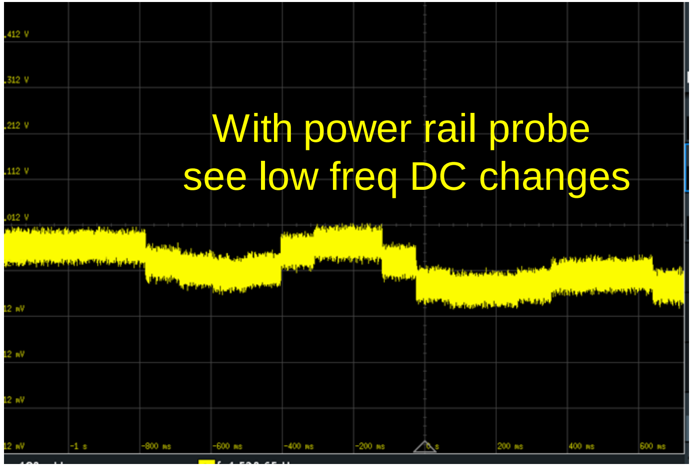
Challenges with Insufficient Scope Offset

AC coupling mode and blocking caps eliminate ability to see DC changes

DC Drift

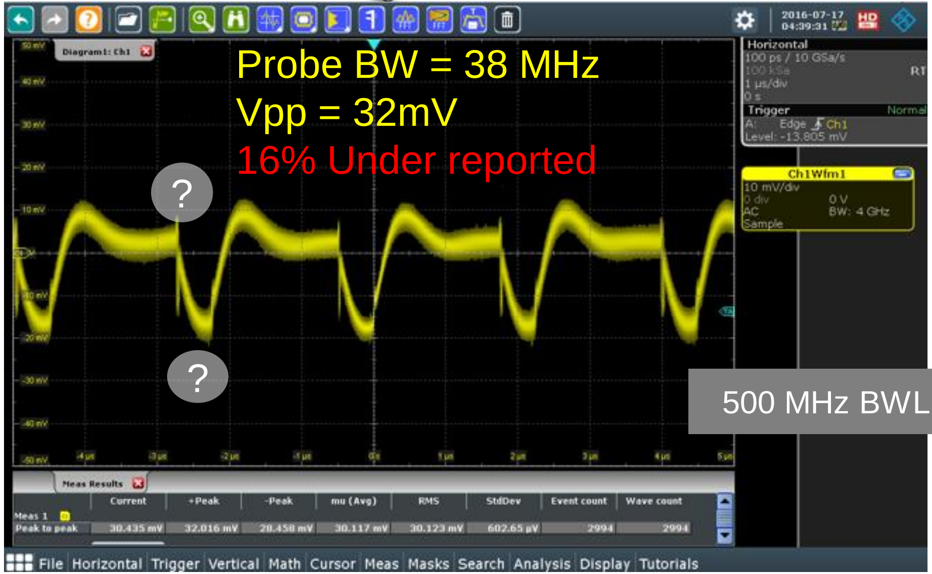


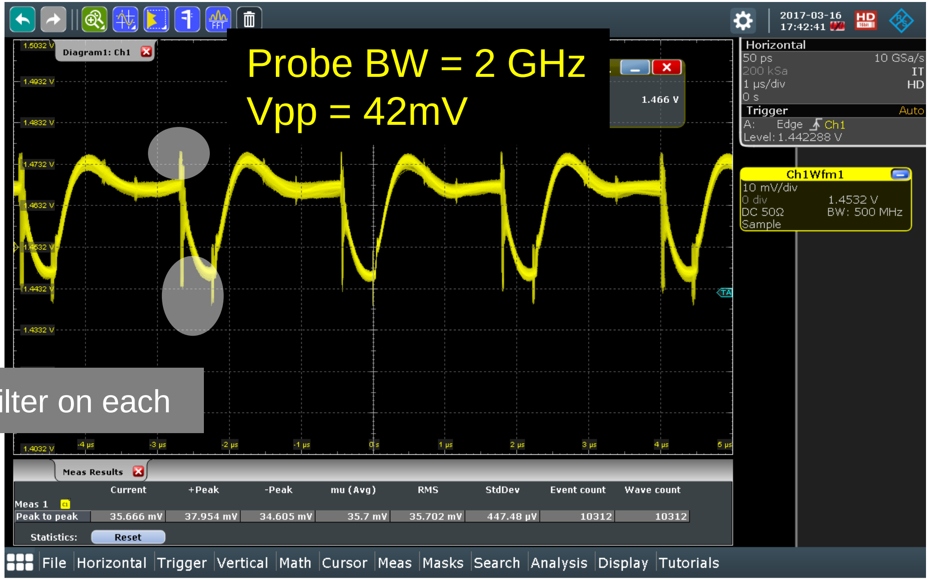




Measurement Accuracy: High BW Needed for High Frequency Transients

Both 1:1 Probes





500 MHz BWL filter on each

1:1 ZP1X passive 38 MHz BW

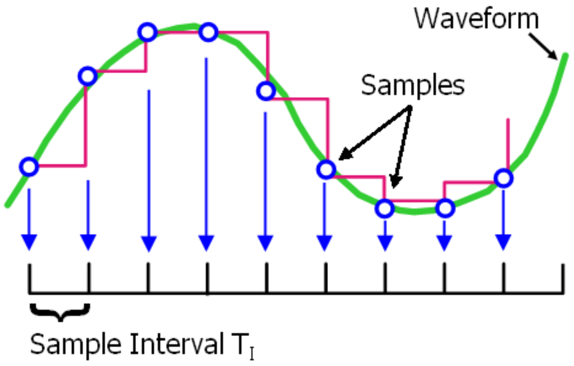
1:1 ZPR20 active 2 GHz BW
Captures high-frequency transients

Measurement techniques for jitter in the time domain (oscilloscope)

Sampling of a signal

- The A/D Converter of the oscilloscope samples the continuous signal at specific points in time and delivers digital values
- Sampling of clock signals at zero-crossing (no phase at high or low)
- ADC sample rate: $f_{ADC} = 1/T_I$
- The result is a waveform record that contains waveform samples
- The waveform samples were displayed at the screen and build up the waveform
- Sample rate: $\frac{number\ of\ waveform\ samples}{time\ in\ s}$
- Nyquist theorem:

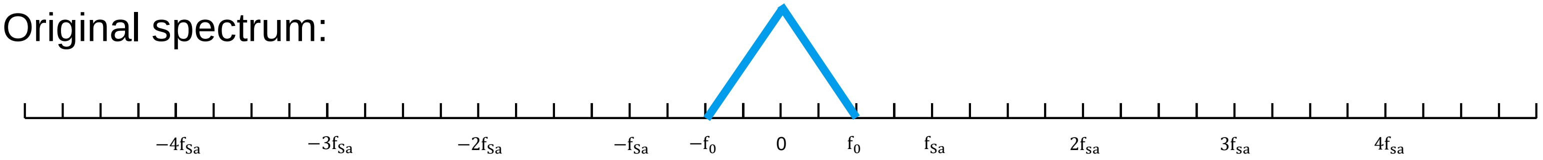
$$f_{sa} \geq 2f_{max}$$



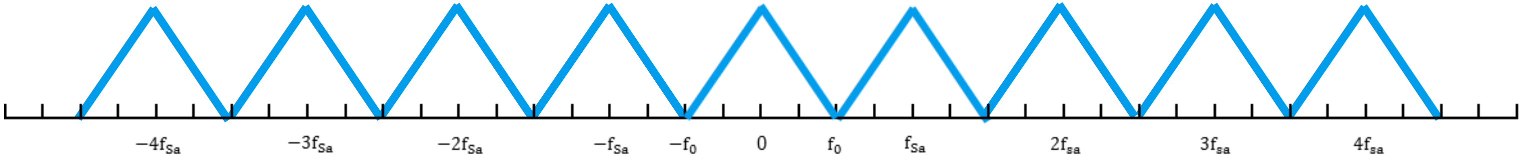
Measurement techniques for jitter in the time domain (oscilloscope)

Sampling of a signal

- Integrated low-pass filter (bandwidth < $0.5 f_{sa}$) in the analog front end → Nyquist theorem is conformed
- Sampling of a signal
  - Original spectrum:



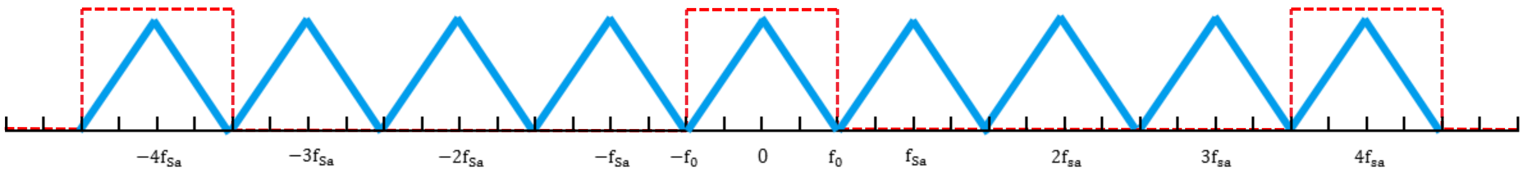
  - Spectrum after sampling:



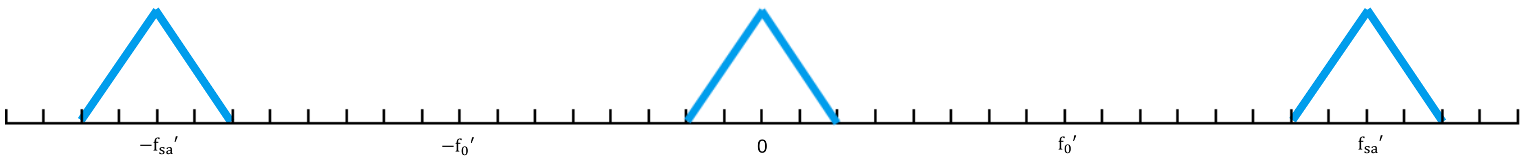
→ Frequency spectrum is copied at multiplies of the sample rate

Measurement techniques for jitter in the time domain (oscilloscope)
Interpolation

- E.g.: 4:1 Interpolation → $f_{sa}' = 4 f_{sa}$
- Rectangular low-pass filter ≙ Sin(x)/x interpolation
  - Attenuates the undesired spectral images



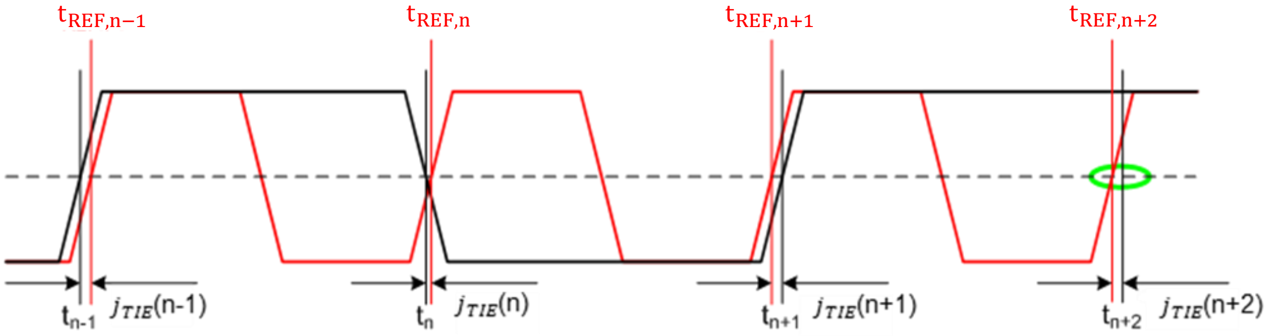
  - Resulting spectrum:



Measurement techniques for jitter in the time domain (oscilloscope)

TIE measurement

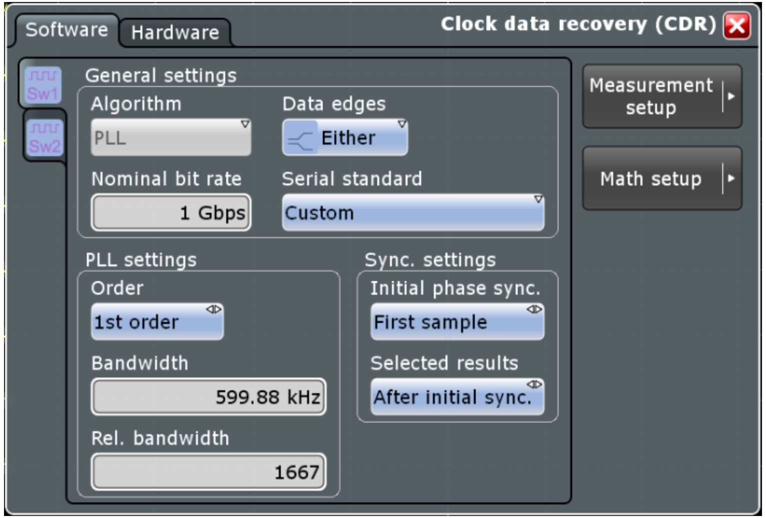
- TIE works for data and clock signals
- CDR/PLL is typically required to generate the $t_{REF,n}$ values
  - CDR (clock data recovery) or PLL
  - Recovery of TX clock
  - TX clock may be modulated (PCIe SSC)
- By recovering the TX clock, the TIE analyzes the impact of transmission

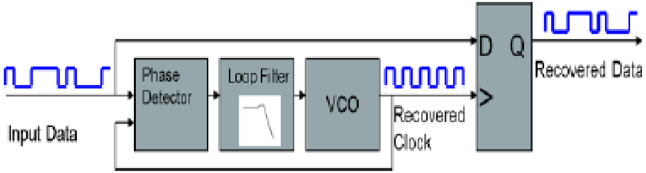


Measurement techniques for jitter in the time domain (oscilloscope)

Software Clock Data Recovery (CDR)

- CDR generates a reference clock from a high-speed serial data stream
- The generated clock signal matches the frequency and is aligned to the phase of the data stream





Measurement techniques for jitter in the time domain (oscilloscope)

Statistics

- Standard deviation, Mean value, Max, Min, Peak-peak...
- Population:
  - Number of individual observations included in the statistical data set (= event count)
  - Important to „judge“ random processes

Meas Results

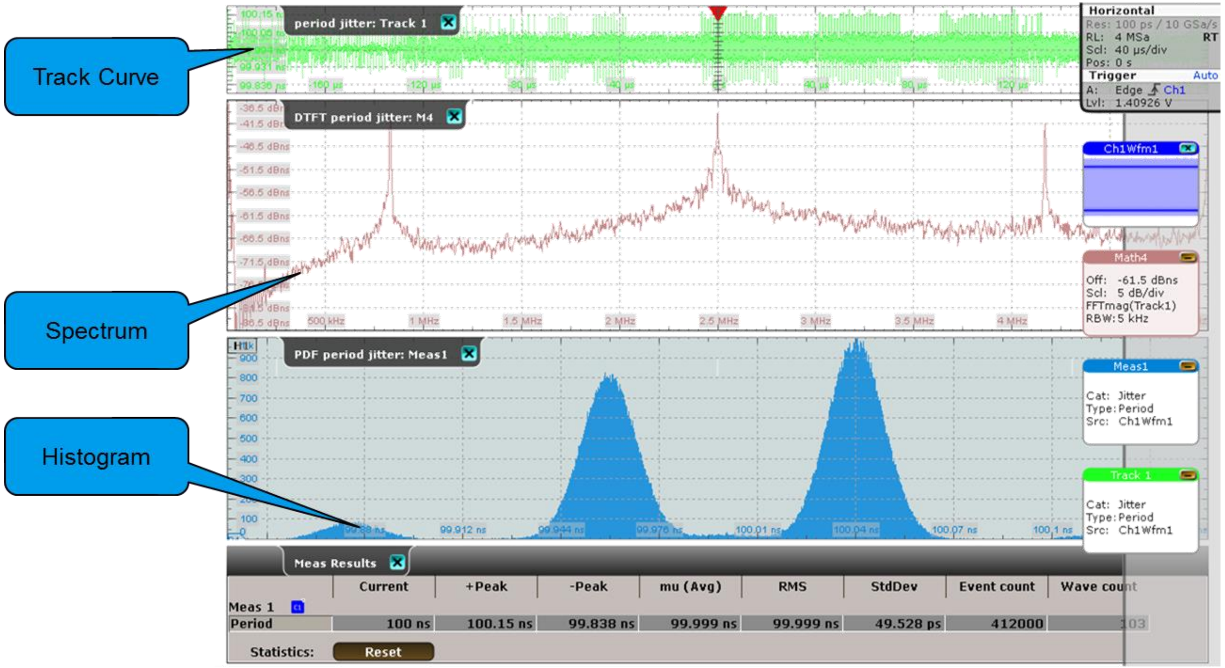
Meas 1 C1	Current	+Peak	-Peak	mu (Avg)	RMS	StdDev	Event count	Wave count
Period	30.7 ns	31.031 ns	29.044 ns	30.001 ns	30.008 ns	637.43 ps	4541	4541

Statistics: Reset

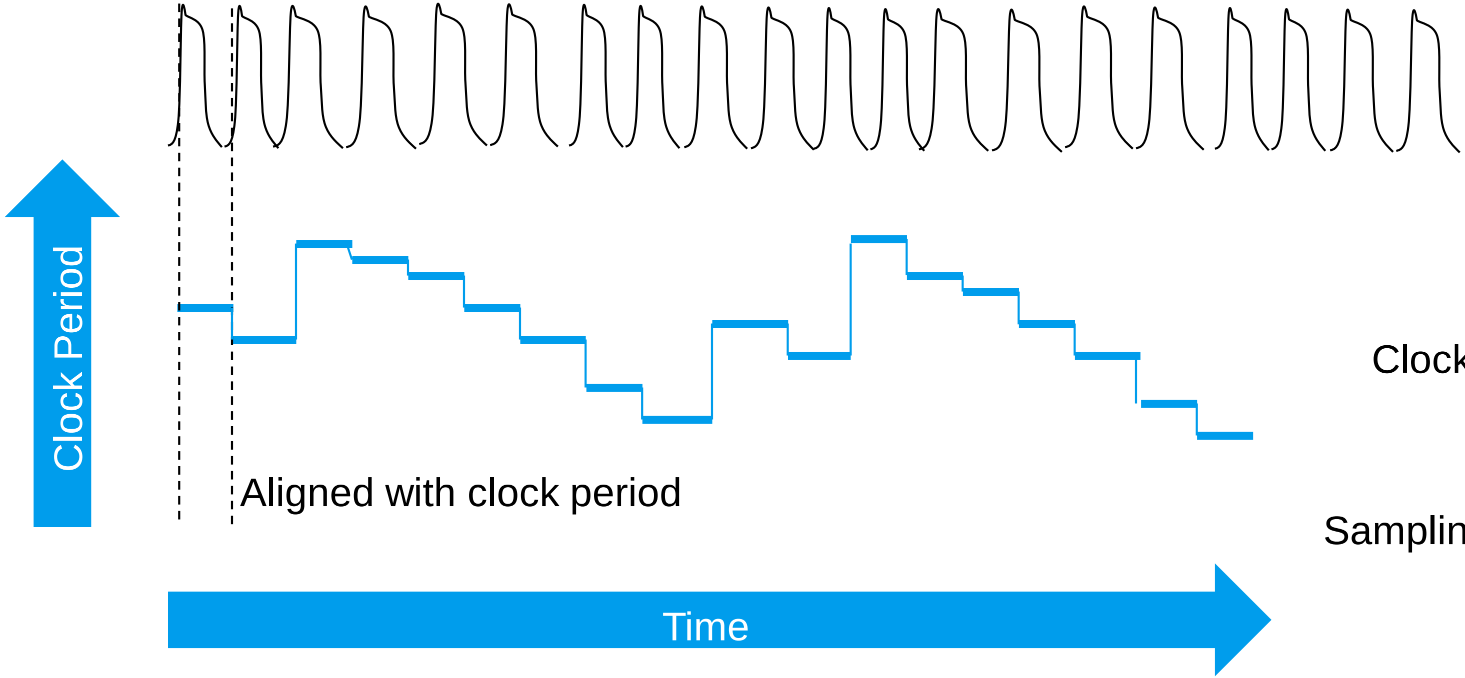
Measurement techniques for jitter in the time domain (oscilloscope)

Combined measurement

- 3 ways of viewing jitter results: track; histogram; spectrum



Jitter Time Trend (track)



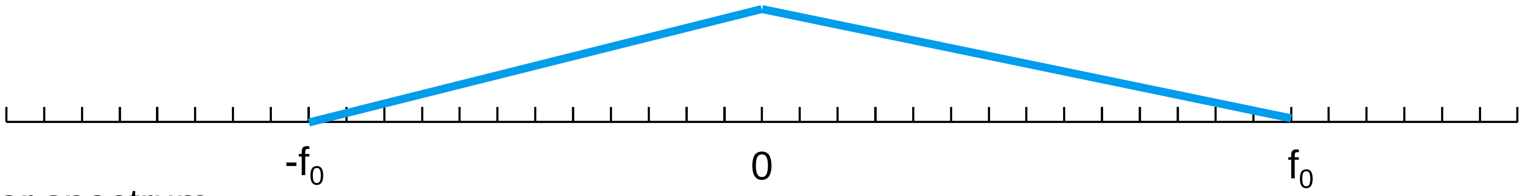
Clock period vs. time

Sampling rate = clock rate

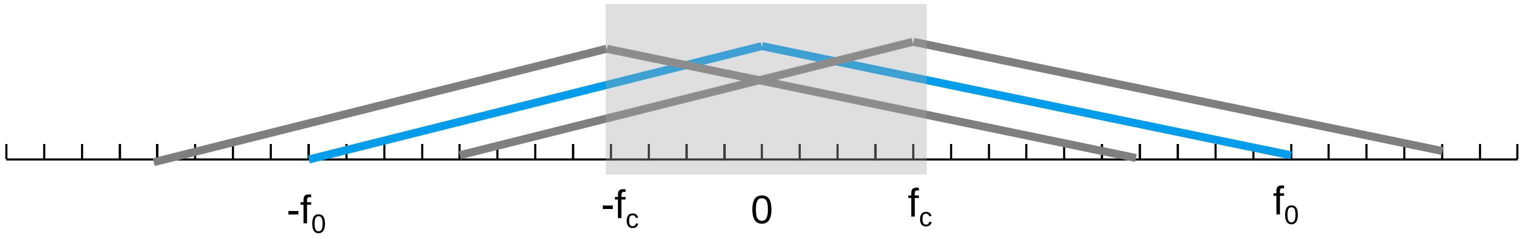
Measurement techniques for jitter in the time domain (oscilloscope)

Sampling of jitter

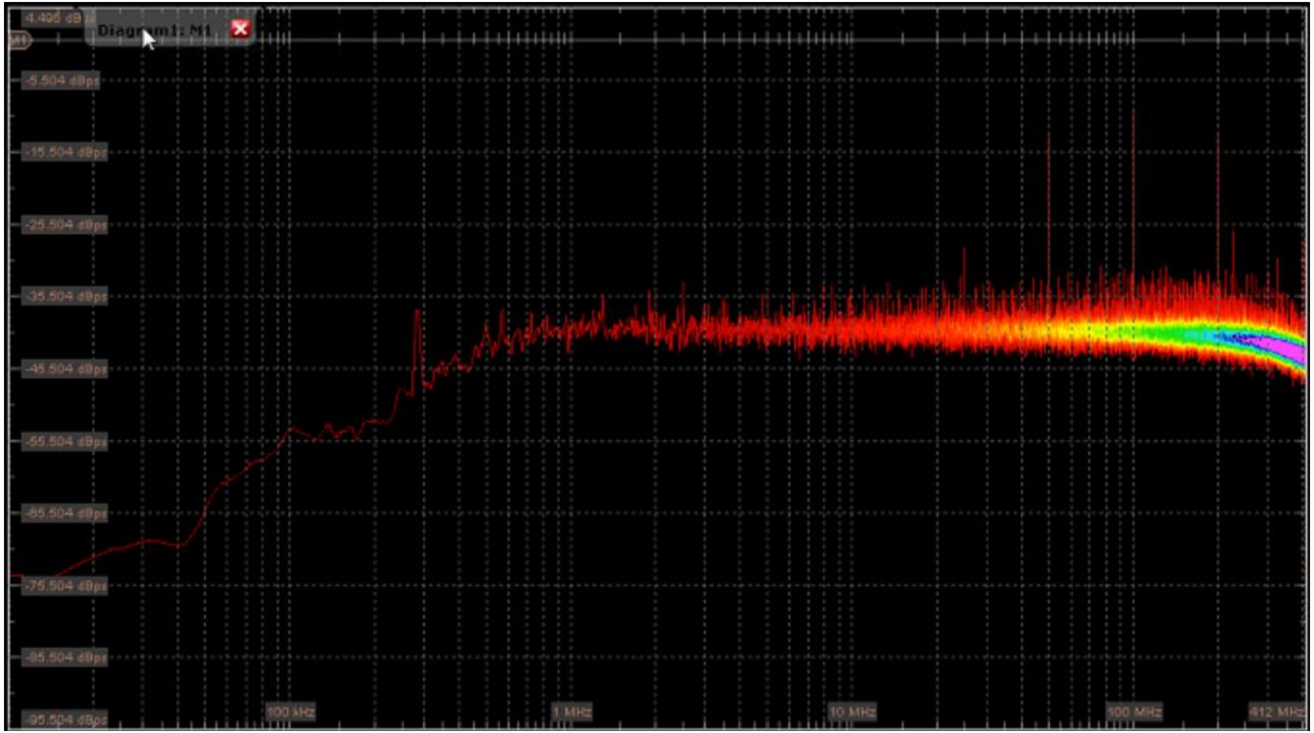
- Original spectrum



- Jitter spectrum

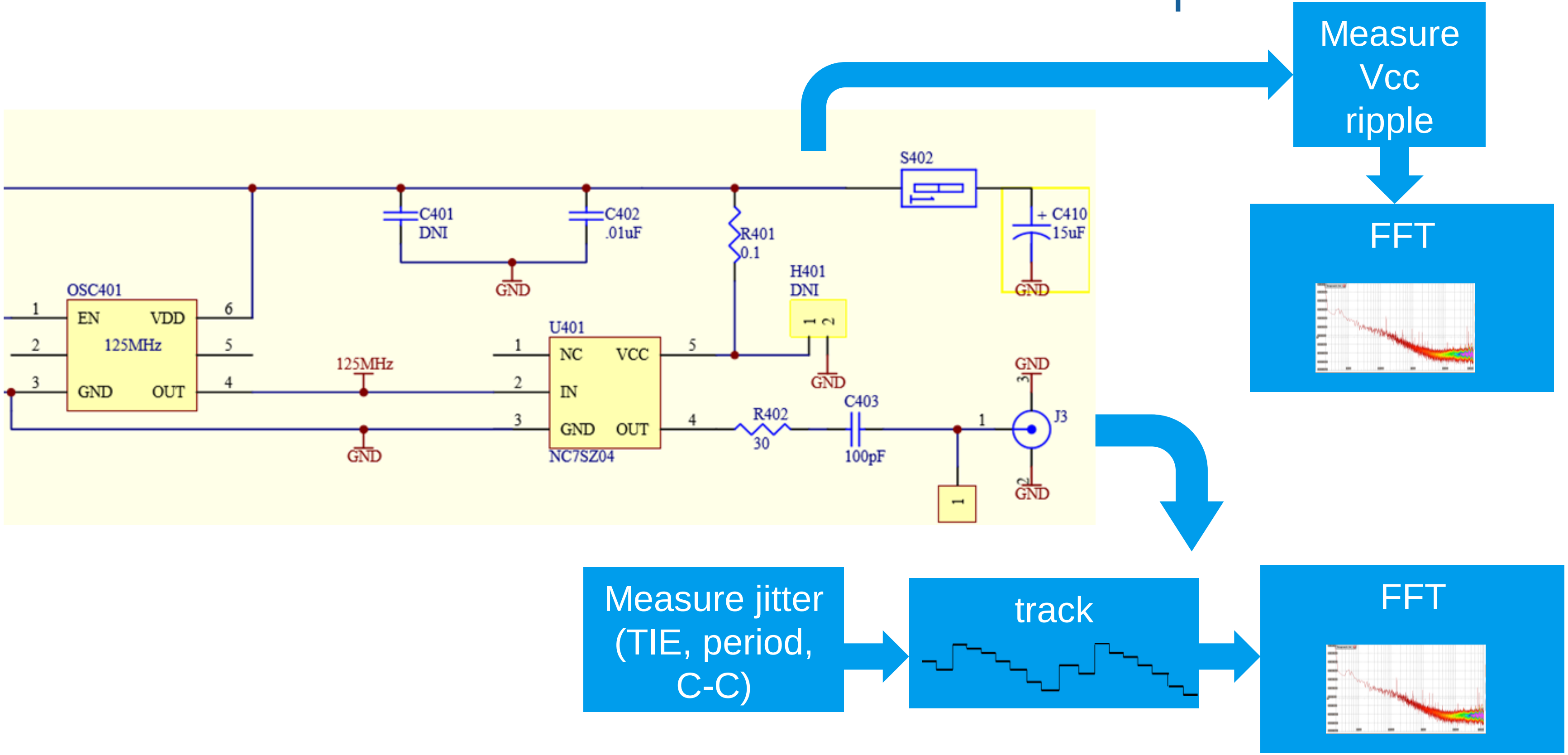


Measurement frequency response (JTF)



TIE measurement with 1 MHz PLL

Jitter and Power Measurement with an Oscilloscope



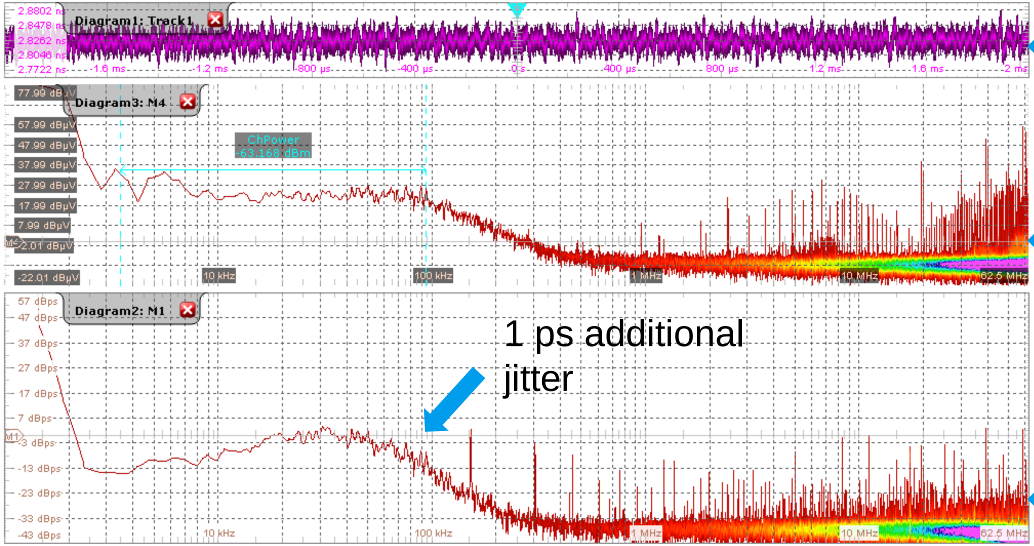
Spectrum Analysis of Jitter and Power Rail

Jitter track

Power Rail Spectrum

Jitter spectrum

Spectrum Analysis of Jitter and Power Rail



Jitter track

Power Rail Spectrum

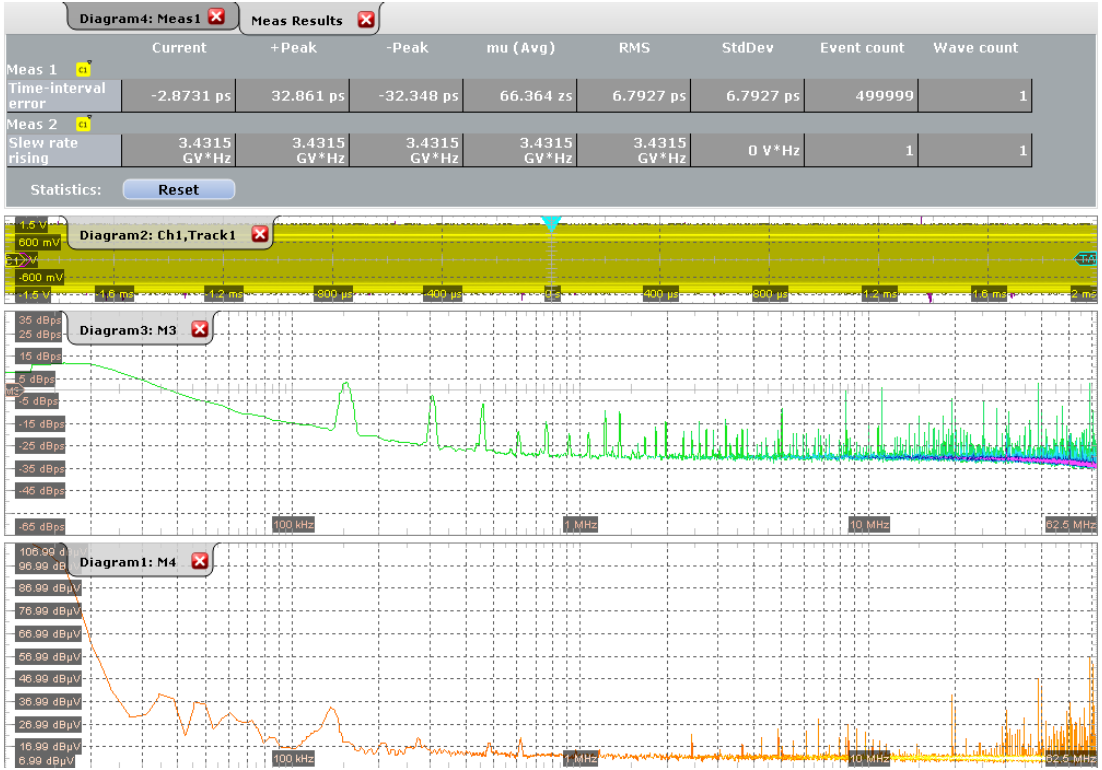
1 ps additional jitter

Jitter spectrum

Meas Results

	Current	+Peak	-Peak	mu (Avg)	RMS	StdDev	Event count	Wave count
Meas 1 C1 Time-interval error	2.821 ns	2.8689 ns	2.7822 ns	2.8249 ns	2.8249 ns	9.0483 ps	499998	1
Meas 2 C1 Slew rate rising	1.958 GV*Hz	3.5575 GV*Hz	1.1431 GV*Hz	1.9179 GV*Hz	1.939 GV*Hz	285.46 MV*Hz	499999	1
Meas 3 M4								

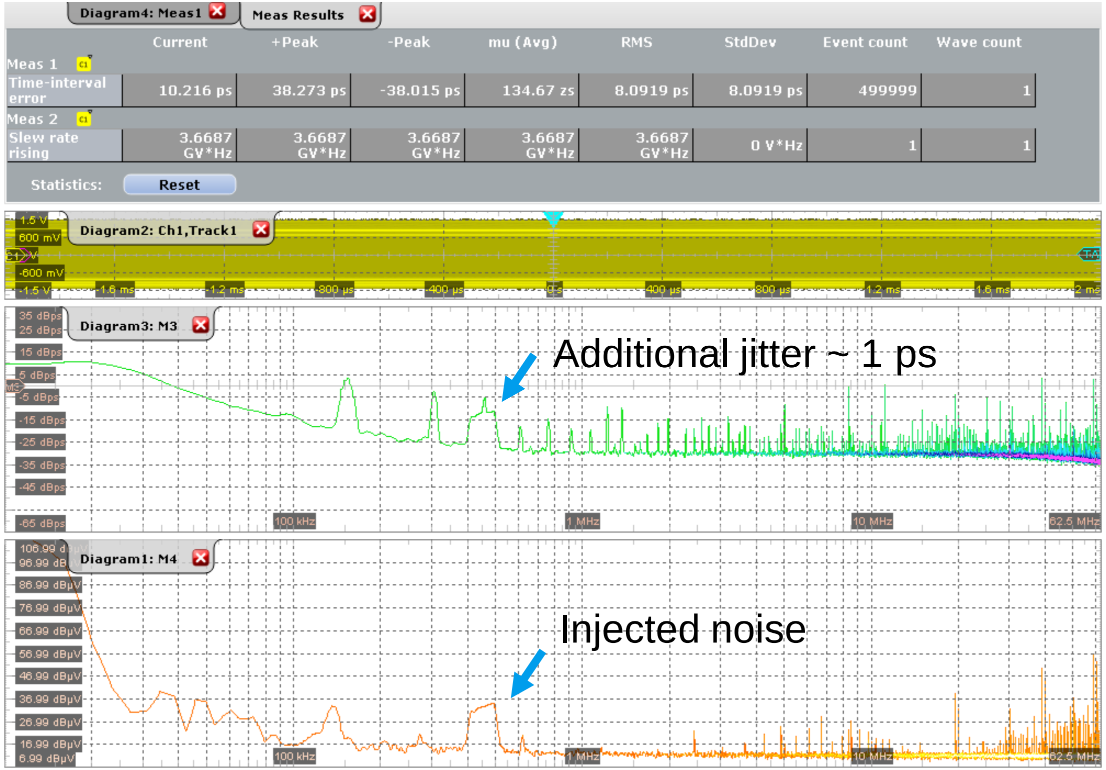
Comparison of power rail ripple and jitter



Jitter spectrum

Noise spectrum

Effect of power rail noise on Jitter



Jitter spectrum

Noise spectrum

Summary

- Voltage ripple on power rails is converted to jitter via the slew rate of clock and data signals
  - Even small ripple voltage can result in significant jitter
  - PSRR will reduce this effect in clock circuits but high frequencies are often passed through
- Specialized power rail probes are ideal for accurate noise measurement
  - Large offset range with 1:1 attenuation
  - Wide bandwidth
  - Low loading
- Spectrum analysis is a powerful tool for analyzing sources of noise and jitter
  - FFT of the Jitter time trend (track) shows frequency content of jitter
  - FFT of voltage ripple displays corresponding spectrum for the power rail
  - Increased voltage noise leads to increased jitter