Stony Brook University | Spellman High Voltage Power Electronics Laboratory

SBU Research on Integrated Power Modules

Yang Li

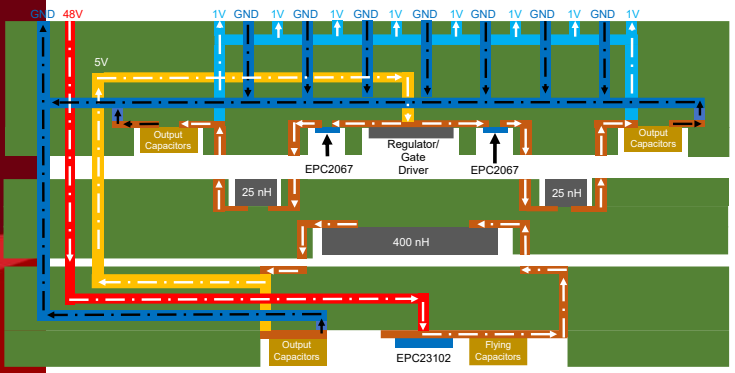
November 9, 2025

Outline

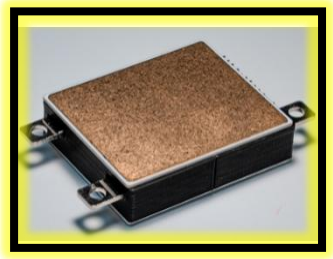
- **Recent SBU Module Development Activities**
- **High-voltage Module Co-design Framework (PA-PDK)**
- **Module Designs for EMI Mitigation**
  - Double Side Cooled GaN Module
  -TNPC SiC Module with Shielding Layer
- **Module Design for EV Traction Inverter**
  - Ex: Three-level X-type Power Module

Recent SBU Integrated Power Module Development

Semiconductor Research Corporation

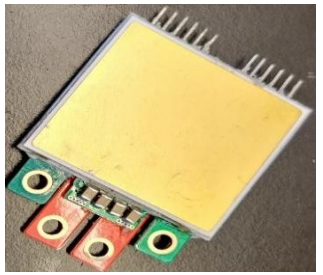


48-1 V, GaN POL in Embedded Sub. Package

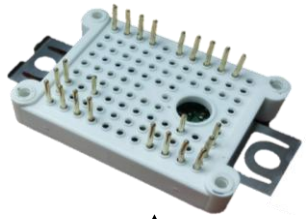


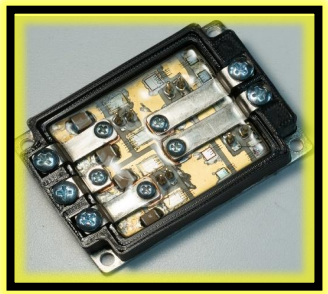
Double-side cooled modules

Hybrid Packaged TNPC modules

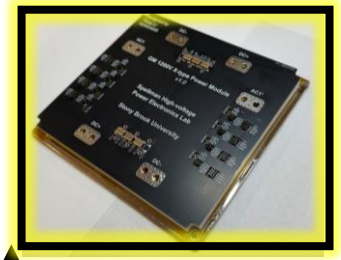


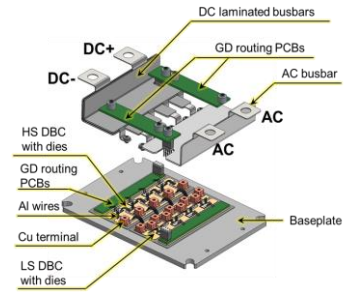
20kV Diamond PCSS





Multi-layer stacked DBC TNPC Modules





10kV Super-Cascode

Sandia National Laboratories

650V GaN

1200/1700V SiC

3.3/6.5 kV SiC

>10 kV

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American Made Silicon Carbide (SiC) Packaging Prize

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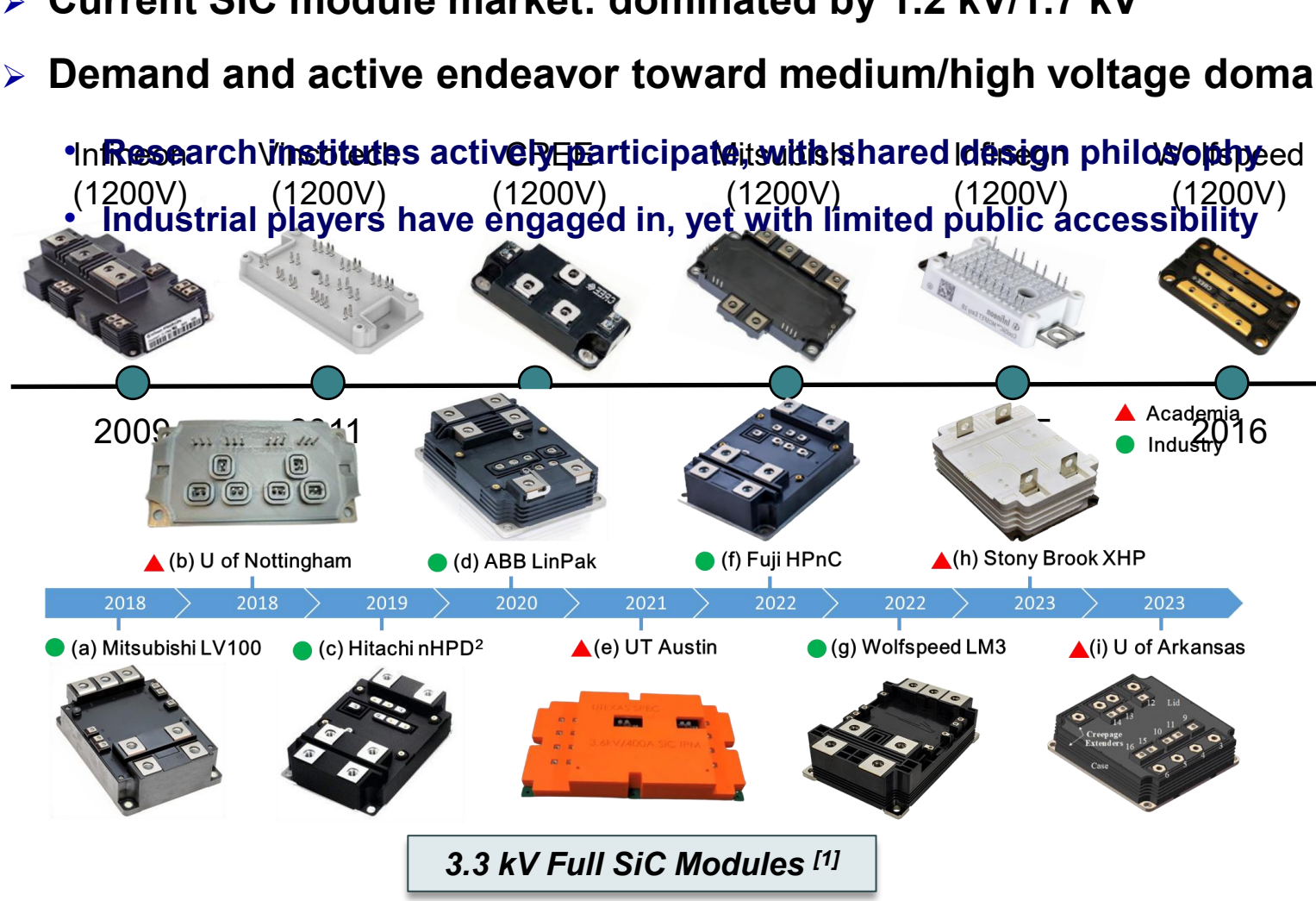
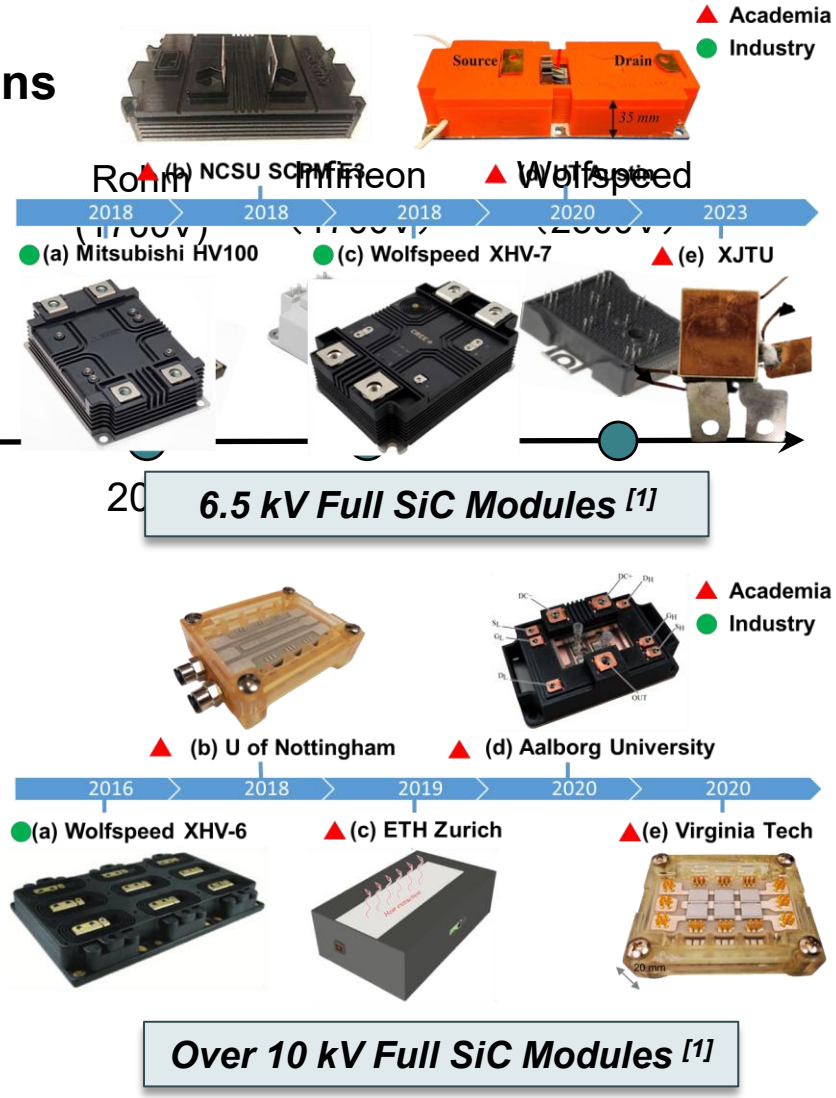
State-of-the-Art and Challenges

- **Current SiC module market: dominated by 1.2 kV/1.7 kV**
- **Demand and active endeavor toward medium/high voltage domains**
  - **Research institutes actively participate with shared design philosophy**
  - **Industrial players have engaged in, yet with limited public accessibility**

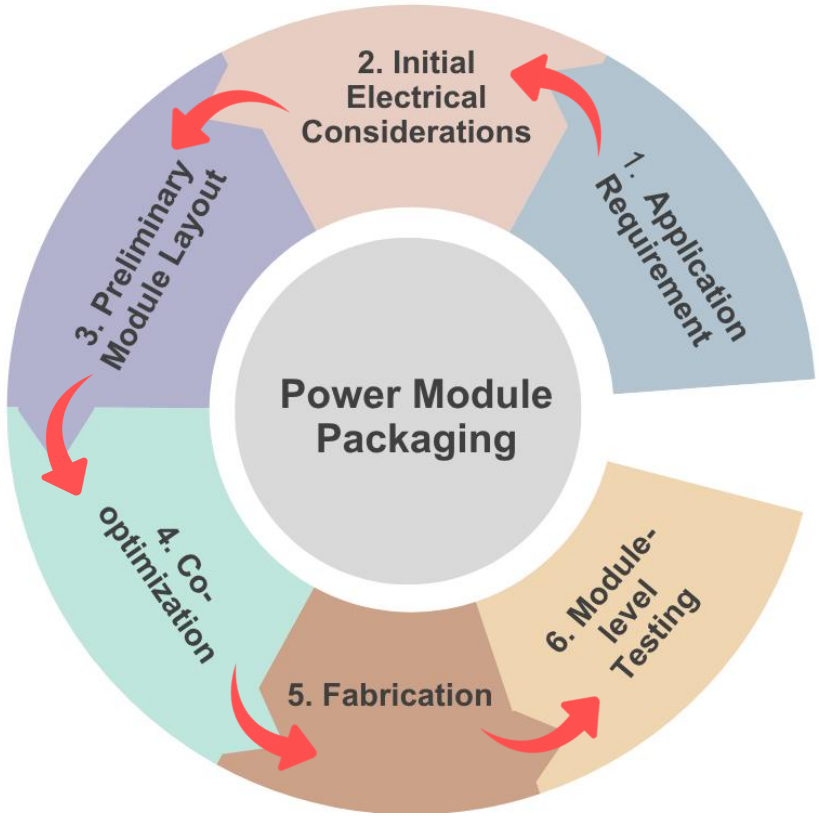




[1] Y. Li *et al.*, "State-of-the-Art Medium- and High-Voltage Silicon Carbide Power Modules, Challenges and Mitigation Techniques: A Review," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 14, no. 12, pp. 2177-2195, Dec. 2024.

State-of-the-Art and Challenges- *cont'd*

- **Module design involves a six-step process** *[2][3]*



4. Co-optimization considerations

- Electrical: parasitics control ✓
- Thermal: R_{th} and T_{jmax} ✓
- Mechanical: stress and warpage ✓
- High voltage concerns for MV/HV applications 🕒 ?

6. Module-level Testing

- Reliability: post-fabrication
- Design for Reliability (DfR): Microelectronics ✓
  Power modules ?

Module packaging design [1][2]

- Packaging and Assembly PDK ?

✓ : Well Investigated

🕒 : Investigation ongoing in Some Research

? : Needs to be addressed

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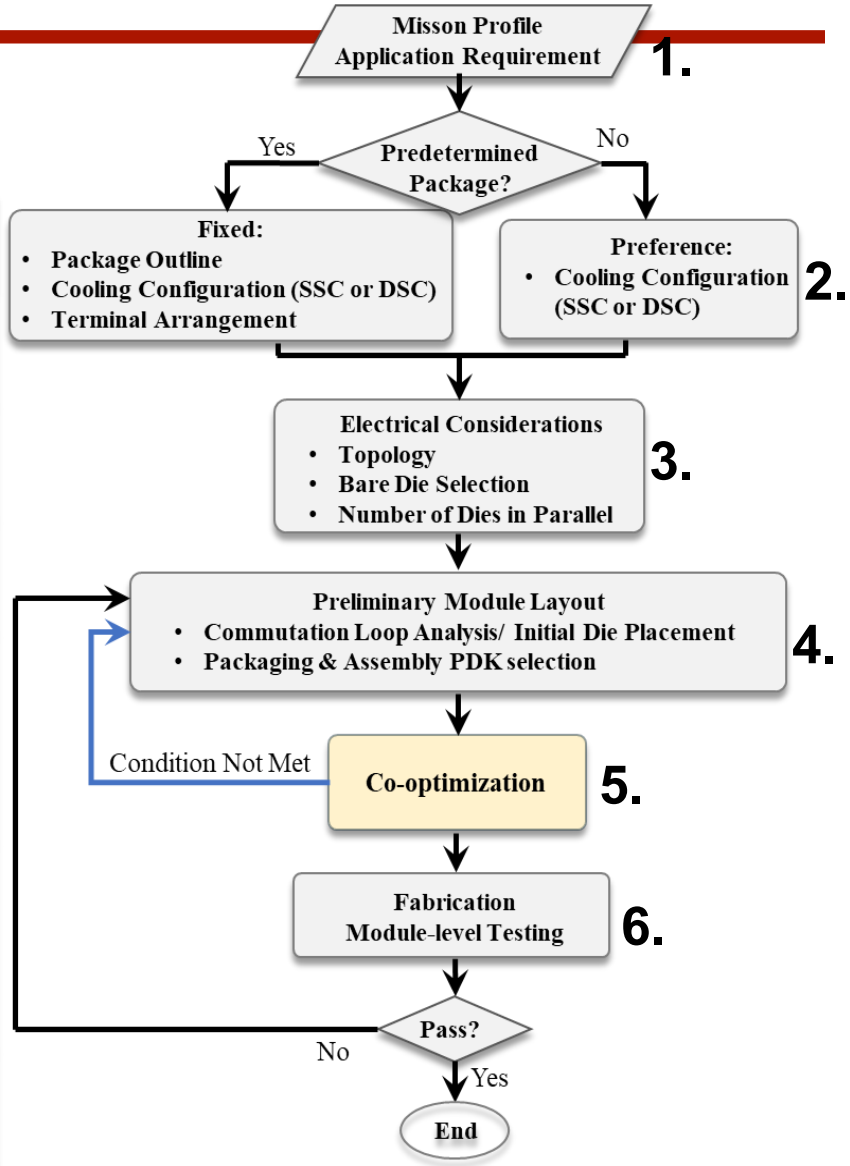
[2] A. I. Emon, Mustafeez-ul-Hassan, A. B. Mirza, J. Kaplun, S. S. Vala and F. Luo, "A Review of High-Speed GaN Power Modules: State of the Art, Challenges, and Solutions," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 11, no. 3, pp. 2707-2729, June 2023

Proposed Co-design Framework

- **Reflect diverse design requirements across device technologies, packaging configurations, and voltage classes.**

Step		Process and Purpose
1	Mission Profile/ Application requirement	• module V/I ratings • performance expectation (ex, efficiency/power density)
2	Package Preference	• If predetermined: package, cooling configuration are fixed; • Or need to set preference of cooling configuration
3	Initial Electrical Considerations	• Topology selection (ex, efficiency, control complexity, cost) • Bare die selection (ex, stress and cost)
4	Preliminary Module Layout	• Current commutation loops identification • Initial die placement and layout • **Packaging & Assembly Process Development Kit (PA-PDK)**: Materials and design rules, manufacturing capabilities
5	Co-optimization	• Multidisciplinary design optimization • HV concerns (ex, creepage & clearance; E-field; common-mode capacitance) • **DfR integration**
6	Fabrication & Module-level testing	• Assembly process verification • Functionality & reliability qualification tests



Y. Li *et al*., "Co-design Framework for High Power, Medium/High Voltage WBG Power Modules: Case Study with 3.3 kV/200 A Wire-Bonded Low-Inductance SiC Half-Bridge Module," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*

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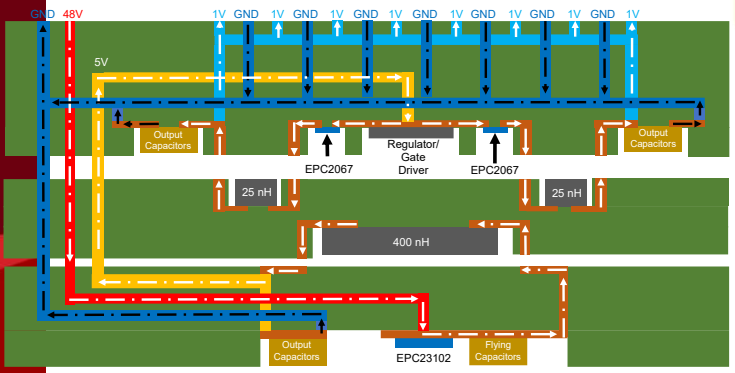

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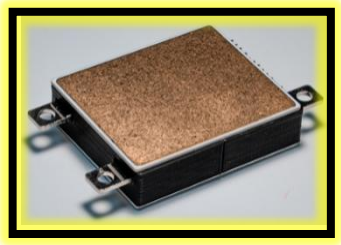

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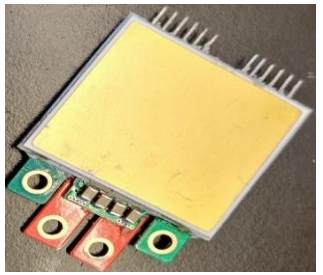

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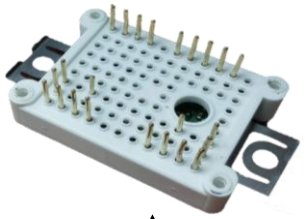

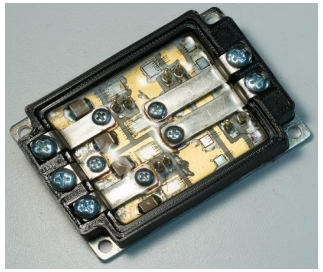

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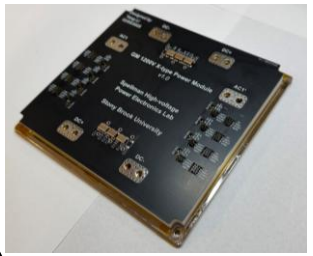

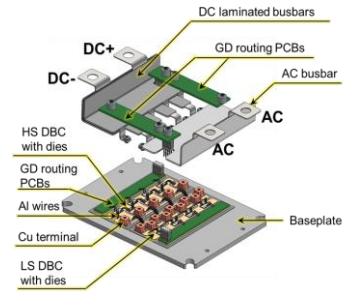

Super-Cascode

650V GaN

1200/1700V SiC

3.3/6.5 kV SiC

>10 kV SiC

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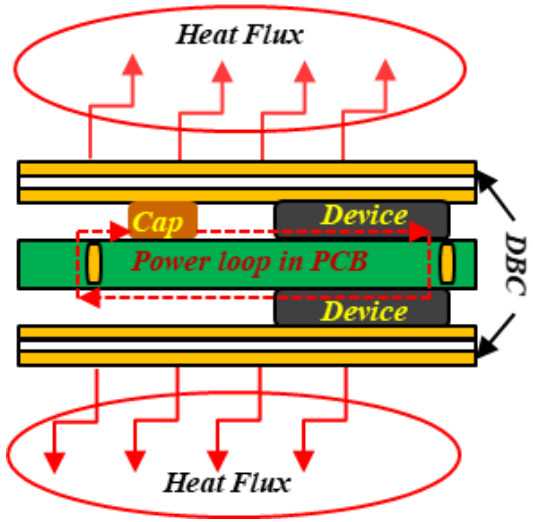
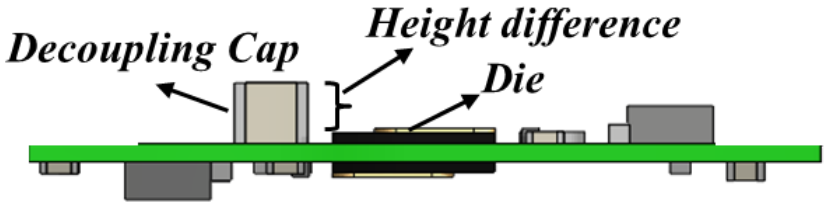
Features of the Designed Module

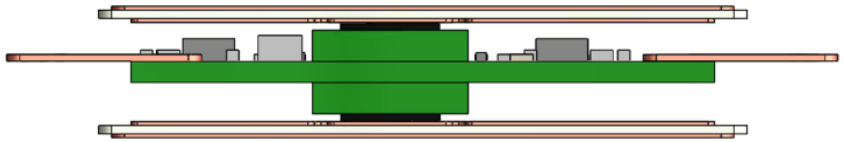
- 650V/60A half bridge phase leg with integrated gate driver
- Vertical commutation loop, thus low power loop inductance and less EMI
- However, it creates challenge in manufacturability. Solution?
- Mother board/Daughter card concept



Conceptual drawing



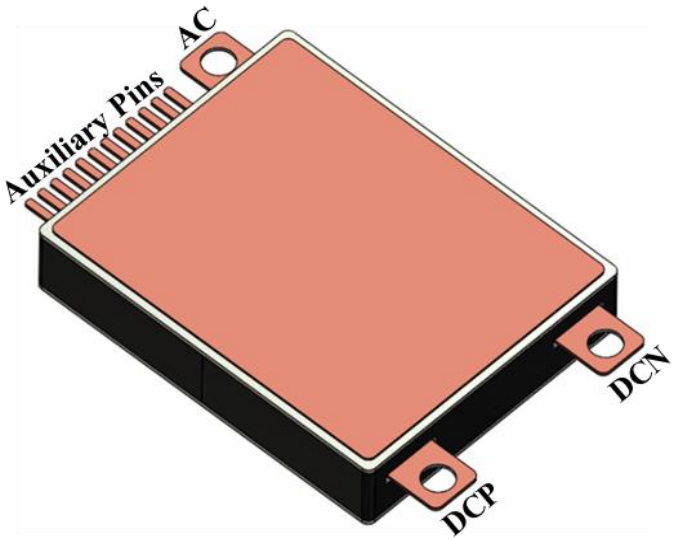
Difficulty in manufacturability



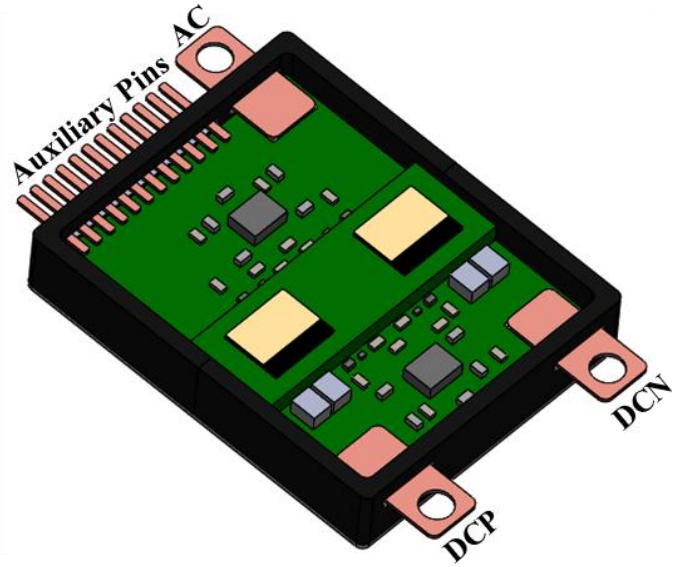
Proposed solution

Detail CAD Model of the Proposed Package

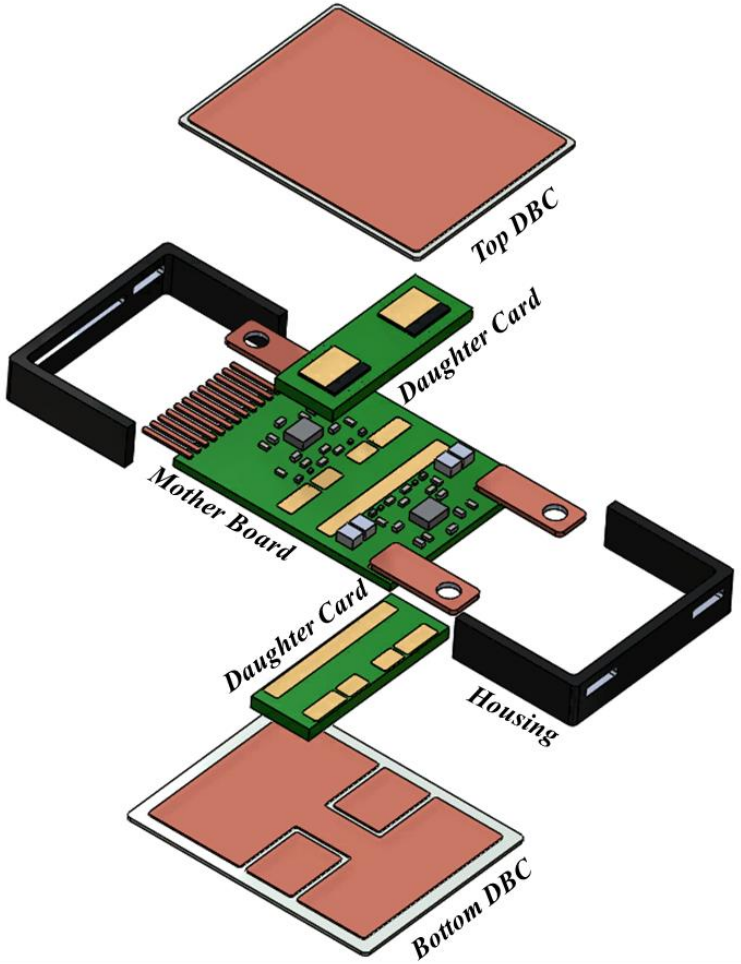
- **Input and output power pins are in the opposite sides of the module**
  - **Auxiliary pins are placed in the same side of the power output**
  - **Decoupling capacitors are integrated inside of the module**
- **Heat can be removed from both top and bottom side**
- **Module is enclosed with 3D printed casing (ABS plastic)**



Completed module



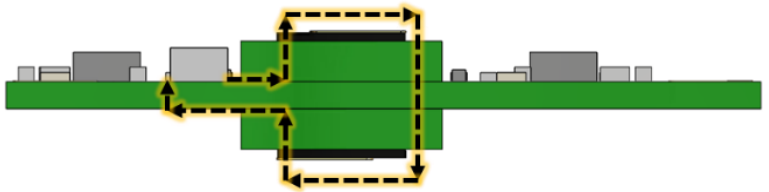
Top DBC removed



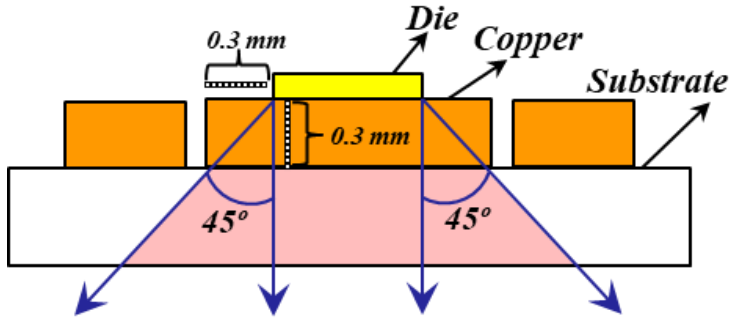
Exploded view

Parasitic Extraction

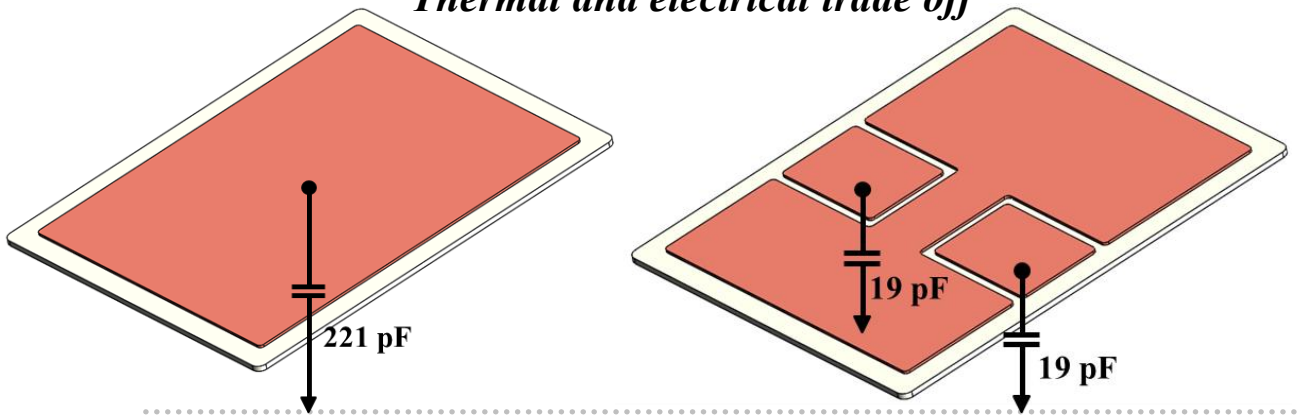
- Ansys Q3D is used as a tool for FEA analysis. Power loop : 0.91 nH
- DBC is optimized to lower C_{CM}
- Trade off analysis is performed for thermal and EMI benefit



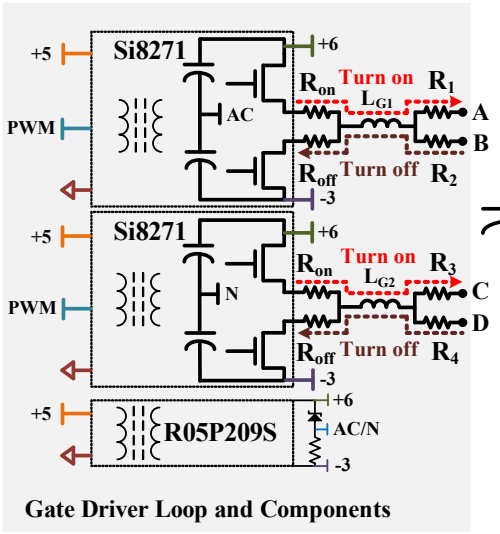
Vertical commutation loop



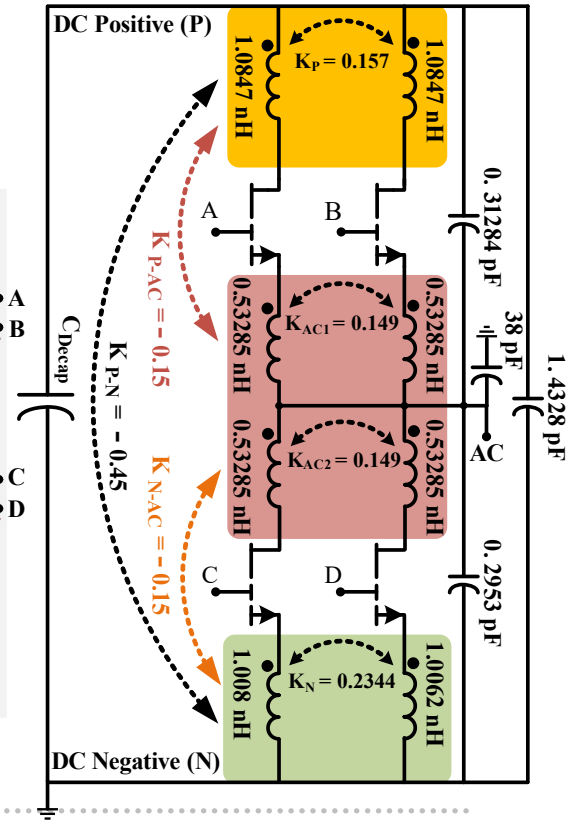
Thermal and electrical trade off



Extracted parasitic capacitance



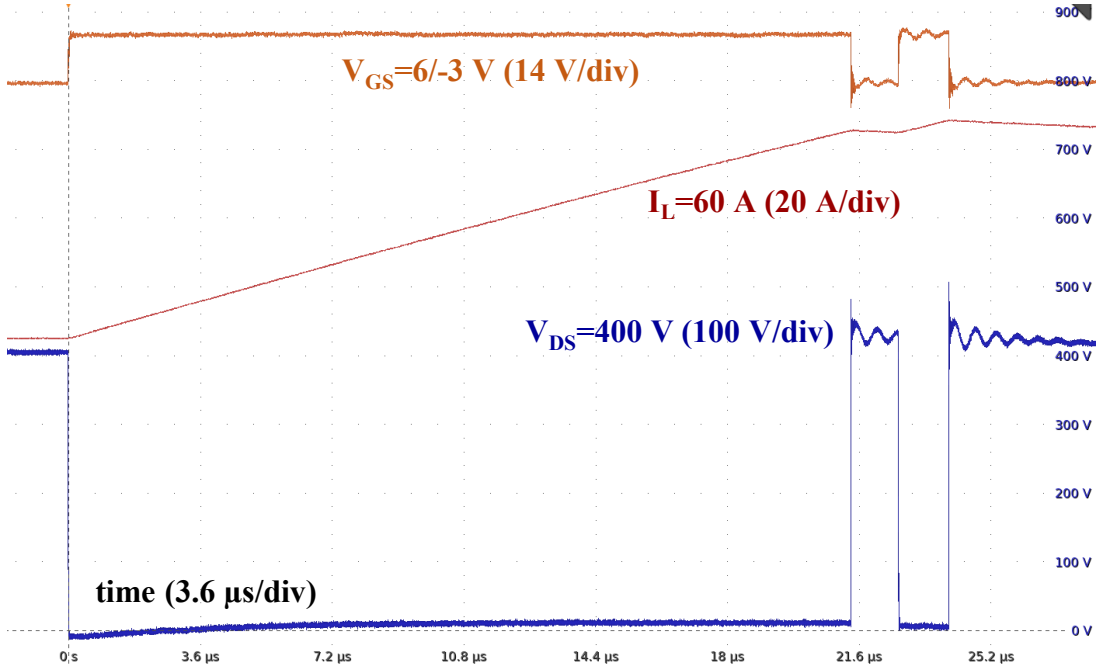
Gate Driver Loop and Components



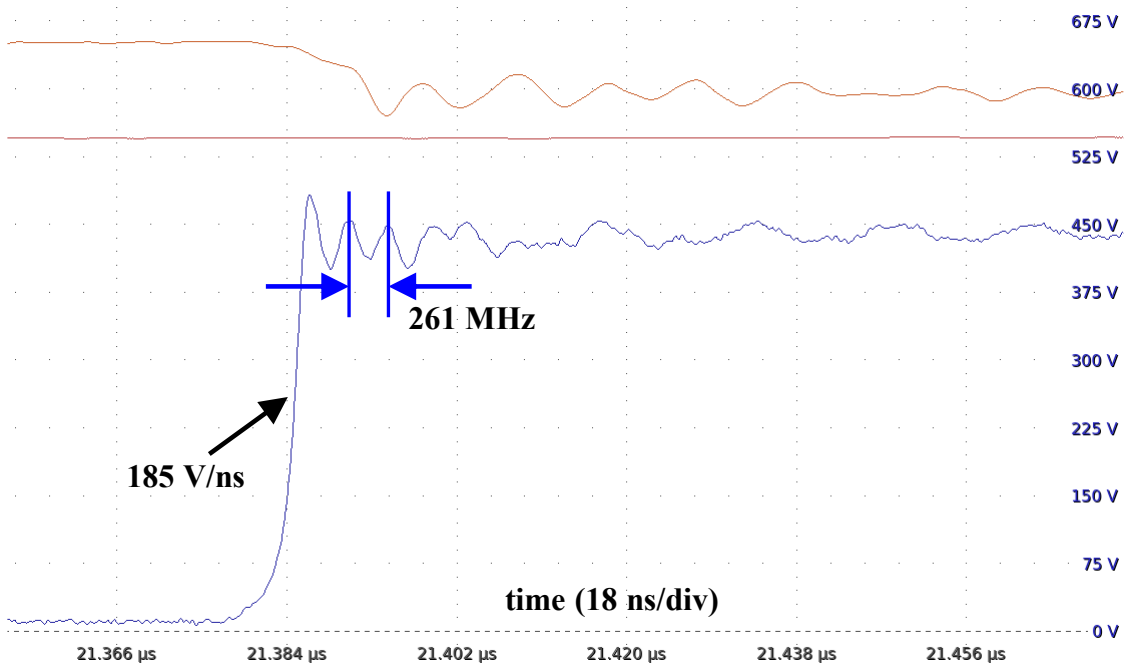
Extracted parasitic network

Electrical Characterization

- Standard Switching test (DPT) is performed in rated condition
- 131 µH air core inductor as clamping load
- Power loop inductance information is verified from ringing frequency of waveform



Switching waveform of the module



Turn off transient

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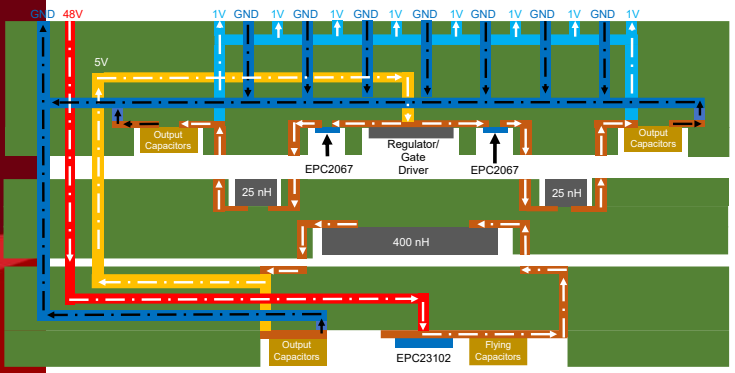

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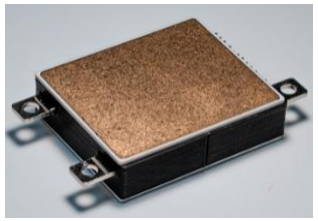

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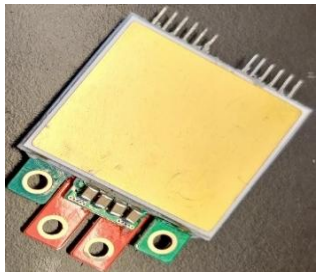

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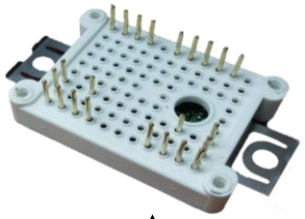

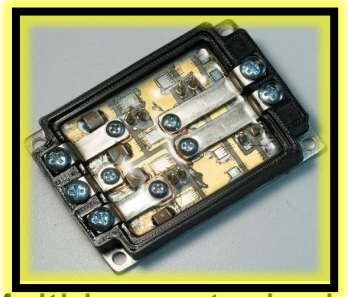

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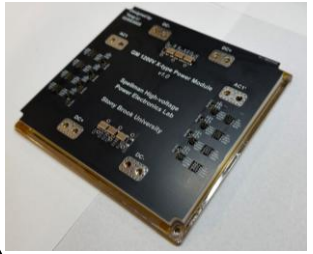

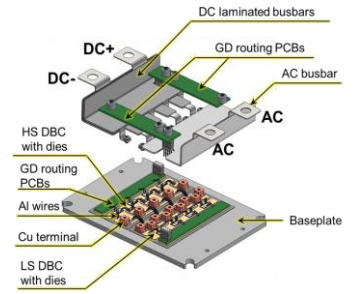

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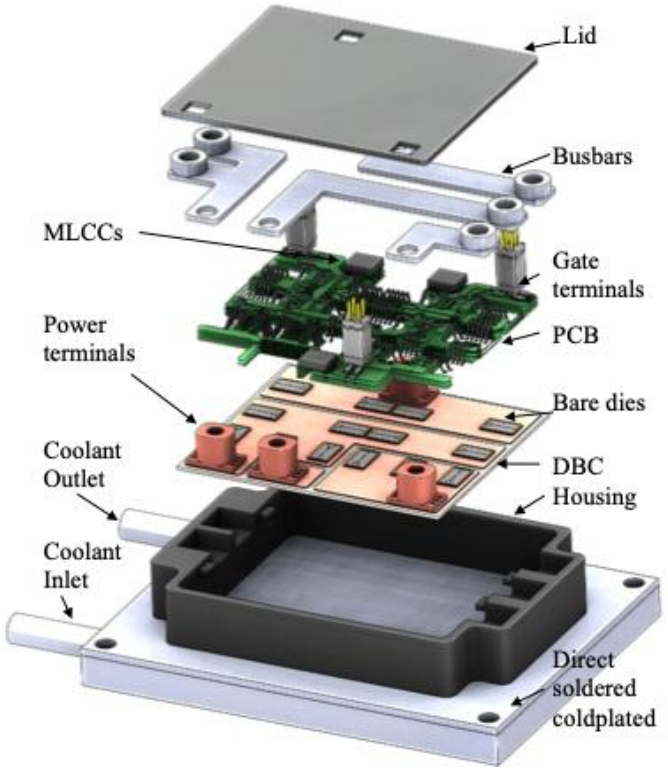
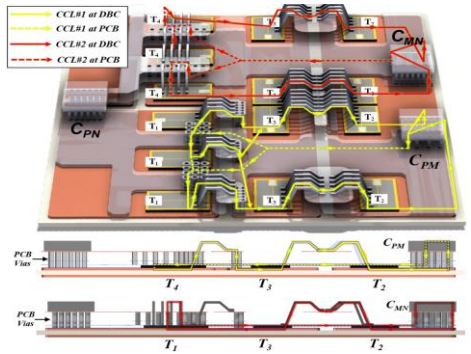
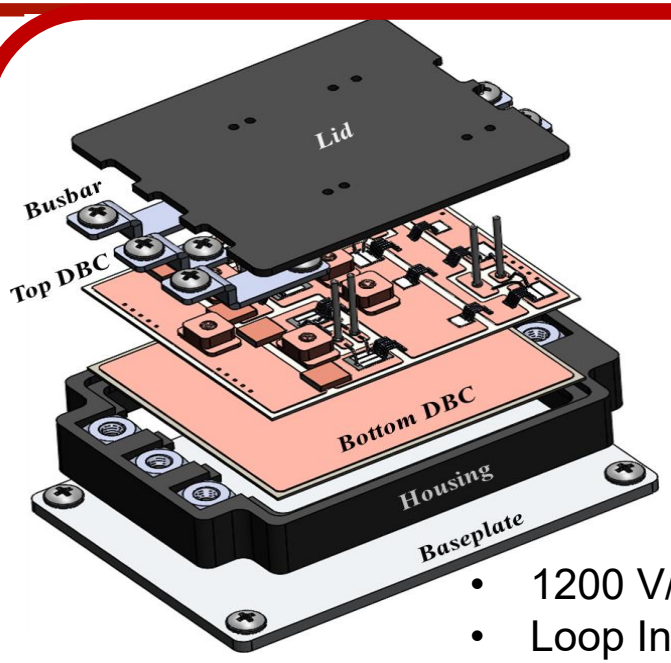
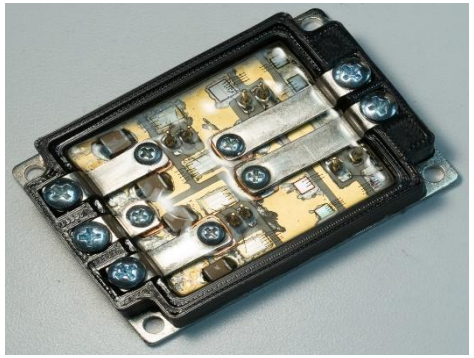




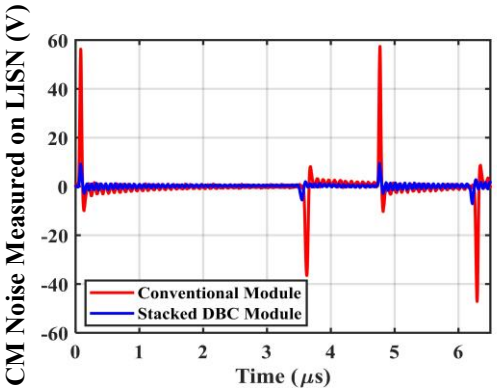
- 1200 V/300 A
- Loop Inductance: 2 nH /4 nH

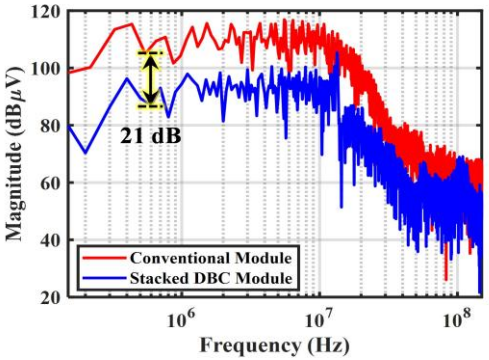
Hybrid Packaged SiC Module





- 1200 V/160 A
- Loop Inductance: 4 nH /8 nH

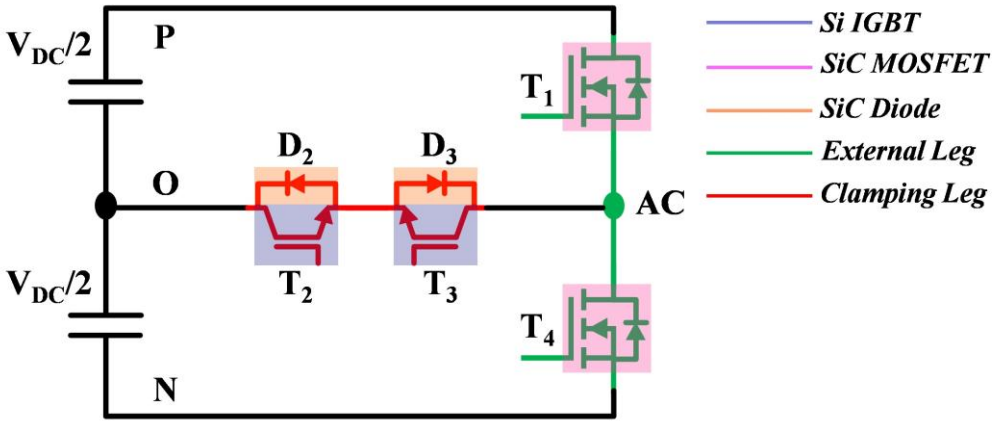




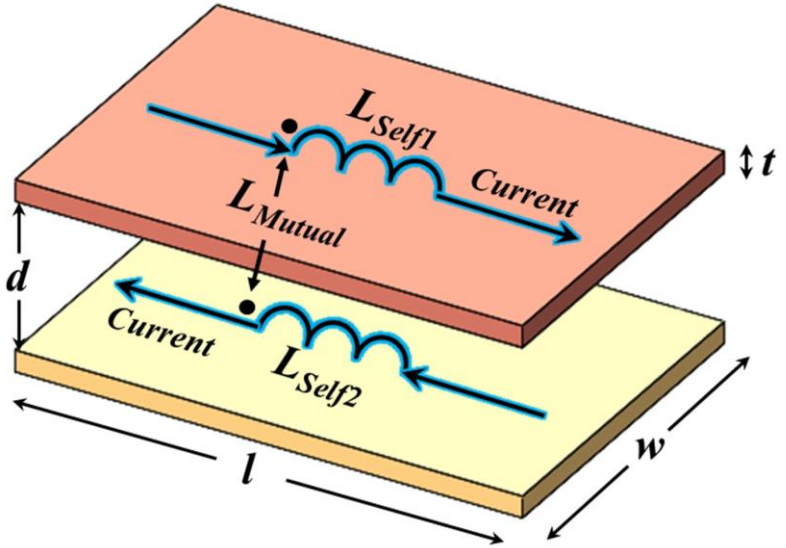
Multi-DBC Packaged SiC Module

Features of the Designed Module

- **1.2 kV/160 A 3-level TNPC module**
  - 3-level TNPC shows efficiency advantages over other multilevel topologies at medium power application
  - Requires lesser switch count compared to other multilevel topologies (3-level NPC and ANPC)
- **Hybrid combination of SiC MOSFET and Si IGBT**
  - Reduce cost without sacrificing on switching loss
- **Stacked DBC enabled vertical power loop and EMI shielding**
  - Power loop inductance : 4.01 nH
  - 20 dB reduction of common mode noise

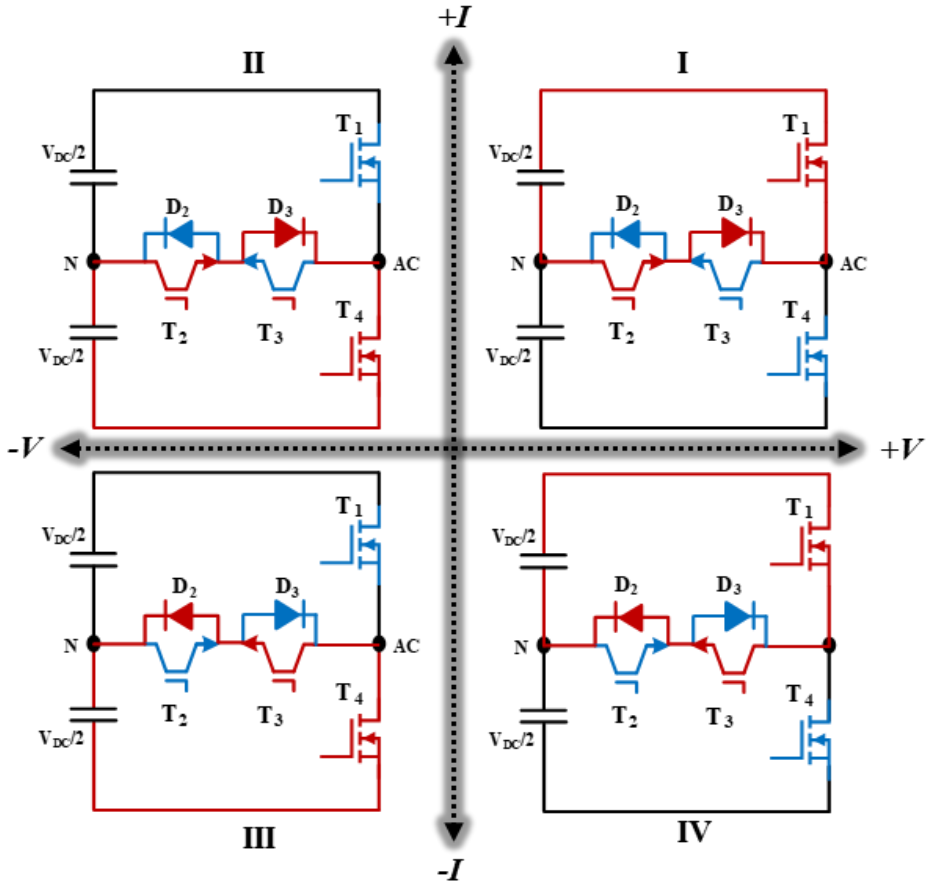


SiC MOSFET in outer leg and Si IGBT in clamping leg

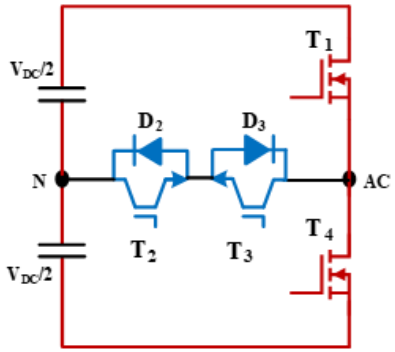


Vertical commutation loop to reduce inductance

Commutation Loop Analysis



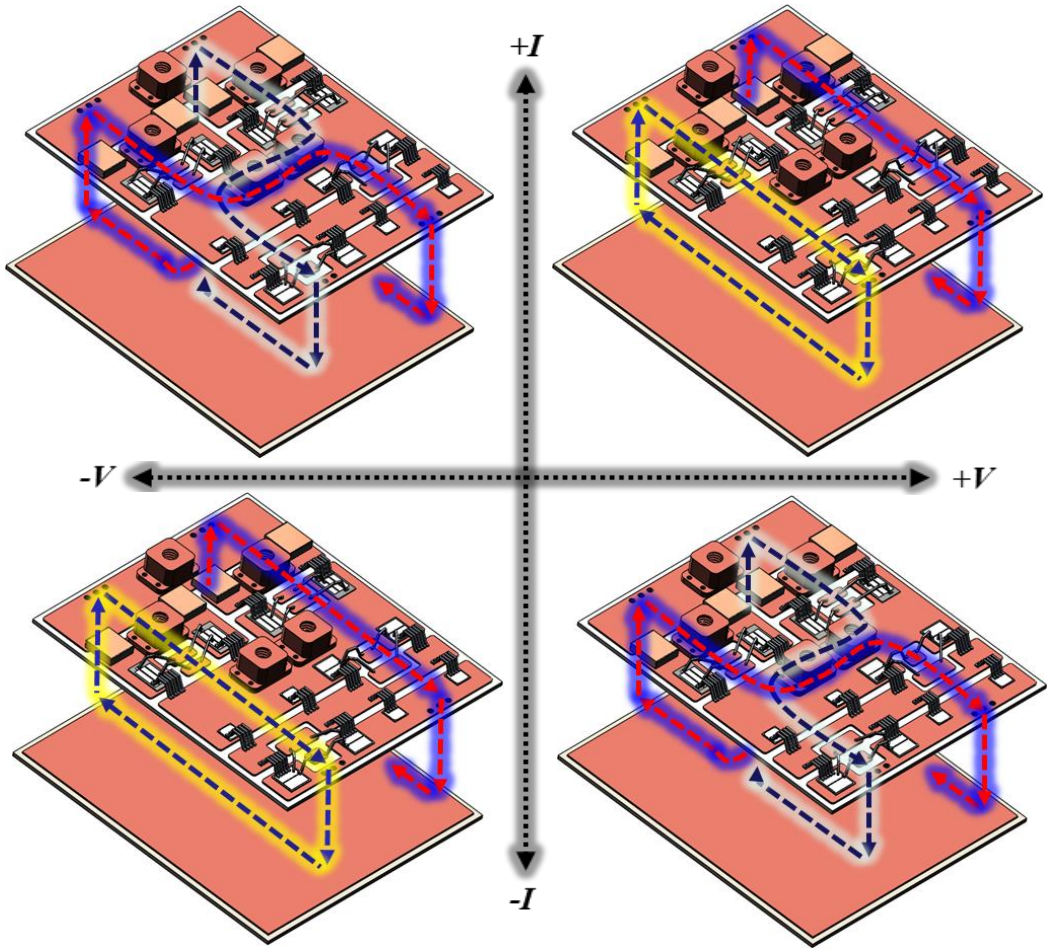
a) Commutation loop for three level operation at four quadrant



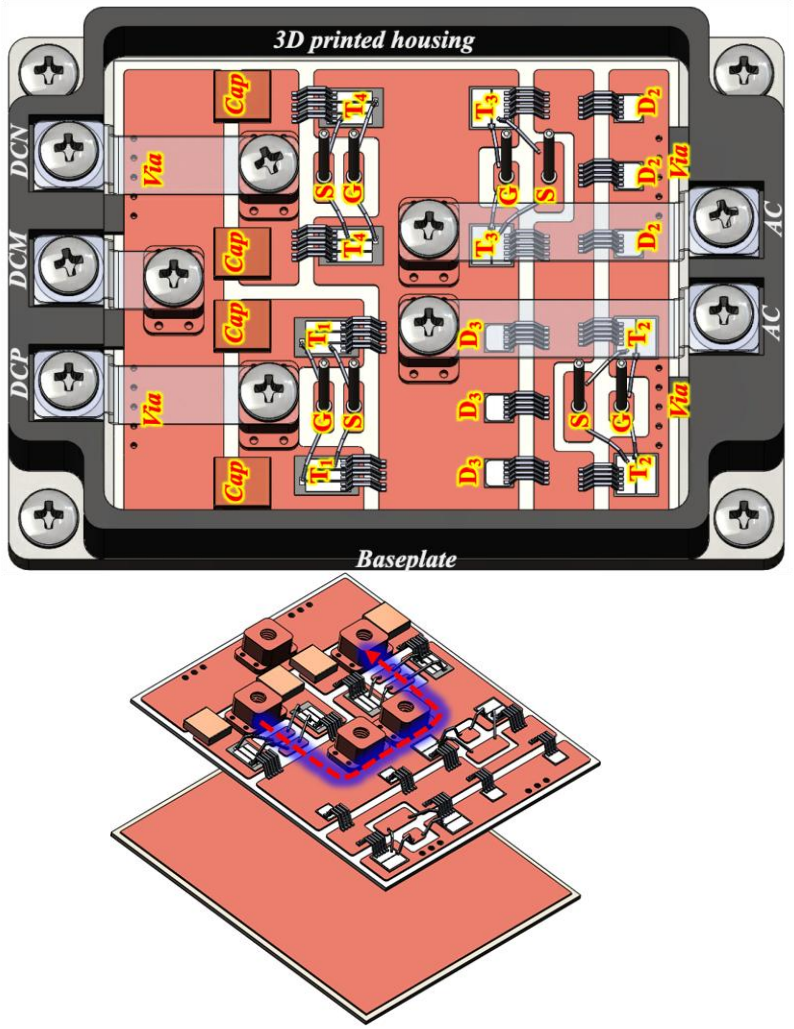
b) Commutation loop for two level operation

Commutation loop for three and two-level operation

Commutation Loop Analysis



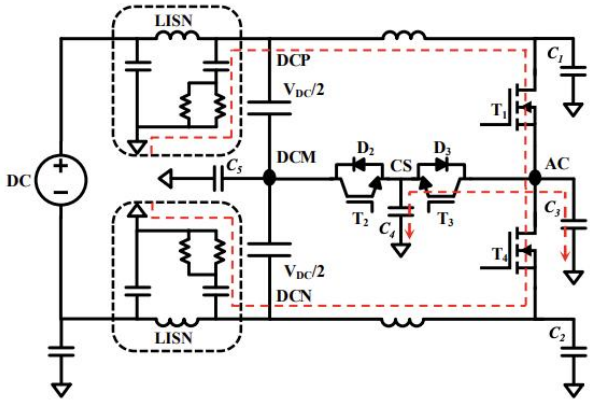
a) Commutation loop for three level operation at four quadrant



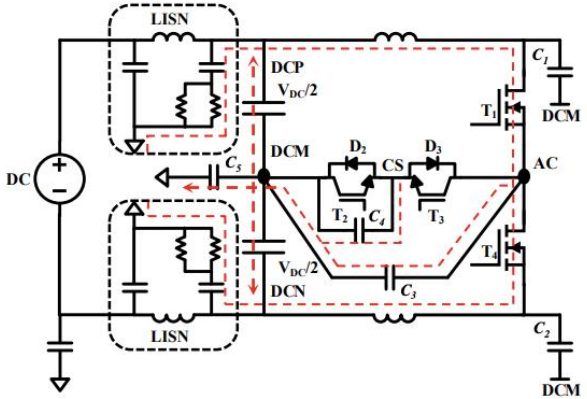
b) Commutation loop for two level operation

Commutation loop for three and two-level operation

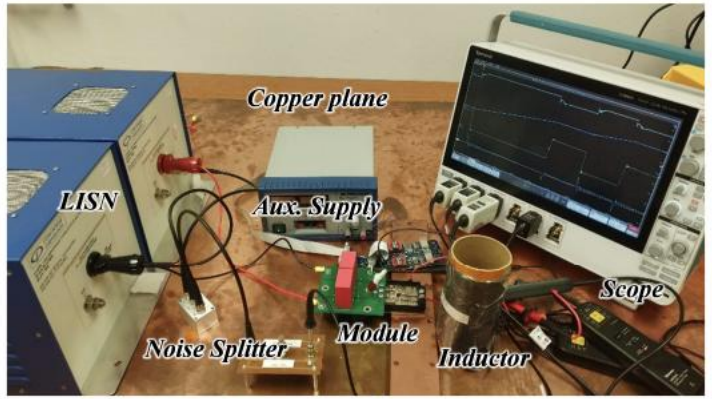
EMI Reduction Through the Shielding Layer



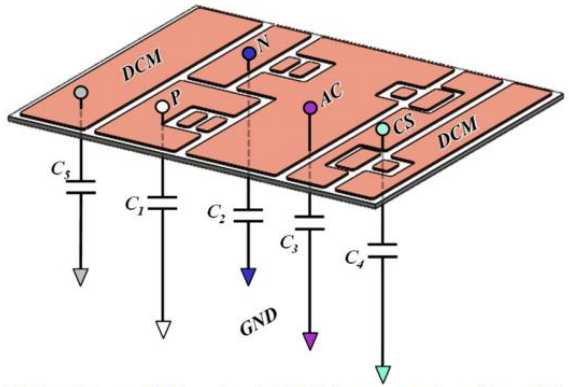
a) CM noise path for single DBC conventional module



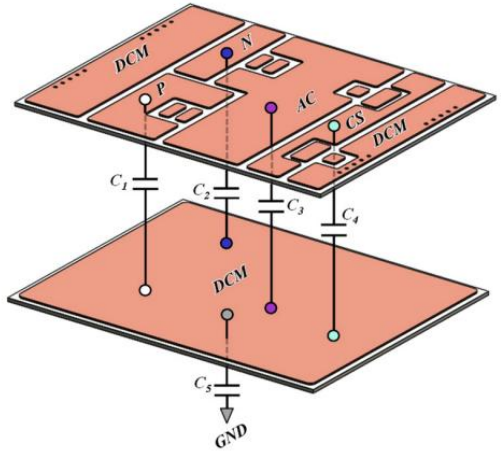
b) CM noise path for stacked DBC module



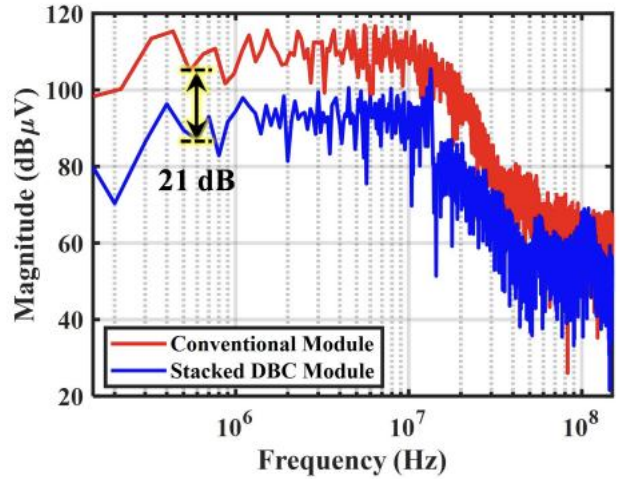
a) EMI test bench for CM noise measurement



c) CM noise path for single DBC conventional module



d) CM noise path for single DBC conventional module



d) Comparison of CM noise in frequency domain

The module has built-in bypass that reroutes switching noise currents internally in the module itself, rather than directly injecting into system ground plane

Summary

- Power module packaging plays an important role in noise propagation/ mitigation
- Use of low inductance package design can help to reduce voltage/current overshoot and ringing, and thus help to reduce EMI noises
- Reducing parasitic capacitance from the AC point to ground can help to reduce the common mode noise emission

Thank you for your time!

Question and Suggestion?