BASIC DESIGN PARAMETERS FOR STATIC H-BRIDGE INVERTERS

IEEE Conference 2022

By

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Sample LC Output Filter Criteria from Reference Designs

Output filter

A simple filter on the output (L1, L2) attenuates the switching frequency, producing a clean sinusoidal waveform for output connections in terminals J4 and J5. The filter inductors and capacitors used on the demo board were chosen to provide the optional combination of benefits: low loss, good attenuation of the switching frequency, and small size. Consult the schematic and/or bill of materials to verify values; but in general, the cutoff frequency will be around 5kHz - 10kHz to accommodate 100Hz switching. The inductors have powder cores with relatively low permeability (60-90) and soft saturation characteristics. The inductors and/or capacitors can be changed to evaluate different filter designs.

Based on the Simulink simulation results we have selected a resonant frequency in the range: 600 to 900 Hz.

Having the resonant frequency we are able to select values of the inductor and capacitor. To achieve the required resonant frequency of the filter we have plenty of variants of L and C distribution. The values of the components have to be selected with consideration of their size, cost and availability. Considering the components available in the market, we have chosen following combination:

- L506 = 5 mH
- C605 = 6.8 μF

The resonant frequency of such a circuit is 863 Hz and falls in our range.

Basic H-Bridge Inverter Schematic

- Familiar H_Bridge Configuration

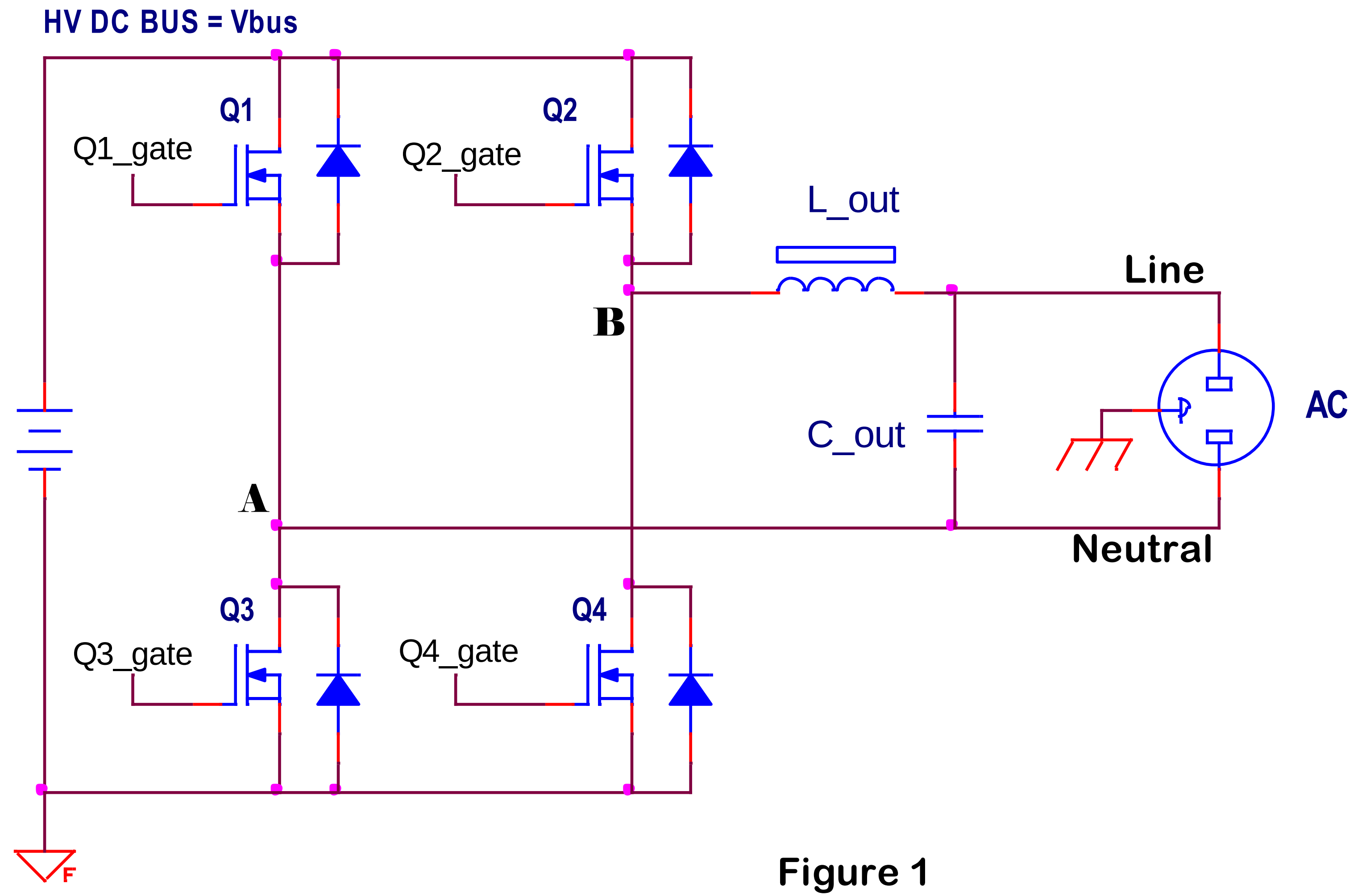


Figure 1

Bipolar Conduction

- For bipolar modulation, both legs of the H-Bridge (noted as A and B in Figure 1) switch at high frequency. In this configuration Q2 and Q3 conduct simultaneously and Q1 and Q4 conduct simultaneously. Refer to the Bipolar Waveforms timing diagram. During the positive half cycle of an AC output voltage waveform, we define the “on time” when Q2 and Q3 are conducting and the “off time” when Q1 and Q4 are conducting. Referring to Figure 2, during t_on, the voltage on L_out equals Vbus minus the instantaneous output voltage. Referring to Figure 3, during t_off, the inductor voltage equals the instantaneous output voltage plus Vbus.

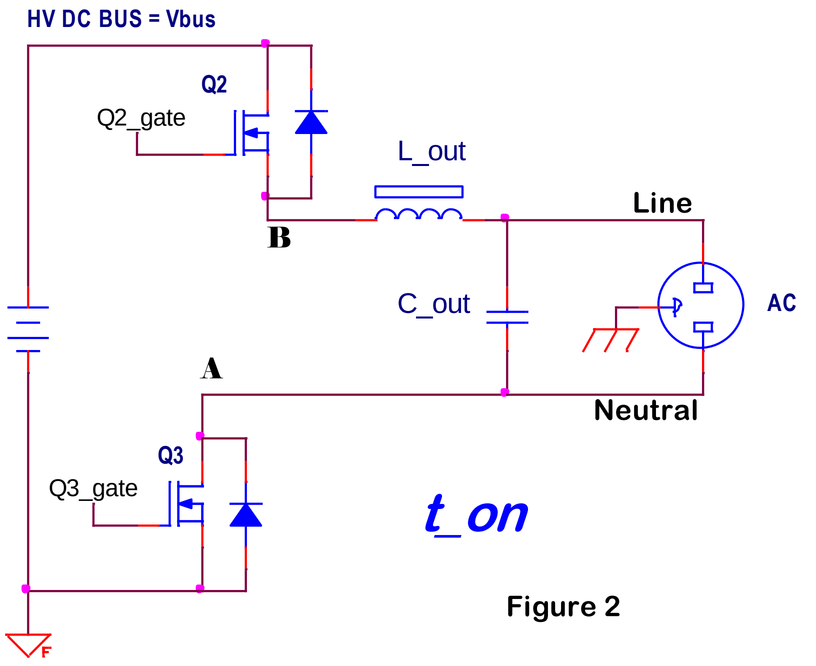


Figure 2

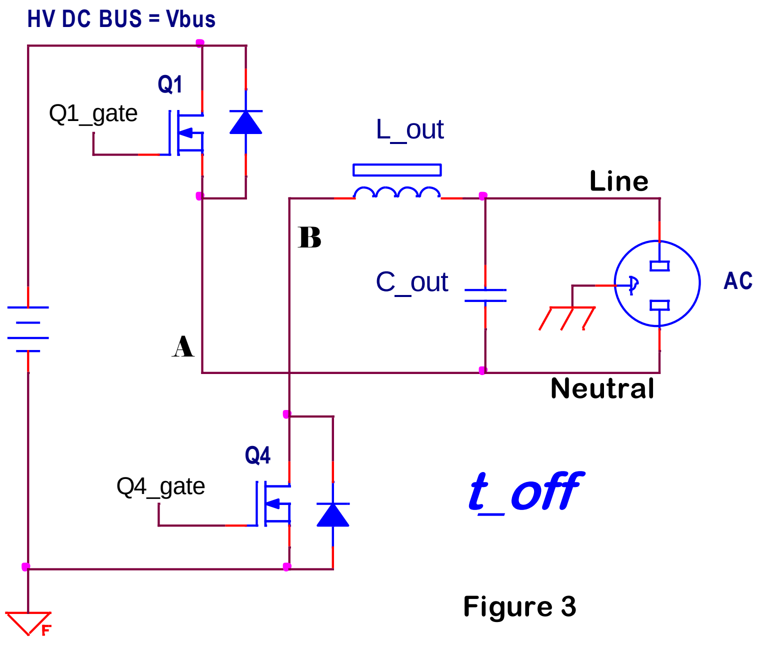
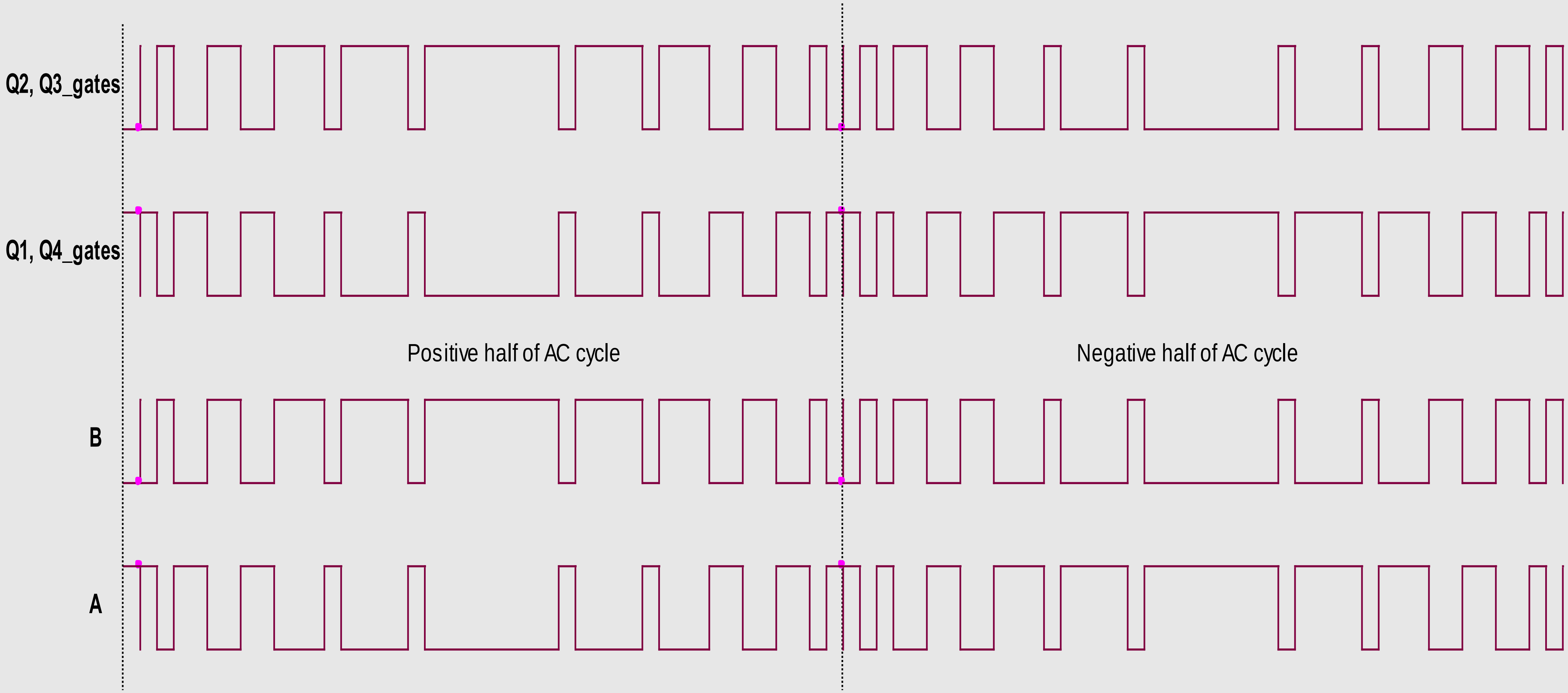


Figure 3

BIPOLAR WAVEFORMS



Bipolar Modulation Duty Cycle

- During the on-time, the pk-pk inductor current is given by – $$\Delta I\_on := \frac{(Vbus - Voi)}{L\_out} \cdot t\_on$$ eq1
- During the off-time, the pk-pk inductor current is given by – $$\Delta I\_off := \frac{(Vbus + Voi)}{L\_out} \cdot t\_off$$ eq 2
- Since the magnitude of the pk-pk inductor during the on time must be equal to the magnitude of the pk-pk current during the off time, eq 1 and eq 2 must be equal in magnitude (though opposite in polarity), we can equate eq 1 and eq 2 and the solve for the duty cycle with respect to the instantaneous output Voi –
- $$\frac{(Vbus - Voi)}{L\_out} \cdot t\_on = \frac{(Vbus + Voi)}{L\_out} \cdot t\_off$$
- By definition, t_on = δ * T and t_off = (1-δ) * T and by substituting into the above equation, we can solve for the duty cycle

$$\delta := \frac{1}{2} + \frac{Voi}{2 \cdot Vbus}$$

eq 3

Bipolar Modulation Pk-Pk Current

- Using the definition t_on = δ/ fsw we can substitute for t_on in eq 1

$$\Delta Ipk\_pk := \frac{(Vbus - Voi)}{L\_out} \cdot \frac{\delta}{fsw}$$

eq 4

- Substituting eq 3 for the duty cycle into eq 4 results

$$\Delta Ipk\_pk := \frac{(Vbus - Voi)}{L\_out \cdot fsw} \cdot \left[\frac{1}{2} + \frac{Voi}{2 \cdot Vbus} \right]$$

eq 5

- Solving for ∆Ipk-pk

eq 6

$$\Delta Ipk\_pk := \frac{Vbus^2 - Voi^2}{2 \cdot L\_out \cdot fsw \cdot Vbus}$$

Bipolar Modulation Output Inductor

- To determine the point where maximum ΔIpk-pk occurs, let the derivative of ΔIpk-pk (eq 6) with respect to Voi equal 0 and then solve for Voi. The derivative is

- $\frac{-Voi}{L\_out \cdot fsw \cdot Vbus}$ = 0 $\qquad Voi := 0$ $\qquad$ eq 7

As a general design practice, we select a value for the output inductor that allows a worst case pk-pk current in the inductor to be between 10% and 40% of the maximum peak load current. The peak load current is given by the expression

$$Ipk\_ac := \frac{\sqrt{2} \cdot Pout}{Vrms} \qquad \text{eq 8}$$

Bipolar Inductor

- We can define a factor ILfac to be ratio of pk-pk inductor current to the peak AC load current.
- i.e. (0.10 < ILfac < 0.40) for a pk-pk current of 10% to 40% of the peak load current.

$$\Delta Ipk\_pk := ILfac \cdot Ipk\_ac$$

eq 9

- Applying the Ilfac of eq 9 to the AC output current of eq 8 yields eq 10.

$$\Delta Ipk\_pk := ILfac \cdot \frac{\sqrt{2} \cdot Pout}{Vrms}$$

eq 10

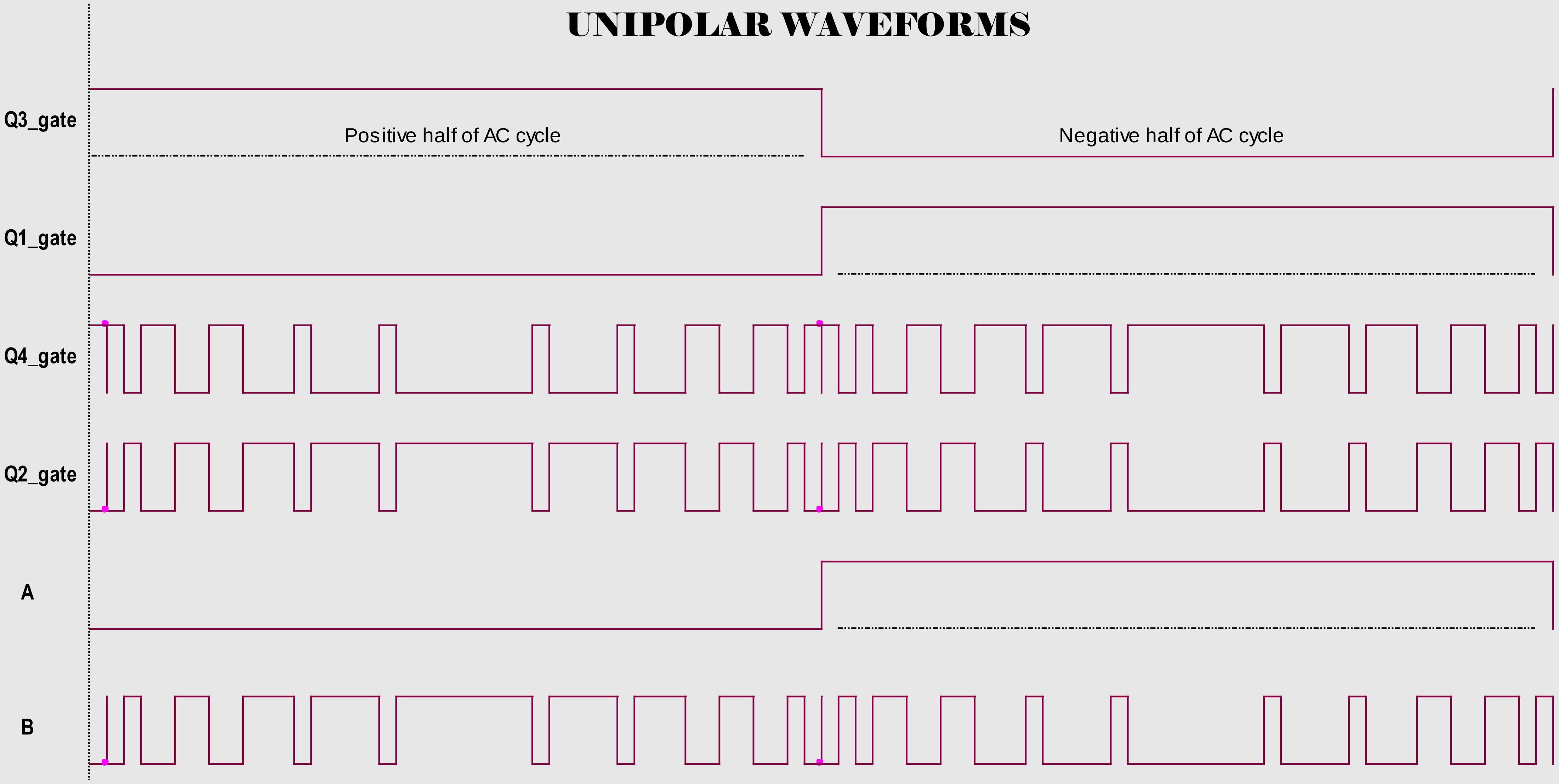
- Equating eq 10 for ΔIpk_pk to eq 1 for Δ*I_on* and solving for L_out yields eq 12.

$$L\_out := \frac{Vbus \cdot Vrms}{2 \cdot \sqrt{2} \cdot Pout \cdot fsw \cdot ILfac}$$

$$L\_out := \frac{0.353 \cdot Vbus \cdot Vrms}{Pout \cdot fsw \cdot ILfac}$$

eq 12

UNIPOLAR WAVEFORMS



Unipolar Conduction

- The equivalent schematics for H-bridge on-time and off-time are shown in Figure 4 and Figure 5 respectively. The relevant waveforms for unipolar modulation are shown below. The left side (the “A” leg) of the bridge switches at the fundamental frequency of the AC output i.e. 50Hz or 60 Hz. The right side of the bridge (the “B” leg) is pulse width modulated at high frequency to produce an AC output waveform. During the positive half of the AC output waveform, Q3 is on, Q1 is off and point A is connected to the negative of the HV DC BUS. Q2 and Q4 then switch in a manner like a synchronous buck regulator. Note that Q2 and Q4 are driven in a complimentary manner i.e. when Q4 is on, then Q2 is off and vice versa.

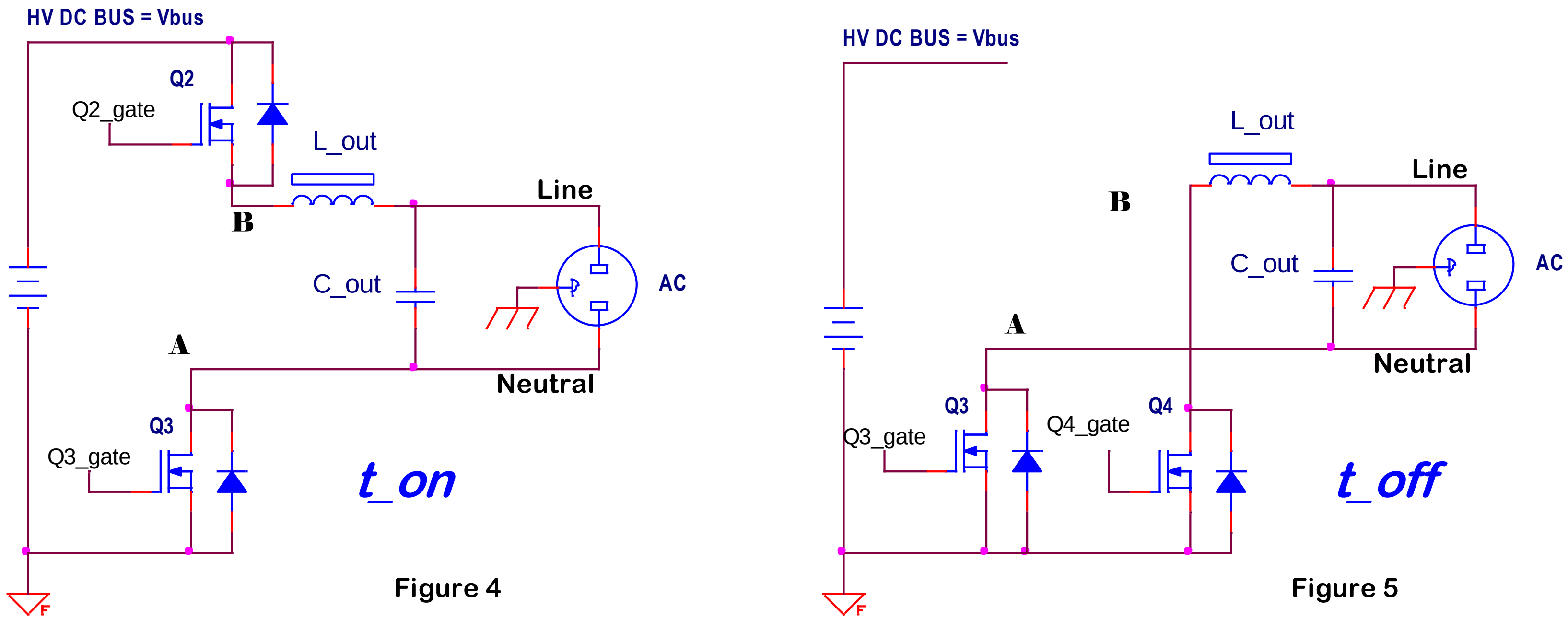


Figure 4

Figure 5

Unipolar Modulation Duty Cycle

- During the on-time, the pk-pk inductor current is given by – $\Delta I\_on := \frac{(Vbus - Voi)}{L\_out} \cdot t\_on$ eq 13

- During the off-time, the pk-pk inductor current is given by – $\Delta I\_off := \frac{(Voi)}{L\_out} \cdot t\_off$ eq 14

- We can equate eq 13 and eq 14 and the solve for the duty cycle with respect to the instantaneous output Voi
  - $\frac{(Vbus - Voi)}{L\_out} \cdot t\_on = \frac{(Voi)}{L\_out} \cdot t\_off$

Substituting t_on = δ * T, and t_off = (1-δ) * T, and solving for the duty cycle

$$\delta := \frac{Voi}{Vbus}$$

eq 15

Unipolar Modulation Pk-Pk Current

- Using the definition t_on = δ/fsw   we can substitute for t_on in eq 13

$$\Delta Ipk\_pk := \frac{(Vbus - Voi)}{L\_out} \cdot \frac{\delta}{fsw}$$

eq 16

- Substituting eq 15 for the duty cycle into eq 16 results in

$$\Delta Ipk\_pk := \frac{(Vbus - Voi)}{L\_out \cdot fsw} \cdot \left[\frac{Voi}{Vbus} \right]$$

eq 17

- Solving for ΔIpk-pk

eq 18

$$\Delta Ipk\_pk := \frac{Vbus \cdot Voi - Voi^2}{L\_out \cdot fsw \cdot Vbus}$$

Unipolar Modulation Output Inductor

- To determine the point where maximum ΔIpk=-pk occurs, let the derivative of eq 18 with respect to Voi equal 0 and then solve for Voi. The derivative is

  - $$\frac{1}{L\_out \cdot fsw} \cdot \frac{-2 \cdot Voi}{L\_out \cdot fsw \cdot Vbus} = 0$$

  $$Voi := \frac{Vbus}{2} \qquad \text{eq 19}$$

  - The solution shown for eq 19 yields the point where the pk-pk current is at a maximum. The maximum pk-pk output current occurs when Voi = Vbus/2, i.e. when the instantaneous AC output voltage is half of the DC bus voltage. Note from eq 15 that when Voi = Vbus/2, the duty cycle is 0.5.

Unipolar Inductor

- The peak load current is given by the expression

$$Ipk\_ac := \frac{\sqrt{2} \cdot Pout}{Vrms}$$

eq 20

- We can define a factor ILfac to be ratio of pk-pk inductor to the peak AC load current.
- i.e. (0.10 < ILfac < 0.40) for a pk-pk current of 10% to 40% of the peak load current.

$$\Delta Ipk\_pk := ILfac \cdot Ipk\_ac$$

eq 21

- Substituting eq 20 into eq 21 yields

$$\Delta Ipk\_pk := ILfac \cdot \frac{\sqrt{2} \cdot Pout}{Vrms}$$

eq 22

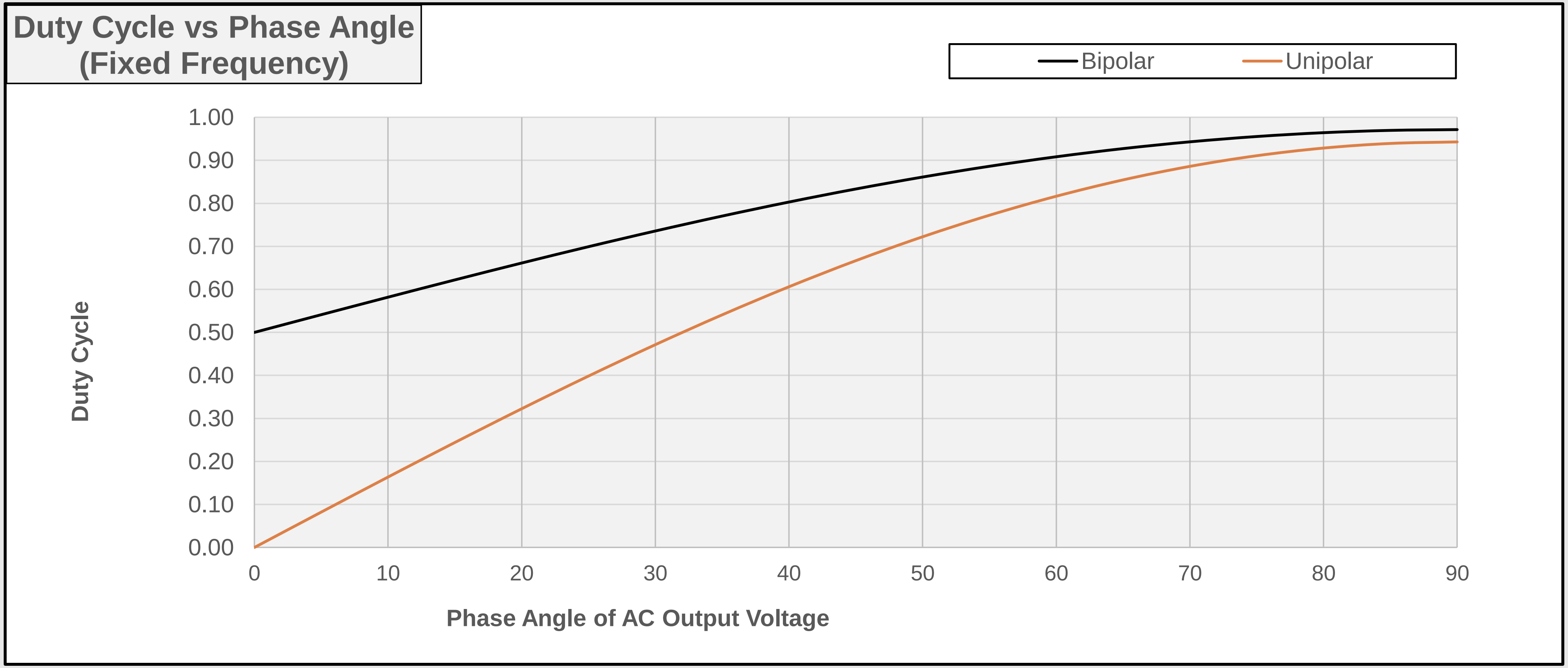
- Substituting eq 22 into eq 13 for ∆I_on and solving for L_out

$$L\_out := \frac{Vbus \cdot Vrms}{4 \cdot \sqrt{2} \cdot Pout \cdot fsw \cdot ILfac}$$

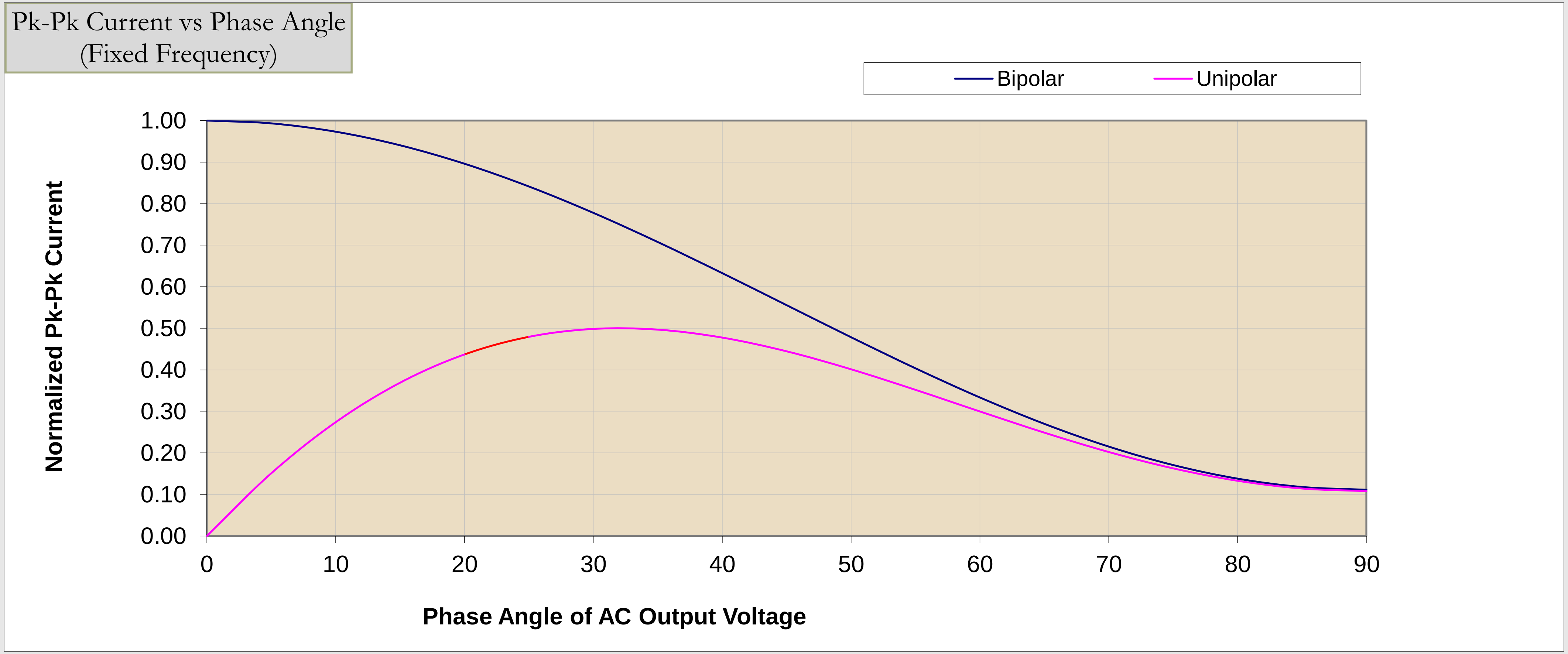
$$L\_out := \frac{0.177 \cdot Vbus \cdot Vrms}{Pout \cdot fsw \cdot ILfac}$$

eq 23

Bipolar vs Unipolar Duty Cycle



Normalized Bipolar vs Unipolar Pk-Pk Current



Summary – Bipolar vs Unipolar

Bipolar Modulation	Unipolar modulation
$\delta := \frac{1}{2} + \frac{Voi}{2 \cdot Vbus}$	$\delta := \frac{Voi}{Vbus}$
$\Delta Ipk\_pk := \frac{Vbus^2 - Voi^2}{2 \cdot L\_out \cdot fsw \cdot Vbus}$	$\Delta Ipk\_pk := \frac{Vbus \cdot Voi - Voi^2}{L\_out \cdot fsw \cdot Vbus}$
Maximum Ipk-pk occurs at Voi = 0	Maximum Ipk-pk occurs at Voi = Vbus/2
$L\_out := \frac{0.353 \cdot Vbus \cdot Vrms}{Pout \cdot fsw \cdot ILfac}$	$L\_out := \frac{0.177 \cdot Vbus \cdot Vrms}{Pout \cdot fsw \cdot ILfac}$

Output Capacitor

- I will discuss three different criteria to be considered in selecting the value of the inverter output capacitor.

First criteria - The minimum output capacitor value required to limit the output ripple voltage to a specified value, defined as ΔVcap.

$$C\_out := \Delta Ipk\_pk \cdot \frac{\Delta t}{\Delta Vcap}$$

eq 25

Using the expression $$\Delta Ipk\_pk := ILfac \cdot \frac{\sqrt{2} \cdot Pout}{Vrms}$$ eq 22

$$C\_out := \frac{0.707 \cdot Pout \cdot ILfac}{Vrms \cdot fsw \cdot \Delta Vcap}$$ eq 26

Using the expression $$\Delta Ipk\_pk := \frac{(Vbus - Voi)}{L\_out \cdot fsw} \cdot \left[\frac{Voi}{Vbus}\right]$$ eq 17

$$C\_out := \frac{Vbus}{4 \cdot L\_out \cdot fsw^2 \cdot \Delta Vcap}$$ eq 27

Output Capacitor continued

- Second Criteria - The preload current is generally required to implement a current mode control scheme so that there is a non-zero signal for the feedback with no load on the inverter output. Too large a capacitor will increase losses as there will be large, low frequency circulating currents in the H-bridge.

$$C\_out := \frac{ICfac \cdot Pout}{2 \cdot \pi \cdot F\_out \cdot Vrms^2}$$

eq

- Third criteria - Calculate the resonant frequency that the output inductor and output capacitor produce. As a rule of thumb, the resonant frequency should be at least a decade lower than the switching frequency (for good filtering), and a decade higher than the AC output frequency to have enough loop gain to regulate the output voltage at the highest output frequency

$$C\_out := \frac{1}{4 \cdot \pi^2 \cdot L\_out \cdot f\_reas^2}$$

eq 29

Conclusion

- 1 – Design equations are derived for the duty cycle and the peak to peak inductor currents for both bipolar and unipolar modulation schemes.

- 2 – Criteria for determining the output inductance and output capacitance are derived for both bipolar and unipolar modulation schemes.

- 3 – The unipolar modulation scheme requires an output inductor half the value required in a bipolar modulation scheme for a given peak to peak inductor current.
- 4 – The unipolar modulation scheme practically eliminates the switching losses in one leg of the bridge (the low switching frequency leg) which allows for a significant improvement in efficiency.

- Thank you.