Strategies for Designing Microwave Multilayer Printed Circuit Boards Using Stripline Structures

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Brief History of Stripline Design

✓ 1964: Matthais, Young and Jones “bible” of microwave coupled circuits published

✓ Interim: PTFE substrates used in radome apps-suspended stripline and lumped element design realizations only

✓ Stripline on soft substrates developed on Long Island, NY


✓ 1970’s: Woven glass reinforced PTFE laminates introduced

✓ 1990’s: Development of 2-d and 3-d EM simulation software (ADS, Microwave Office, HFSS, etc.)

✓ Today: Reliable PTFE/multilayer materials and techniques allow for empirical realizations of simulated performance
Outline

- Stripline vs Microstrip…or both in one pwb?
- Broadside vs Edge Coupled Traces (Designers Perspective)
- Via Design…often the limiting factor at High Frequency
- Registration and effect on RF Properties
- Prepreg Characteristics to 40 GHz
- Fusion Bonding Thermoplastics vs Low Temperature Bonding with Thermosets
- Fabricating multilayers with PTFE and thermoplastic films
- Quick Word on Hybrid Multilayers…
- Thermal Reliability of thermoplastics vs thermosets
- Copper Roughness and effect on Line Widths
- Sequential Lamination
Stripline vs Microstrip

STRIPLINE

(1) Allows densification-multilayer designs
Can combine SMT amplifier and converter
Circuits with embedded couplers, filters, Feed networks, external radiators, and dc
Power/digital control features in reduced size, Streamline structures
(2) Eliminate cross talk between multiple channels, more confined fields
(3) Stripline EM field distribution is more symmetrical offering better control over even/odd mode impedances
(5) Striplines don’t radiate as readily and Exhibit better RF confinement…less Propensity for intercavity oscillation
(6) Broadband; multioctave couplers and filters

MICROSTRIP

(1) Lower cost, cheaper fabricators
(2) Can be tuned, stripline can’t
(3) In Microstrip one worries that the grounds are properly brought to the ground layer
(4) Microstrip doesn’t have concerns of prepreg variation, easier to fabricate

STRIPLINE WITH MICROSTRIP

(1) Combining the benefits of both approaches
(2) Power amplifier can be put on surface in microstrip with capacitors, transistors, resistors ect,
Automotive Radar (Adaptive Cruise Control @77 GHz)

Stripline - you might be combining many radiating elements with multiple feed elements. Radiating and receiving at high frequency where you need the lowest loss feed to the radiators (suspended striplines also common for 24-26GHz...air bag deployment).
Edge Coupled vs Broadside

(1) Coupling driven by core thickness tolerance in typical RF app.
(2) Puts burden of registration from top to bottom layer on core for simple RF pwbs
(3) For many layer digital apps the S distance will have to be controlled by both cores and prepregs….need very tight fabrication
(4) Uses more PWB real estate
(5) More asymmetrical – signal via drives to deeper depth on one signal layer.
Via Design
Optimized Vias vs Non Optimized Vias

(Smooth transition through via should not cause S21 rolloff)

An optimized via should show no roll off of S21 with frequency and no impedance spikes by TDR.
RF Via Measurement Data vs Simulation
10 mil Misregistration
- Return Loss -

Provided by Anaren Microwave
Via Design for Semiconductor Test
Verigy (former Agilent) Optimized Via – Heidi Barnes

Variables:
1. Number of ground vias (4 vs 6?)
2. Size of pads and anti pads
3. Distance of pad to antipads on grounds
4. Thru via vs back drilled via vs blind/buried via
Verigy Optimized Via

Non optimized

Optimized

Measured by Heidi Barnes at Verigy
Dimensional Stability
Registration
RF Properties
Poor Registration Around Pads
Factors Leading to Poor Registration

1. PWB Thickness and drill deflection
2. Dimensional stability of core
3. Dimensional stability of core at lamination temperature
4. Dimensional stability/melting of prepreg during drilling

Top side of pwb
Drill wander on reverse side of pwb
HFSS Simulation of 50 Ohm Microstrip to Stripline Via Transition

- Taconic TSM-30 dielectric, each of two sections is 0.015” in height
- 1 oz Cu
- Microstrip linewidth is 0.036”
- Stripline linewidth is 0.0165”
- Via diameter is 0.016”
- Pad diameter is 0.036”
HFSS Simulation of Microstrip to Stripline 50 Ohm Line Input

Return Loss

Curve Info
- dB(S(WavePort1,WavePort1))
  - Setup4 : Sweep1
    Move_X='0mil' Move_Y='16mil'

- dB(S(WavePort1,WavePort1))
  - Setup4 : Sweep1
    Move_X='0mil' Move_Y='0mil'

- dB(S(WavePort1,WavePort1))
  - Setup4 : Sweep1
    Move_X='16mil' Move_Y='0mil'

Courtesy of L3 Narda
Ensuring Via to Pad Registration
Dimensional Stability Optimization of Copper Clad Laminate Core

Machine direction (pph)

After etch =1, after bake=2, after thermal stress=3
Dimensional Changes in Glass Reinforced TLY vs Non Reinforced Laminate

**Dimensional changes in Warp direction**
- Non reinforced laminate
- Glass reinforced TLY

**Dimensional changes in Fill direction**
- Non reinforced laminate
- Glass Reinforced TLY
Ceramic filled PTFE/fastRise27 low temperature thermoset lamination

Almost no fiberglass reinforcement

Good layer to layer registration, no pad distortion
Registration consistency of Dimensionally Stable Core

The key is layer to layer consistency

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<td></td>
<td>1.00021</td>
<td>1.00029</td>
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Values are mils/inch
Prepreg Thickness Variation
Prepreg Dielectric Thickness Variation

Dielectric Thickness spacing of prepreg will vary with artwork – the amount of copper etched, the thickness of the copper etc.
Prepreg Filling Difficult Circuitry

2 oz traces

3 oz traces

One ply fastRise27 prepreg

2 plies fastRise27 prepreg

Lamination pressure and stacking of artwork affect flow and final prepreg thickness.
Variations in Dielectric Thickness

There can be variations in dielectric constant – pure resin or voids?
Predicting Dielectric Thickness of Pressed Prepregs

<table>
<thead>
<tr>
<th>Material</th>
<th>Pressed Thickness (mil)</th>
<th>Pressed Thickness (mil)</th>
<th>Pressed Thickness (mil)</th>
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<tr>
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<td>2.13</td>
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<td>FR270040-25</td>
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<td>5.8</td>
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<td>FR27-0050-40</td>
<td>6.1</td>
<td>5.5</td>
<td>4.85</td>
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With stripline structures there is a balancing act between:
(1) Do I have enough flow to fill all the artwork without voids?
(2) Do I have excessive flow where resin flows into a cavity?
(3) Can I accurately product the z axis distances for impedance and how reproducible will they be?
Strategy for Simple RF Multilayers

Core – copper etched off one side

Thin prepreg

Core – signal etched one side

Strategy allows you to minimize prepreg thickness and overall variation of dielectric thickness on impedance – not practical for high layer count multilayers
# Dielectric Materials for Multilayer Stripline Applications

<table>
<thead>
<tr>
<th>MATERIAL</th>
<th>$\varepsilon_r$ (10 GHz)</th>
<th>DF (10 GHz)</th>
<th>DF (40 GHz)</th>
<th>Fiberglass (wt%)</th>
<th>Construction</th>
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<tbody>
<tr>
<td>FR4, prepreg/core</td>
<td>4.4</td>
<td>0.025</td>
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<td>35-75</td>
<td>epoxy, E fiberglass</td>
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<td>Nelco 4000-13EP SI</td>
<td>3.13-3.28</td>
<td>0.008</td>
<td></td>
<td>55-75</td>
<td>epoxy, CE, NE glass Nittobo</td>
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<td>Rogers 4403, prepreg</td>
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<td></td>
<td></td>
<td></td>
<td>butadiene rubber, silica, E glass</td>
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<td>Rogers 4450B, prepreg</td>
<td>3.54</td>
<td>0.004</td>
<td>~25-35</td>
<td></td>
<td>Expanded PTFE/ silica, epoxy</td>
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<tr>
<td>Speedboard C</td>
<td>2.6</td>
<td>0.004</td>
<td>0.0064 X</td>
<td>0</td>
<td>polychlorotrifluoroethylene (HT1.5 Bondfilm, RO3001, Arlon 6700)</td>
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<tr>
<td>PCTFE thermoplastic</td>
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<td>0.0035</td>
<td>0.0057 X</td>
<td>0</td>
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<tr>
<td>Taconic fastRise27</td>
<td>2.7</td>
<td>0.0014</td>
<td>0.0017 X, Y</td>
<td>0</td>
<td>silica (≥50%), thermoset, pTFE</td>
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<td>Taconic TSM29, core</td>
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<td>9</td>
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<td>0</td>
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<tr>
<td>Taconic TLY-5 RO5880</td>
<td>2.8</td>
<td>0.009</td>
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<td></td>
<td>PTFE / E glass</td>
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## Design Considerations

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<tr>
<th>Material</th>
<th>DK</th>
<th>DF (10 GHz)</th>
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<tbody>
<tr>
<td>E Fiberglass</td>
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<td>NE Glass Nittobo</td>
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<td>Epoxy</td>
<td>3.2 - 3.8</td>
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<td>Butadiene Rubber</td>
<td>2.3</td>
<td>0.004</td>
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<tr>
<td>Silica</td>
<td>3.2</td>
<td>0.0028</td>
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<tr>
<td>PTFE</td>
<td>2.1</td>
<td>0.0006</td>
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mmWave Loss Tangents for Various Multilayer Bonding Films
Glass Reinforced vs non glass reinforced mmWave Properties

![Graphs showing mmWave properties](image)

**Resonant Split Cavity DK Data**

- Dielectric Constant (dK)
  - Frequency (GHz)
  - Data points for different thicknesses:
    - Fastrise t = 32mils
    - Fastrise t = 17mils
    - TSM30 t = 30mils
    - TSM30 t = 10mils

**Resonant Split Cavity DF Data**

- Loss Tangent (dF)
  - Frequency (GHz)
  - Data points for different thicknesses:
    - Fastrise t = 32mils
    - Fastrise t = 17mils
    - TSM30 t = 30mils
    - TSM30 t = 10mils

**TSM mmWave Performance (Damaskos)**

- Frequency (GHz)
  - Linear (In-Plane X)
  - Linear (In-Plane Y)

**fast Rise27 (Damaskos)**

- Frequency (GHz)
  - Linear (In-Plane X)
  - Linear (In-Plane Y)
Fiberglass Reinforced Laminate at mmWave
Experimental Insertion Loss Results
(provided by Verigy)
Impedance Fluctuations with Fiber Glass Weave

Figure 1. 1080 Glass Cloth with 3.5 Mil Wire

Figure 3.3313 Glass Cloth with 3.5 Mil Wire

Figure 2. Impedance vs. Length Over 1080 Glass

Figure 4. Impedance vs. Length Over 3313 Glass

(With permission of Lee W. Ritchey – Speeding Edge)
Fusion Bonding (295-400°C)

Fusion Bonding – the multilayer thermoplastic lamination of pure PTFE or ceramic filled PTFE composites with no prepregs (no thermosets)

NEGATIVES:
(1) 10-12 Hour press cycle – high cost
Other options 3-4 hour press cycle
(2) Limited fabricator base – high cost
(3) High temperatures and pressures cause circuitry to float
(4) High viscosity of PTFE not ideal for encapsulating copper
(5) FEP bonding prone to melting during drilling, thermal reliability problems
(6) High loadings of PTFE → drill smear

POSITIVES
(1) Loss tangents of 0.009-0.0014 can be obtained
(2) Homogeneous stackup
Example – 6dk core with 6dk unclad
(3) Low moisture absorption, high Temperature stability of pure PTFE
(4) Capable out to very high frequency
Fiberglass Reinforced PTFE Laminate Thermal Expansion

Rapid Acceleration Of Z axis expansion

Fusion Bonding
Fusion Bonded Multilayer

Fusion bonding may cause change in dielectric thickness, dielectric constant, and build in residual stress.
Fusion Bonded Multilayer
FEP fusion bonded Multilayer

Pad distortion during high temperature lamination and Remelting of the FEP film during drilling can lead to Pad/post reliability questions
Ceramic filled PTFE/fastRise27
(215°C Lamination)

Low temperature lamination – no pad/post distortion
Ceramic filled PTFE/Speedboard C
(215°C Lamination)

Low temperature lamination – no pad/post distortion
Fabricating with High PTFE Content Laminates and Thermoplastic Films (little or no ceramic….not advised)
Drilling / Plating Defects (FEP Bonded multilayer)

Does the melting of the thermoplastic film cause all these drilling defects.....serious problem for long term reliability.
Problems with High Resin Content PTFE and Thermoplastic Films (RO5880, TLY5 etc)

- PTFE (gel = 325°C), FEP (mp = 255°C), and PCTFE (mp = 215°C)…melt during drilling
- Melting or softening causes smearing of thermoplastic across posts
- Plating chemistry does not get a 3 point connection to pad, worst case an open
Taconic fastRise27-TSM29/epoxy hybrid

“balance the construction“

A balanced construction with a low glass content will lie flat and conform to the higher modulus.
Unbalanced Hybrid subassemblies or pwbs may warp, crack, bow, twist, and delaminate

Unbalanced construction leading to stress induced delamination
Temperature of Decomposition
Various thermoset Prepregs vs PTFE Benchmark

- TPG30
  - $T_d$ (2% = 288ºC)
  - $T_d$ (5% = 366ºC)

- FastRise27
  - $T_d$ (2% = 377ºC)
  - $T_d$ (5% = 421ºC)

- Speedboard C
  - $T_d$ (2% = 125)
  - $T_d$ (5% = 236)

- Pure PTFE fiberglass Laminate TLX-9
Effect of Thermal Aging on Dielectric Constant (PTFE vs RO4003 series rubber)

Effect of Thermal Aging on \( D_k \) at 195°C

- RF-34 Mode 1
- RF-34 Mode 3
- RF-34 Mode 5
- RO-4003 Mode 1
- RO-4003 Mode 3
- RO-4003 Mode 5

Time (Days)

Dielectric Constant

0 2 4 6 8 10 12 14 16
Effect of Thermal Aging on Dissipation Factor (PTFE vs RO4003 series rubber)

Effect of Thermal Aging on $D_f$ at 195C

![Graph showing the effect of thermal aging on dissipation factor $D_f$ at 195C for different modes and materials.]
Z axis Expansion and Reliability
(stdandard ED copper expands 3.5%)

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<th>Z AXIS EXPANSION (PPM)</th>
<th>(25 to 288°C)</th>
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<th>20</th>
<th>30</th>
<th>60</th>
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<td></td>
<td>(%)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td>TLY</td>
<td></td>
<td></td>
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<td>0.05</td>
<td>0.11</td>
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<td></td>
<td>(%)</td>
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<td>0.08</td>
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TLY does well in a lot of thin multilayer applications
Z axis expansion is not the whole story!!!!
How does Modulus affect the stress on solder joints? Young’s modulus is directly related to stress.
Thermoset vs Thermoplastic Z Axis Expansion

Thermoset Tg (glass transition)

PTFE Thermoplastic ceramic filled
Copper Line Width Variations

Inconsistent etching can lead to varying trace width, varying distances between trace widths, copper nuggets left behind in laminate (shadow copper) that can attract other plating chemistries (shadow ENIG)…

……real problem for fine lines and spaces
Copper Roughness Considerations

Skin depth

TL32 With Various Copper (16 mil DT)

TLS116
TLCO16
TLH116
TLSH16
TLHH16

Skin depth graph:

<table>
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<th>GHz</th>
<th>dB/in</th>
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<td>0.01</td>
<td>-1.2</td>
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<td>0.1</td>
<td>-1</td>
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<tr>
<td>1</td>
<td>-0.8</td>
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<tr>
<td>10</td>
<td>-0.6</td>
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<tr>
<td>100</td>
<td>-0.4</td>
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Graph showing dB/in vs GHz for different copper types.

Table:

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<th>Treatment Density</th>
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<td>2 – 4μ</td>
<td>1500x all in 35μ</td>
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<tr>
<td>LP4</td>
<td>4 – 5μ</td>
<td>2000x</td>
</tr>
<tr>
<td>TW</td>
<td>7 – 9μ</td>
<td>2000x</td>
</tr>
<tr>
<td>TWS</td>
<td>9 – 11μ</td>
<td>2000x</td>
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Roughness Profile in cross section (2000x)
Sequential Laminations Enable Buried Vias and Elimination of Stubs

- Thermal reliability of prepregs necessary for multiple Lamination cycles, high temp 260C lead free reflow temperatures and multiple rework cycles
- Buried and blind vias with no stubs offer smoothest via transitions

(IPC Technology Roadmap 2000-2001)
Many Variables Affect Stripline RF Performance and Reliability

- Via Design and Registration to pads critical to performance
- Low temperature lamination an advantage to maintaining dimensional control, reducing stress in finished pwbs and reducing costs
- A lot of hidden factors like copper roughness and smooth etching affect RF performance
- Less obvious factors like low modulus, high drill quality affect reliability
- Final pwb quality will vary significantly with the fabricator
- Many variables not captured on any data sheet