Using Dynamic MOSFET Parameters to Predict DC-DC Converter Performance

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Agenda

- Why traditional switching-loss estimates fall short for RESURF MOSFETs
- Redefining Q_{SW} to reflect measured switching behavior
- Validating loss predictions through device and converter testing
- Application case studies: active-clamp forward and QR flyback

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The Engineering Problem:

A familiar equation can fail when its interval no longer tracks the loss-producing transition.

- Switching energy is fundamentally the overlap integral:

(1) $$E_{SW} = \int_a^b v_{DS}(t)\, i_{DS}(t)\, dt$$

- The common shortcut:

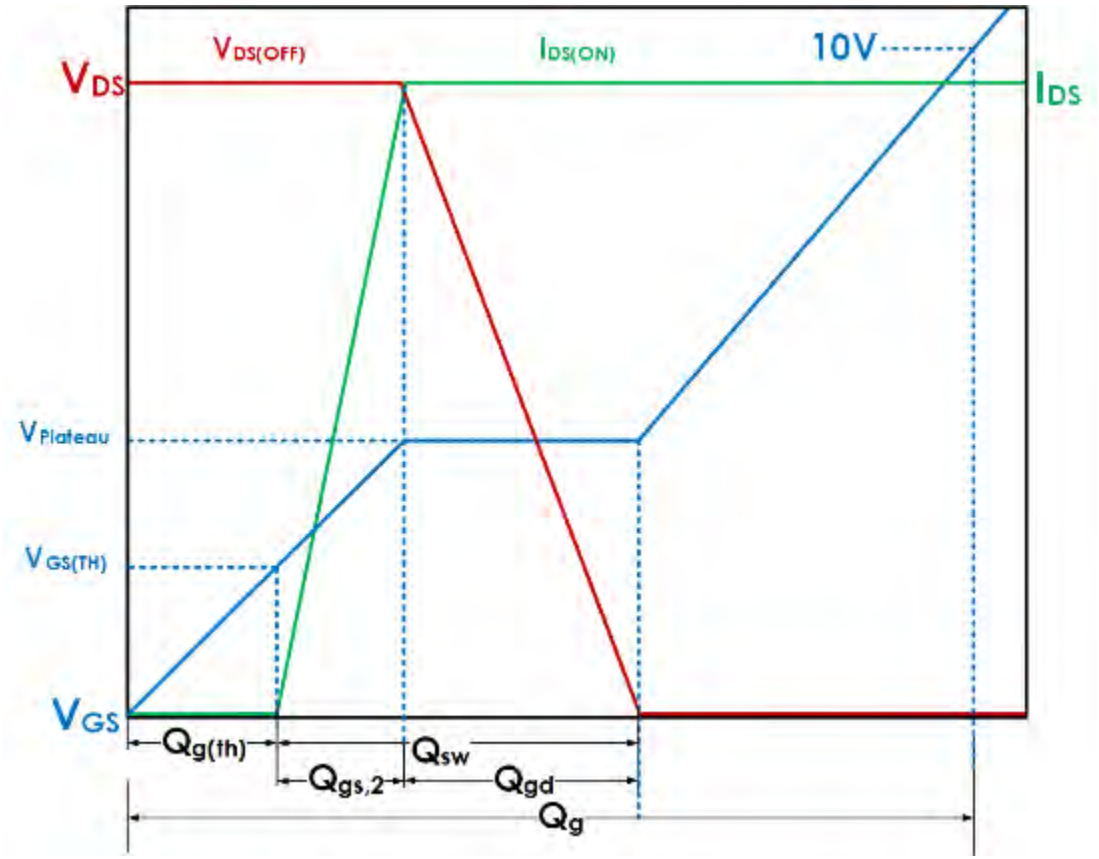
(2) $$P_{SW} = \frac{1}{2} V_{DS(OFF)} * I_{DS} * f_{SW} * \frac{Q_{SW}}{I_g}$$

- The shortcut assumes a near-triangular $V_{DS} \times I_{DS}$ overlap.
- It assumes Q_{SW} spans the physically relevant switching interval.
- For RESURF devices, nonlinear capacitance changes the waveform shape.
- Result: a mathematically correct expression fed by a physically mismatched interval.

The Question: **Where should Q_{SW} begin and end?**

Traditional Q_{SW}: Why the shortcut worked

- For a non-RESURF device, the conventional gate-charge segmentation approximates triangular overlap.

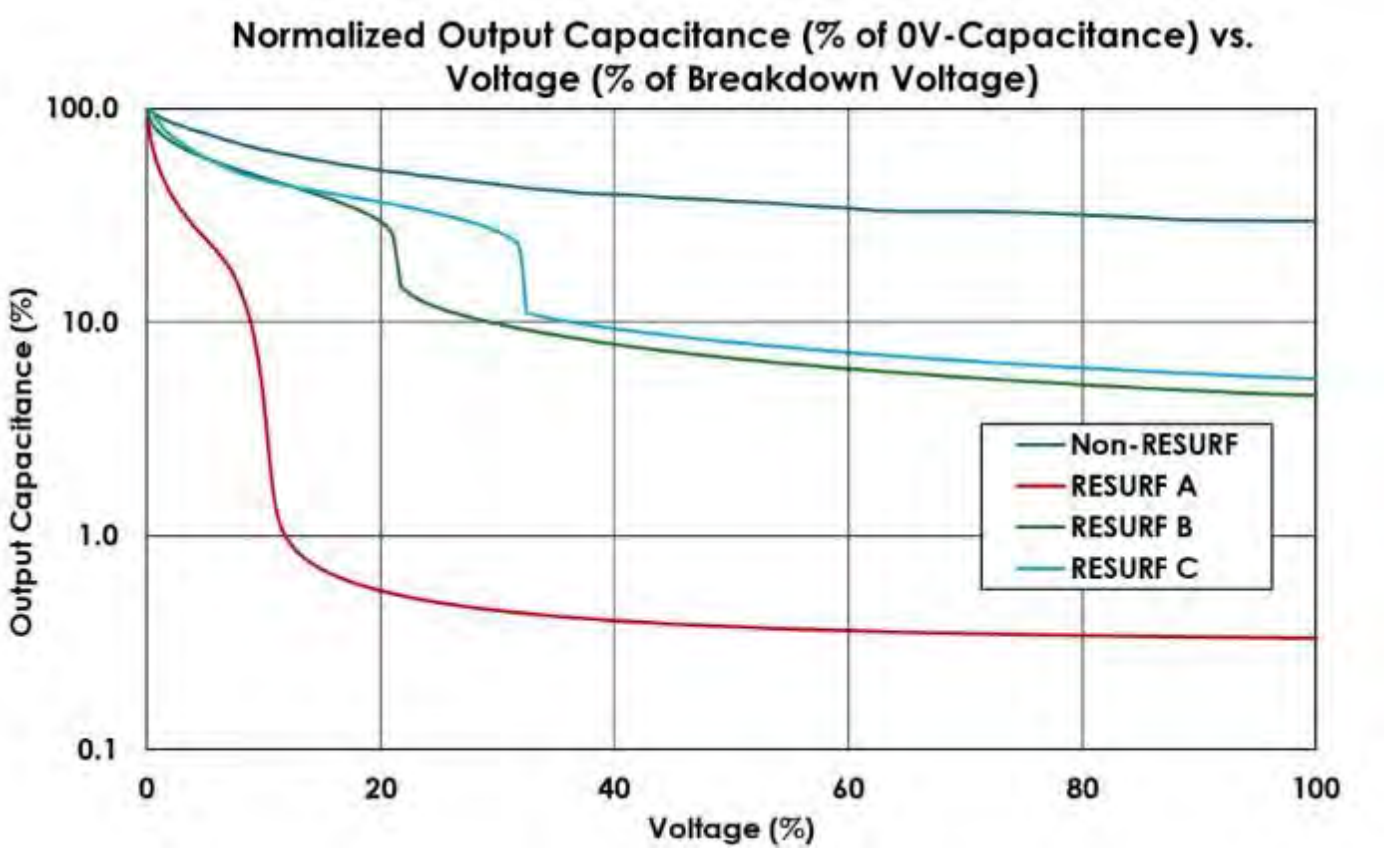


Traditional interval

- Begins near threshold charge $Q_{G(th)}$.
- Extends through the end of the Miller plateau.
- Treats V_{DS} and I_{DS} transitions as approximately linear.

What Changed: C_{OSS} became more nonlinear

- RESURF and charge-balance structures alter the timing and shape of the drain-voltage transition.



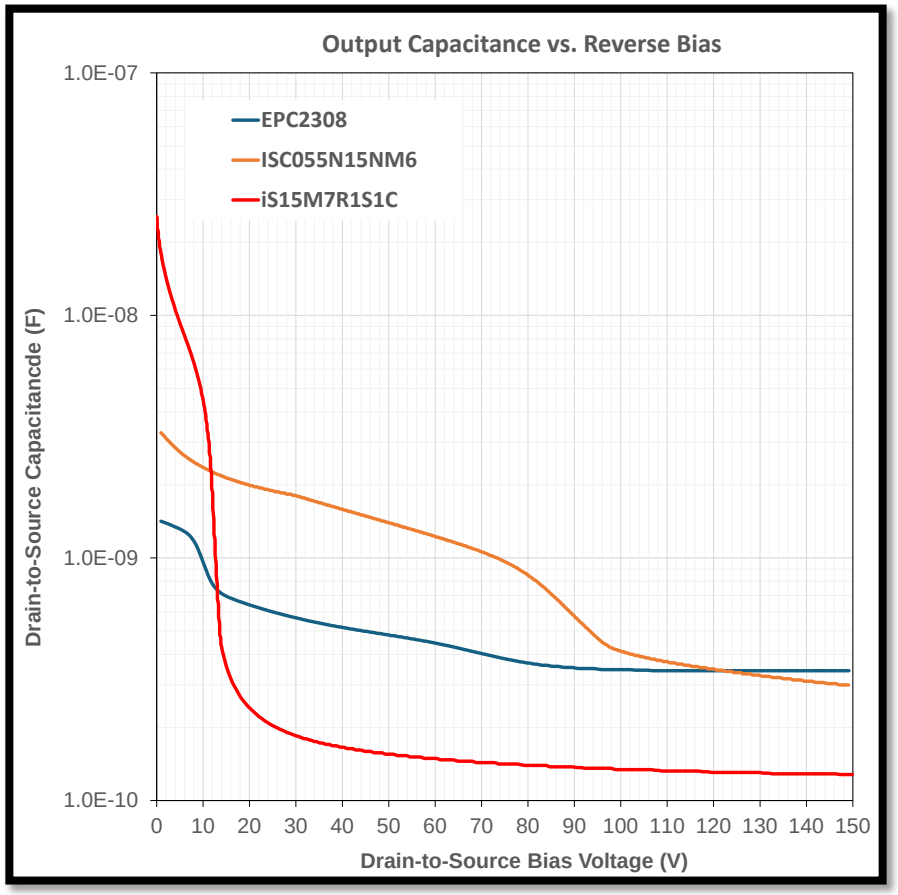
Consequence

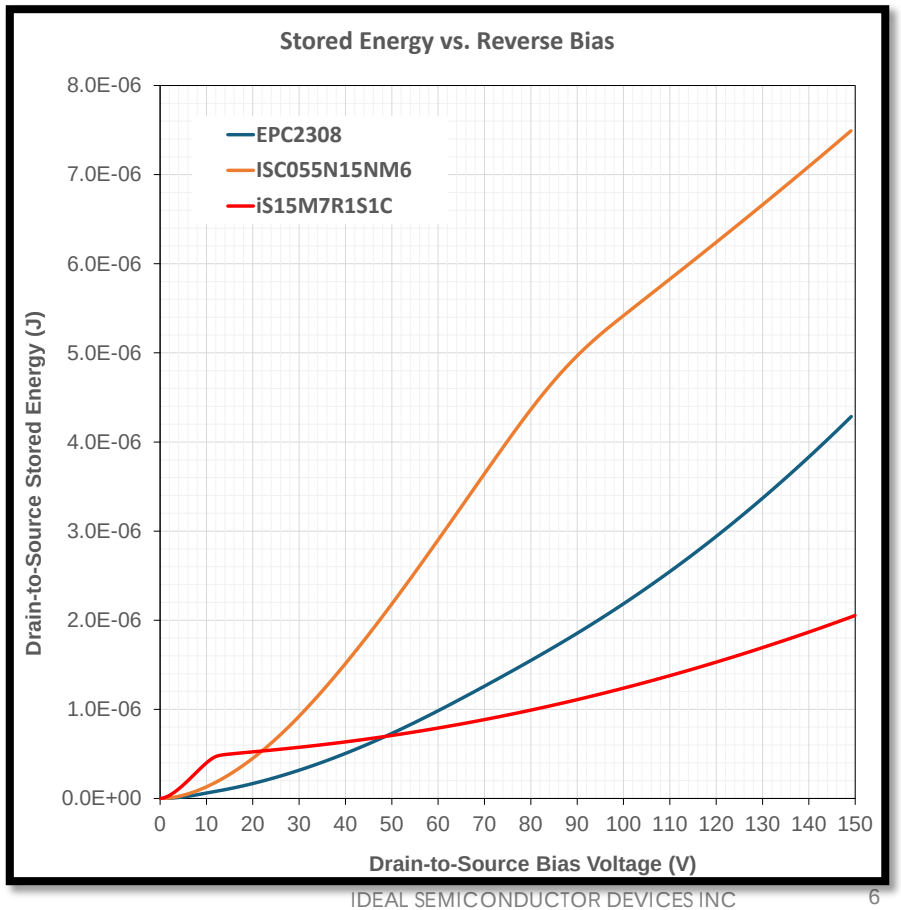
- The same incremental gate charge does not produce a linear V_{DS} transition.
- The major $V_{DS} \times I_{DS}$ overlap can collapse into a smaller portion of the Miller-region charge.
- Q_{SW} becomes sensitive to boundary convention, not only device performance.
- You can no longer assume a near-triangular transition of MOSFET drain voltage and current

A datasheet value can look larger without implying proportionally larger measured switching energy.

What Changed: E_{OSS} became more nonlinear

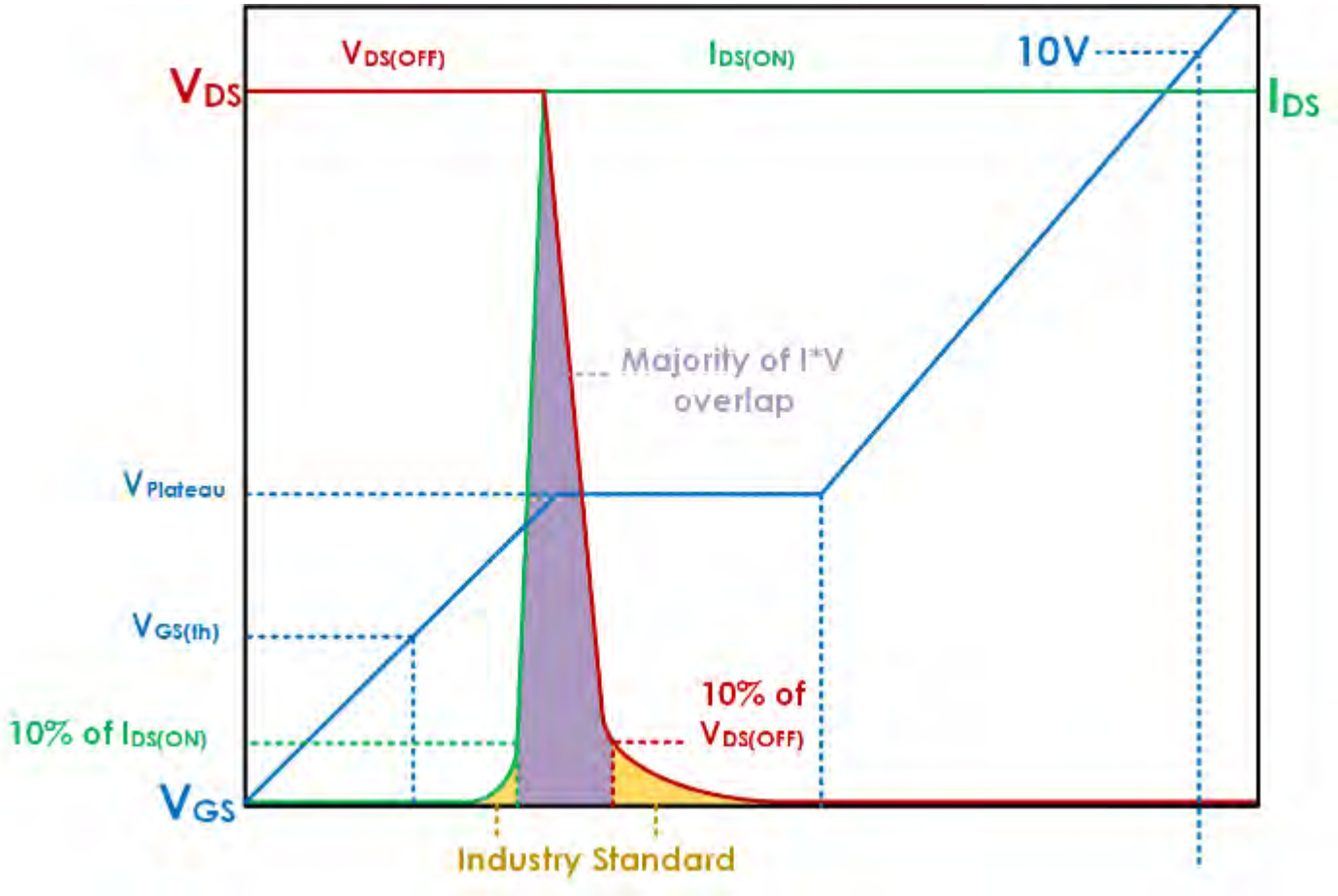
- All MOSFET E_{OSS} will increase with drain voltage
- RESURF MOSFETs' C_{OSS} curves have very low stored energy
- RESURF MOSFETs have a slower rate of increase in E_{OSS} versus drain voltage





Measured RESURF behavior breaks the triangular-overlap assumption

- Most of the energy-producing overlap occurs in a compact subinterval.

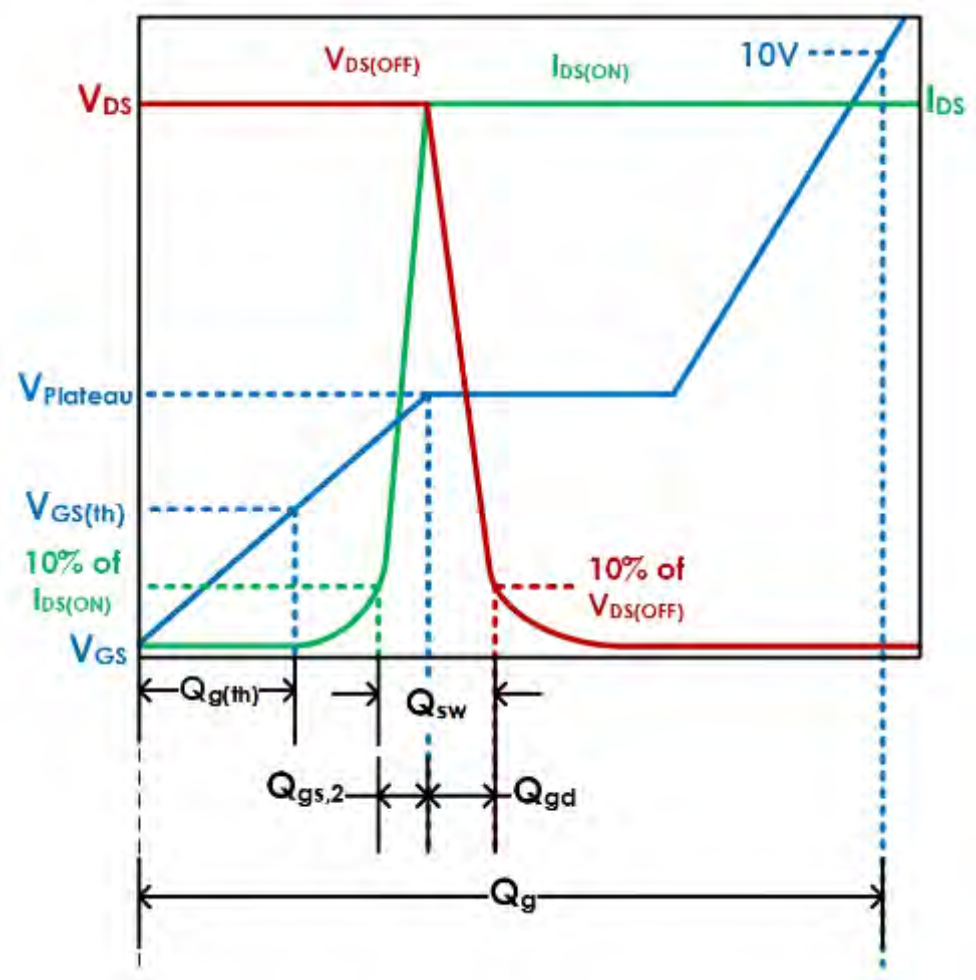


Measured observation

- **>82%** of I x V overlap falls within a small portion of the traditional Q_{SW} interval.
- The remaining area contributes only 18% of the total overlap.
- Including this area leads to **>300%** in estimating RESURF switching loss using Equation 2.

Proposed Redefinition: Use waveform percent points

- Define Q_{SW} by the observed I_{DS} rise and V_{DS} fall, not by legacy curve landmarks alone.



New Q_{SW} Boundaries

Start: I_{DS} = 10% of $I_{DS(ON)}$

End: V_{DS} = 10% of $V_{DS(OFF)}$

Also move the Q_{GD} right boundary to the V_{DS} 10% point.

These "percent-point" boundaries are a standard method of measurement for a variety of MOSFET parameters such as in measurements of switching time.

Assessing Datasheet Switch Parameters

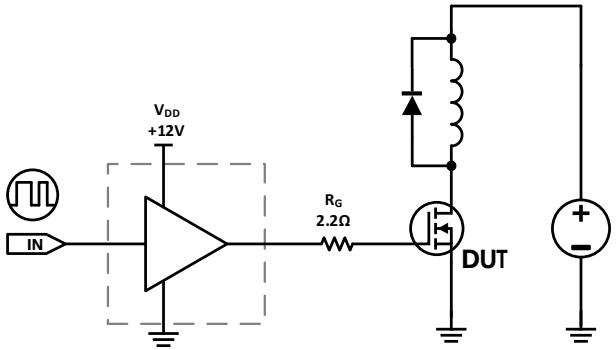
- The Time and energy-related parameters are only valid for a fixed set of gate drive conditions
  - External non-MOSFET-related items like Gate Voltage, Gate Resistor, and Gate Driver IC will significantly vary switching energy (E_{SW}) and, conversely, switching losses (P_{SW})
- The P_{SW} loss equation using Q_{SW} charge eliminates this external component dependency
  - Allows the user to predict switching loss based on their exact application requirements.
  - MOSFET Gate current (Ig) can be estimated by looking at the Gate Resistor differential voltage during the MOSFET Gate, Miller Plateau voltage.

Typical MOSFET Datasheet Switching Information
Note **fixed** test conditions in yellow box below

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Effective output capacitance, time related [10]	$C_{o(tr)}$	-	256	-	pF	I_D = constant, V_{GS} = 0 V, V_{DS} = 0…500 V
Turn-on delay time	$t_{d(on)}$	-	11	-	ns	V_{DD} = 500 V, V_{GS} = 0/18 V, I_D = 44.7 A, $R_{G(ext)}$ = 1.8 Ω, L_{stray} = 15 nH; see table 10
Rise time	t_r		10		ns	
Turn-off delay time	$t_{d(off)}$		22		ns	
Fall time	t_f		7		ns	
Turn-ON switching losses [11]	E_{on}		70		µJ	
Turn-OFF switching losses [11]	E_{off}		44		µJ	
Total switching losses [11]	E_{tot}		114		µJ	

Qsw P_{SW} Equation

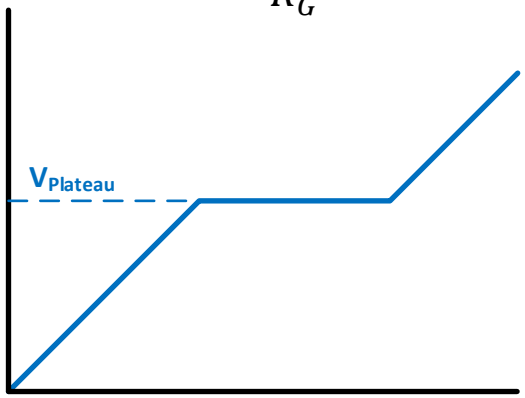
$$P_{SW} = V_{DS} * I_{DS} * f_{SW} * \frac{Q_{SW}}{I_g}$$



Typical Gate Drive

Estimate I_g Equation

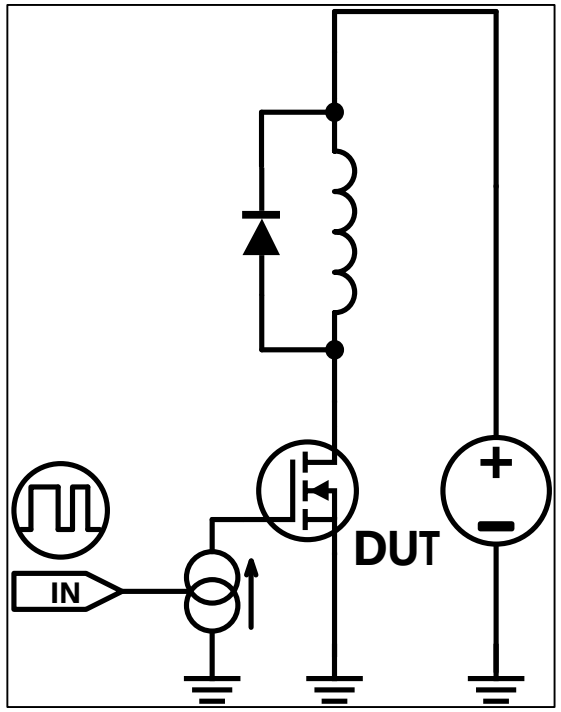
$$I_g = \frac{V_{DRV} - V_{Plateau}}{R_G}$$



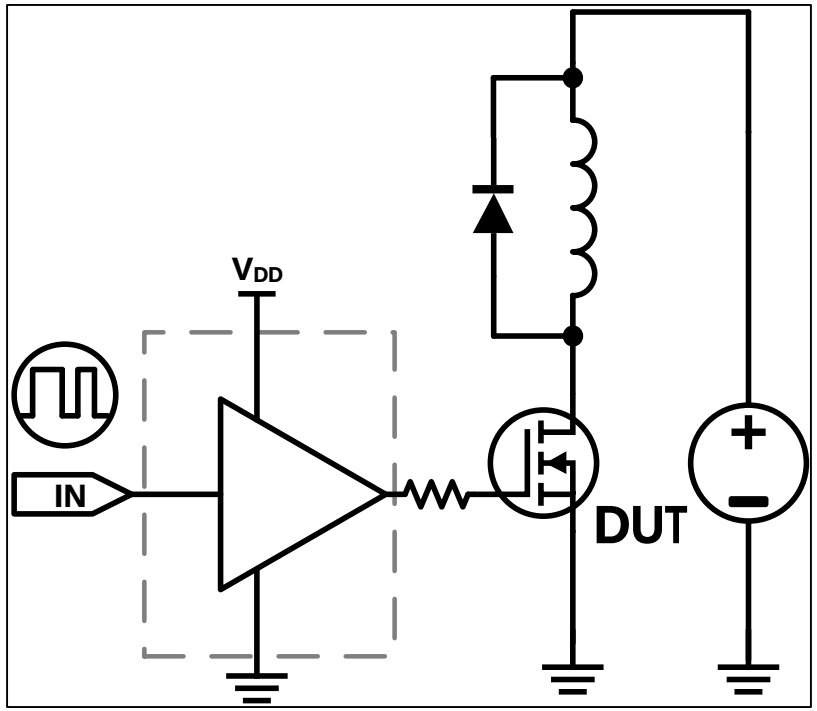
Typical Gate Charge Curve

Validating the Proposal: Datasheet Level and Application Level

- Measure Q_{SW} during Q_G measurement and verify against application-level data.



Gate Charge Characterization



Application-Level Hard Switching Test

Verifying Q_{SW} redefinition

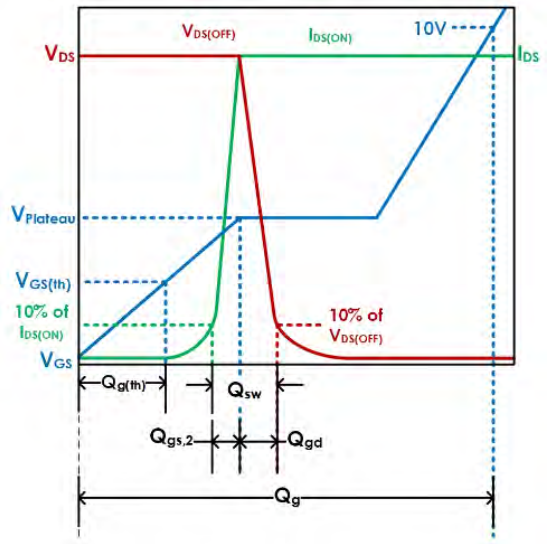
Q_G characterization: Switching test with constant-current drive.

Using the obtained Q_{SW} values, estimate losses and compare to the switching loss in:

Application-level test: Double-pulse test with constant-voltage drive

150V MOSFET Q_{SW} Analysis: Datasheet vs. Measured

- Three 150V MOSFETs were selected based on typical $R_{DS(on)}$
  - By normalizing the $R_{DS(on)}$, we can have a fair comparison of Q_{SW} and E_{OSS} losses.
- All three MOSFETs were tested and measured for Q_{SW} using industry-standard gate charge tester
- Measured data shows a >30% error in Q_{SW} over datasheet values.
  - Q_{SW} measured based on 10% points of drain voltage and current



Datasheet Comparison

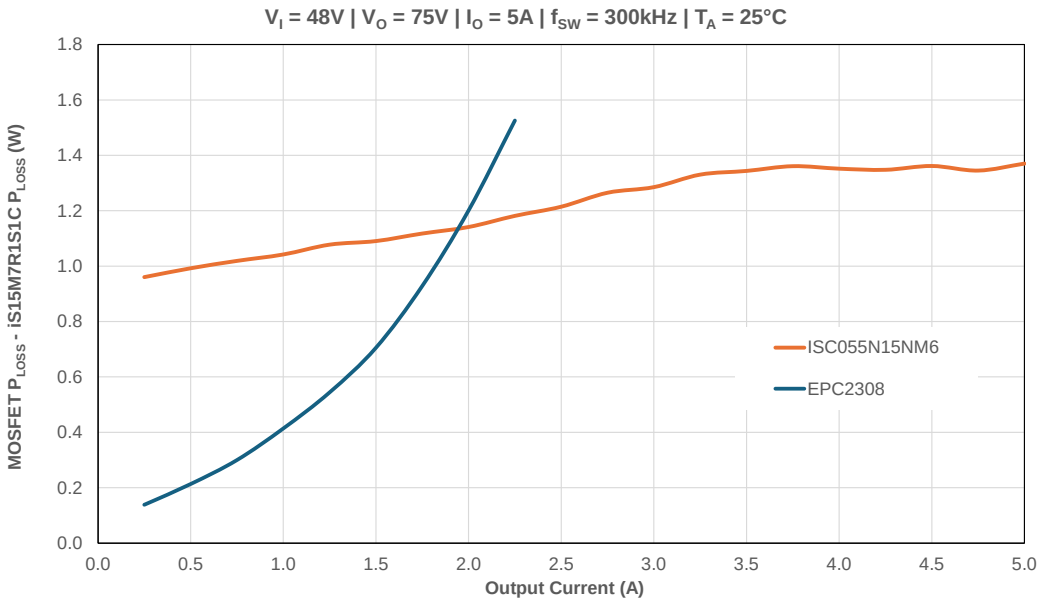
MOSFET Spec	EPC2308	ISC055N15NM6	iS15M7R1S1C
BVdss (V)	150	150	150
Vgs_Max (V)	6	20	20
Vth_typ (V)	1.2	3.5	3.3
Rg_typ (Ω)	0.4	0.74	1.1
Rdson_typ (mΩ)	4.5 @ 5Vgs	4.5 @ 15Vgs	4.9 @ 15Vgs
Qg_typ (nC)	11.7	43	48
Qsw_typ (nC)	3.1	15.9	4.9
Qoss_110V (nC)	60	150	130
Eoss_110V (µJ)	2.55	5.83	1.38

Q_{SW} Review

MOSFET Spec	EPC2308	ISC055N15NM6	iS15M7R1S1C
Datasheet Q_{SW}_typ (nC)	3.1	15.9	4.9
Measured Q_{SW}_typ (nC)	2.1	10.4	4.6
Percent Error (%)	32.3%	34.6%	6.1%

Application Testing on a Boost Converter

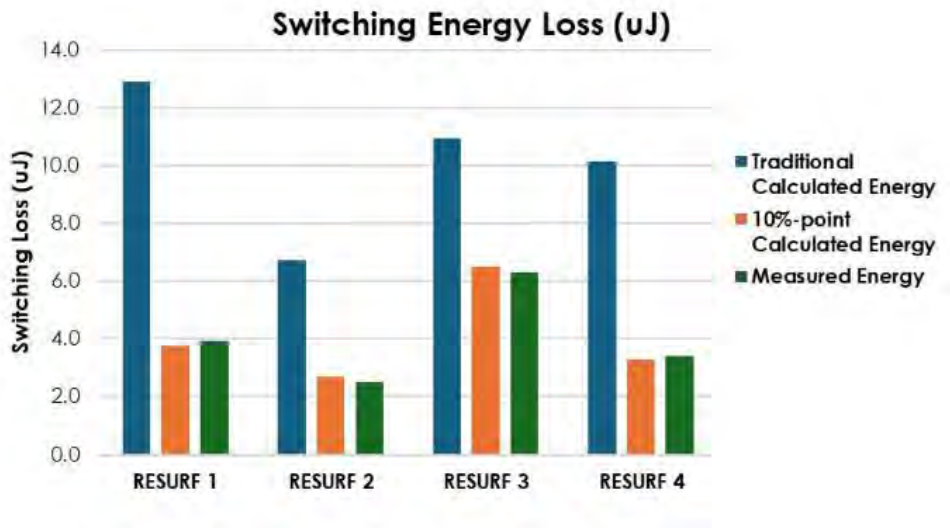
- 375W Boost Converter running at 300kHz and 75V_{OUT}
  - Rectifier is a SiC Schottky to minimize reverse recovery influence
- Gate drive voltage was adjusted to maintain equivalent $R_{DS(on)}$ across all MOSFETs
- Consideration of technology/product differences
  - Gate drive voltage: 5V_{GS} vs 12V_{GS}
  - Standard PDFN packaging vs. low inductance custom package
- Optimization based on V_{GS} ABS MAX requirements (6V_{GS} vs 20V_{GS} max)



Delta LOSS - Measured Difference
MOSFET Power Loss – iDEAL Power Loss
EPC2308 and ISC055N15NM6 are higher in P_{LOSS}

Key Learnings so Far

- Modern RESURF C_{OSS} vs V_{DS} curves invalidate the assumed triangular overlap
- Q_{SW} should be bounded by 10% $I_{DS(ON)}$ and 10% $V_{DS(OFF)}$
- The application test improves from >3x overprediction to <7% error
- With this proposed change, Q_{GD} would also be changed to better reflect the nonlinear behavior of Superjunction devices
- The case studies on the following slides illustrate the impact of switching charge, stored energy, and capacitance-curve shape of SuperQ's modern RESURF technology on application performance.



Traditional Q_{SW}

>3×

the measured switching loss

Percent-point Q_{SW}

<7% error

versus measured energy

SuperQ: Device Behavior in Two Case Studies

TWO CASE STUDIES



In **active-clamp forward**: Q_{SW} and E_{OSS} reduction yields 0.8% eff improvement, t_{MAX} down **31°C!**

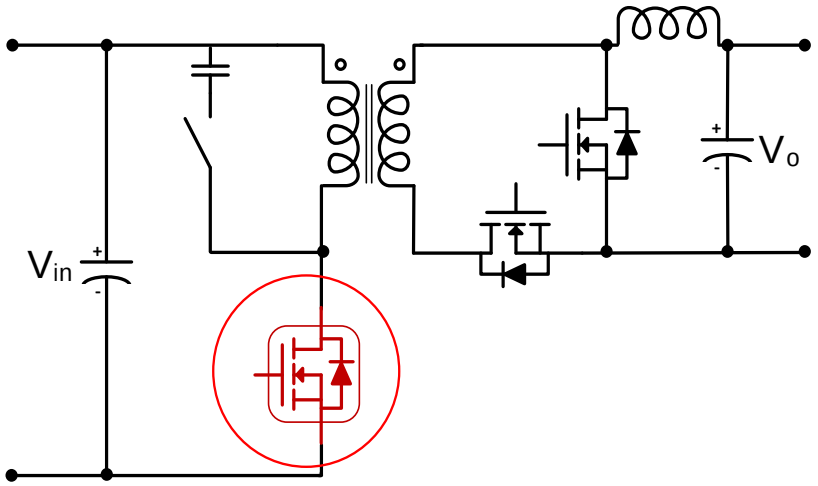


In **QR Flyback**: Capacitance profile reduces temperature in primary GaN HEMT by up to **20°C!**

Case Study 1: 200W Active-Clamp Forward ¼ Brick Design



V_{IN}	18 – 75V
V_{OUT}	12V
I_{OUT}	17A
f_{SW}	270kHz



- Major losses mechanisms in the primary switch:
  - **Conduction**
  - **Switching Charge Q_{SW}**
    - At turn-on in continuous conduction mode (CCM)
    - At turn-off always
  - **Stored energy E_{OSS}**
    - At turn-on in CCM.

	iS15M7R1S1C	ISC055N15NM6
$R_{DS(ON),TYP}$ (mΩ)	**5.5**	5.6
Q_{SW} (nC)	**4.6**	10.7
E_{OSS} (µJ)	**0.75**	2.1

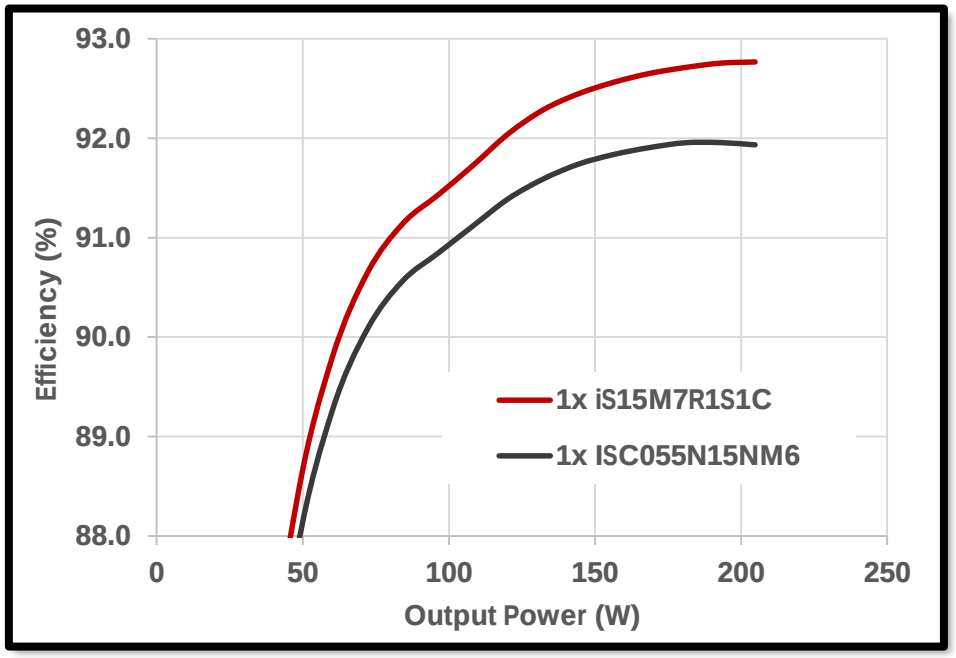
SuperQ RESURF Technology Influences 2 of the 3 most important Loss mechanisms.

Case Study 1: Efficiency Improves Across the Load Range



V_{IN}	18 – 75V
V_{OUT}	12V
I_{OUT}	17A
f_{SW}	270kHz

- At 200W, 0.8% efficiency improvement is ~ 2W less total loss
- Saved loss can be traded for smaller cooling, higher frequency, or lower component stress.



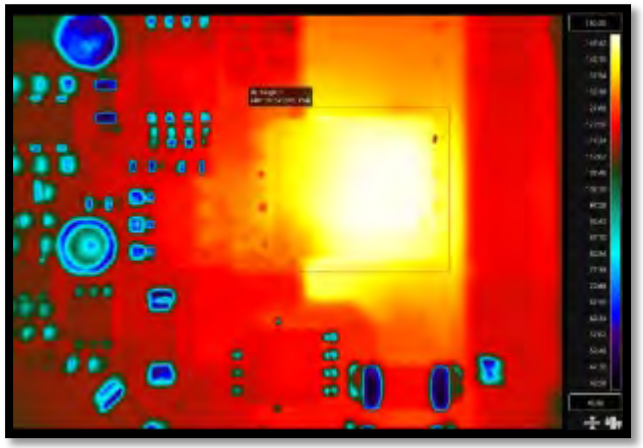
Lower energy (EOSS) and charge-related parameters lead to better efficiency in hard-switched applications.

Case Study 1: 31°C More Margin at the Primary Switch



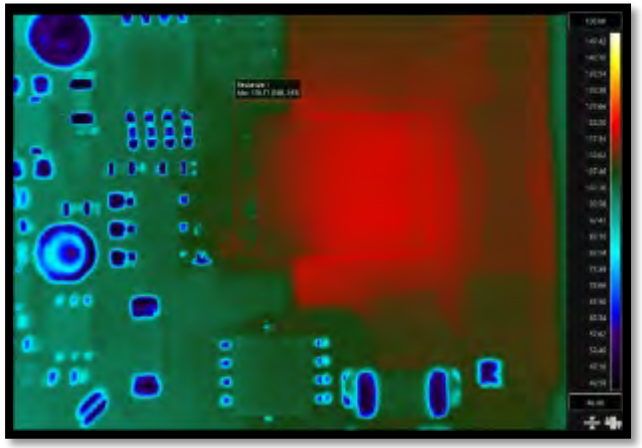
V_{IN}	18 – 75V
V_{OUT}	12V
I_{OUT}	17A
f_{SW}	270kHz

- Lower dynamic loss reduces the primary MOSFET temperature from 151.5°C to 120.5°C
- Increased thermal margin lets you run the converter harder or shrink the heatsinking.



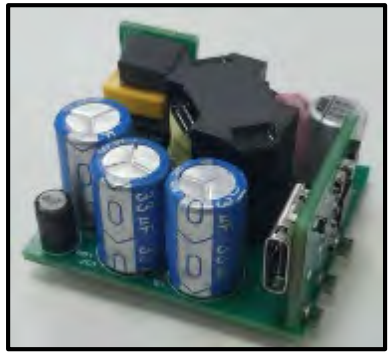
IFX
1x ISC055N15NM6
Primary MOSFET
151.5°C Max

↓ 31°C

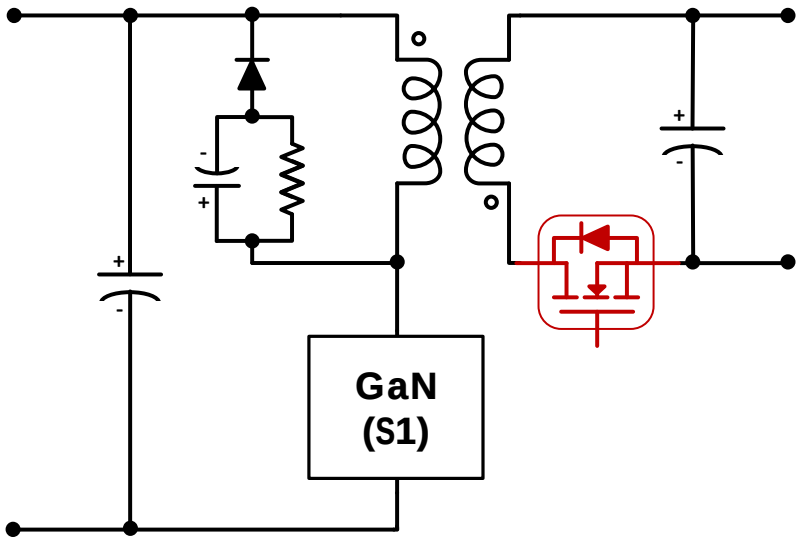


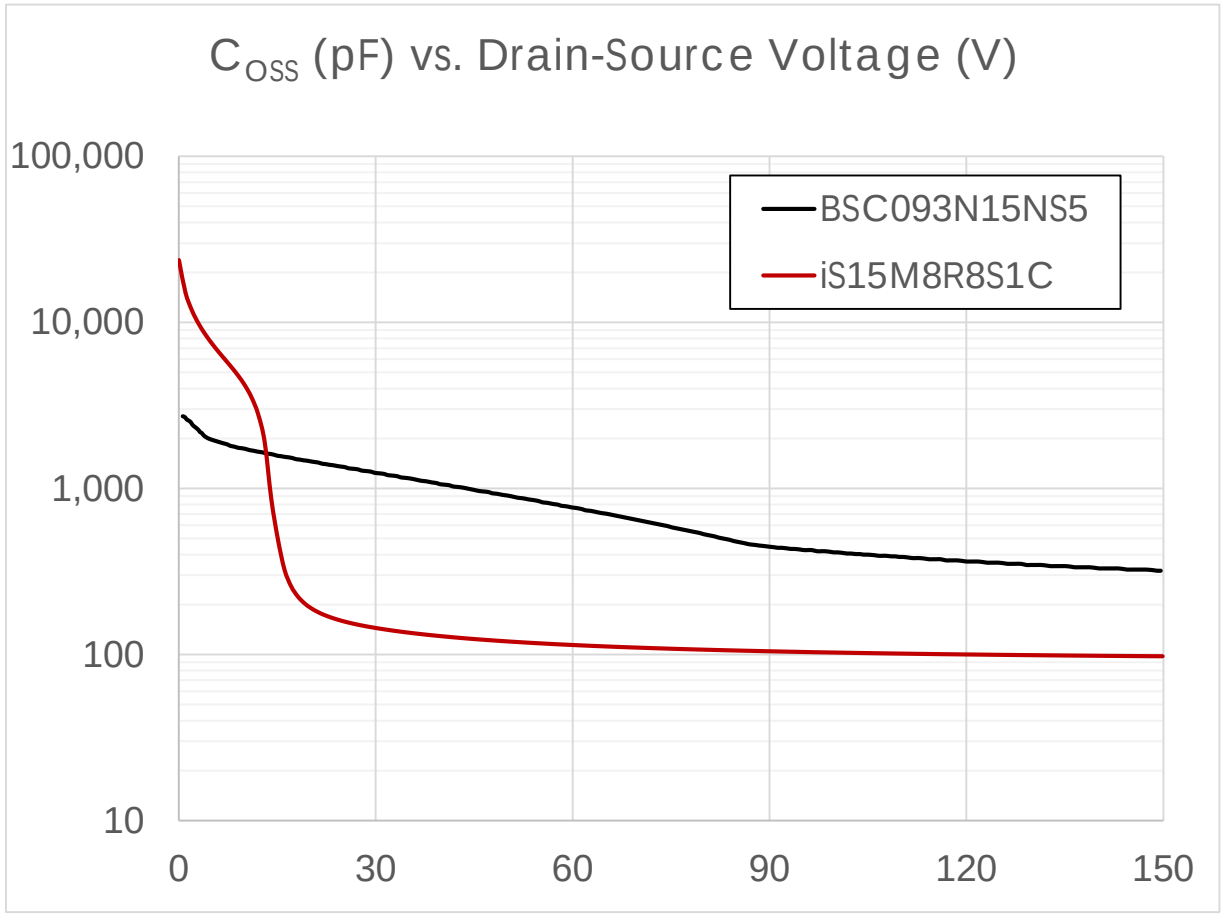
iDEAL
1x iS15M7R1S1C
Primary MOSFET
120.5°C Max

Case Study 2: 65W Quasi-Resonant Flyback



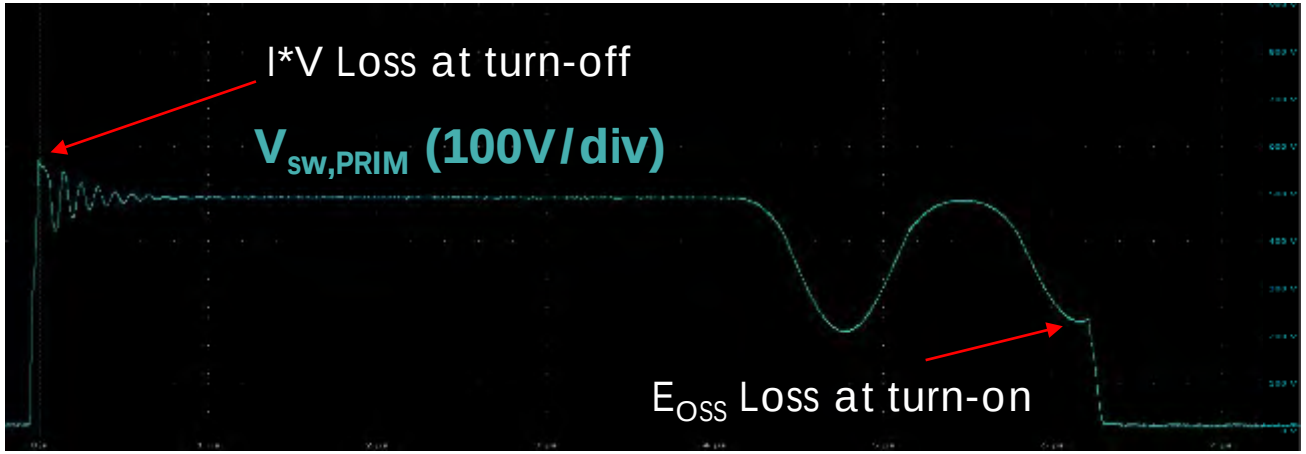
V_{IN}	90 – 264V
V_{OUT}	5 – 20V
I_{OUT}	0 – 3.25A
f_{SW}	~140kHz

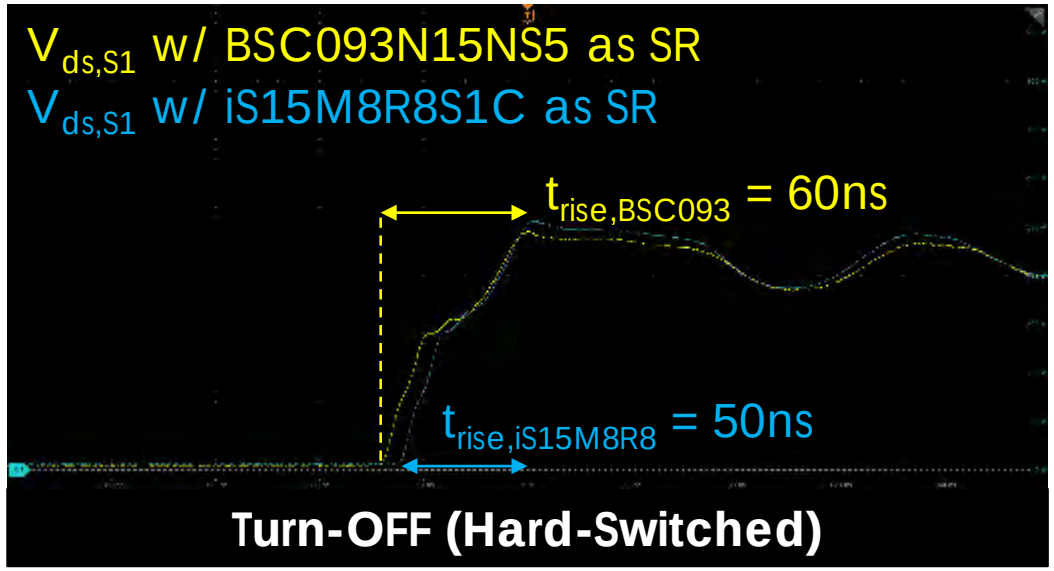


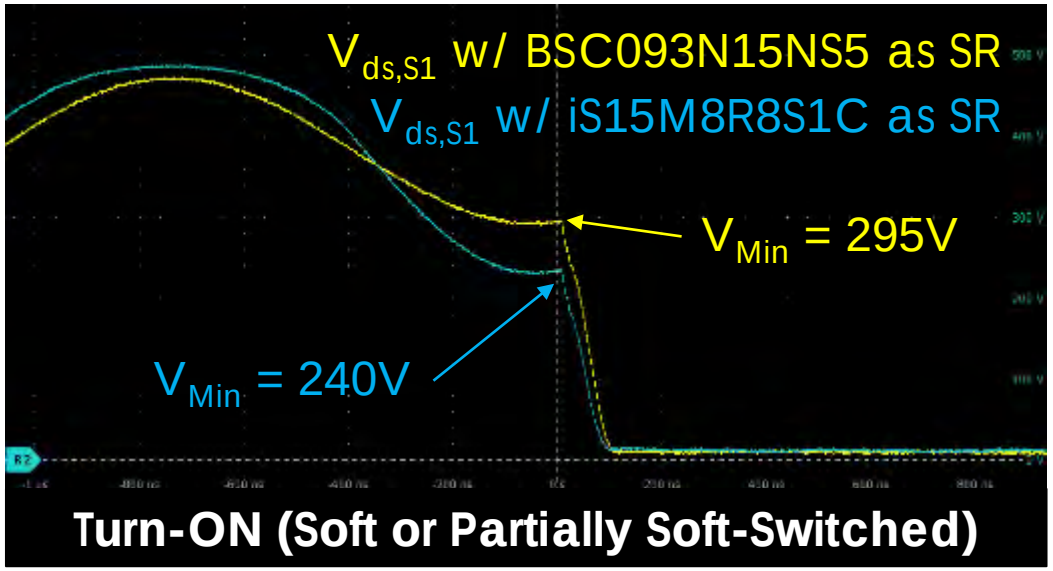


Soft-switching control techniques are common to increase efficiency and power density, but the choice of SR must be considered.

Case Study 2: SR Capacitance Reflects to the Primary

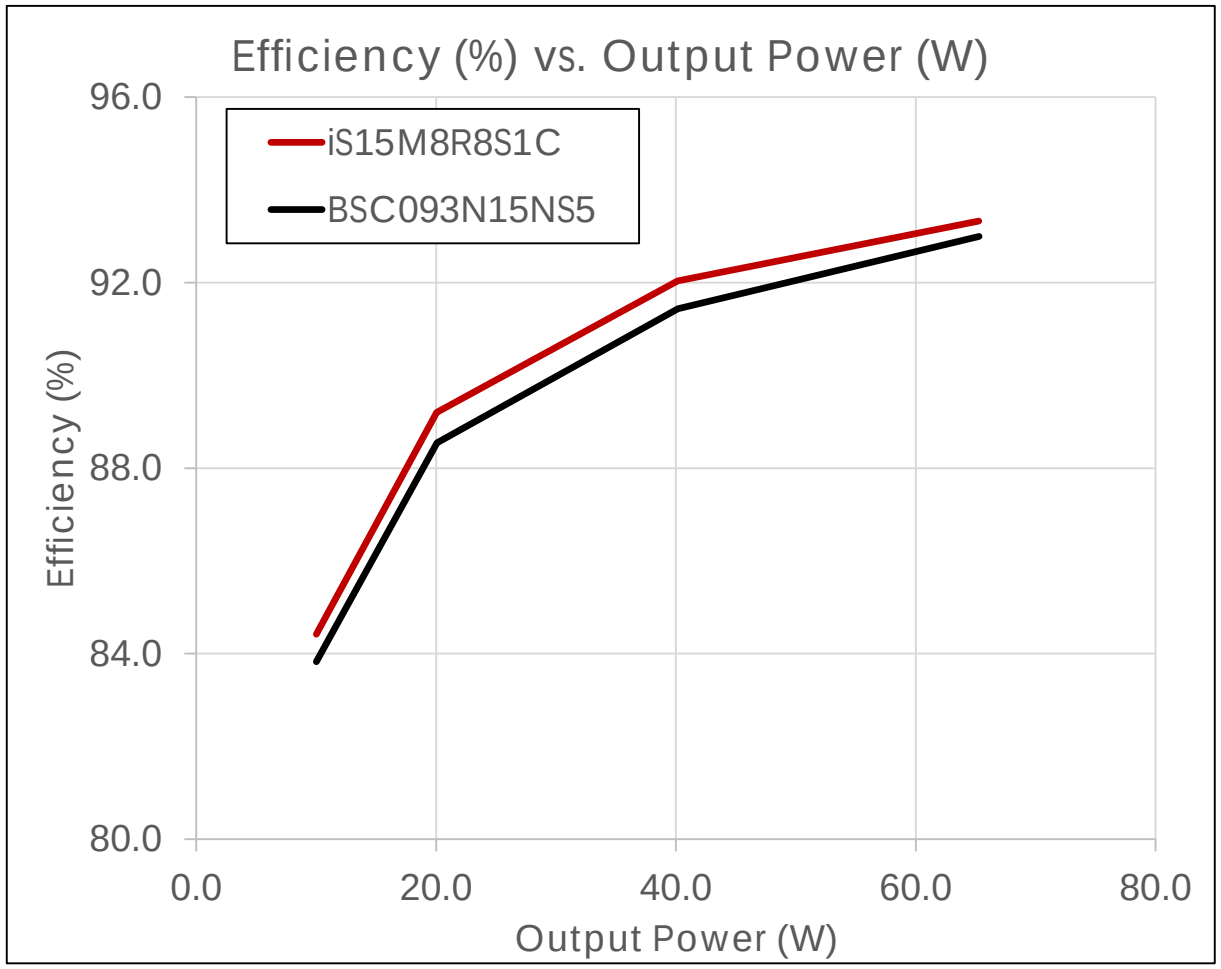


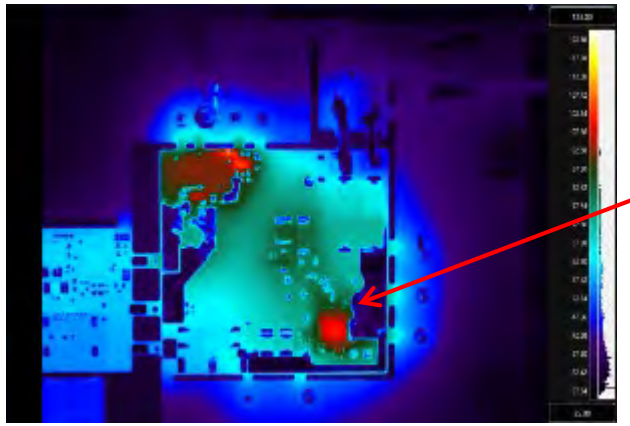




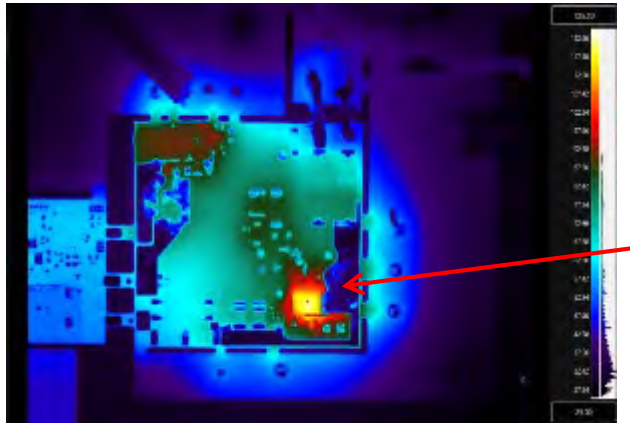
In QR flyback, SR capacitance reflects to primary, affecting transitions.

Case Study 2: A Cooler Primary GaN





SuperQ
SR: iS15M8R8S1C
Primary GaN
103°C



IFX
SR BSC093N15NS5
Primary Gan
123°C

Lower SR capacitance leads to better efficiency through secondary-to-primary capacitive reflection.

Conclusion

- Traditional estimates overstate RESURF switching losses
  - You can no longer assume a near-triangular transition of MOSFET drain voltage and current
- Q_{SW} should follow the measured switching transition
  - Capture the relevant interval rather than relying on legacy gate-charge landmarks
- Testing supports the revised approach
  - Device characterization revealed datasheet-to-measured Q_{SW} differences exceeding 30%
  - Application testing improved from more than 3× loss overprediction to less than 7% error
- Dynamic parameters translate into converter benefits for multiple topologies
  - Active-clamp forward: Lower Q_{SW} and E_{OSS} improve efficiency, power density, and thermal margin
  - QR flyback: SuperQ's SR capacitance profile improves efficiency and reduces primary GaN temperature by 20°C

Choose the MOSFET by the loss mechanism the topology exposes.