A Flexible Volterra-Based Adaptive Digital Pre-Distortion Solution for Wideband RF Power Amplifier Linearization

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Abstract

This presentation discusses highlights of a paper published in August, September and October 2008 issues of *Microwaves & RF Magazine*
Base Stations/PA’s
The Problem

The present 3G and other emerging air interfaces use non-constant envelope modulation schemes and are spectrally more efficient than their predecessors.

**Problem:** This technique causes high PAR, necessitating higher PA back-off. This leads to decrease in PA efficiency and increase in cooling and operational costs of a base-station.
How does DPD fix the problem?

**Solution:** Drive the PA harder to get more power

**Added Problem:** Signal distortion occurs

**Ultimate Solution:** Predict the type of distortion, pre-distort the signal in a reverse manner

**Result:** Distortion is cancelled out. This extends the linear region of the operation range and produces more output power at an efficiency approaching 40%. Now a smaller amplifier at higher efficiency can be used with DPD to achieve the desired output power
Introduction

- DPD (Digital Pre-Distortion) improves efficiency of PA’s
- Most PA’s are LDMOS class AB designs and rarely achieve 10% efficiency
- This inefficiency is inherent in the class AB design but also is a result of having to reduce the PA output to deal with signals that exhibit high PAR (Crest Factor) power and to prevent distortion that results in adjacent channel power leakage
Classes of operation of Power amplifier based on transfer characteristics
Typical PA improvement from this DPD solution

• Reduce PAR’s (or Crest Factor) for 3G signals up to 6 dB

• Reduce PAR’s (or Crest Factor) for OFDM signals by up to 4 dB

• All while meeting ACPR (Adjacent Channel Power Ratio) and EVM (Error Vector Magnitude) specs

• Correct for up to 11\textsuperscript{th} order non-linearities and PA (Power Amplifier) memory effects up to 200 ns

• Greater than 20 dB ACPR improvement

• Over 4X increase in power efficiency

• As much as 60% reduction in static power consumption
PAR/Crest Factor

The crest factor or peak-to-average ratio (PAR) or peak-to-average power ratio (PAPR) is a measurement of a waveform, calculated from the peak amplitude of the waveform divided by the RMS (time-averaged) value of the waveform.

\[ C = \frac{|x|_{\text{peak}}}{x_{RMS}} \]

It is therefore a dimensionless value. While this quotient is most simply expressed by a positive rational number, as shown below, in commercial products it is also commonly stated as the ratio of two whole numbers, e.g., 2:1.

The minimum possible crest factor is 1.
DC voltages have a crest factor of 1 since the RMS and the peak amplitude are equal, and it is the same for a square wave (of 50% duty cycle).
This table provides values for some other normalized waveforms:

<table>
<thead>
<tr>
<th>Wave type</th>
<th>Crest factor (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC</td>
<td>0.00 dB</td>
</tr>
<tr>
<td>Sine wave</td>
<td>3.01 dB</td>
</tr>
<tr>
<td>Full-wave rectified sine</td>
<td>3.01 dB</td>
</tr>
<tr>
<td>Half-wave rectified sine</td>
<td>6.02 dB</td>
</tr>
<tr>
<td>Triangle wave</td>
<td>4.77 dB</td>
</tr>
<tr>
<td>Square wave</td>
<td>0.00 dB</td>
</tr>
<tr>
<td>QPSK</td>
<td>3.5 - 4 dB</td>
</tr>
<tr>
<td>64 QAM</td>
<td>7.7 dB</td>
</tr>
<tr>
<td>128 QAM</td>
<td>8.2 dB</td>
</tr>
<tr>
<td>WCDMA downlink carrier</td>
<td>10.6 dB</td>
</tr>
</tbody>
</table>
PAR/Crest Factor

Notes:
1. Crest factors specified for QPSK, QAM, WCDMA are typical factors needed for reliable communication, not the theoretical crest factors which can be larger.
2. Waveform factor is the ratio of DC average to RMS and is used to scale resistors for measurements with DC or AC meters. The waveform factor for the half wave rectified sine wave should be 2.22 as the DC average is $VP/\pi$.
Memory-less Linearization Techniques

A generalized look up table can be used for pre-distorter gain/phase correction if no memory effects are taken into consideration.

Thus we are able to characterize a PA by:
1. Amplitude or AM-to-AM (or Gain Compression)
2. Phase Transfer or AM-to-PM
Performance Analyses of Efficiency Enhancement Techniques of PA’s
Figure 1: Gain compression and AM-PM characteristics for a typical Doherty PA
A more accurate PA model

Gain and Phase of PA’s change with:
- Temperature
- Voltage
- Component ageing

This requires an adaptive control of look-up tables for effective linearization
Volterra-based DPD Linearizer

- Volterra series and Theorem developed by Vito Volterra in 1887
- It is used to predict non-linear response of a system to a given input
  - Similar to Taylor series but Volterra has ability to capture “memory” effects
Volterra series /Equation 1

\[ Y(n) = Y_1(n) + Y_2(n) + Y_3(n) + Y_4(n) + Y_5(n) + \ldots + v(n) \quad (1) \]

Where,

\[ Y_1(n) = \sum_{i=0}^{M_1} h_1(i) \cdot x(n-i) \]
\[ Y_2(n) = \sum_{i_1=0}^{M_2} \sum_{i_2=0}^{M_2} h_2(i_1, i_2) \cdot x(n-i_1) \cdot x(n-i_2) \]
\[ Y_3(n) = \sum_{i_1=0}^{M_3} \sum_{i_2=0}^{M_3} \sum_{i_3=0}^{M_3} h_3(i_1, i_2, i_3) \cdot x(n-i_1) \cdot x(n-i_2) \cdot x(n-i_3) \]
\[ Y_4(n) = \sum_{i_1=0}^{M_4} \sum_{i_2=0}^{M_4} \sum_{i_3=0}^{M_4} \sum_{i_4=0}^{M_4} h_4(i_1, i_2, i_3, i_4) \cdot x(n-i_1) \cdot x(n-i_2) \cdot x(n-i_3) \cdot x(n-i_4) \]
\[ Y_5(n) = \sum_{i_1=0}^{M_5} \sum_{i_2=0}^{M_5} \sum_{i_3=0}^{M_5} \sum_{i_4=0}^{M_5} \sum_{i_5=0}^{M_5} h_5(i_1, i_2, i_3, i_4, i_5) \cdot x(n-i_1) \cdot x(n-i_2) \cdot x(n-i_3) \cdot x(n-i_4) \cdot x(n-i_5) \]
Simplify

WOW!! We need to simplify this!
Memory Polynomial Model

This technique constrains the Volterra Series so that everything except the diagonal terms in the kernels are zero, thus giving a memory polynomial model:

\[ Y(n) = \sum_{k=0}^{K} \sum_{i=0}^{M} h_k(i) \cdot x(n-i) |x(n-i)|^k \]

This simplification method has been proven to effectively model PA:
1. Thermal effects
2. Active matching network
3. Bias circuits due to slowly varying, non-constant amplitude of PA input signal
Figure 2: DPD System Diagram

A complete digital pre-distortion transmit signal chain with the GC5322SEK (System Evaluation Kit) based on TI high-speed analog and DSP technology.
Figure 2A: GC5322 Diagram
GC5322 DPD blocks

1. Linear Equalizer
2. Non-Linear DPD
3. Feedback Non-Linear Compensator and Smart Capture Buffers
Equation Reduction/Simplification Techniques Used

We used a combination of algorithmic and model reduction approaches:

1. The number of terms in (1) significantly reduced by eliminating redundancies associated with various index permutations.
2. Volterra coefficients assumed to be symmetric
3. Real input signal to the PA $x(n)$ expressed in terms of its complex baseband representation significantly reducing the number of terms. For band-limited systems we are only interested in frequency components close to the carrier frequency $f_0$.
4. Even order inter-modulation terms lie far away from frequency band of interest, allowing us to further drop half the terms in (1).
We used a combination of algorithmic and model reduction approaches:

5. The model is rotationally invariant, this simplifies things since a phase shift on the input of the PA produces exactly the same phase shift on the output. This allows (1) to be reduced to terms involving products of the signal and powers of its magnitude squared.

6. The PA is causal, so we assume the linear portion of the PA is minimum phase. This further restricts Volterra terms

7. Since PA implementations perform the processing in stages, this also helps simplify the model into cascade sections with each matched to the needs of compensating the distortions induced by the particular PA stage.
We get the model for the Linear Equalizer block by restricting the Volterra Series to only linear terms with memory $M_1$:

$$Y_1(n) = \sum_{i=0}^{M_1} h_1(i) \cdot x(n-i)$$  \hspace{1cm} (2)
Second Stage-- Non-Linear DPD ----- Equation 3

We get the Non-Linear DPD block by restricting the Volterra Series to only the non-linear terms with memory M2, and dropping even terms we get:

\[
Y(n) = \sum_{i=0}^{M2} h3(i,i,i).x(n-i).|x(n-i)|^2 + \sum_{i=0}^{M2} h5(i,i,i,i,i).x(n-i).|x(n-i)|^4 + \sum_{i=0}^{M2} h7(i,i,i,i,i,i,i).x(n-i).|x(n-i)|^6 + \text{other higher order terms depending on the polynomial modeling accuracy requirements of the adaptation algorithm.}
\] (3)
Rearranging Equation 3

Rearranging terms in Equation 3 gives:

\[ Y(n) = \sum_{i=0}^{M2} \{ h3(i,i,i).|x(n-i)|^2 + h5(i,i,i,i,i).[|x(n-i)|^2]^2 + h7(i,i,i,i,i,i,i).[|x(n-i)|^2]^3 + \text{higher order terms}\}.x(n-i) \]

\[ = \sum_{i=0}^{M2} \text{LUT}(|x(n-i)|2).x(n-i) \]
Simplifying Equation 1 Volterra Series terms:

\[ Y(n) = \sum_{i=0}^{M3} h3(i,i,0) |x(n-i)|^2 \cdot x(n-i) + \]
\[ \sum_{i=0}^{M3} h5(i,i,0,0,0) |x(n-i)|^2 \cdot |x(n)|^2 \cdot x(n) + \]
\[ \sum_{i=0}^{M3} h5(i,i,i,0) |x(n-i)|^4 \cdot x(n) + \]
\[ \sum_{i=0}^{M3}, i \neq j \sum_{j=0}^{M3} h5(i,i,j,j,0) |x(n-i)|^2 \cdot |x(n-j)|^2 \cdot x(n) + \]
\[ \sum_{i=0}^{M3} h7(i,i,0,0,0,0) |x(n-i)|^4 \cdot |x(n)|^2 \cdot x(n) + \]
\[ \sum_{i=0}^{M3} h7(i,i,i,0,0,0) |x(n-i)|^6 \cdot x(n) + \]
\[ \sum_{i=0}^{M3}, i \neq j \sum_{j=0}^{M3} h7(i,i,j,j,0,0) |x(n-i)|^2 \cdot |x(n-j)|^2 \cdot |x(n)|^2 \cdot x(n) + \]
\[ \sum_{i=0}^{M3}, i \neq j \sum_{j=0}^{M3} h7(i,i,i,j,j,0) |x(n-i)|^4 \cdot |x(n-j)|^2 \cdot x(n) + \]
\[ + \text{higher order terms} \quad (4) \]
Third Stage---Feedback Non-Linear Compensator and Smart Capture Buffers

Feedback signal from PA used to compute the instantaneous error, which along with reference transmit signal can be captured by a pair of on-chip memories.

DSP processor reads back these captured signals and implements the adaptation algorithms for the pre-distorter blocks.
Pre-Distortion Adaptation Algorithm

A Direct Learning architecture is used in the pre-distortion algorithm implemented on the DSP.

A model of the pre-distorter is maintained in software---its parameters optimized to minimize the error signal captured in the hardware.
Figure 3: GC5322 evaluation platform system diagram
# Table 1: GC5322 evaluation platform system parameters

<table>
<thead>
<tr>
<th>Evaluation System Configuration</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>RF Card Version</td>
<td>WiMax</td>
<td>WCDMA</td>
</tr>
<tr>
<td>DUC Input Sample Rate</td>
<td>11.2 MSPS (WiMax)</td>
<td>3.84 MSPS (WCDMA), 1.28 MSPS (TD-SCDMA), 4.333 MSPS (MC-GSM), 30.72 MSPS (LTE)</td>
</tr>
<tr>
<td>CFR Sample Rate</td>
<td>67.2 MSPS (WiMax)</td>
<td>61.44 MSPS (WCDMA, TD-SCDMA, LTE), 69.333 MSPS (MC-GSM)</td>
</tr>
<tr>
<td>DPD Sample Rate</td>
<td>112 MSPS</td>
<td>122.88 MSPS</td>
</tr>
<tr>
<td>DAC</td>
<td>DAC5682 @ 672 MHz Complex</td>
<td>DAC5682 @ 737.28 MHz Complex</td>
</tr>
<tr>
<td>ADC</td>
<td>ADS5444 @ 224 MHz Real</td>
<td>ADS5444 @ 245.76 MHz Real</td>
</tr>
<tr>
<td>IF Frequency</td>
<td>168 MHz</td>
<td>184.32 MHz</td>
</tr>
<tr>
<td>RF Frequency</td>
<td>2.123 GHz</td>
<td>2.139 GHz</td>
</tr>
<tr>
<td>IQ Modulator</td>
<td>TRF3703</td>
<td></td>
</tr>
<tr>
<td>Mixer</td>
<td>HMC214</td>
<td></td>
</tr>
<tr>
<td>LO</td>
<td>TRF3761</td>
<td></td>
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<tr>
<td>PLL</td>
<td>CDCM7005</td>
<td></td>
</tr>
</tbody>
</table>
Figure 4-A: Adjacent channel ACLR Vs. Pout at different PAR levels & test signals, pre & post DPD
Figure 4-B: Alternate channel ACLR Vs. Pout at different PAR levels & test signals, pre & post DPD
Figure 5-A: Pre-DPD spectrum at 46.75dBm Pout and 6dB PAR (TM1-64 data)
Figure 5-B: Post-DPD spectrum at 46.75dBm Pout and 6dB PAR (TM1-64 data)

<table>
<thead>
<tr>
<th>Carrier Power</th>
<th>Offset Freq</th>
<th>Integ BW</th>
<th>Lower dBc</th>
<th>Lower dBm</th>
<th>Upper dBc</th>
<th>Upper dBm</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 -32.13 dBm / 3.840 MHz</td>
<td>5.000 MHz</td>
<td>3.840 MHz</td>
<td>-52.86</td>
<td>-84.99</td>
<td>-53.51</td>
<td>-95.84</td>
</tr>
<tr>
<td>2 -32.55 dBm / 3.840 MHz</td>
<td>10.00 MHz</td>
<td>3.840 MHz</td>
<td>-58.86</td>
<td>-90.79</td>
<td>-60.89</td>
<td>-93.02</td>
</tr>
<tr>
<td></td>
<td>15.00 MHz</td>
<td>3.840 MHz</td>
<td>-60.65</td>
<td>-92.78</td>
<td>-62.72</td>
<td>-94.85</td>
</tr>
<tr>
<td></td>
<td>20.00 MHz</td>
<td>3.840 MHz</td>
<td>-62.59</td>
<td>-94.72</td>
<td>-64.37</td>
<td>-96.49</td>
</tr>
<tr>
<td></td>
<td>25.00 MHz</td>
<td>3.840 MHz</td>
<td>-63.01</td>
<td>-95.14</td>
<td>-64.91</td>
<td>-97.04</td>
</tr>
</tbody>
</table>
Figure 6-A: PCDE Vs. Pout at different PAR levels and test signals, pre and post DPD
Figure 6-B: EVM Vs. Pout at different PAR levels and test signals, pre and post DPD
Figure 7: PA drain power efficiency Vs. output power

![Graph showing PA drain power efficiency vs. output power. The graph displays a linear increase in PA Efficiency (%) as output power (Pout) increases from 40 dBm to 48 dBm, with efficiency values ranging from 10% to 45%.](image-url)
Figure 8-A: WCDMA: Pre-DPD spectrum at 42.75dBm
Pout and 6dB PAR (TM1-64 data)
Figure 8-B: WCDMA: Post-DPD spectrum at 42.75dBm
Pout and 6dB PAR(TM1-64 data)
Figure 9-A: WiMax: Pre (red) and post (blue) DPD spectrums at 43.75dBm Pout and 8.5dB PAR
Figure 9-B: WiMax: Clockwise from top left:
Pre-DPD Constellation, Post-DPD Constellation, Post-DPD Error vector spectrum,
Pre-DPD Error Vector Spectrum plots for 43.75dBm Pout, 8.5dB PAR
Figure 10-A: TD-SCDMA: Pre (blue) and post (green) DPD spectral plots at 46dBm Pout and 8dB PAR
Figure 10-B: TD-SCDMA: Pre-DPD (left) and post-DPD (right) Constellation plots for 46dBm Pout, 8dB PAR
Figure 11: MC-GSM: Pre (blue) and post (green) DPD spectral plots at 42dBm Pout and 6.3dB PAR
Figure 12: LTE: Pre(red) and post(blue) DPD spectrums at 43.5dBm Pout and 7.5dB PAR

Center Freq 2.139320000 GHz

ΔMkr2 15.00 MHz
Band Power -50.71 dB

Center 2.13932 GHz
#Res BW 100 kHz
#VBW 300 kHz
Span 100.0 MHz
#Sweep 3.00 s (601 pts)
Summary

The pre-distortion scheme presented here is shown to be highly efficient at improving amplifier linearity and power efficiency.

The GC5322 integrated transmit solution presented here not only provides a significant environmental benefit, but also provides a substantial cost savings both in capital expenditure and operational expenditure for next generation base stations.

By providing an integrated DUC-CFR-DPD signal processing hardware solution, along with optimized DSP-based adaptation software and a proven reference RF board design, faster time to market can be achieved.